AC/DC WLED Driver with External MOSFET Universal High Brightness

DESCRIPTION

The TS19450 is an open loop, current mode control LED driver IC. It can be programmed to operate in either a constant frequency or constant off-time mode. It includes an 8V~450V linear regulator which allows it to work from a wide range of input voltages without the need for an external low voltage supply. The TS19450 includes a PWM dimming input that can accept an external control signal with a duty ratio of 0~100% and a frequency of up to a few kHz. It also includes a 0~250mV linear dimming input which can be used for linear dimming of the LED current.

The TS19450 is ideally suited for buck LED drivers. Since it operates in open loop current mode control, the controller achieves good output current regulation without the need for any loop compensation. PWM dimming response is limited only by the rate of rise and fall of the inductor current, enabling very fast rise and fall times. The TS19450 requires only free external components (apart from the power stage) to produce a controlled LED current making it an ideal solution for low cost LED drivers.

FEATURES

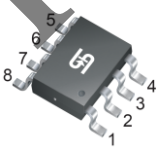
- Switch mode controller for single switch LED drivers
- Open loop peak current controller
- Internal 8V~450V linear regulator
- Constant frequency or constant off-time operation
- Linear and PWM dimming capability
- Requires few external components for operation

APPLICATION

- DC/DC or AC/DC LED driver applications
- RGB backlighting LED driver
- Back lighting of flat panel displays
- General purpose constant current source
- Signage and decorative LED lighting
- Charger

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8

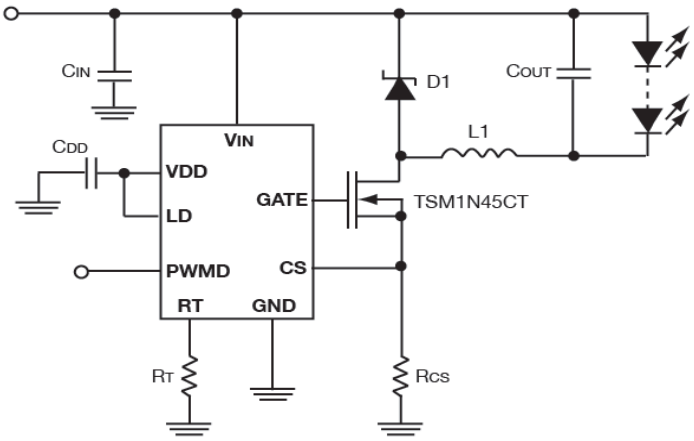


Pin Definition:

1. V_{IN}	8. RT
2. CS	7. LD
3. GND	6. V_{DD}
4. Gate	5. PWMD

Notes: Moisture sensitivity level: level 3. Per J-STD-020

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified) (Note 1)			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Input Voltage Range	V_{IN} to GND	-0.5 ~ +470	V
Internal Regulated Voltage	V_{DD} to GND	13.5	V
CS, LD, PWMD, Gate, RT to GND		-0.3 ~ (V_{DD}+0.3)	V
Continuous Power Dissipation (Note 2)	P_D	630	mW
Storage Temperature Range	T_A	-65 to +150	°C
Junction Temperature Range	T_J	-40 to +150	°C

THERMAL PERFORMANCE (Note 3)			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	128	°C/W

ELECTRICAL SPECIFICATIONS (T_A= 25°C, V_{IN}= 12V, unless otherwise noted) (Note 4)						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Input						
DC Input Voltage Range	V_{INDC}	DC input voltage	8.0	--	450	V
Shut-down Mode Supply Current	I_{INSD}	Pin PWMD to GND	--	0.5	1.0	mA
Internal Regulator						
Internally Regulated Voltage	V_{DD}	V_{IN}=8V, $I_{DD(EXT)}$=0, 500pF at Gate, R_T=226kΩ	7.25	7.5	7.75	V
Line Regulation of V_{DD}	ΔV_{DDLine}	V_{IN}=8~450V, $I_{DD(EXT)}$=0 500pF at Gate, R_T=226kΩ	0	--	1.0	V
Load Regulation of V_{DD}	ΔV_{DDLoad}	$I_{DD(EXT)}$= 0 ~ 1mA 500pF at Gate, R_T=226kΩ, PWMD=V_{DD}	0	--	100	mV
Undervoltage Lockout Threshold	UVLO	V_{IN} rising	6.45	6.7	6.95	V
Undervoltage Lockout Hysteresis	ΔUVLO	V_{IN} falling	--	500	--	mV
VDD current available for external circuitry (Note 5)	$V_{DD\ (EXT)}$	V_{IN}=8V~100V	--	--	1.0	mA
Dimming						
PWMD Input Low Voltage	V_{ENL}	V_{IN}=8V~450V	--	--	1.0	V
PWMD Input High Voltage	V_{ENH}	V_{IN}=8V~450V	2.4	--	--	V
PWMD Pull-down resistance at PWMD	R_{EN}	V_{PWMD}=5V	50	100	150	kΩ
Linear Dimming pin Voltage	V_{LD}	V_{IN}=12V	0	--	250	mV

ELECTRICAL SPECIFICATIONS (T_A= 25°C, V_{IN}= 12V, unless otherwise noted) (Note 4)						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Current Sense Comparator						
Current Sense Pull-in Threshold Voltage	V_{CSTH}	-40ºC < T_A < +85ºC	225	250	275	mV
		T_A < +125ºC	213	250	287	
Offset Voltage for LD Comparator	V_{OFFSET}		-12	--	12	mV
Current Sense Blanking Interval	T_{BLANK}	V_{LD}=V_{DD} , V_{CS}=0.55V_{LD}	150	215	280	ns
Delay to Output	T_{DELAY}	V_{IN}=12V, V_{LD}=0.15V, V_{CS}=0~0.22V after T_{BLANK}	--	--	300	ns
Oscillator						
Oscillator Frequency	f_{OSC}	R_T=1MΩ	20	25	30	kHz
		R_T=223kΩ	80	100	120	
Max. Oscillator PWM Duty Cycle	D_{MAX}	F=25kHz at Gate, CS to GND	--	--	100	%
Gate Driver						
Gate Sourcing Current	I_{SOURCE}	V_{GATE}=0V, V_{DD}=7.5V	165	--	--	mA
Gate Sinking Current	I_{SINK}	V_{GATE}=V_{DD}, V_{DD}=7.5V	165	--	--	mA
Gate High Output Voltage	$V_{GATE(HI)}$	I_{OUT}=-10mA	V_{DD}-0.3	--	V_{DD}	V
Gate Low Output Voltage	$V_{GATE(LO)}$	I_{OUT}=10mA	0	--	0.3	V
Gate Output Rise Time	T_{RISE}	C_{GATE}=500pF, 10%~90% V_{GATE}	--	30	50	ns
Gate Output Fall Time	T_{FALL}	C_{GATE}=500pF, 90%~10% V_{GATE}	--	30	50	ns

Note:

1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
2. Limited by package power dissipation, whichever is lower.
3. Thermal Resistance is specified with the component mounted on a low effective thermal conductivity test board in free air at T_A=25°C.
4. Denotes the specifications which apply over the full operating ambient temperature range of -40ºC<T_A<+125ºC.
5. V_{DD} load current external to the TS19450.

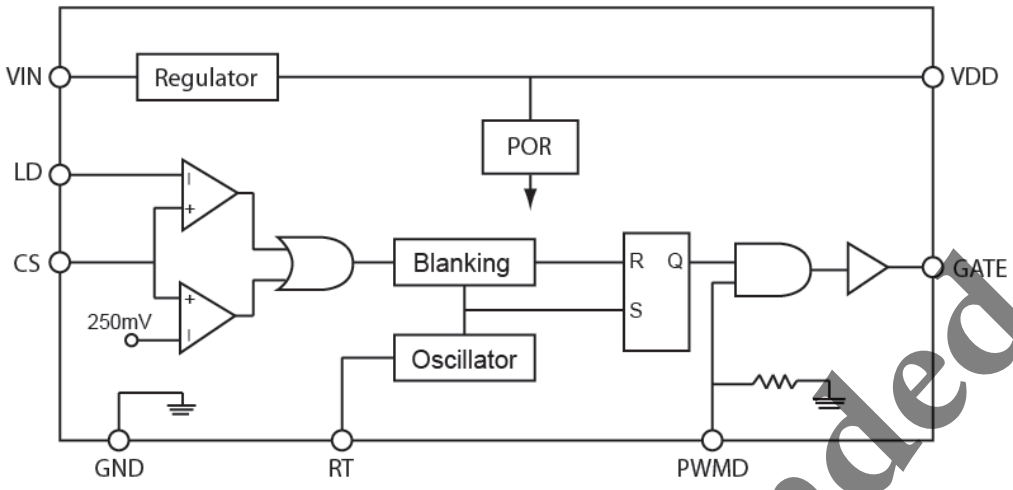
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TS19450CS RLG	SOP-8	2,500pcs / 13” Reel

Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC.
2. Halogen-free according to IEC 61249-2-21 definition.

FUNCTION BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	VIN	This pin is the input of 8V~450V linear regulator
2	CS	This pin is the current sense pin used to sense the MOSFET current by means of an external sense resistor. When this pin exceeds the low of either the internal 250mV or the voltage at the LD pin, the GATE output goes low
3	GND	Ground return for all internal circuitry. This pin must be electrically connected to the ground of the power train.
4	GATE	This pin is the output GATE driver for an external N-CH Power MOSFET
5	PWMD	This is the PWM dimming input of the IC. When this pin is pulled to GND, the Gate Driver is turned off. When the pin is pulled high, the GATE driver operates normally.
6	VDD	This is the power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (≥0.1μF)
7	LD	This pin is the linear dimming input and sets the current sense threshold as long as the voltage at the pin is less than 250mV (typ.)
8	RT	This pin sets the oscillator frequency. When a resistor is connected between RT and GND, the IC operates in constant frequency mode. When the resistor is connected between RT and GATE, the IC operates in constant off-time mode.

APPLICATION INFORMATION

The TS19450 is optimized to drive buck LED drivers using open-loop peak current mode control. This method of control enables fairly accurate LED current control without the need for high side current sensing or the design of any closed loop controllers. The IC uses very few external components and enables both linear and PWM dimming of the LED current.

A resistor connected to the RT pin programs the frequency of operation (or the off-time). The oscillator produces pulses at regular intervals. These pulses set the SR flip-flop in the TS19450 which causes the GATE driver to turn on. The same pulses also start the blanking timer which inhibits the reset input of the SR flip flop and prevent false turn-offs due to the turn-on spike. When the FET turns on, the current through the inductor starts ramping up. This current flows through the external sense resistor R_{CS} and produces a ramp voltage at the CS pin. The comparators are constantly comparing the CS pin voltage to both the voltage at the LD pin and the internal 250mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip flop. When the output of either one of the two comparators goes high, the flip flop is reset and the GATE output goes low. The GATE goes low until the SR flip flop is set by the oscillator. Assuming a 30% ripple in the inductor, the current sense resistor R_{CS} can be set using:

$$R_{CS} = \frac{0.25V(\text{or } V_{LD})}{1.15 \times I_{LED}\ (A)}$$

Constant frequency peak current mode control has an inherent disadvantage – at duty cycles greater than 0.5, the control scheme goes into sub harmonic oscillations. To prevent this, an artificial slope is typically added to the current sense waveform. This slope compensation scheme will affect the accuracy of the LED current in the present form. However, a constant off-time peak current control scheme does not have this problem and can easily operate at duty cycles greater than 0.5 and also gives inherent input voltage rejection making the LED current almost insensitive to input voltage variations. But, it leads to variable frequency operation and the frequency range depends greatly on the input and output voltage variation. TS19450 makes it easy to switch between the two modes of operation by changing one connection (see oscillator section).

Input Voltage Regulator

The TS19450 can be powered directly from its VIN pin and can work from 8.0V~450VDC at its VIN pin. When a voltage is applied at the VIN pin, the TS19450 maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The TS19450 can be also operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the TS19450 will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 12V.

Although the VIN pin of the TS19450 is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an SOP-8 (junction to ambient thermal resistance $R\theta_{JA}$ = 128°C/W) TS19450 draws about I_{IN} = 2.0mA from the VIN pin, and has a maximum allowable temperature rise of the junction temperature limited to about ΔT=10ºCm the maximum voltage at the VIN pin would be:

$$V_{IN(MAX)} = \frac{\Delta T}{R\theta_{JA}} \times \frac{1}{I_{IN}} = \frac{100ºC}{128ºC/W} \times \frac{1}{2mA} = 390V$$

In these cases, to operate the TS19450 from higher input voltages, a Zener diode can be added in series with the VIN pin to divert some of the power loss from the TS19450 to the Zener diode. In the above example, using a 100V Zener diode will allow the circuit to easily work up to 450V.

APPLICATION INFORMATION (CONTINUE)

The input current drawn from the VIN pin is a sum of the 1.0mA current drawn by the internal circuit and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the external

$$I_{IN} \approx 1mA + Q_G \times f_S$$

In the above equation, f_S is the switching frequency and Q_G is the GATE charge of the external MOSFET (which can be obtained from the datasheet of the MOSFET).

Current Sense

The current sense input of the TS19450 goes to the non-inverting inputs of two comparators. The inverting terminal of one comparator is tied to an internal 250mV reference whereas the inverting terminal of the other comparator is connected to the LD pin. The outputs of both these comparators are fed into an OR GATE and the output of the OR GATE is fed into the reset pin of the flip-flop. Thus, the comparator which has the lowest voltage at the inverting terminal determines when the GATE output is turned off.

The outputs of the comparators also include a 150~280ns blanking time which prevents spurious turn-offs of the external MOSFET due to the turn-on spike normally present in peak current mode control. In rare cases, this internal blanking might not be enough to filter out the turn-on spike. In these cases, an external RC filter needs to be added between the external sense resistor (R_{CS}) and the CS pin.

Please note that the comparators are fast (with a typical 80ns response time). Hence these comparators are more susceptible to be triggered by noise than the comparators of the TS19450. A proper layout minimizing external inductances will prevent false triggering of these comparators.

Oscillator

The oscillator in the TS19450 is controlled by a single resistor connected at the RT pin. The equation governing the oscillator time period t_{OSC} is given by:

$$t_{OSC} = \frac{RT(k\Omega)+22}{25}$$

If the resistor is connected between RT and GND, TS19450 operates in a constant frequency mode and the above equation determines the time-period. If the resistor is connected between RT and GATE, the TS19450 operates in a constant off-time mode and the above equation determines the off-time.

PWM Dimming

PWM Dimming can be achieved by driving the PWMD pin with a low frequency square wave signal. When the PWM signal is zero, the GATE driver is turned off and when the PWMD signal if high, the GATE driver is enabled. Since the PWMD signal does not turn off the other parts of the IC, the response of the TS19450 to the PWMD signal is almost instantaneous. The rate of rise and fall of the LED current is thus determined solely by the rise and fall times of the inductor current.

To disable PWM dimming and enable the TS19450 permanently, connect the PWMD pin to VDD.

APPLICATION INFORMATION (CONTINUE)

Linear Dimming

The Linear Dimming pin is used to control the LED current. There are two cases when it may be necessary to use the Linear Dimming pin.

***** In some cases, it may not be possible to find the exact value required to obtain the LED current when the R_{CS} internal 250mV is used. In these cases, an external voltage divider from the VDD pin can be connected to the LD pin to obtain a voltage (less than 250mV) corresponding to the desired voltage across R_{CS}.

***** Linear dimming may be desired to adjust the current level to reduce the intensity of the LEDs. In these cases, an external 0~250mV voltage can be connected to the LD pin to adjust the LED current during operation.

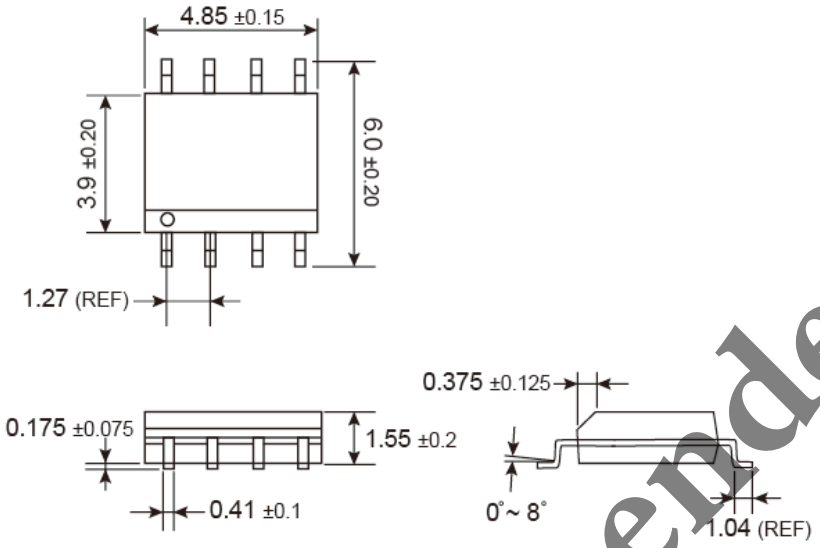
To use the internal 250mV, the LD pin can be connected to VDD.

Note:

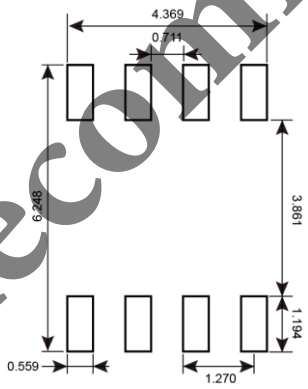
Although the LD pin can be pulled to GND, the output current will not go to zero. This is due to the presence of a minimum on-time (which is equal to the sum of the blanking time and the delay to output time) which is about 450ns. This will cause the MOSFET to be on for a minimum of 450ns and thus the LED current when LD = GND will not be zero. This current is also dependent on the input voltage, inductance value, forward voltage of the LEDs and circuit parasitic. To get zero LED current, the PWMD pin has to be used.

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

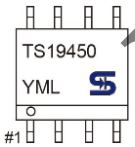
SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



Marking Diagram



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan	**P** =Feb	**Q** =Mar	**R** =Apr
S =May	**T** =Jun	**U** =Jul	**V** =Aug
W =Sep	**X** =Oct	**Y** =Nov	**Z** =Dec

L = Lot Code (1~9, A~Z)

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