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Automotive Four-Switch Buck-Boost LED Controller for Combination Head Lights

MAX25603

General Description

The MAX25603 is a synchronous four-switch, buck-boost LED driver controller suitable for multifunction automotive combination head lamps. The controller regulates the LED current for LED string voltages from 0V to 60V. The MAX25603 can be used as a seamless buck-boost LED driver for applications that require an efficient buck-boost LED driver with synchronous rectification. The MAX25603 is ideal for high-power applications that require a current source with PWM dimming capability.

The device provides seamless transition between buck, boost, and buck-boost modes depending on the ratio of input to output voltage. The MAX25603 is ideal for LED driver applications in automotive, industrial, and other LED lighting applications. A fault flag indicates open LED or thermal shutdown conditions. The device uses Analog Devices' proprietary average-current-mode control scheme and allows adjustable 200kHz to 440kHz fixed-frequency operation. In addition, ±6% triangular spread-spectrum is added internally to the oscillator to improve EMI performance. The MAX25603 provides both analog and digital PWM dimming in dual string applications with time sharing. A single device can be used to power a daytime running light (DRL), position light, high beam, and low beam in an automotive front headlamp. The MAX25603 integrates two high-side pMOS drivers for PWM dimming applications that require fast rising and falling edges of the LED current. It also features robust output open and short protection, is AEC qualified, and is suitable for automotive applications.

The MAX25603 uses Analog Devices' proprietary architecture to limit LED current overshoots and overshoot durations during switchover in dual-string applications in time-sharing mode. In multistring applications in time-sharing mode, LED current overshoots during switchover between strings is minimized by an Analog Devices' proprietary control scheme.

Applications

- Combination Automotive Head Lamps

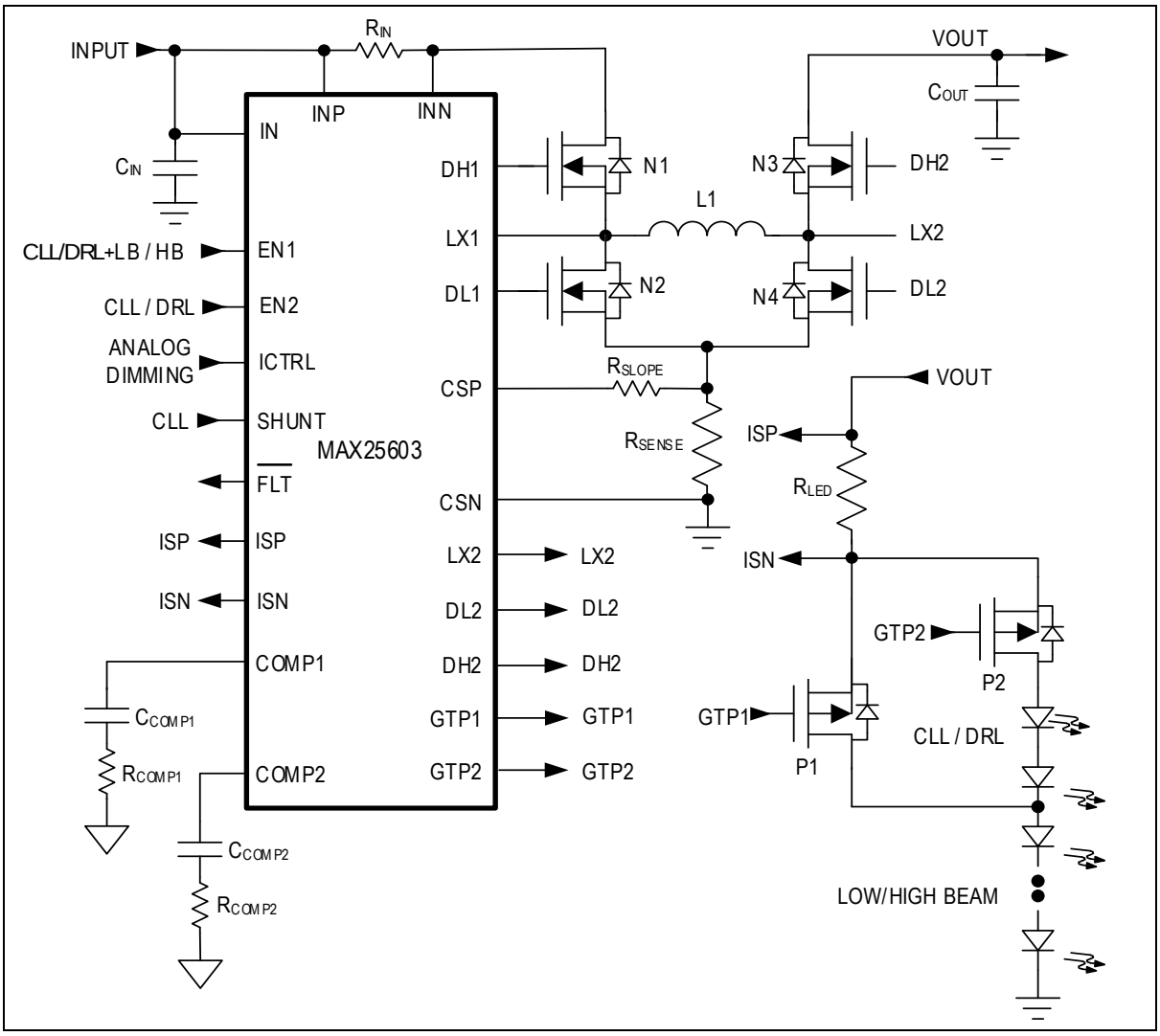
Benefits and Features

- Automotive Ready: AEC-Q100 Qualified
- Integration Minimizes BOM for High-Brightness LED Driver, Saving Space and Reducing Cost
  - Wide Input Voltage Range from 5V to 60V
  - H-Bridge Single Inductor Buck-Boost Architecture
  - Built-In Fast LED Current Limit During Transients
  - Suitable for Dual-String Applications with Time-Sharing
  - 28-Pin TSSOP with EP Pad
- Full Featured Dual String Driver
  - Analog and PWM Dimming on Both Channels (EN1 and EN2)
  - Analog Devices' Proprietary Control Architecture Limits LED Current Spikes and Spike Duration in Dual-String Mode
  - Flicker-Free PWM Dimming with Spread-Spectrum
  - Dual Integrated pMOS Dimming FET Gate Driver
- Protection Features and Wide Temperature Range Increase System Reliability
  - Short Circuit, Overvoltage, and Thermal Protection
  - Fast LED Current Limit and Input Current Limiter
- -40ºC to +150ºC Operating Junction-Temperature Range

***Ordering Information* appears at end of data sheet**

19-101257; Rev 0; 12/21

Simplified Application Diagram



Absolute Maximum Ratings

IN, INN, INP, ISP, ISN, GTP1, GTP2 to PGND ..... -0.3V to +65V

ISP to ISN ..... -0.3V to +0.6V

ISP to GTP_ ..... -0.3V to +6.0V

LX1, LX2 to PGND ..... -1.0V to +65V

BST_ to LX_ ..... -0.3V to +6V

DH_ to LX_ ..... -0.3V to V_{BST} + 0.3V

DL1, DL2 to PGND ..... -0.3V to (V_{CC} + 0.3) V

CSP, CSN to SGND ..... -2.5V to +6V

CSP to CSN ..... -0.5V to +0.5V

COMP1, COMP2, to SGND ..... -0.3V to V_{CC} + 0.3V

V_{CC} to SGND ..... -0.3V to +6V

ICTRL, EN1, EN2, SHUNT, FB, FLT to SGND ..... -0.3V to +6V

PGND to SGND ..... -0.3V to +0.3V

V_{CC} Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (TSSOP) (T_A = +70°C, derate 29.76mW/°C above +70°C) 2381mW

Operating Junction-Temperature Range (Note 1, 2) -40°C to +150°C

Storage-Temperature Range ..... -40°C to +150°C

Soldering Temperature (Reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28-TSSOP

Package Code	U28E+1C
Outline Number	*21-100182*
Land Pattern Number	*90-100069*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	33.6°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3.3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = V_{INP} = 14V, T_J = -40°C to +125°C unless otherwise noted, (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
INP Input Voltage Range	V_{INP}		5.0		60	V
Supply Current	I_{INQ}	No switching, IN = 12V		4	8	mA
UNDERVOLTAGE LOCKOUT						
Undervoltage Lockout Rising	$UVLOR_{IN}$	V_{IN} rising	3.85	4.1	4.3	V
Undervoltage Lockout Falling	$UVLOF_{IN}$	V_{IN} falling	3.55	3.8	4.0	V
Hysteresis				300		mV
Startup Delay	t_{START_DELAY}			550		µs
V_{CC} REGULATOR						

(V_{IN} = V_{INP} = 14V, T_J = -40°C to +125°C unless otherwise noted, (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{CC}	5.5V < V_{IN} < 65V; I_{VCC} = 1mA	4.85	5.0	5.1	V
		I_{VCC} = 30mA, 5.5V < V_{IN} < 36V	4.85	5.0	5.1	
		I_{VCC} = 1mA to 60mA, 6V < V_{IN} < 25V	4.85	5.0	5.1	
Dropout Voltage	V_{CC_DROP}	V_{IN} = 4.5V, I_{VCC} = 5mA		60	110	mV
V_{CC} UVLO Rising	V_{CC_UVLOR}	Rising		4.2		V
V_{CC} UVLO Falling	V_{CC_UVLOF}	Falling		3.9		V
Short-Circuit Current Limit	I_{VCC_SC}			110		mA
BUCK-BOOST CONTROLLER						
Switching Frequency (Dither Disabled)	fsw	R_{DL1} = 10kΩ R_{DL2} = 10kΩ		200		kHz
		R_{DL1} = 20kΩ R_{DL2} = 10kΩ		230		
		R_{DL1} = 30kΩ R_{DL2} = 10kΩ		260		
		R_{DL1} = 10kΩ R_{DL2} = 20kΩ		290		
		R_{DL1} = 20kΩ R_{DL2} = 20kΩ		320		
		R_{DL1} = 30kΩ R_{DL2} = 20kΩ		350		
		R_{DL1} = 10kΩ R_{DL2} = 30kΩ		380		
		R_{DL1} = 20kΩ R_{DL2} = 30kΩ		410		
		R_{DL1} = 30kΩ R_{DL2} = 30kΩ		440		
Frequency Accuracy	fsw		-15		15	%
Frequency Dither				+/-6		%
Minimum On-Time (Buck)	t_{ON_MIN}			180	270	ns
INPUT CURRENT-SENSE AMPLIFIER						
Input Current-Sense Common-Mode Range			5		60	V
Input Current-Sense Threshold		3V < V_{INP} < 60V	88	100	112	mV
INP Bias Current		V_{INP} - V_{INN} = 100mV, V_{INP} = 60V		50		µA
INN Bias Current		V_{INP} - V_{INN} = 100mV, V_{INP} = 60V		10		µA
CSP CSN CURRENT-SENSE AMPLIFIER						
CSP, CSN Input Bias Current			-1		1	µA
Voltage Gain (Boost, Buck Mode)		V_{CSP} = 100mV, V_{CSN} = 0mV		10		V/V
ANALOG DIMMING						
ICTRL Control Input Voltage Range	$ICTRL_{RNG}$		0.2		1.2	V
ICTRL Zero Current Threshold	I_{CTRLZC_VTH}	(V_{ISP} - V_{ISN}) < 5mV	0.16	0.18	0.2	V

(V_{IN} = V_{INP} = 14V, T_J = -40°C to +125°C unless otherwise noted, (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ICTRL Clamp Voltage	$ICTRL_{CLMP}$	ICTRL sink = 1µA	1.25	1.30	1.35	V
ICTRL Input Bias Current	$ICTRLI_{IN}$	V_{ICTRL} = 0 to 5.0V		20	500	nA
LED CURRENT-SENSE AMPLIFIER						
Common-Mode Input Range			0		+60	V
Differential Signal Range			0		200	mV
ISN Input Bias Current	IB_{ISN}	V_{ISP} - V_{ISN} = 200mV, V_{ISP} = 60V		24	50	µA
ISP Input Bias Current	IB_{ISP}	V_{ISP} - V_{ISN} = 200mV, V_{ISP} = 60V		800	1300	µA
LED Current-Sense Regulation Voltage		V_{ICTRL} = 1.4V, 5.4V < V_{ISP} < 60V	213.8	220	226.2	mV
		V_{ICTRL} = 1.2V, 5.4V < V_{ISP} < 60V	194	200	206	
		V_{ICTRL} = 0.4V, 5.4V < V_{ISP} < 60V	36	40	44	
		V_{ICTRL} = 1.4V, 2.15V < V_{ISP} < 5.4V	210	220	232	
		V_{ICTRL} = 1.2V, 2.15V < V_{ISP} < 5.4V	190	200	210	
		V_{ICTRL} = 0.4V, 2.15V < V_{ISP} < 5.4V	36	40	44	
LED Current-Sense Regulation Voltage (Low Range)		V_{ICTRL} = 1.2V, 0V < V_{ISP} < 2.15V	190	200	210	mV
		V_{ICTRL} = 0.4V, 0V < V_{ISP} < 2.15V	35	40	45	
Common-Mode Input Range Selector	RNG_{SEL}	V_{ISP} rising	1.9	2.05	2.15	V
Common-Mode Input Range Selector Hysteresis				100		mV
LED Current Limit	V_{CL}	V_{ICTRL} = 1.4V, 3V < V_{ISP} < 60V	247	275	303	mV
		V_{ICTRL} = 1.2V, 3V < V_{ISP} < 60V	225	250	275	
		V_{ICTRL} < V_{ICTRL_CLMP}, 3V < V_{ISP} < 60V	40	55	70	
ICTRL LED Current Limit Clamp	V_{ICTRL_CLMP}	ICTRL rising		420		mV
OUTPUT VOLTAGE DISCHARGE						
Discharge Activation Threshold		V_{ICTRL} = 1.4V, V_{ISP} = 12V		275		mV
		V_{ICTRL} = 1.2V, V_{ISP} = 12V	225	250	275	
		V_{ICTRL} < V_{ICTRL_CLMP}, V_{ISP} = 12V		55		
Discharge Deactivation Deglitch				5		µs
Negative Current Limit During Discharge				63		mV
Hysteresis				15		mV
SLOPE COMPENSATION ON CSP						
Slope Compensation Current-Ramp Height	I_{SLOPE_PK}	Peak-current ramp added to CSP input per switching cycle at 100% duty cycle	42.5	50	57.5	µA
ERROR AMPLIFIER						
Transconductance	g_m	V_{ISP} - V_{ISN} = 200mV	1170	1800	2430	µS
COMP Sink Current	$COMP_{ISINK}$	V_{COMP} = 5V		300		µA
COMP Source Current	$COMP_{ISRC}$	V_{COMP} = 0V		300		µA
nMOS GATE DRIVERS						

(V_{IN} = V_{INP} = 14V, T_J = -40°C to +125°C unless otherwise noted, (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DH1 Sourcing Resistance	R_{DH1_SRC}			2.2		Ω
DH2 Sourcing Resistance	R_{DH2_SRC}			1.2		Ω
DH_ Sinking Resistance	R_{DH_SINK}			1.2		Ω
DL_ Sourcing Resistance	R_{DL_SRC}	DL_ = high		1.6		Ω
DL_ Sinking Resistance	R_{DL_SINK}	DL_ = low		0.9		Ω
DH_ to DL_ Dead Time		DH_ fall to DL_ rise		20		ns
DL_ to DH_ Dead Time		DL_ fall to DH_ rise		20		ns
PWM DIMMING						
EN1, EN2 Turn-On Threshold		EN_ rising	1.3	1.4	1.5	V
EN1, EN2 Hysteresis				250		mV
EN1, EN2 Input Bias Current	I_{EN1}, I_{EN2}		-1		1	µA
SHUNT High Threshold		SHUNT rising	1.3	1.4	1.5	V
SHUNT Hysteresis				250		mV
SHUNT Input Bias Current	I_{SHUNT}		-1		1	µA
DIMMING pMOS GATE DRIVERS						
Peak Pullup Current	$I_{DIMOUTPU}$	EN1, EN2 = 0V, (V_{ISP} – $V_{GTP\_}$) = 5V	5	7.5	10	mA
Peak Pulldown Current	$I_{DIMOUTPD}$	(V_{ISP} – V_{GTP}) = 0V	4.5	7	9.5	mA
GTP_ Low Voltage with Respect to ISP			-5.5	-5.0	-4.4	V
GTP_ Turn-On Voltage		ISP rising	4.6	5.0	5.4	V
GTP_ Turn-Off Voltage				3.0		V
FAULT						
FB Overvoltage Threshold	V_{TH_OVP}	FB rising	1.22	1.24	1.28	V
FB Overvoltage Hysteresis				0.1		V
FB Input Bias Current	I_{FB}		-1		1	µA
Short Protection Threshold		ISP falling		4.7		V
Short Protection Hysteresis				0.1		V
Short Protection Timer				10		ms
Short Regulation	V_{ISP} - V_{ISN}	V_{ICTRL} > 0.32V		0.024		V
		V_{ICTRL} < 0.32V		(V_{ICTRL} – 0.2)/5		
FLT Output Voltage		I_{SINK} is 1mA after fault		0.05	0.3	V
FLT Leakage Current		V_{FLT} = 5.5V			1	µA
OFF TIME CONTROL						
Linear Range of Pulse Doubler				5		µs

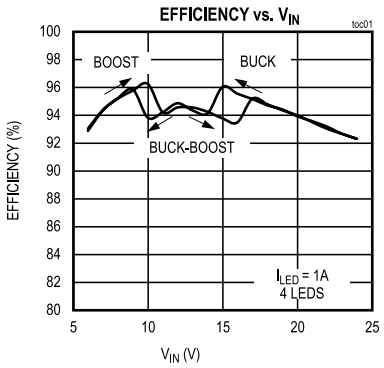
(V_{IN} = V_{INP} = 14V, T_J = -40°C to +125°C unless otherwise noted, (Note 1))

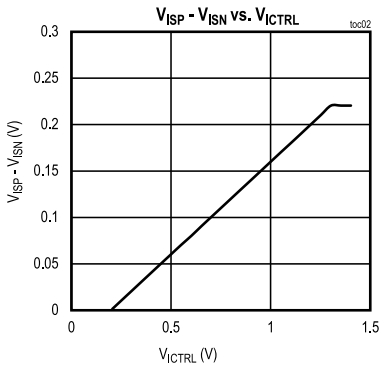
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	$T_{SHUTDOWN}$	Temperature Rising		165		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

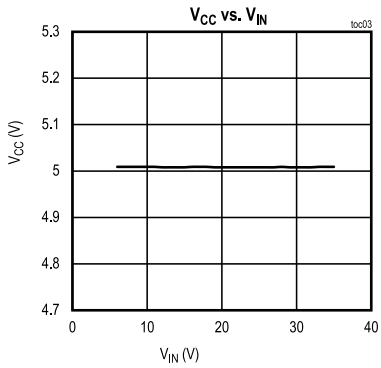
Note 1:	The MAX25603 is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.
Note 2:	The MAX25603 includes overtemperature protection to protect the device during momentary overload conditions. Junction temperature exceeds the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

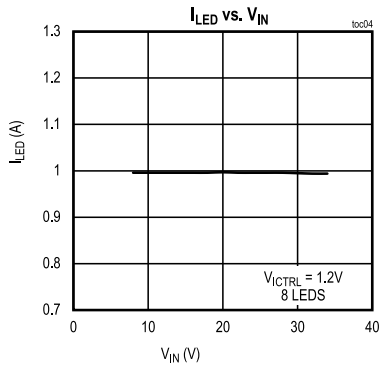
Typical Operating Characteristics

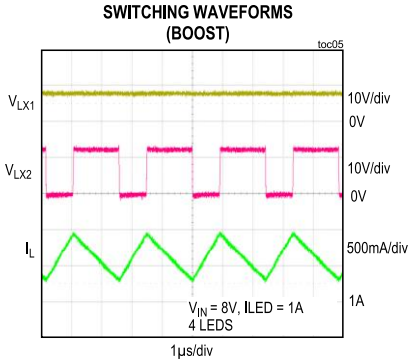
(TA = +25°C, unless otherwise noted.)

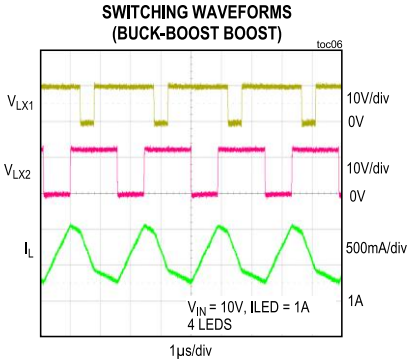






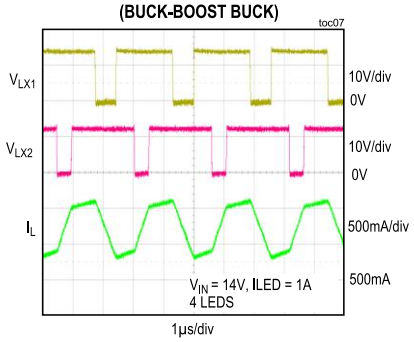




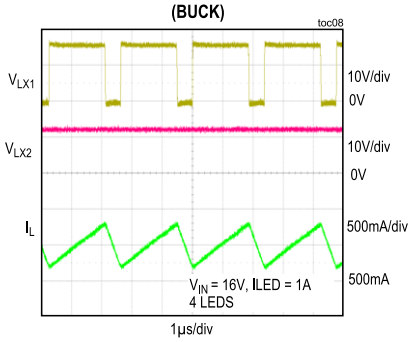


(TA = +25°C, unless otherwise noted.)

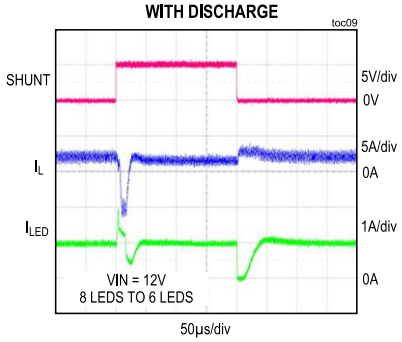
SWITCHING WAVEFORMS (BUCK-BOOST BUCK)



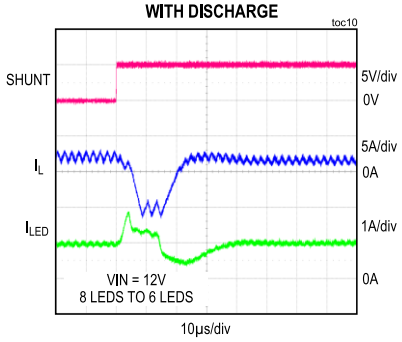
SWITCHING WAVEFORMS (BUCK)



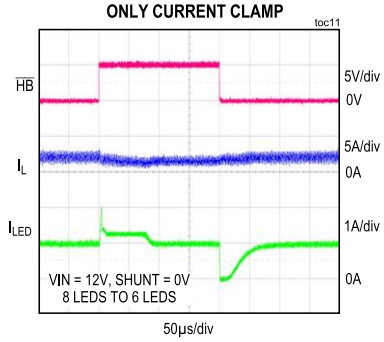
SHUNTING LEDS WITH DISCHARGE



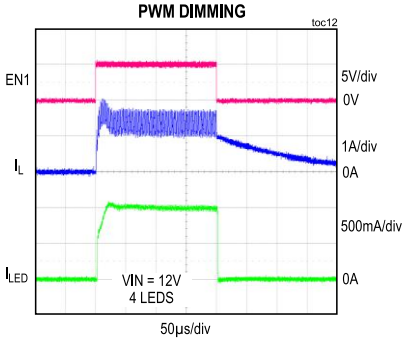
SHUNTING LEDS WITH DISCHARGE



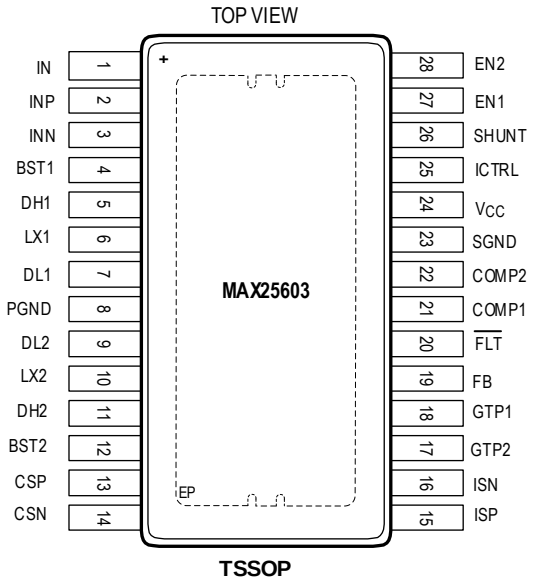
SHUNTING LEDS ONLY CURRENT CLAMP



PWM DIMMING



Pin Configurations



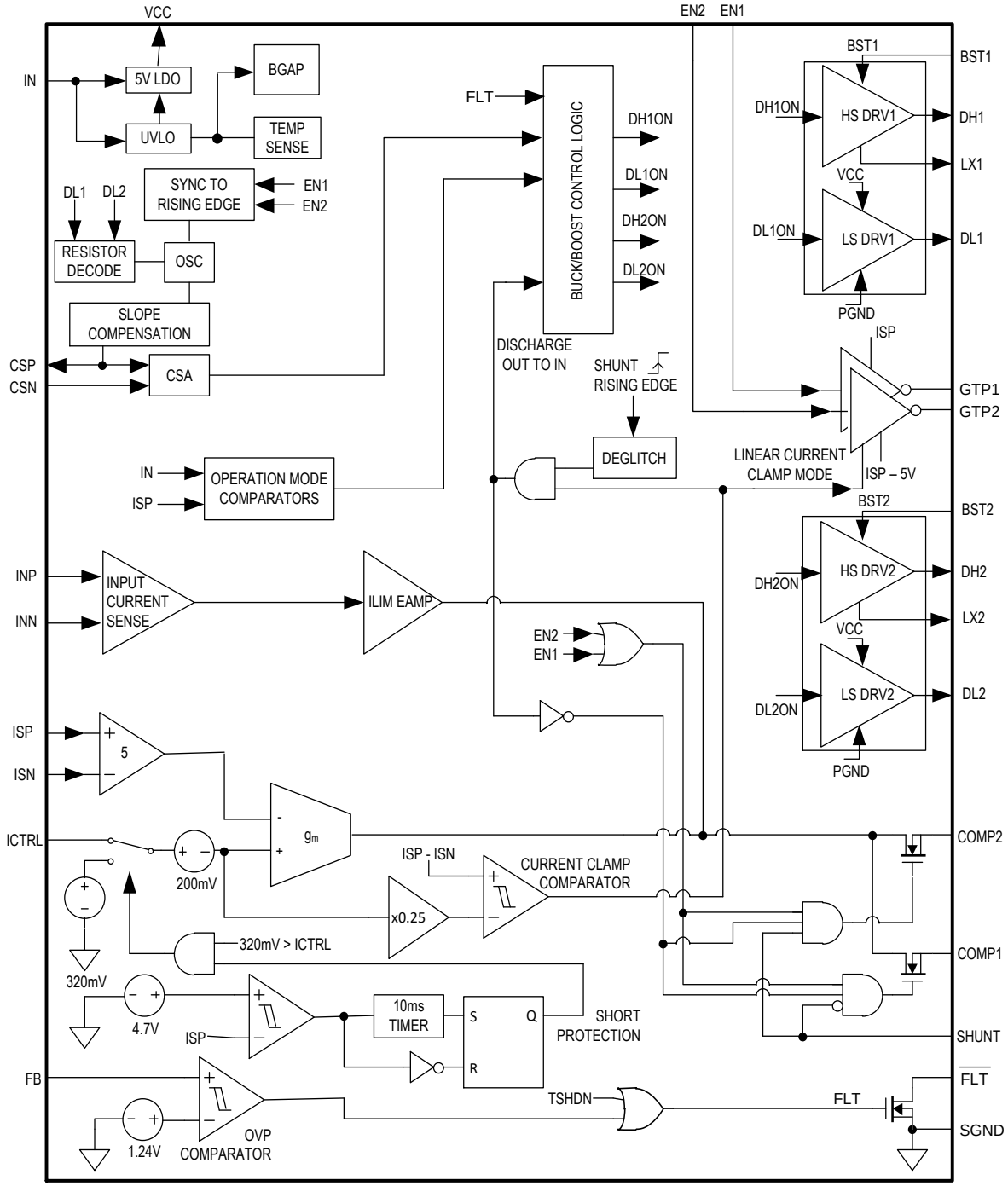
Pin Descriptions

PIN	NAME	FUNCTION
1	IN	Positive Power-Supply Input. Bypass IN to PGND with at least a 1µF ceramic capacitor.
2	INP	Positive Input for the Input Current Limit
3	INN	Negative Input for the Input Current Limit. Add an RC low-pass filter from INN to INP to provide a filtered DC voltage from INP to INN. The resistor should be 100Ω and the capacitor 0.1µF.
4	BST1	High-Side Power Supply for High-Side Gate Drive for Buck Section. Connect a 0.1µF ceramic capacitor from BST1 to LX1.
5	DH1	Top Gate Drive for Buck Section of the MAX25603. Drives the gate of the high-side nMOS.
6	LX1	Buck-Side Switching Node. LX1 pin swings from a diode voltage drop below ground up to V_{IN}.
7	DL1	Bottom Gate Drive for Buck Section of the MAX25603. Drives the gate of the low-side nMOS. A resistor from this pin to SGND also sets the switching frequency. Connect appropriate resistor from DL1 to SGND to set the switching frequency.
8	PGND	Power Ground Connection
9	DL2	Bottom Gate Drive for the Boost Section of the MAX25603. Drives the gate of the low-side nMOS. A resistor from this pin to SGND also sets the switching frequency. Connect appropriate resistor from DL2 to SGND to set the switching frequency.
10	LX2	Switching Node of Boost Section of the MAX25603. LX2 pin swings from a diode voltage drop below ground up to V_{OUT}.
11	DH2	Top Gate Drive for Boost Section of the MAX25603. Drives the gate of the high-side nMOS.
12	BST2	High-Side Power Supply for High-Side Gate Drive for Boost Section. Connect a 0.1µF ceramic capacitor from BST2 to LX2.
13	CSP	Positive Input to the Current-Sense Comparator for the Average-Current-Mode Controller.
14	CSN	Negative Input to the Current-Sense Comparator for the Average-Current-Mode Controller.
15	ISP	Positive LED Current-Sense Input. The voltage between ISP and ISN is proportionally regulated to 1.1V/5 or (V_{ICTRL} - 0.2)/5, whichever is less.

16	ISN	Negative LED Current-Sense Input
17	GTP2	Channel 2 High Side Gate Drive. The GTP2 pin drives an external high-side pMOS PWM switch with a voltage swing from V_{OUT} to (V_{OUT} – 5V). Leave this pin unconnected if not used.
18	GTP1	Channel 1 High-Side Gate Drive. The GTP1 pin drives an external high-side pMOS PWM switch with a voltage swing from V_{OUT} to (V_{OUT} –5V). Leave this pin unconnected if not used.
19	FB	Overvoltage-Protection Input for the LED String. Connect a resistive divider between the output, FB, and GND. When the voltage on FB exceeds 1.24V, a fast-acting comparator immediately stops PWM switching. V_{OVP} = 1.24 x (R_{FB1} + R_{FB2})/ R_{FB2}.
20	FLT	Active-Low, Open-Drain Fault Indicator Output. See the Fault Indicator (FLT) section.
21	COMP1	Compensation-Network Connection when SHUNT is low. For proper compensation, connect a suitable RC network from COMP1 to SGND.
22	COMP2	Compensation-Network Connection when SHUNT is high. For proper compensation, connect a suitable RC network from COMP2 to SGND.
23	SGND	Signal Ground Connection
24	V_{CC}	5V Regulator Output. Connect a minimum 2.2µF ceramic capacitor from V_{CC} to SGND for stable operation.
25	ICTRL	Analog Dimming-Control Input. Connect an analog voltage from 0 to 1.3V for analog dimming of LED current. I_{LED} = (V_{ICTRL} − 0.2V)/(5 × R_{LED}). Bypass ICTRL to GND with at least a 10nF ceramic capacitor for noise filtering. If V_{ICTRL} > 1.3V, the capacitor is not needed and LED current is clamped to I_{LED} = 1.1V/(5 × R_{LED}).
26	SHUNT	Drive this pin high when using PWM dimming across some LEDs in the string. SHUNT high enables compensation network on COMP2 and SHUNT low enables compensation network on COMP1.
27	EN1	Drive EN1 to enable pMOS gate drive on GTP1 and turn on LED string connected to pMOS drain on GTP1. Drive EN1 low to disable gate drive on GTP1 and turn off LED string on GTP1. Drive with a PWM signal to implement PWM dimming on GTP1.
28	EN2	Drive EN2 to enable pMOS gate drive on GTP2 and turn on LED string connected to pMOS drain on GTP2. Drive EN2 low to disable gate drive on GTP2 and turn off LED string on GTP2. Drive with a PWM signal to implement PWM dimming on GTP2.
-	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP must be connected to SGND.

Functional Diagrams

Block Diagram



Detailed Description

The MAX25603 is a synchronous four-switch, buck-boost LED driver controller suitable for multifunction automotive combination head lamps. The controller regulates the LED current for LED string voltages from 0V to 60V. The MAX25603 can be used as a seamless buck-boost LED driver for applications that require an efficient buck-boost LED driver with synchronous rectification. The MAX25603 is ideal for high-power applications that require a current source with PWM dimming capability.

The device provides seamless transition between buck, boost, and buck-boost modes depending on the ratio of input to output voltage. The MAX25603 is ideal for LED driver applications in automotive, industrial, and other LED lighting applications. A fault flag indicates open LED and thermal shutdown conditions. The device uses Analog Devices' proprietary average-current-mode control scheme and allows adjustable 200kHz to 440kHz fixed-frequency operation. In addition, ±6% triangular spread-spectrum is added internally to the oscillator to improve EMI performance. The MAX25603 provides both analog and digital PWM dimming in dual-string applications with time sharing. A single device can be used to power a daytime running light (DRL), position light, high beam, and low beam in an automotive front headlamp. The MAX25603 integrates two high-side pMOS drivers for PWM dimming applications that require fast rising and falling edges of the LED current. It also features robust output open and short protection, is AEC qualified, and is suitable for automotive applications.

The MAX25603 uses Analog Devices' proprietary architecture to limit LED current overshoots and overshoot durations during switchover in dual-string applications in time-sharing mode. In multistring applications in time-sharing mode, LED current overshoots during switchover between strings is minimized by an Analog Devices proprietary control scheme.

V_{CC} Regulator

The V_{CC} supply is the low-voltage analog supply for the chip and derives power from the input voltage from IN to PGND. An internal power-on-reset (POR) monitors the V_{CC} voltage and the IN voltage. A POR is generated when V_{CC} drops below its UVLO threshold, causing the IC to reset. The chip exits reset state once the input voltage goes back up and the V_{CC} linear regulator output is back in regulation.

Undervoltage Lockout

The MAX25603 features undervoltage lockout (UVLO) using the positive power-supply input (IN). The IC is enabled when IN exceeds the 4.1V threshold and disabled when IN drops below the 3.8V threshold. The IN UVLO is internally fixed and cannot be adjusted. When IN exceeds its UVLO, the internal LDO is enabled. Once V_{CC} exceeds 4.2V, there is a start-up delay of 550µs. Then, the converter is enabled.

H-Bridge Operation

The H-bridge configuration using the MAX25603 is shown in *Figure 1*. The H-bridge consists of the four switches: N1, N2, N3, and N4. Switches N1 and N2 are in series with the input voltage, and switches N3 and N4 are connected to the output. Inductor L is connected as shown in *Figure 1*. There are four different configurations in which the circuit operates, depending on the ratio of the input and output voltages.

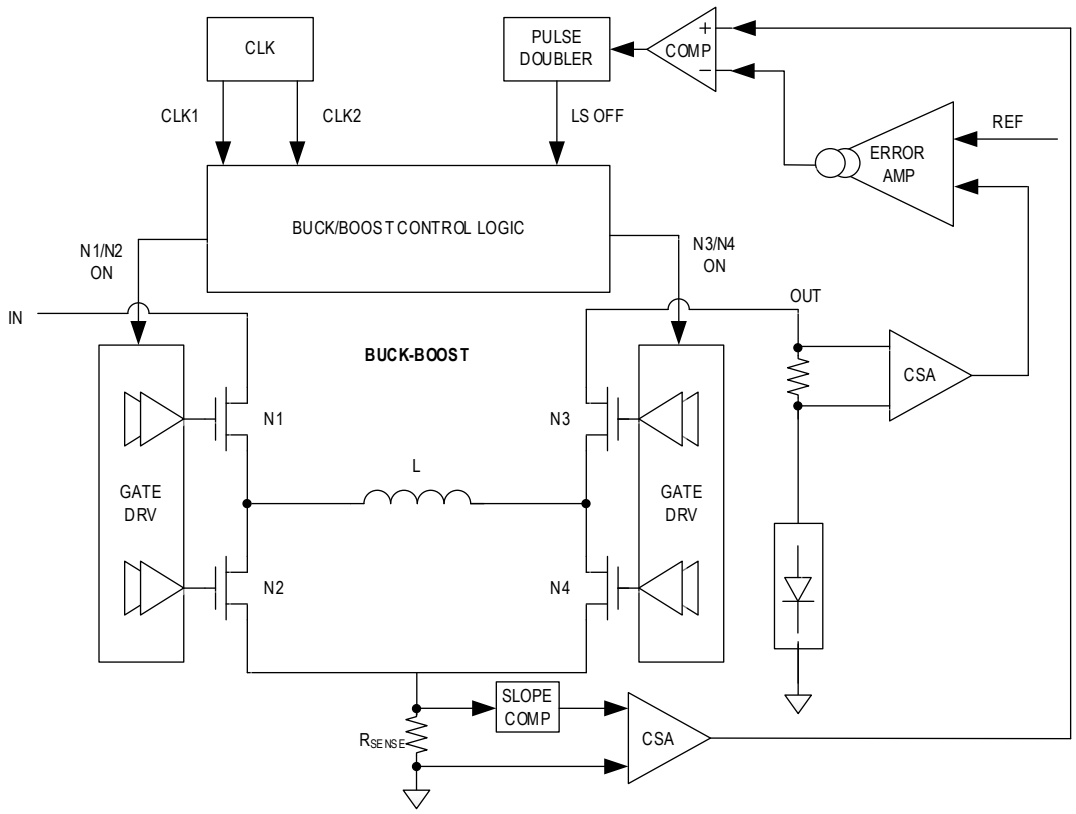


Figure 1. Bridge LED Driver

Table 1 shows the status of the switches in the H-Bridge in each configuration.

Table 1. Status of Switches in H-Bridge

SWITCH	BOOST MODE	BUCK-BOOST MODE (BOOST CONTROL)	BUCK-BOOST MODE (BUCK CONTROL)	BUCK MODE
N1	ON	SWITCHING	SWITCHING	SWITCHING
N2	OFF	SWITCHING	SWITCHING	SWITCHING
N3	SWITCHING	SWITCHING	SWITCHING	ON
N4	SWITCHING	SWITCHING	SWITCHING	OFF

Buck Mode

When the input voltage is much higher than the output voltage, the MAX25603 operates in buck mode. In this configuration, switch N3 is always on and switch N4 is always off. Switch N2 is turned on at the beginning of the clock cycle (CLK1), and the inductor current ramps down. The MAX25603 uses an average-current-mode control scheme to determine the ON pulse width for switch N2. Once N2 is turned off, N1 is turned on. Switches N1 and N2 alternate, behaving like a synchronous buck regulator.

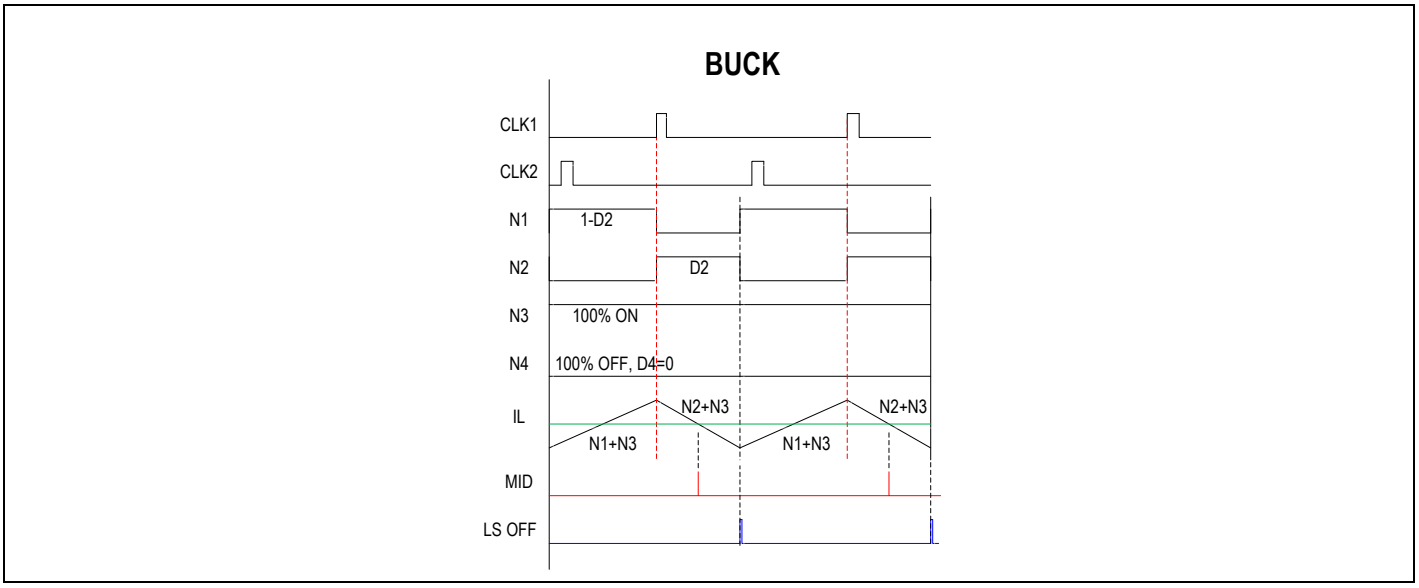


Figure 2. Buck-Mode Waveforms

Boost Mode

When the input voltage is much lower than the output voltage, the MAX25603 operates in boost mode. In this configuration, switch N1 is always on and switch N2 is always off. Switch N4 is turned on at the beginning of the clock cycle (CLK2), and the inductor current ramps up. The MAX25603 uses an average-current-mode control scheme to determine the ON pulse width for switch N4. Once N4 is turned off, N3 is turned on. Switches N3 and N4 alternate, behaving like a synchronous boost regulator.

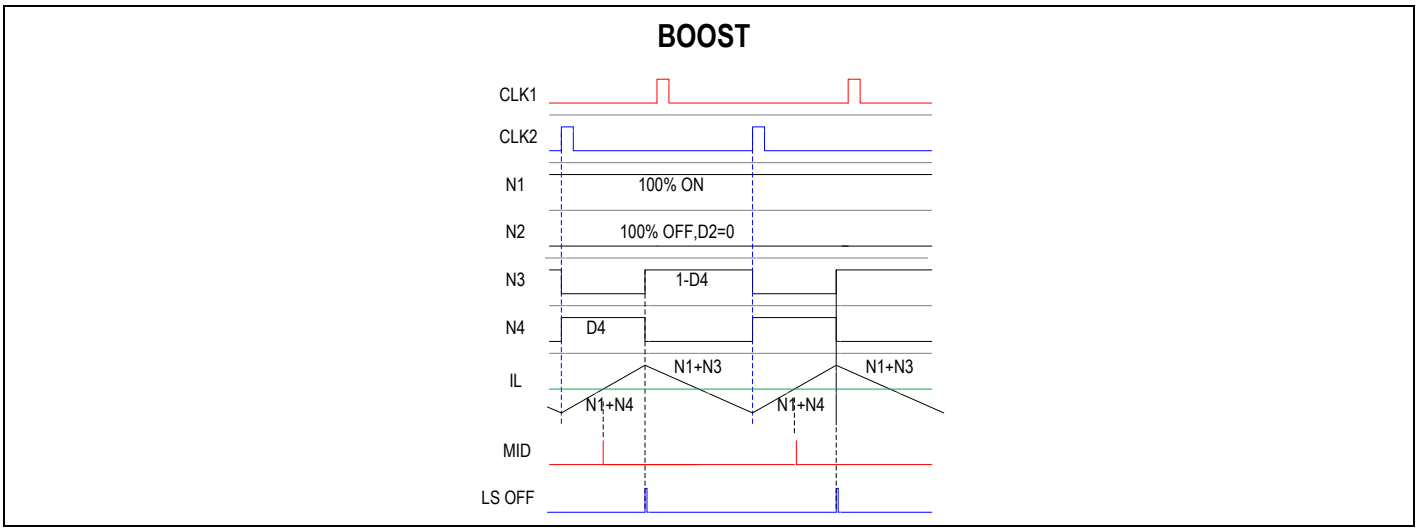


Figure 3. Boost-Mode Waveforms

Buck-Boost Mode

When V_{IN} is close to V_{OUT}, the MAX25603 operates in buck-boost configuration. In this configuration, all four switches have PWM voltages on the gates, and all four switches are switching at the switching frequency. There are two different configurations in the buck-boost mode.

When V_{IN} is slightly higher than V_{OUT}, the MAX25603 operates in the buck-boost region, where switch N2 is controlled by the PWM. Switch N4 is turned on for the beginning 16.7% cycle triggered by clock CLK2, and switch N3 is turned on for the remaining 83.3% cycle. Control of switch N2 is initiated by clock CLK1. N2 is turned on and N1 is turned off when CLK1 goes

high. The MAX25603 uses average-current-mode control to determine the ON pulse width of N2. When N2 is turned off, N1 is turned on immediately.

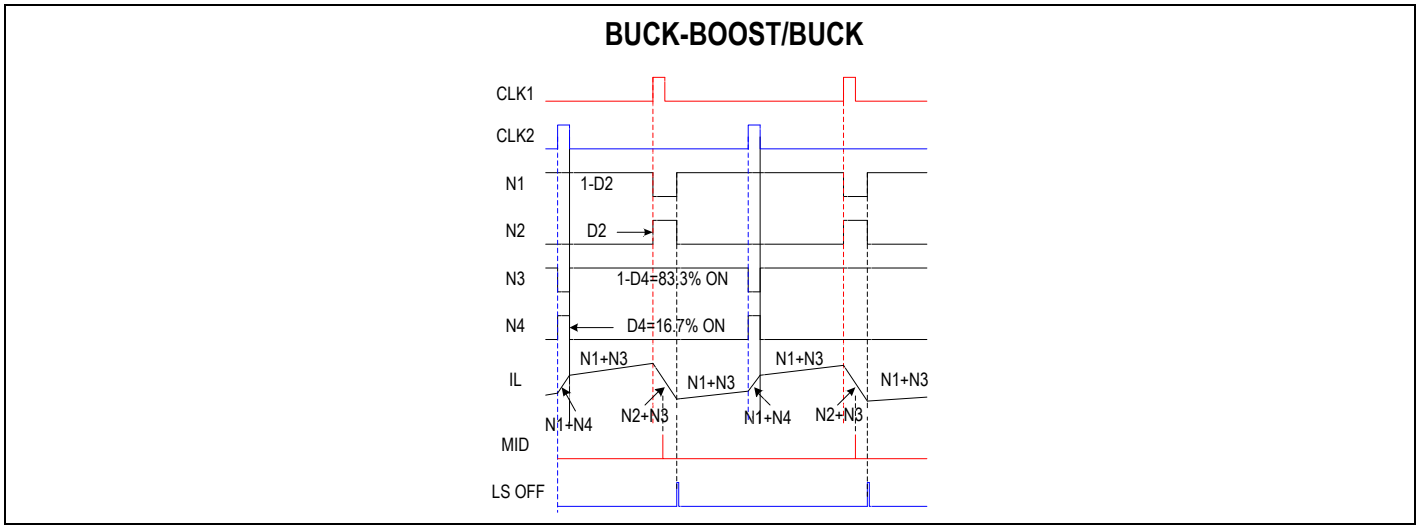


Figure 4. Buck-Boost Buck-Mode Waveforms

When V_{IN} is slightly lower than V_{OUT}, the MAX25603 operates in the buck-boost region where switch N4 is controlled by the PWM. Switch N2 is turned on for the beginning 16.7% cycle triggered by clock CLK1 and switch N1 is turned on for the remaining 83.3% cycle. Control of switch N4 is initiated by clock CLK2. N4 is turned on and N3 is turned off when CLK2 goes high. The MAX25603 uses average-current-mode control to determine the ON pulse width of N4. When N4 is turned off, N3 is turned on immediately.

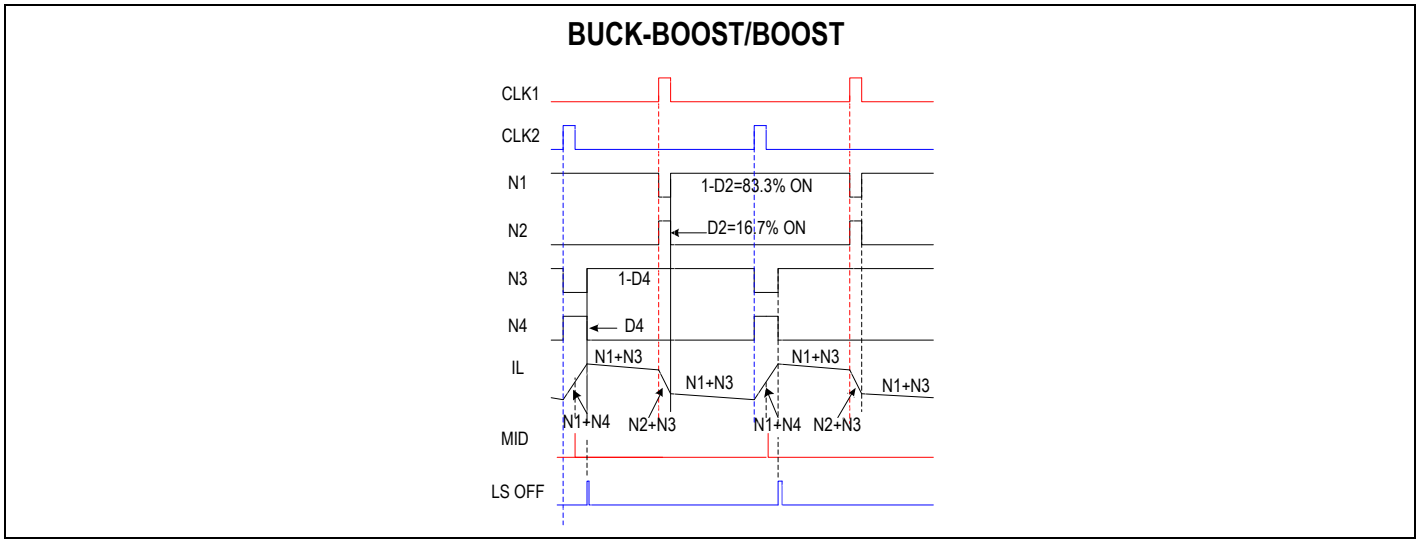


Figure 5. Buck-Boost Boost-Mode Waveforms

Maximum Proprietary Average-Current-Mode Control

A novel average-current-mode control scheme is used in this current-mode buck-boost H-bridge converter. Instead of regulating the peak/valley current in buck/boost mode, average inductor current is regulated regardless of operating mode. As long as the inductor current is not changed abruptly during the mode transitions, the command signal remains at a nearly constant value unrelated to operating modes. As a result, seamless mode transition can be achieved. Since the converter is

operating at a fixed switching frequency, additional slope compensation must be added to the inductor current-sense signal, which may require slight changes to the command signal to compensate for the error introduced by the slope compensation signal.

Average-Current-Mode Buck

When operating in buck mode, the pulse doubler controls the duty cycle of switch N2. The pulse width of switch N2 is 2x tpw.

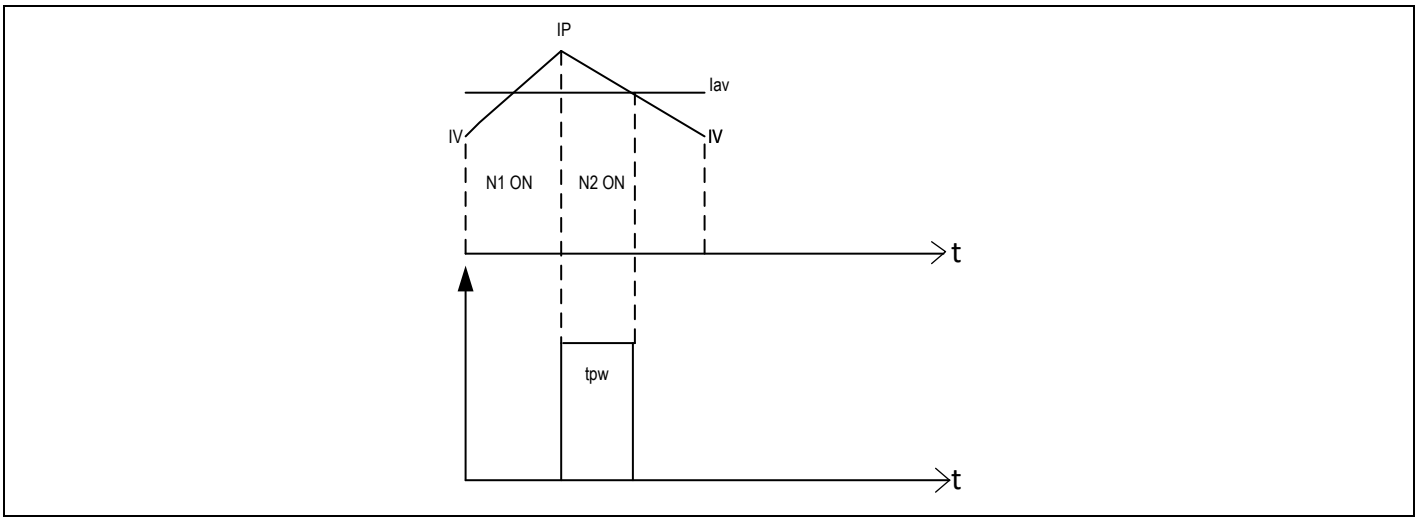


Figure 6. Pulse Doubler Buck

Average Current-Mode Boost

When operating in boost mode, the pulse doubler controls the duty cycle of switch N4. The pulse width of switch N4 is 2x tpw.

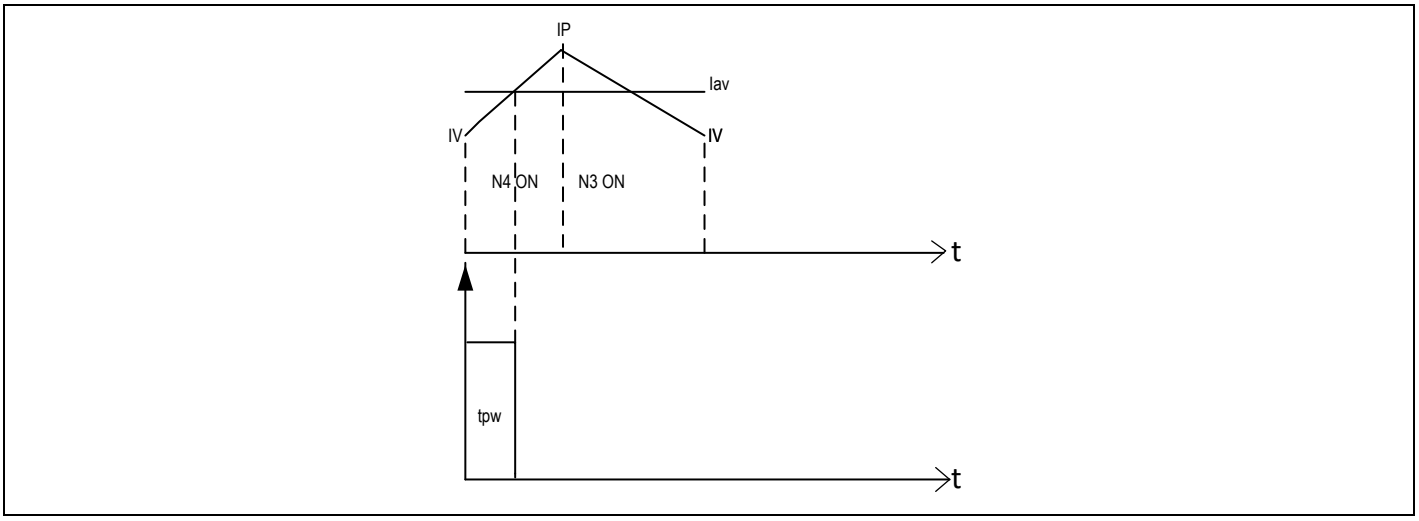


Figure 7. Pulse Doubler Boost

Switching Frequency

The internal oscillator of the MAX25603 is programmable from 200kHz to 440kHz using a single resistor at DL1 and DL2. An additional ±6% spread spectrum is added internally to the oscillator to improve EMI performance.

Analog Dimming (ICTRL)

The MAX25603 offers an analog dimming-control input (ICTRL). The LED current can be linearly adjusted from zero to full scale for ICTRL voltage in the range of 0.2V to 1.2V. Full scale regulates V_{ISP} - V_{ISN} to 200mV. For V_{ICTRL} > 1.3V, an

internal reference sets the LED current and regulates V_{ISP} - V_{ISN} to 220mV. The maximum withstand voltage of this input is 5.5V. The LED current is guaranteed to be at zero when the ICTRL voltage is at or below 0.18V.

EN1 and EN2

EN1 and EN2 are the input signals that control the switching of the H-bridge and control the two high-side pMOS gate drivers on the MAX25603. EN1 turns on the H-bridge and the pMOS connected on GTP1. EN2 turns on the H-bridge and the pMOS connected to GTP2. EN1 has priority over EN2. If both EN1 and EN2 are high, only the pMOS on GTP1 is turned on. When EN1 is low GTP1 is turned off and when EN2 is low, GTP2 is turned off. PWM dimming is achieved by applying the appropriate dimming signal to EN1 or EN2. EN2 can be left high while EN1 is toggled. If simultaneously toggling EN1 and EN2, ensure there is at least a 1µs dead time between the falling and rising edges of the inputs.

SHUNT and COMP1/COMP2

The MAX25603 includes two compensation pins, which are connected to the output of the internal error amplifier depending on the state of the SHUNT pin. When the SHUNT input is low, the error amplifier output is connected to COMP1 and when SHUNT input is high, the error amplifier is connected to COMP2. Connect the appropriate compensation network from COMP1 to ground and from COMP2 to ground for stable operation.

Current Clamp and Output Discharge

Typical LED drivers experience a sharp overshoot in LED current when transitioning from driving a higher number to a lower number of LEDs. The MAX25603 features a comparator that trips when the voltage across the LED current-sense resistor, V_{ISP} - V_{ISN}, indicates that the LED current is more than 125% of the current programmed by ICTRL. When this occurs, GTP1 or GTP2 drive the high-side pMOS dimming switch as a linear current clamp to limit the LED current. The clamp level scales linearly with ICTRL. For ICTRL less than 420mV, the regulated voltage across $V_{ISP - ISN}$ is fixed to 55mV.

If the current clamp comparator is concurrently triggered on a rising edge on the SHUNT pin, MAX25603 controls the H-bridge to build negative inductor current and discharge the output capacitor back to IN. The H-bridge turns on N2 and N3 while N1 and N4 are off to drive the inductor current negative. N1 and N4 then commutate with N2 and N3 to hysterically regulate V_{CSP} - V_{CSN} to 63mV with a hysteresis of 15mV. Once current clamp deactivates, there is a 5µs deglitch to deactivate discharge. At that time, the H-bridge turns on N1 and N4 while N2 and N3 are off until the inductor current is positive again and normal switching resumes. To prevent discharge from triggering inadvertently, SHUNT has a 2µs deglitch filter and the current clamp comparator is blanked for an additional 1µs after the deglitch before discharge begins. Once discharge is activated, it cannot trigger again until the next rising edge of SHUNT.

In *Figure 8*, the solid waveforms on SHUNT and ILED indicate events when output discharge occurs. The dashed waveforms indicate events when output discharge does not occur.

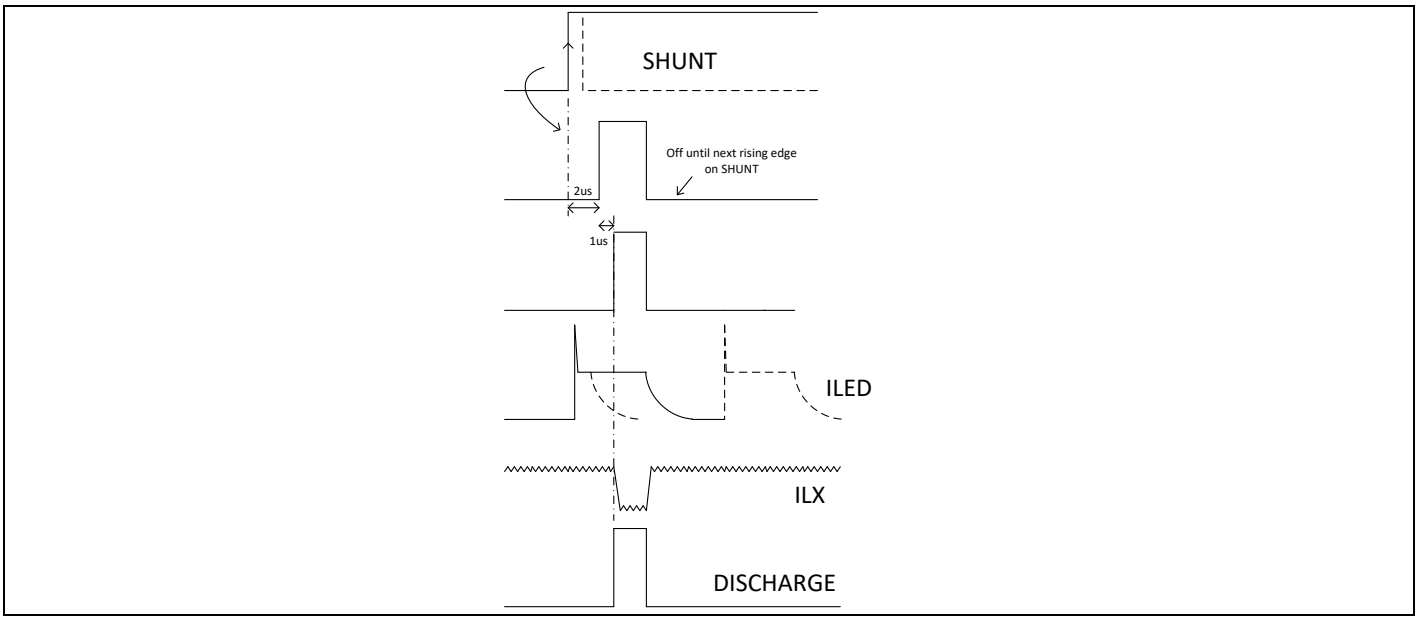


Figure 8. Output Discharge

In the typical application circuit shown in *Figure 11*, the clearance lamp LEDs (CLL) are normally dimmed with a 200Hz to 400Hz PWM signal on EN1. This same PWM can also be tied to SHUNT to improve transient response. When SHUNT changes state, the GTP1 switch turns on or off and the output of the error amplifier alternates between COMP1 and COMP2. COMP1 and COMP2 store the appropriate COMP voltage for each of the respective number of LEDs active on the string – i.e., COMP1 has the COMP voltage for 8 LEDs while COMP2 has the COMP voltage stored for 4 LEDs. When SHUNT is a rising edge, the voltage across the LED current-sense resistor hits the clamp voltage and the output discharge is triggered. When the HB_ON/OFF switch is toggled, the voltage across the LED current-sense resistor triggers the LED current clamp, but the output discharge routine does not begin if SHUNT is stable.

Error Amplifer

The sensed inductor current is controlled by the voltage on either the COMP1 or COMP2 pin, which is the output of the error amplifier. When utilizing PWM dimming on EN1 or EN2, the MAX25603 disconnects the error amplifier from the compensation network when EN1 and EN2 are low. The error amplifier is also disconnected during the output discharge routine. The error amplifier is reconnected only when either EN1 or EN2 is high and the output discharge routine is complete.

Start-Up

An initial start-up sequence is performed for both COMP1 and COMP2 the first time either compensation network is selected by the SHUNT pin. N1 and N3 are off while N2 and N4 are on and switching begins once COMP rises above an internal threshold.

Input-Current Limit

The MAX25603 features circuitry that limits the input current during line dropouts. If desired, this circuitry can be disabled by shorting INN and INP pins together. If DC input-current limiting is desired during low input voltages, then a current-sense resistor R_{IN} should be used. Use the circuit shown in *Figure 9* to limit the input current.

An RC filter and a series resistor to INN should be used as shown. The input current is limited to IN_{MAX}, where IN_{MAX} is given by the following equation:

$$IN_{MAX} = 0.1/R_{IN}$$

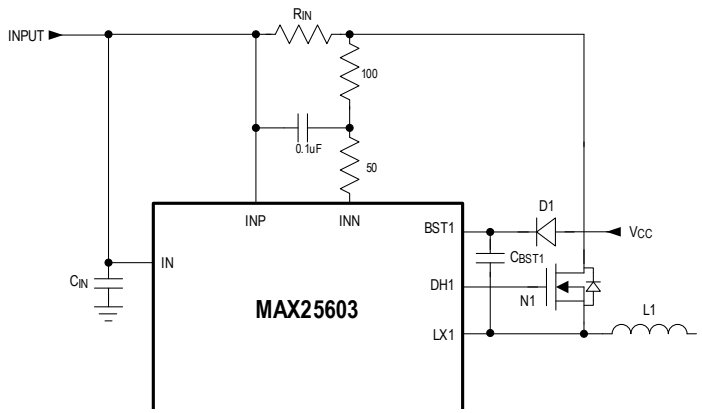


Figure 9. Input-Current Limit

Overvoltage Protection (FB)

Pin FB sets the overvoltage-threshold limit across the LEDs. Use a resistive divider between ISP to FB and SGND to set the overvoltage-threshold limit. An internal overvoltage-protection comparator senses the voltage across FB and SGND. If the voltage is greater than 1.24V, the switching is turned off and FLT asserts. Switching resumes when the voltage at FB drops below 1.23V and EN1 or EN2 is high. EN1 and EN2 maintain control of GTP1 and GTP2 during an overvoltage condition. FLT deasserts only if EN1 or EN2 is high and V_{ISP} - V_{ISN} is > 24mV.

Short-Circuit Protection

A short-circuit condition across the LED string is detected when the voltage on ISP falls below 4.7V for at least 10ms. The regulation point of the voltage across the LED current-sense resistor is determined by the lower of 320mV or ICTRL. A short-circuit does not assert FLT. The short-circuit condition is cleared when ISP rises above 4.8V.

Fault Indicator (FLT)

The MAX25603 features an active-low, open-drain fault indicator (FLT). FLT asserts when one of the following conditions occur:

- Overvoltage or open across the LED string
- Overtemperature condition

For overvoltage, FLT asserts only when a fault occurs with EN1 or EN2 in the high state. Once asserted, the FLT remains low and only changes state if EN1 or EN2 is high, the fault condition is removed, and the voltage across the LED current-sense resistor is greater than 24mV. The FLT signal never changes state when EN1 and EN2 are low.

Applications Information

Figure 11 shows a typical MAX25603 application circuit. External-component selection is driven by the input voltage range and LED string voltage and current requirements.

V_{CC} Regulator

The internal 5V regulator is used to power the internal control circuitry inside the MAX25603. This regulator can provide a load of 50mA to the internal and external circuitry, and requires an external ceramic capacitor for stable operation. A 2.2µF ceramic capacitor is adequate for most applications. Place the ceramic capacitor close to the IC to minimize trace length to the internal V_{CC} pin and also to the IC ground. Choose a low-ESR, X7R ceramic capacitor for optimal performance. The IC powers up once the voltage on V_{CC} crosses the undervoltage lockout (V_{CC} UVLO) rising threshold and shuts down when V_{CC} falls below the (V_{CC} UVLO) falling threshold.

Bootstrap Capacitor and Diode

A bootstrap circuit is used to drive the floating gate drivers on DH1 and DH2. The bootstrap capacitors, C_{BST1} and C_{BST2}, provide the gate charge to the high-side nMOS when they are on and are recharged when the low-side nMOS are on. Connect a 0.1µF ceramic capacitor from BST1 to LX1 and BST2 to LX2.

Select the bootstrap diode based on the average gate-drive current and blocking voltage for the diode. The maximum blocking voltage must be high enough to block the maximum drain-to-source voltage for the high-side nMOS. The average gate-drive current through the diode can be calculated as:

$$I_G = Q_G \times f_{SW}$$

where Q_G is the total gate charge of the nMOS. Use a silicon diode. A Schottky diode has a lower forward voltage drop and can minimize loss, but also has the downside of a large reverse leakage current at high temperatures. This can discharge the bootstrap capacitor and shut off the gate driver. Connect the bootstrap diodes from V_{CC} to BST1 and from V_{CC} to BST2.

Programming the LED Current

Normal sensing of the LED current should be done on the high side, where the LED current-sense resistor is connected to the anode of the LED string. The LED current is programmed using the resistor R_{LED} (see the Simplified Application Circuit). The LED current can also be programmed by adjusting the voltage on ICTRL when $V_{ICTRL} \le 1.2V$ (analog dimming). The current is given by the following equation:

$$I_{LED} = (V_{ICTRL} - 0.2)/(5 \times R_{LED})$$

For voltages greater than 1.3V on the ICTRL pin, the LED current is clamped to the current given by the following equation:

$$I_{LED} = (1.3 - 0.2)/(5 \times R_{LED})$$

LED current can also be sensed on the ground side, if needed. In some applications, the LED current can be sensed by a current-sense resistor R_{LED} to ground.

Programming the Switching Frequency

The internal oscillator of the MAX25603 is programmable from 200kHz to 440kHz using a single resistor at DL1 and DL2. Select the appropriate R_{DL1} and R_{DL2} resistors according to *Table 2*:

Table 2. Frequency Selection R_{DL1} and R_{DL2}

f_{SW}	R_{DL1}	R_{DL2}
200kHz	10kΩ	10kΩ
230kHz	20kΩ	10kΩ
260kHz	30kΩ	10kΩ
290kHz	10kΩ	20kΩ
320kHz	20kΩ	20kΩ
350kHz	30kΩ	20kΩ
380kHz	10kΩ	30kΩ
410kHz	20kΩ	30kΩ
440kHz	30kΩ	30kΩ

An additional ±6% spread-spectrum is added internally to the oscillator to improve EMI performance.

Programming Input-Current Limit

The MAX25603 has an input current-sense amplifier that can be used to limit the input, as calculated by the following equation:

$$IIN = 0.1/R_{IN}$$

A low-pass RC filter is needed for loop stability. For most applications, a 100Ω resistor RF and a 100nF capacitor CF are sufficient. An added 50Ω resistor RINN in series with the INN pin should be added, as shown in *Figure 9*.

Setting the Overvoltage Threshold

The overvoltage threshold is set by resistors R_{FB1} and R_{FB2}. The overvoltage circuit in the MAX25603 is activated when the voltage on FB with respect to GND exceeds 1.24V. Use the following equation to set the desired overvoltage threshold:

$$V_{OVP} = 1.24 \times (R_{FB1} + R_{FB2})/R_{FB2}$$

Selecting the Inductor

In the boost converter, the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage. When operating the boost converter, the average inductor current is equal to the input current. Calculate maximum duty cycle using the following equation:

$$D_{MAX} = (V_{LED} - V_{INMIN})/V_{LED}$$

where V_{LED} is the forward voltage of the LED string, in volts, and V_{INMIN} is the minimum input supply voltage, in volts.

Use the following equations to calculate the maximum average inductor current (IL_{AVG}), peak-to-peak inductor-current ripple (ΔIL), and peak inductor current (I_{LP}):

Maximum average inductor current is given by:

$$IL_{AVG} = I_{LED}/(1 - D_{MAX})$$

Allowing the peak-to-peak inductor ripple to be ΔIL, the peak inductor current is given by:

$$IL_P = IL_{AVG} + 0.5 \times \Delta IL$$

The inductance value (L) of inductor L1, in Henrys (H), is calculated as:

$$L = V_{INMIN} \times D_{MAX}/(f_{SW} \times \Delta IL)$$

where f_{SW} is the switching frequency in Hertz, V_{INMIN} is in volts, and ΔIL is in amperes.

Choose an inductor with a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than I_{LP} at the operating temperature.

When operating in buck mode, the average inductor current is the same as the LED current. The peak inductor current occurs at the maximum input line voltage where the duty cycle is at the minimum:

$$D_{MIN} = V_{LED}/V_{INMAX}$$

where V_{LED} is the forward voltage of the LED string, in volts, and V_{INMAX} is the maximum input supply voltage, in volts.

The peak inductor current is given by:

$$I_{LP} = I_{LED} + 0.5 \times \Delta IL$$

The inductance value (L) of inductor L1, in Henrys, is calculated as:

$$L = (V_{INMAX} - V_{LED}) \times D_{MIN}/(f_{SW} \times \Delta IL)$$

where f_{SW} is the switching frequency in Hertz, V_{INMAX} is in volts, and ΔIL is in amperes.

Choose an inductor with a minimum inductance greater than the calculated value. The chosen inductor for the application should have an inductance larger of the two calculated values from the boost and the buck configurations.

Selecting the Input Capacitor

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. The input ripple consists of ΔVQ (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. A good starting point for the selection of C_{IN} is to use an input-voltage ripple of 2% to 10% of V_{IN}. C_{IN_MIN} can be selected as follows:

$$C_{IN\_MIN} = (D \times (1\text{-}D) \times I_{LED} \times t_{ON})/\Delta V_{IN}$$

where t_{ON} is the on-time pulse width per switching cycle.

When selecting a ceramic capacitor, pay special attention to the operating conditions of the application. Ceramic capacitors can lose more than half of their capacitance at their rated DC-voltage bias and also lose capacitance with extremes in temperature. In applications with PWM dimming, where the input connections to the source have wiring inductance, additional electrolytic capacitors may need to be added at the input to prevent large sags and surges in the input voltages during the PWM rising and falling edges. These line sags and surges can also cause the H-bridge to switch between boost, buck-boost, and buck configurations in one dimming cycle, which is undesirable and can cause flicker problems.

Selecting the Output Capacitor

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise generated by the ceramic capacitors during PWM dimming, it may be necessary to minimize the number of ceramic capacitors on the output. In these cases, an additional electrolytic or tantalum capacitor provides most of the bulk capacitance.

For simplicity, assume the bulk capacitance accounts for most of the output ripple. The capacitance for boost configuration is given by:

$$C_{BOOSTOUT} > (I_{LED} \times D_{MAX})/(V_{OUTRIPPLE} \times f_{SW})$$

where I_{LED} is in amperes, C_{OUT} is in farads, f_{SW} is in Hertz, and $V_{OUTRIPPLE}$ is in volts.

The corresponding LED current ripple is then given by:

$$I_{LEDRIPPLE} = V_{OUTRIPPLE}/(R_{LED} + R_D)$$

where R_{LED} is the LED current-sense resistor and R_D is the dynamic impedance of the LED string.

Minimizing Crosstalk Between LED Strings

Some designs have additional capacitance placed immediately across the LED string to minimize LED current ripple. When simultaneously togging EN1 and EN2, in either a two-string design or a one-string design in which the pMOS on GTP1 is used a shunting switch, ensure the extra capacitance across the LEDs is minimized. In *Figure 10*, when EN2 is high, the MAX25603 drives four LEDs and when EN1 is high, it drives two LEDs.

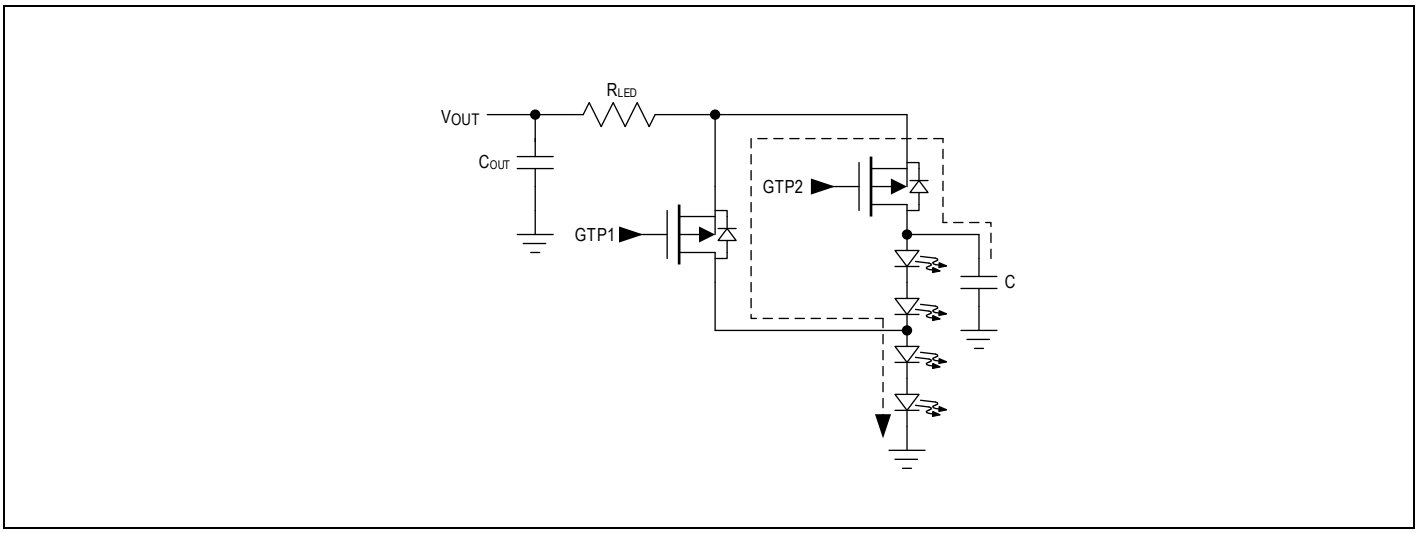


Figure 10. LED Current Ripple Capacitor

When EN1 goes high, V_{OUT} begins to slew down to the output voltage necessary to drive two LEDs. At the same time, the body diode on the GTP2 pMOS becomes forward biased and the extra charge on capacitor C slightly increases the LED current while V_{OUT} is slewing. This additional current, as indicated by the dashed line, can be approximated by:

$$I = C \times dVOUT/dt$$

Where dVOUT is the change in output voltage and dt is the time it takes to slew to the new output voltage. For most designs, keep the additional LED current ripple capacitor below 0.1µF.

H-Bridge Control Loop Current-Sense Selection (R_{SENSE})

The control loop uses average-current-mode control in both boost and buck mode to control the H-bridge switches. The current-sense resistor on the low side of the H-bridge, R_{SENSE}, is chosen based on the peak inductor current and slope compensation. This occurs in boost mode with the maximum output power at minimum input voltage, V_{INMIN}. R_{SENSE} is given by:

$$R_{SENSE} = 80mV/(IL_P + (D_{MAX} \times (V_{LED} - 2 \times V_{INMIN}) \times 3)/(2 \times L \times f_{SW}))$$

R_{SENSE} also determines the peak, negative inductor current during the discharge sequence:

$$IL_{PDIS} = 63mV/R_{SENSE}$$

Slope Compensation

Slope compensation should be added to fixed-frequency converters operating in continuous-conduction mode with more than 50% duty cycle to avoid current-loop instability and sub-harmonic oscillations.

In the MAX25603, the slope-compensating ramp is added to the current-sense signal before it is fed to the PWM comparator. The device generates a current ramp with a slope of 50µA × f_{SW} for slope compensation. The current-ramp signal is forced into the slope compensation resistor, R_{SLOPE}, thereby adding a programmable slope-compensating voltage, V_{SLOPE}, at the current-sense input, CSP. Connect R_{SLOPE} between CSP and R_{SENSE}.

$$dV_{SLOPE}/dt = (R_{SLOPE} \times 50\mu A) \times f_{SW}$$

The slope-compensation voltage that must be added to the current signal at minimum line voltage, with margin of 1.5x, is as follows:

Boost configuration:

$$V_{SLOPE} = ((V_{LED} - 2 \times V_{INMIN}) \times R_{SENSE})/(2 \times L \times f_{SW}) \times 2 \times 1.5$$

Buck configuration:

$$V_{SLOPE} = (V_{LED} \times R_{SENSE})/(L \times f_{SW}) \times 2 \times 1.5$$

Control Loop Compensation

The LED current-control loop comprising the switching converter, LED current amplifier, and the error amplifier should be compensated for stable control of the LED current in all modes of operation. For most applications, the design must first be stabilized for boost mode of operation. The buck mode loop has a higher loop gain and higher frequency load pole. After compensation components are calculated for boost operation, ensure these values still place the unity gain in buck operation to less than 1/10 of f_{SW}.

The switching converter small-signal transfer function has a right half-plane (RHP) zero for the boost configuration as the inductor current is in the continuous-conduction mode. The RHP zero adds a 20dB/ decade gain together with a 90° phase lag, which is difficult to compensate. The easiest way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

Boost configuration:

$$f_{ZRHP} = (V_{LED} \times (1- D_{MAX})^2)/(2\pi \times L \times I_{LED})$$

The switching converter small-signal transfer function also has an output pole for the boost configuration. The effective output impedance that determines the output pole frequency together with the output filter capacitance is calculated as:

Boost configuration:

$$R_{OUT} = ((R_{LED} + R_D \times V_{LED})/((R_{LED} + R_D) \times I_{LED} + V_{LED})$$

where R_D is the dynamic impedance of the LED string at the operating current and R_{LED} is the LED current-sense resistor.

The output pole frequency is calculated as follows:

$$f_P = 1/(2\pi \times R_{OUT} \times C_{OUT})$$

The feedback-loop compensation is done by connecting a resistor (R_{COMP}) and capacitor (C_{COMP}) in series from COMP to GND. R_{COMP} is chosen to set the high frequency integrator gain for fast transient response, while C_{COMP} is chosen to set the integrator zero to maintain loop stability. For optimum performance, choose the components using the following equations:

$$f_C = 0.2 \times f_{ZRHP}$$

$$R_{COMP} = (2 \times f_{ZRHP} \times R_{SENSE})/(f_P \times (1- D_{MAX}) \times R_{LED} \times 5 \times g_m)$$

where g_m = 1.8mS (transconductance of error amplifier), R_{SENSE} is the current-sense resistor on the low side of H-Bridge, and R_{LED} is the LED current-sense resistor.

$$C_{COMP} = 1/(2\pi \times R_{COMP} \times f_P)$$

With R_{COMP} and C_{COMP} selected, confirm that when in buck mode, the unity gain is still less than 1/10 of f_{SW}. Note that in buck mode, R_{OUT} reduces as there are a lower number of LEDs.

Buck configuration:

$$f_C = f_{P\_BUCK} \times ((g_m \times R_{LED} \times R_{COMP})/(2 \times R_{SENSE}) - 1)$$

Typical Application Circuits

Single LED String Application Circuit

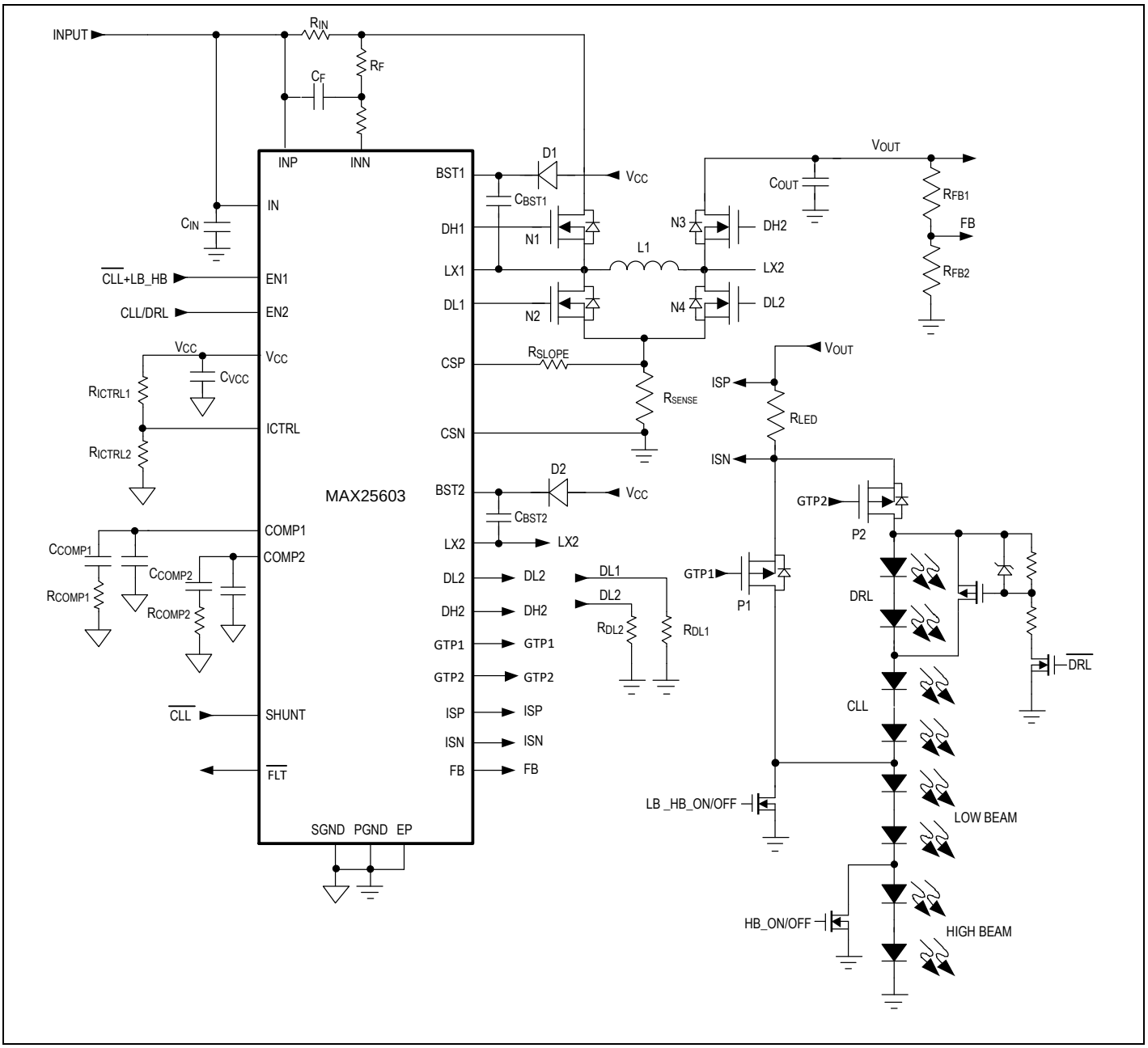


Figure 11. MAX25603 in a Combination Head Lamp

Multiple LED String Application Circuit

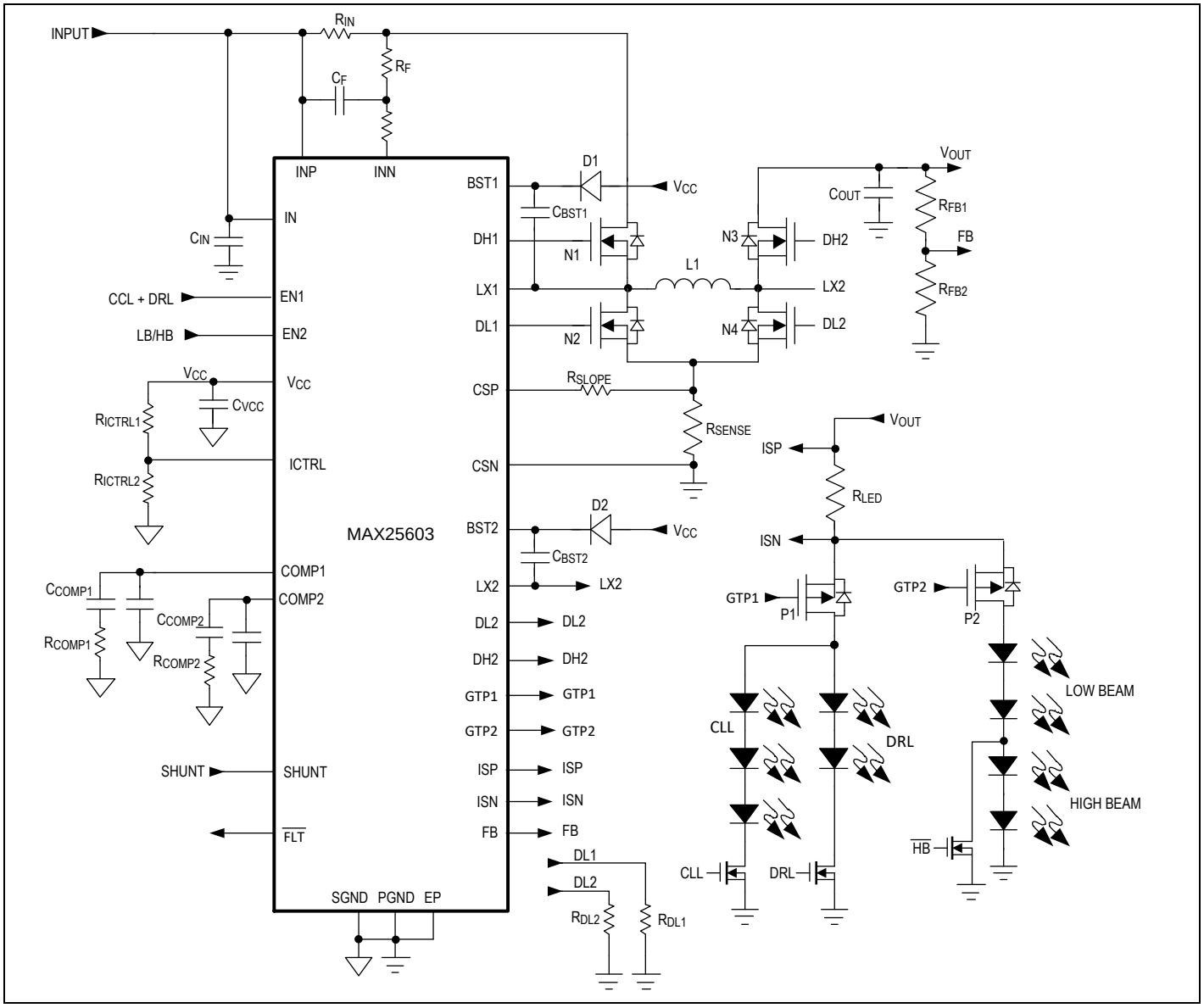


Figure 12. MAX25630 in a Multistring Configuration

Time-Sharing Application Circuit

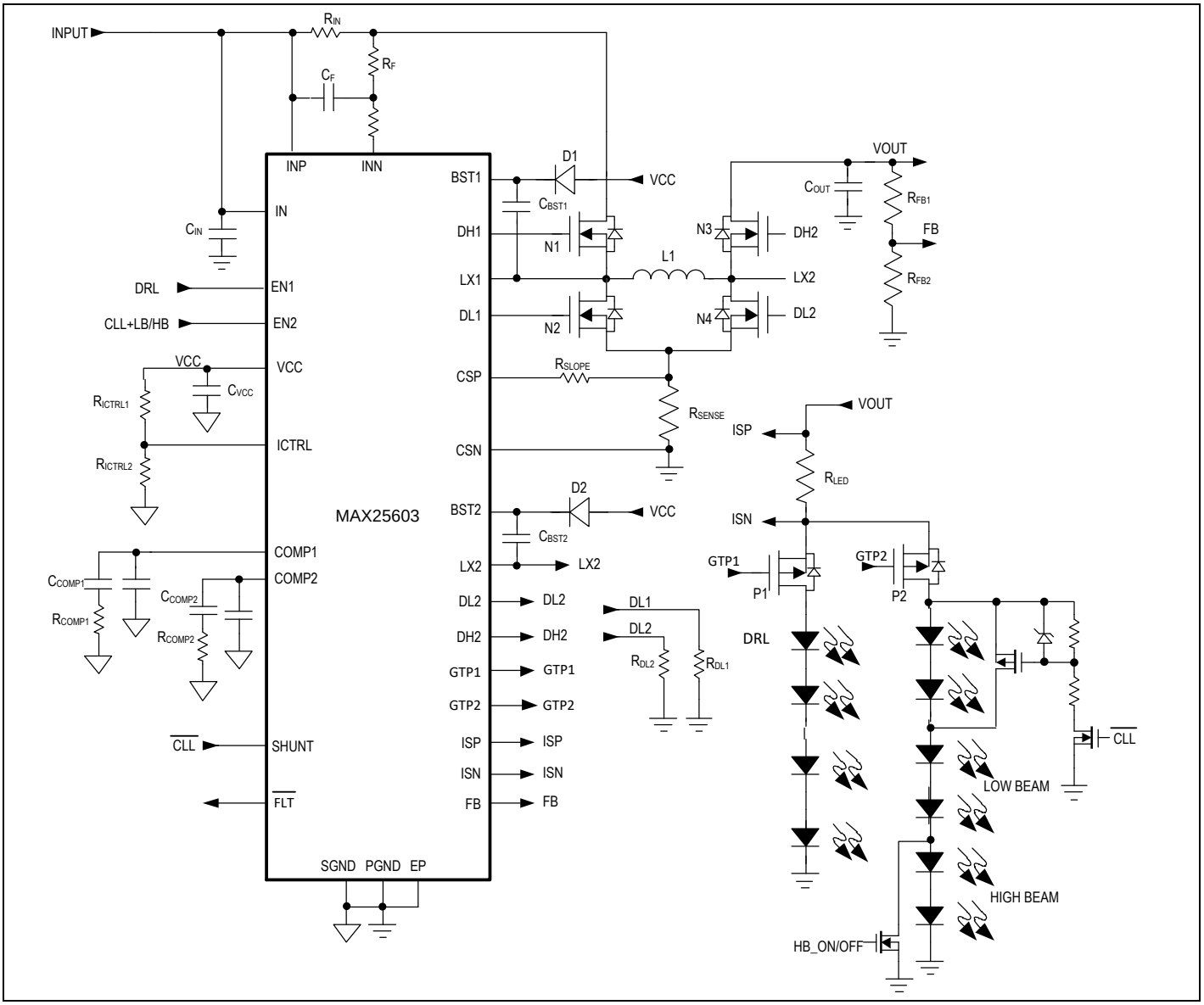


Figure 13. MAX25603 in a Time-Sharing Configuration

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX25603AUI/V+	-40°C to 125°C	28 TSSOP-EP*

+Denotes a lead (Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/21	Release for market intro	—