

Description

The AP1662 is an active power factor control IC which is designed mainly for use as a pre-converter in electronic ballast, AC-DC adapter and off-line SMPS applications.

The IC includes an internal start-up timer for stand-alone applications, a one-quadrant multiplier to realize near unity power factor and a zero current detector to ensure DCM boundary conduction operation.

The totem pole output stage is capable of driving power MOSFET with 600mA source current and 800mA sink current.

Designed with advanced BiCMOS process, the AP1662 features low start-up current, low operation current and low power dissipation. The AP1662 also has rich protection features including over-voltage protection, input under-voltage lockout with hysteresis and multiplier output clamp to limit maximum peak current.

The AP1662 meets IEC61000-3-2 standard even at one-quadrant load and THD lower than 10% at high-end line voltage and full load.

The IC is available in SO-8 package.

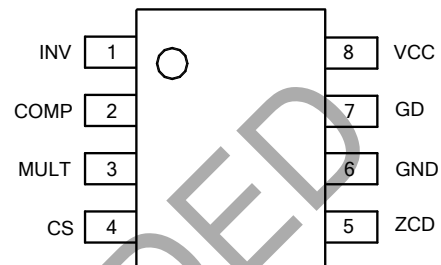
Features

- Comply with IEC61000-3-2 Standard
- Proprietary Design for Minimum THD
- Zero Current Detection Control for DCM Boundary Conduction Mode
- Adjustable Output Voltage with Precise Over-Voltage Protection
- Low Start-up Current with 40µA Typical Value
- Low Quiescent Current with 2.5mA Typical Value
- 1% Precision Internal Reference Voltage @ $T_J = +25^\circ\text{C}$
- Internal Start-up Timer
- Disable Function for Reduced Current Consumption
- Totem Pole Output with 600mA Source Current and 800mA Sink Current Capability
- Under-Voltage Lockout with 2.5V of Hysteresis
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignments

(Top View)

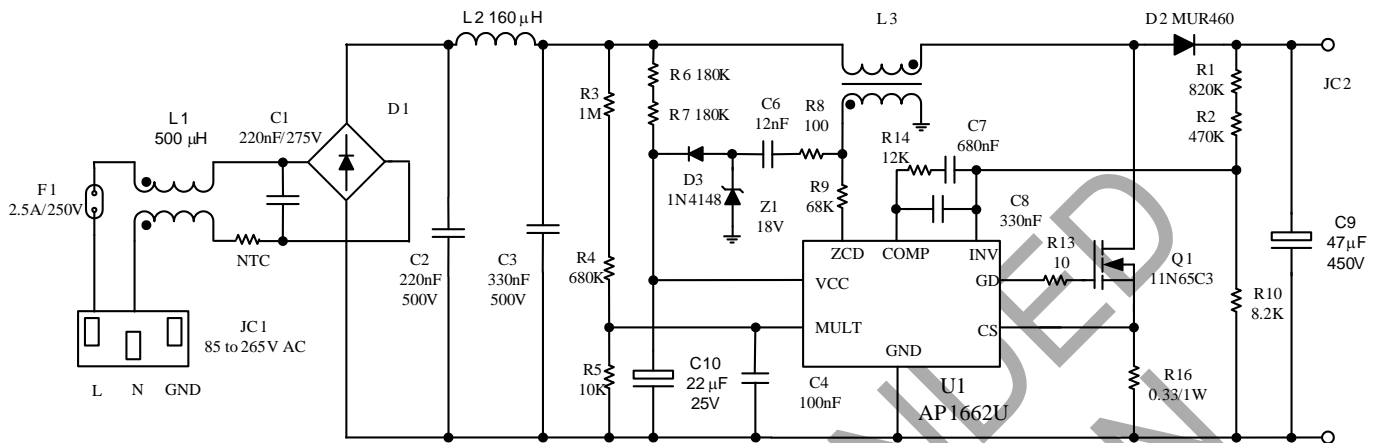


SO-8

Applications

- Electronic Ballast
- AC-DC Adapter
- Off-line SMPS
- Single Stage PFC LED Driver

Typical Applications Circuit



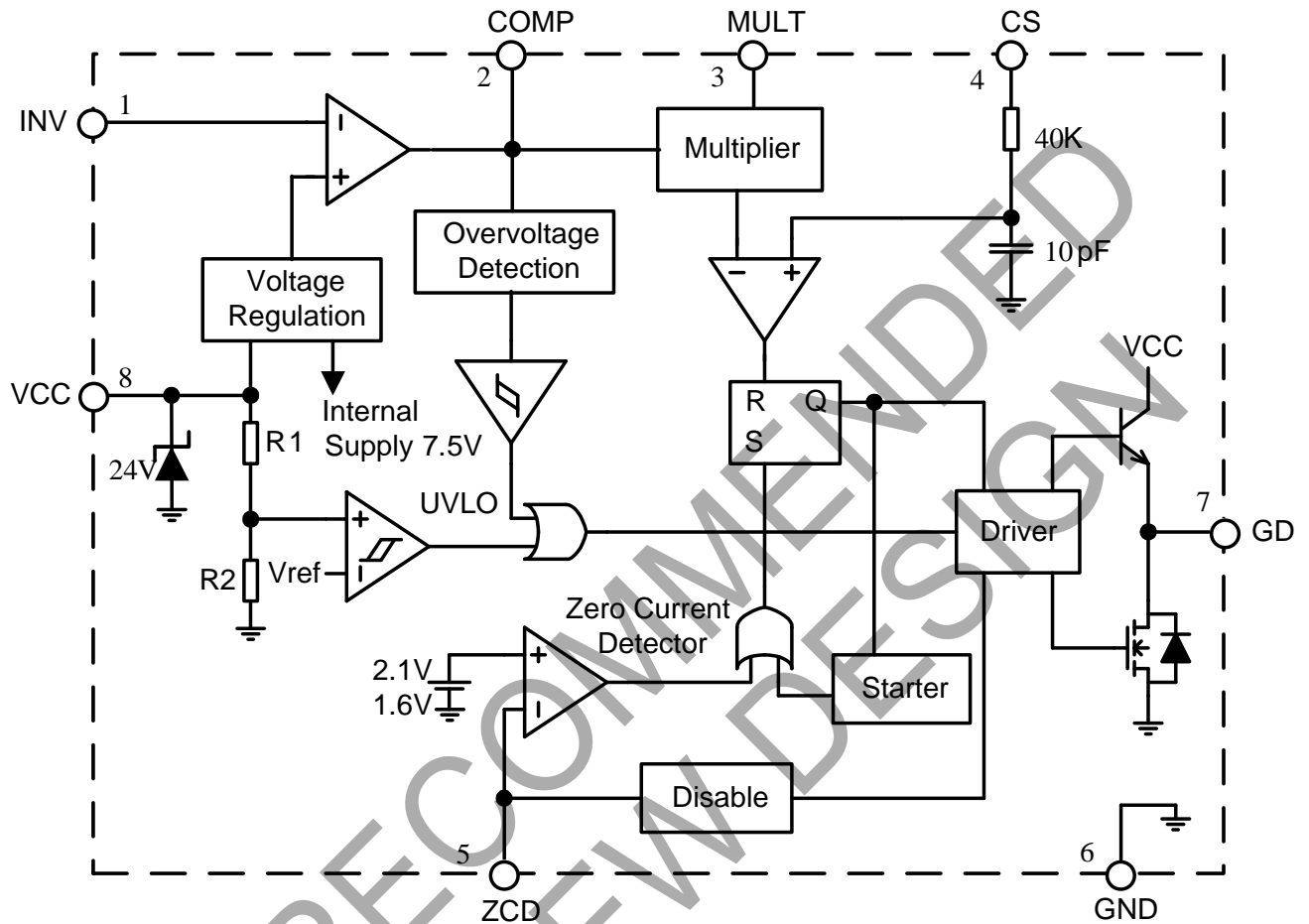
L3:
Core type RM10, material 3C90
primary: 660 μ H, 66 turns of litze wire 0.1mm*30
secondary: 7 turns wire of 0.2mm

85 to 265V Wide Range Input 90W PFC Demo Board Electrical Schematic Circuit

Pin Descriptions

Pin Number	Pin Name	Function
1	INV	Inverting input of the error amplifier
2	COMP	Output of the error amplifier
3	MULT	Input of the multiplier
4	CS	Input of the current control loop comparator
5	ZCD	Zero current detection input. If it is connected to GND, the device is disabled.
6	GND	Ground. Current return for gate driver and control circuits of the IC
7	GD	Gate driver output
8	VCC	Supply voltage of gate driver and control circuits of the IC

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating		Unit
V _{CC}	Power Supply Voltage	Self-limited		V
I _{CC}	Operating Supply Current	30		mA
V _{INV} , V _{COMP} , V _{MULT}	Input/Output of Error Amplifier, Input of Multiplier	-0.3 to 7		V
V _{CS}	Current Sense Input	-0.3 to 7		V
I _{ZCD}	Zero Current Detector Input	Source	-50	mA
		Sink	10	
P _{TOT}	Power Dissipation and Thermal Characteristics @ T _A =+50°C	0.65		W
R _{θJA}	Thermal Resistance (Junction to Ambient)	150		°C/W
T _J	Operating Junction Temperature	-40 to +150		°C
T _{STG}	Storage Temperature Range	-65 to +150		°C
T _{LEAD}	Lead Temperature (Soldering, 10 Seconds)	+260		°C
V _{ESD(HBM)}	ESD (Human Body Model)	3000		V
V _{ESD(MM)}	ESD (Machine Model)	200		V

Note 4: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Electrical Characteristics ($V_{CC}=12V$, $T_J=-25^{\circ}C$ to $+125^{\circ}C$, $C_O=1nF$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
Under Voltage Lockout Section							
V_{CC-ON}	Turn-on Threshold	V_{CC} Rising	11	12	13	V	
V_{CC-OFF}	Turn-off Threshold	V_{CC} Falling	8.7	9.5	10.3	V	
V_{CC-HYS}	Hysteresis	–	2.2	2.5	2.8	V	
V_{CC}	V_{CC} Operating Range	After turn-on	10.3	–	22	V	
V_Z	Zener Voltage	$I_{CC}=20mA$	22	24	–	V	
Total Supply Current Section							
$I_{START-UP}$	Start-up Current	$V_{CC}=11V$ before turn-on	–	40	70	μA	
I_{CC}	Operating Supply Current	Frequency=70kHz	–	3.5	5	mA	
		In OVP condition $V_{INV}=2.7V$	–	1.4	2.2		
I_Q	Quiescent Current	After turn-on	–	2.5	3.75	mA	
I_Q	Quiescent Current	$V_{ZCD}\leq 150mV$, $V_{CC}>V_{CC-OFF}$	–	–	2.2	mA	
		$V_{ZCD}\leq 150mV$, $V_{CC}<V_{CC-OFF}$	20	50	90	μA	
Error Amplifier Section							
V_{INV}	Voltage Feedback Input Threshold	$T_J=+25^{\circ}C$	2.465	2.5	2.535	V	
		$10.3V < V_{CC} < 20V$	2.44	–	2.56		
–	Line Regulation	$V_{CC}=10.3V$ to $20V$	–	2	5	mV	
I_{INV}	Input Bias Current	$V_{INV}=0$ to $3V$	–	-0.1	-1	μA	
G_V	Voltage Gain	Open Loop	60	80	–	dB	
G_B	Gain Bandwidth	–	–	1	–	MHz	
V_{COMP-H}	Output Voltage	Upper Clamp Voltage	$I_{SOURCE}=0.5mA$	5.15	5.55	5.85	V
V_{COMP-L}		Lower Clamp Voltage	$I_{SINK}=0.5mA$	2.1	2.25	2.4	
I_{COMP-H}	Output Current	Source Current	$V_{COMP}=4V$, $V_{INV}=2.4V$	-2	-4	-8	mA
I_{COMP-L}		Sink Current	$V_{COMP}=4V$, $V_{INV}=2.6V$	2.5	4.5	–	
Multiplier Section							
V_{MULT}	Linear Input Voltage Range	–	0 to 3	0 to 3.5	–	V	
$\Delta V_{CS}/\Delta V_{MULT}$	Output Maximum Slope	V_{MULT} : 0 to 0.5V, V_{COMP} =Upper Clamp Voltage	1.65	1.9	–	–	
k	Gain	$V_{MULT}=1V$, $V_{COMP}=4V$	0.6	0.75	0.9	1/V	

Electrical Characteristics ($V_{CC}=12V$, $T_J=-25^{\circ}C$ to $+125^{\circ}C$, $C_O=1nF$, unless otherwise specified.) (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Current Sense Section						
I_{CS}	Input Bias Current	$V_{CS}=0V$	-	-	-1	μA
$V_{CS-OFFSET}$	Current Sense Offset Voltage	$V_{MULT}=0V$	-	30	-	mV
		$V_{MULT}=2.5V$	-	5	-	
$V_{CS-CLAMP}$	Current Sense Reference Clamp	V_{COMP} =Upper Clamp Voltage, $V_{MULT}=2.5V$	1.6	1.7	1.8	V
$t_{d(H-L)}$	Delay to Output	-	-	200	350	ns
Zero Current Detection Section						
V_{ZCDA}	Arming Voltage (positive-going edge)	(Note 5)	-	2.1	-	V
V_{ZCDT}	Triggering Voltage (negative-going edge)	(Note 5)	-	1.6	-	V
V_{ZCD-H}	Upper Clamp Voltage	$I_{ZCD}=20\mu A$	4.5	5.1	5.9	V
		$I_{ZCD}=3mA$	4.7	5.2	6.1	
V_{ZCD-L}	Lower Clamp Voltage	$I_{ZCD}=3mA$	0.3	0.65	1	V
I_{ZCD-SR}	Source Current Capability	-	-2.5	-	-10	mA
I_{ZCD-SN}	Sink Current Capability	-	3	-	-	mA
I_{ZCD-B}	Sink Bias Current	$1V \leq V_{ZCD} \leq 4.5V$	-	2	-	μA
$V_{ZCD-DIS}$	Disable Threshold	-	150	200	250	mV
$V_{ZCD-HYS}$	Disable Hysteresis	-	-	100	-	mV
$I_{ZCD-RES}$	Restart Current After Disable	$V_{ZCD} < V_{DIS}$, $V_{CC} > V_{CC-OFF}$	-80	-120	-	μA
Drive Output Section						
V_{OH}	Dropout Voltage	$I_{GD-SOURCE}=200mA$	-	2.5	3	V
		$I_{GD-SOURCE}=20mA$	-	2	2.8	
V_{OL}		$I_{GD-SINK}=200mA$	-	0.9	1.9	
t_R	Output Voltage Rise Time	-	-	40	80	ns
t_F	Output Voltage Fall Time	-	-	30	70	ns
$V_{O-CLAMP}$	Output Clamp Voltage	$I_{GD-SOURCE}=5mA$, $V_{CC}=20V$	9	11	13	V
V_{OS}	UVLO Saturation	$V_{CC}=0$ to V_{CC-ON} , $I_{SINK}=10mA$	-	-	1.1	V

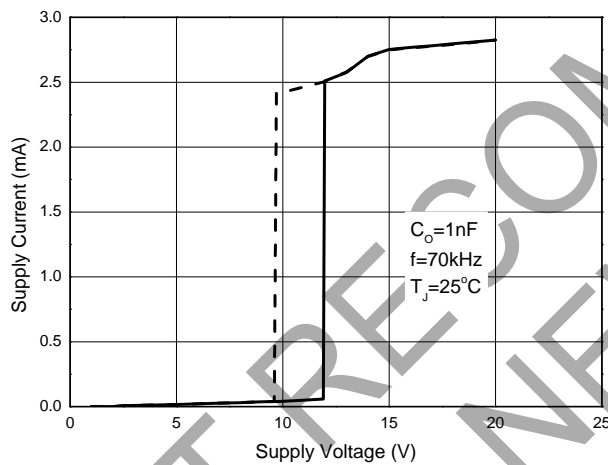
Electrical Characteristics ($V_{CC}=12V$, $T_J=-25^{\circ}C$ to $+125^{\circ}C$, $C_O=1nF$, unless otherwise specified.) (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Output Over Voltage Section						
I_{OVP}	OVP Triggering Current	–	35	40	45	μA
V_{OVP_TH}	Static OVP Threshold	–	2.1	2.25	2.4	V
Starter						
t_{START}	Start Timer Period	–	75	130	300	μs

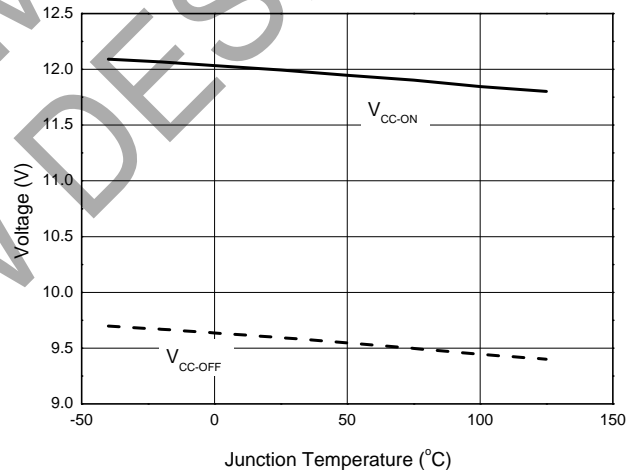
Note 5: Limits over the full temperature are guaranteed by design, but not tested in production.

Performance Characteristics

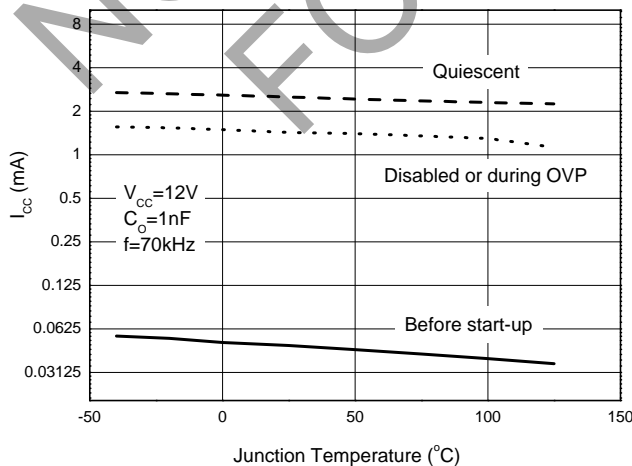
Supply Current vs. Supply Voltage



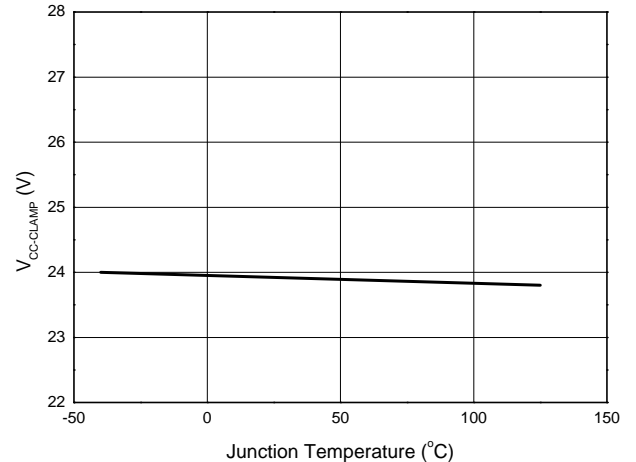
Start-up & UVLO vs. T_J



I_{CC} Consumption vs. T_J

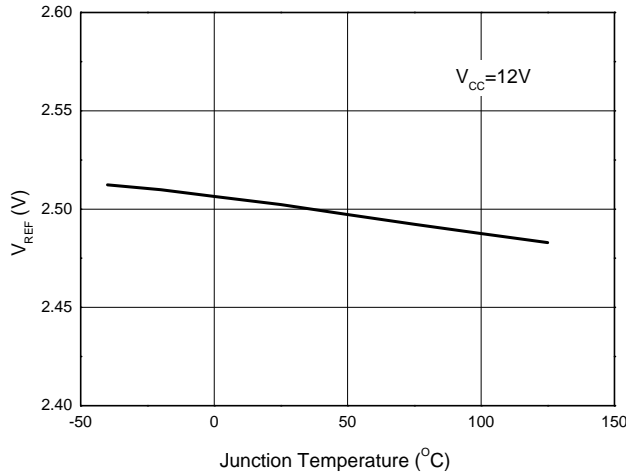


V_{CC} Zener Voltage vs. T_J

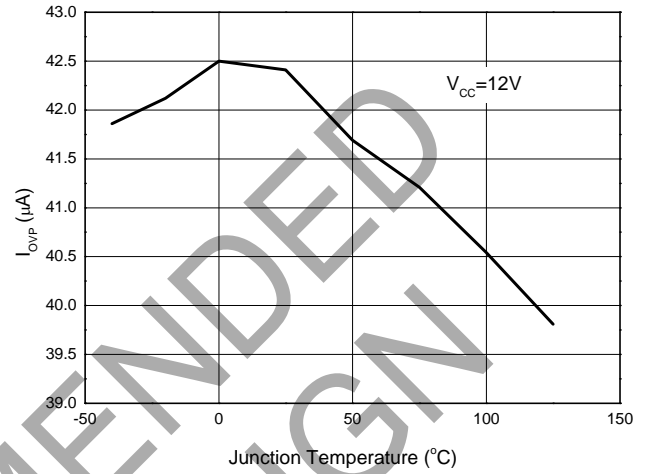


Performance Characteristics (Cont.)

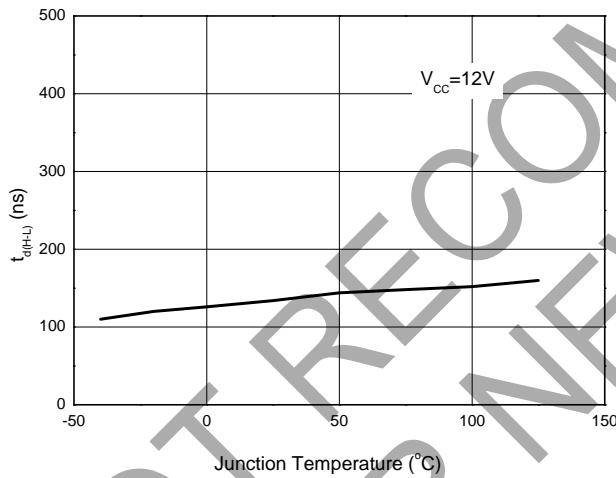
Feedback Reference Voltage vs. T_J



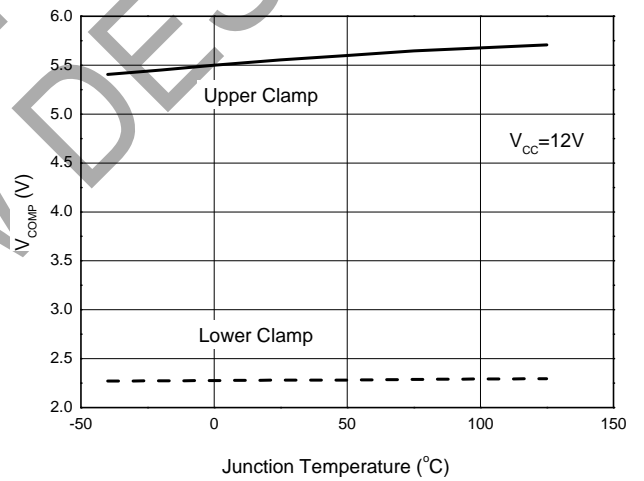
OVP Current vs. T_J



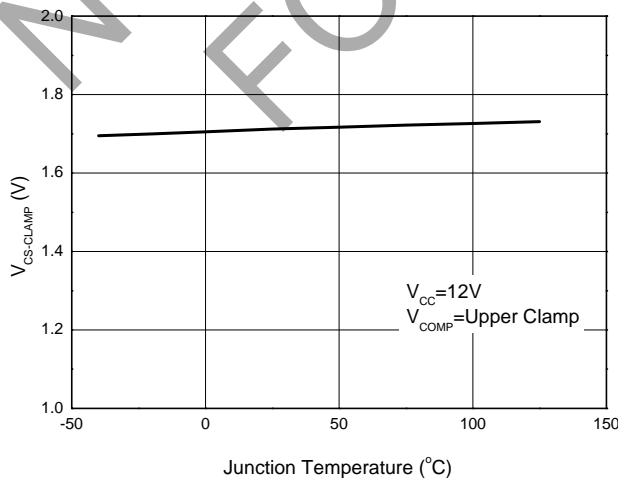
Delay-to-Output vs. T_J



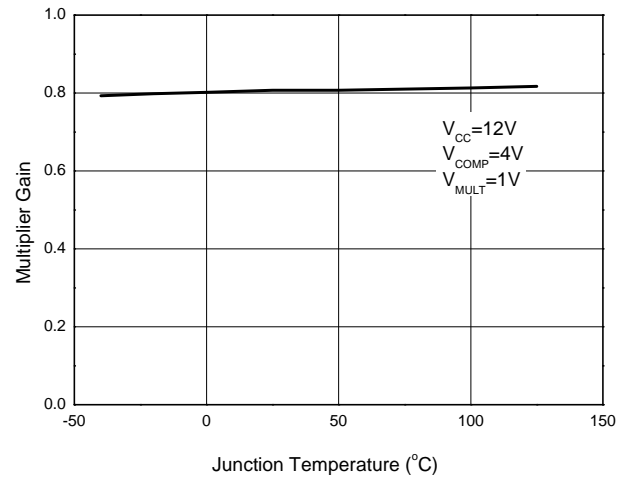
E/A Output Clamp Levels vs. T_J



$V_{CS-CLAMP}$ vs. T_J

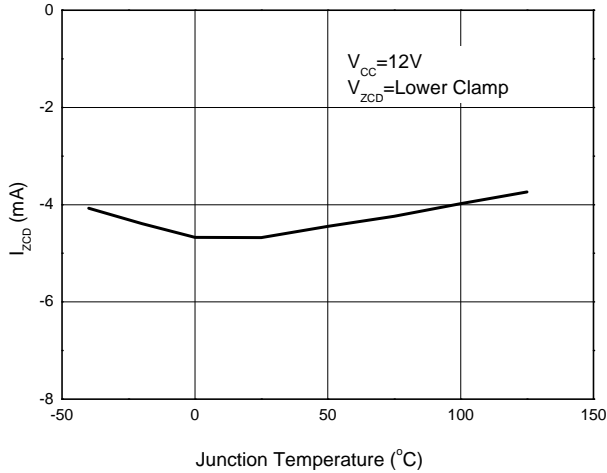


Multiplier Gain vs. T_J

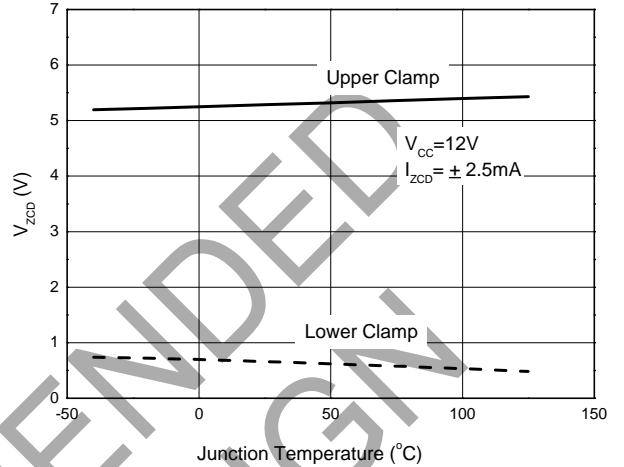


Performance Characteristics (Cont.)

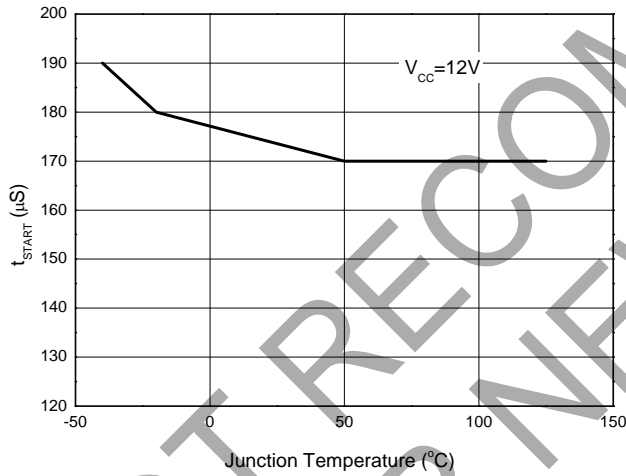
ZCD Source Capability vs. T_J



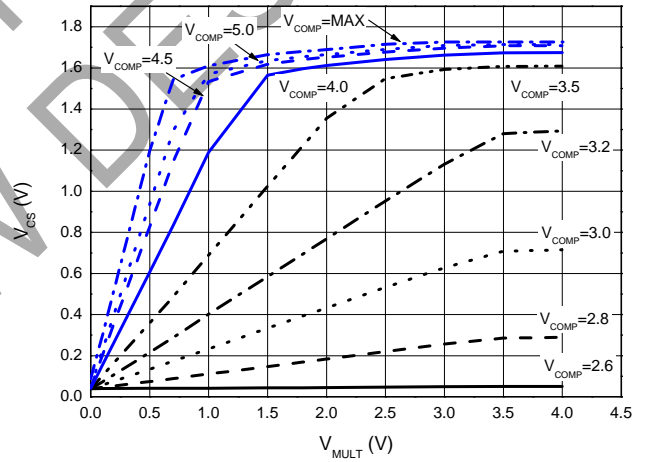
ZCD Clamp Levels vs. T_J



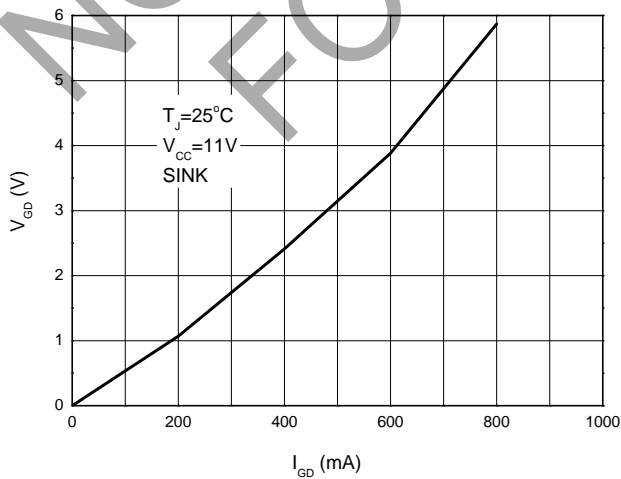
Start-up Timer vs. T_J



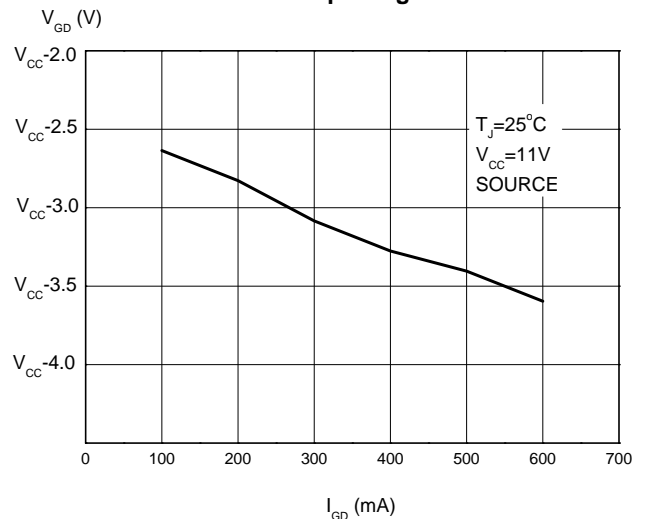
Multiplier Characteristics



Gate-driver Output Low Saturation

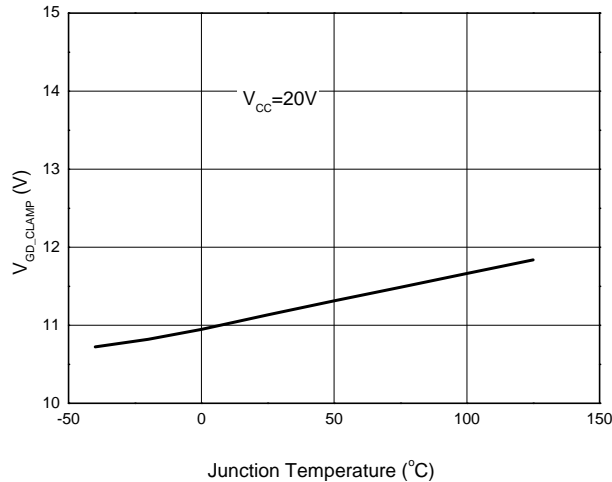


Gate-driver Output High Saturation

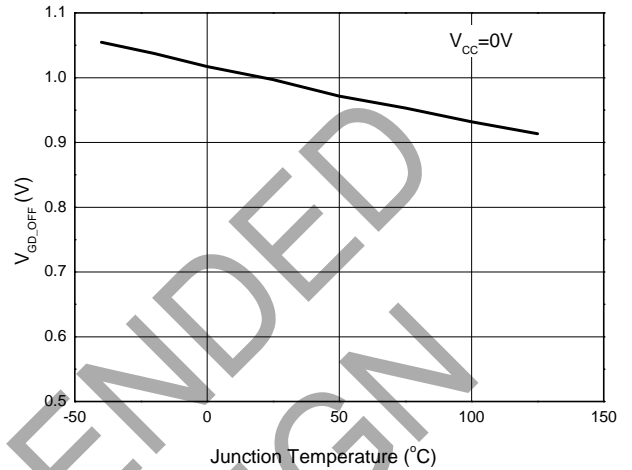


Performance Characteristics (Cont.)

Gate-driver Clamp vs. T_J



UVLO Saturation vs. T_J



Functional Block Description

AP1662 is a high performance power factor correction controller which operates in DCM boundary conduction mode. The PFC converter's switch will be turned on when the inductor current reduces to zero and turned off when the sensed inductor current reaches the required reference which is decided by the output of multiplier.

Error Amplifier and Over-Voltage Protection

The error amplifier regulates the PFC output voltage. The internal reference on the non-inverting input of the error amplifier is 2.5V. The error amplifier's inverting input (INV) is connected to an external resistor divider which senses the output voltage. The output of error amplifier is one of the two inputs of multiplier. A compensation loop is connected outside between INV and the error amplifier output. Normally, the compensation loop bandwidth is set very low to realize high power factor for PFC converter.

To make the over voltage protection fast, the internal OVP function is added. If the output over voltage happens, excess current will flow into the output pin of the error amplifier through the feedback compensation capacitor. (see Figure 1) The AP1662 monitors the current flowing into the error amplifier output pin. When the detected current is higher than 40μA, the dynamic OVP is triggered. The IC will be disabled and the drive signal is stopped. If the output over voltage lasts so long that the output of error amplifier goes below 2.25V, static OVP will take place. Also the IC will be disabled until the output of error amplifier goes back to its linear region. R1 and R2 (see Figure 1) will be selected as below:

$$\frac{R1}{R2} = \frac{V_o}{2.5V} - 1$$

$$R1 = \frac{\Delta V_{OVP}}{40\mu A}$$

Functional Block Description (Cont.)

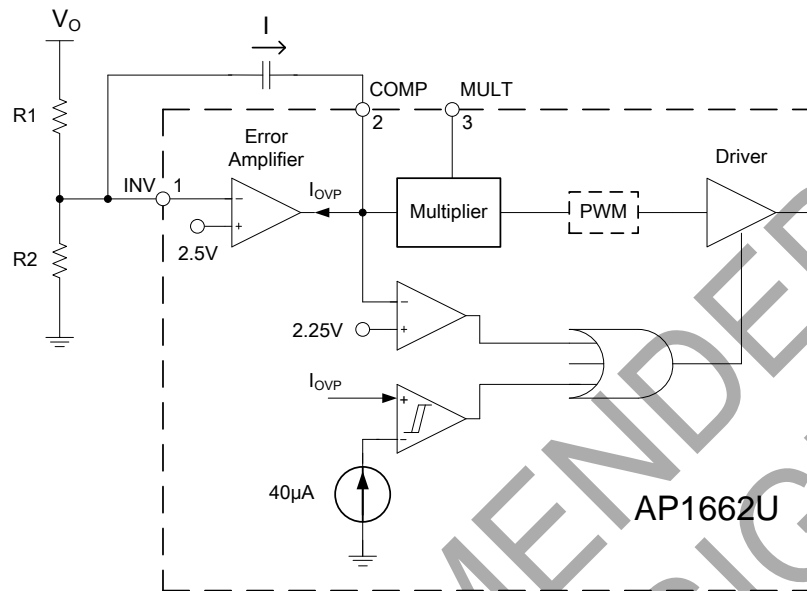


Figure 1. Error Amplifier and OVP Block

Multiplier

The multiplier has two inputs. One (Pin 3) is the divided AC sinusoidal voltage which makes the current sense comparator threshold voltage vary from zero to peak value. The other input is the output of error amplifier (Pin 2). In this way, the input average current wave will be sinusoidal as well as reflects the load status. Accordingly a high power factor and good THD are achieved. The multiplier transfer character is designed to be linear over a wide dynamic range, namely, 0V to 3V for Pin 3 and 2V to 5.8V for Pin 2. The relationship between the multiplier output and inputs is described as below equation:

$$V_{CS} = k \times (V_{COMP} - 2.5) \times V_{MULT}$$

Where V_{CS} (Multiplier output) is the reference for the current sense, k is the multiplier gain, V_{COMP} is the voltage on pin 2 (error amplifier output) and V_{MULT} is the voltage on pin 3.

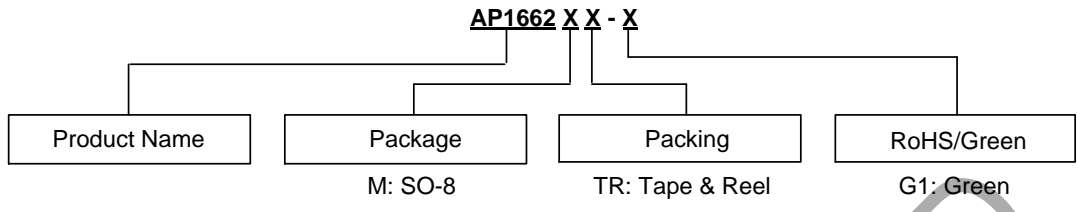
Current Sense/Current Sense Comparator

The PFC switch's turn-on current is sensed through an external resistor in series with the switch. When the sensed voltage exceeds the threshold voltage (the multiplier output), the current sense comparator will become low and the external MOSFET will be turned off. This insures a cycle-by-cycle current mode control operation. The maximum current sense reference is 1.8V. The max value usually happens at startup process or abnormal conditions such as short load.

Zero Current Detection

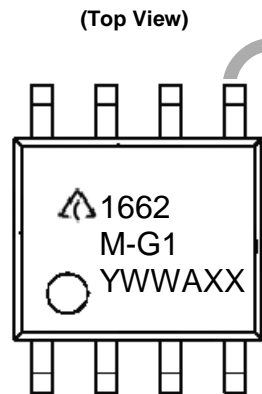
AP1662 is a DCM boundary conduction current mode PFC controller. Usually, the zero current detection (ZCD) voltage signal comes from the auxiliary winding of the boost inductor. When the ZCD pin voltage decreases below 1.6V, the gate drive signal becomes high to turn on the external MOSFET. 500mV of hysteresis is provided to avoid false triggering. The ZCD pin can be used for disabling the IC. Making its voltage below 0.15V or short to the ground will disable the device thus reduce the IC supply current consumption.

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing
SO-8	-40 to +105°C	AP1662MTR-G1	1662M-G1	4000/ 13" Tape & Reel

Marking Information

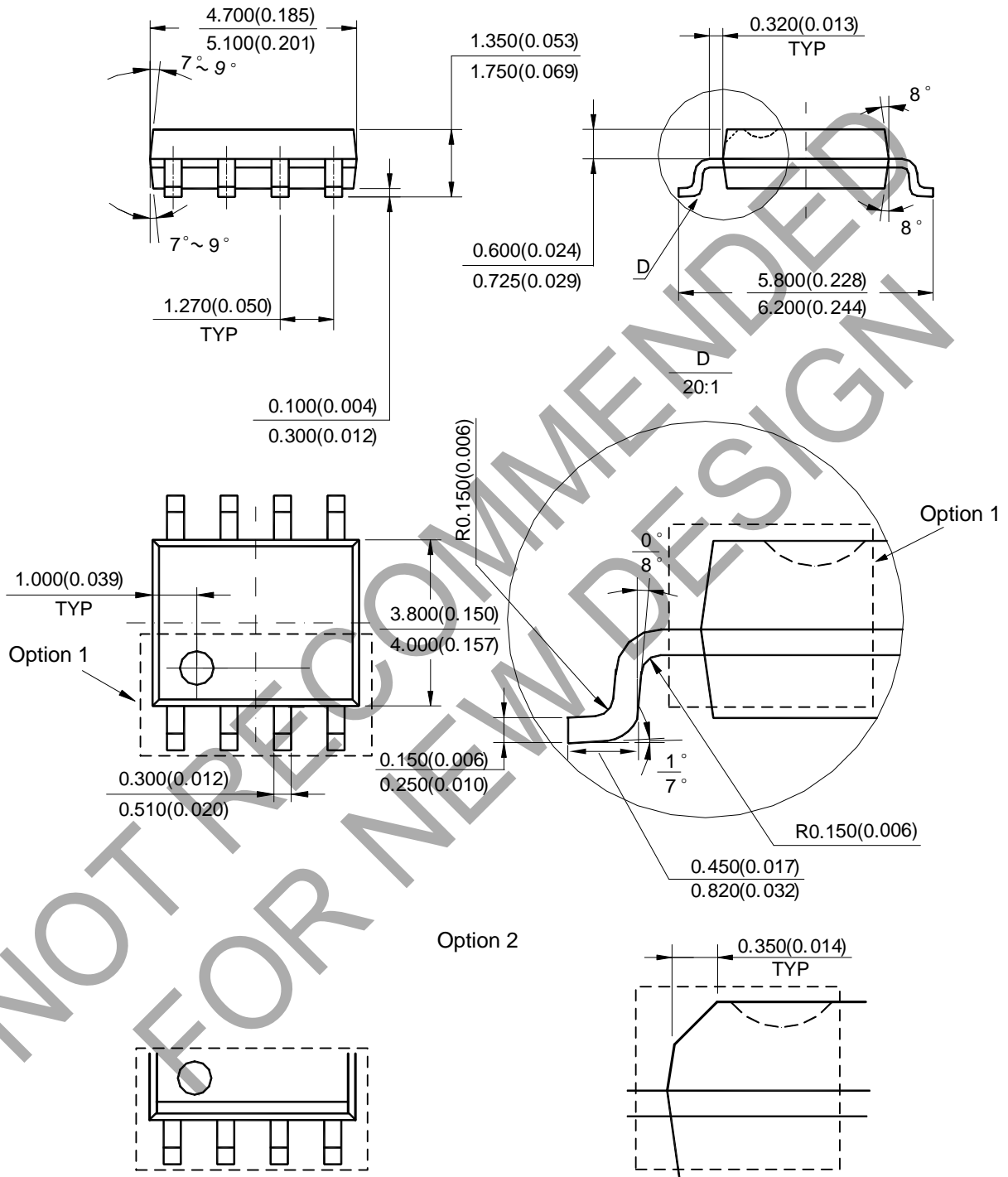


First and Second Lines: Logo and Marking ID
(See Ordering Information)
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch No.

NOT FOR NEW DESIGN

Package Outline Dimensions (All dimensions in mm(inch).)

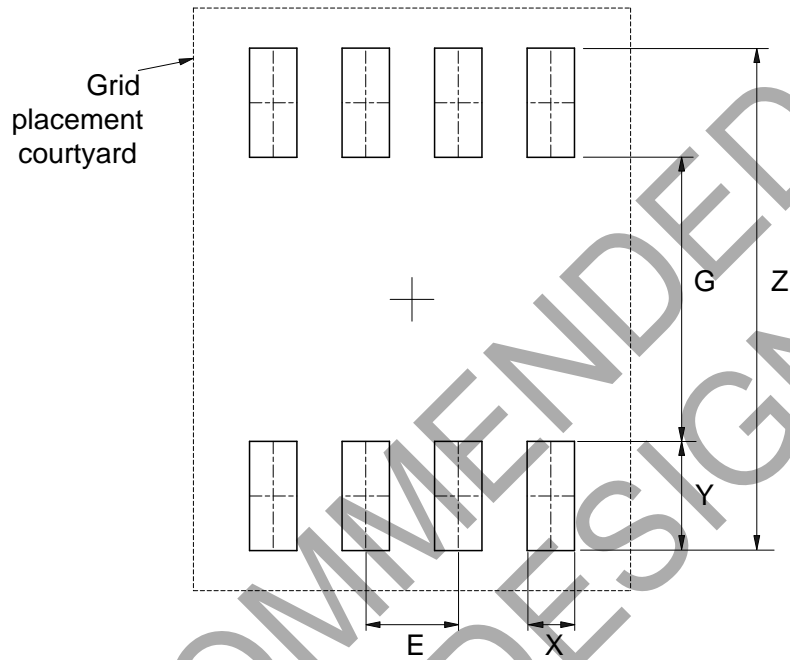
(1) Package Type: SO-8



Note: Eject hole, oriented hole and mold mark is optional.

Suggested Pad Layout

(1) Package Type: SO-8



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	1.270/0.050

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