IS32LT3123

QUAD CHANNEL EXTERNAL NMOS FET HIGH CURRENT AUTOMOTIVE LED CONTROLLER WITH INTERNAL PWM DIMMING

May 2020

GENERAL DESCRIPTION

The IS32LT3123 is a quad channel linear controller capable of accurately regulating LED current with external NMOS FETs. It integrates PWM dimming for two LED brightness levels for RCL (Rear Combination Lamp) or DRL (Daytime Running Lamp) applications. It is fully programmable with two LED brightness levels for the different intensity requirements, such as “Stop” (full brightness) and “Tail” dim (PWM dimming). A logic level at the PWMB pin is used to switch between the two brightness levels. A logic high provides the highest intensity output, while a logic low utilizes an internally generated PWM signal to reduce the intensity of the LEDs’ light output.

Multiple devices also can be connected in parallel in a master-slave structure for larger lighting applications.

For added system reliability, the IS32LT3123 integrates fault detection circuitry for LED open/short circuit, input over voltage and over temperature conditions. The FAULTB pin is dedicated to the fault conditions reporting and the MODE pin can control the action of the device in case of a fault condition.

The device also supports the NTC resister to monitor the LED string temperature. In case of the temperature exceeds the setting threshold, the device will reduce the drive current to protect the LED string.

The device package is an eTSSOP-24 with exposed pad for enhanced thermal dissipation.

FEATURES

- Low side external NMOS FETs support high output current with independent current setting
- One resistor to simultaneously adjust all channels for LED binning
- 200mV reference feedback voltage for high efficiency
- ±4% current accuracy over -40°C ~125°C
- 5.0V to 40V supply voltage
- PWMB voltage input to select between full brightness and PWM dimming
- Flexible LED PWM dimming options
  - Internal PWM dimming set by resistors
    - ✓Programmable duty cycle, 5%~95%
    - ✓Programmable frequency, 100Hz~1kHz
  - External PWM signal input dimming
  - Analog voltage input for PWM dimming
- PWM slew rate control on each output to optimize EMI performance
- Robust fault protection
  - Fault reporting
    - ✓LED string open/short
    - ✓Thermal shutdown
  - LED string over temperature thermal rolloff
  - Input over voltage current derating
  - Controller junction over temperature thermal rolloff
- Multiple parallel IC operation for higher number of strings with fault condition and PWM dimming sync
- AEC-Q100 Qualified

APPLICATIONS

- Automotive and avionic lighting
- Rear combination light (STOP/TAIL lights)
- Center high mounted stop light
- Position light
- Daytime running light (DRL)
- Turn light

TYPICAL APPLICATION CIRCUIT

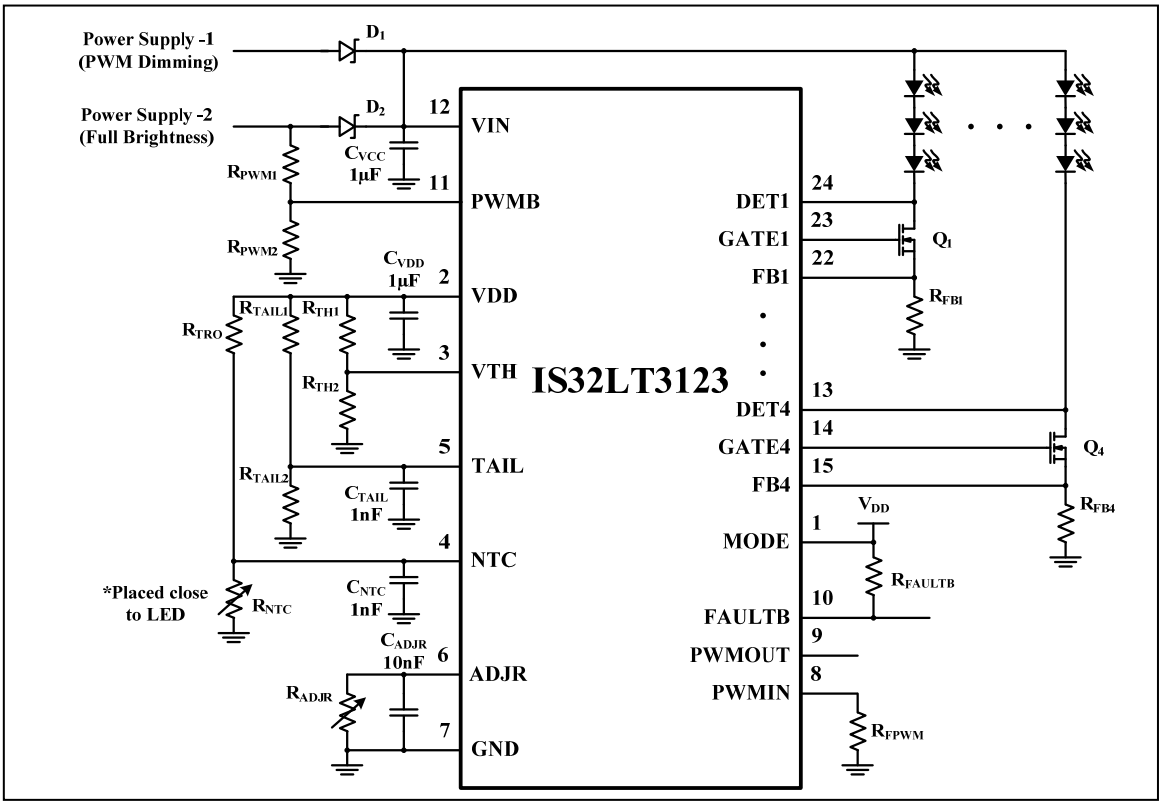


Figure 1 Typical Application Circuit of Internal PWM Dimming

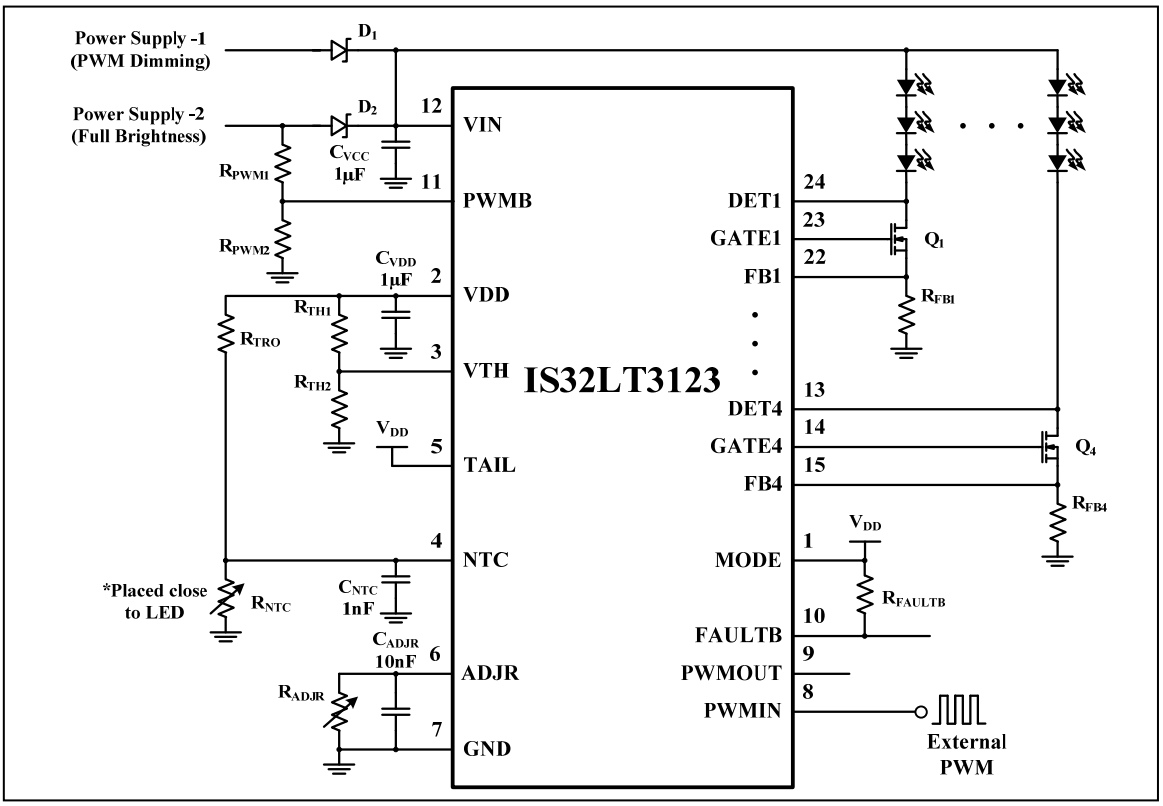


Figure 2 Typical Application Circuit of External PWM Dimming

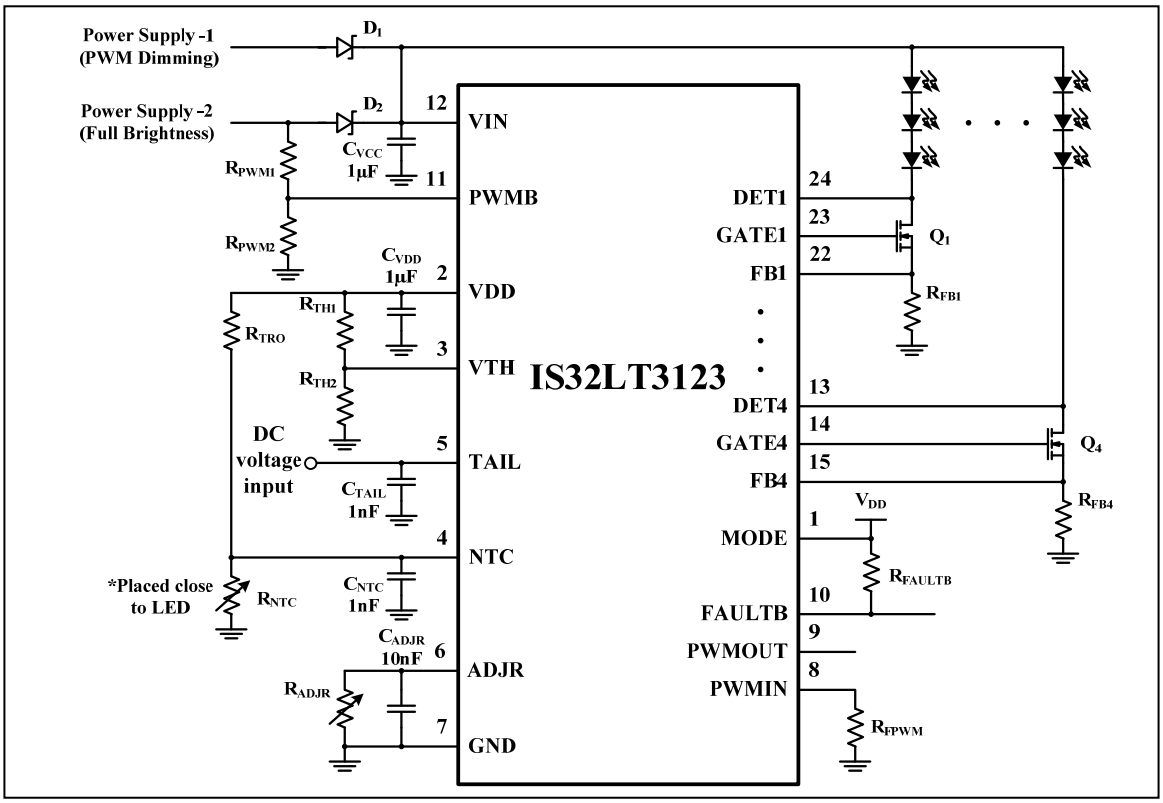


Figure 3 Typical Application Circuit of Analog Input PWM Dimming

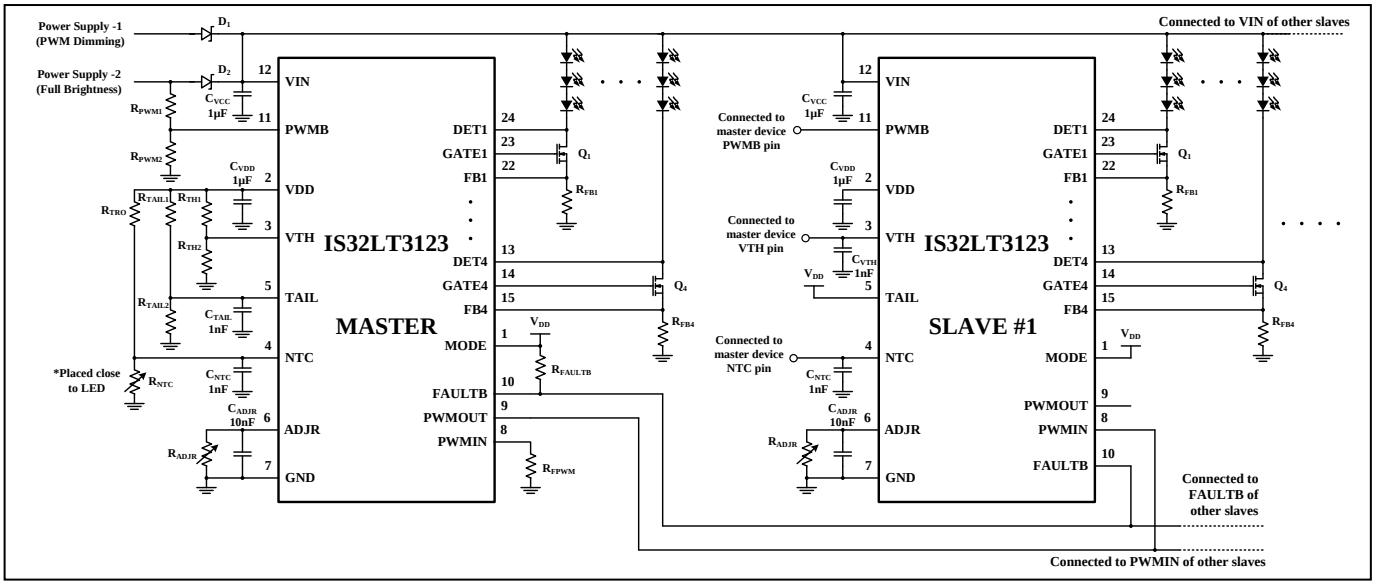
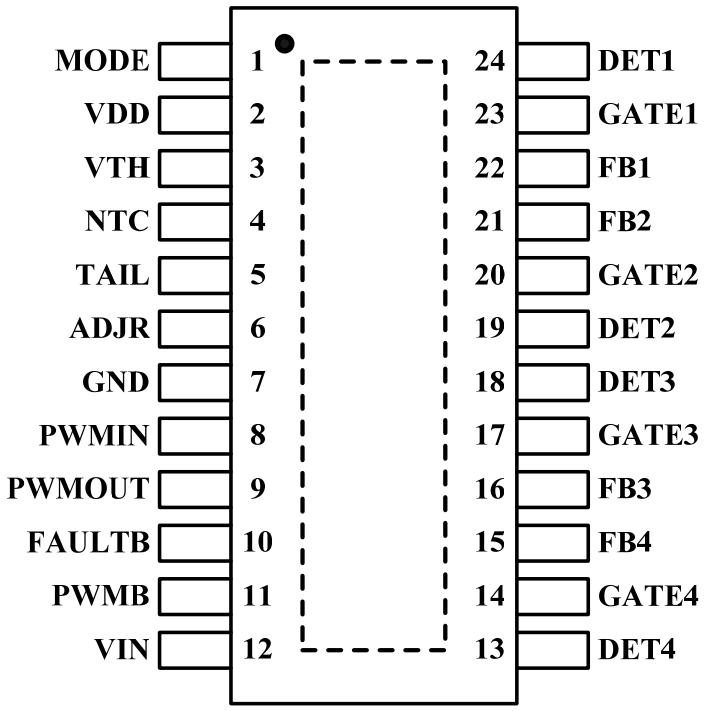


Figure 4 Typical Application Circuit of Several Devices in Parallel (one master with several slaves)

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-24	

PIN DESCRIPTION

No.	Pin	Function
1	MODE	MODE pin decides the fault mode. Tie to VDD or GND. Do not leave unconnected.
2	VDD	Internal LDO output. Connect to GND through a 1μF X7R capacitor which should be placed as close to VDD pin as possible. It is capable to drive external circuitry with minimum 14mA current capability.
3	VTH	Voltage at this pin sets the V_{IN} over voltage current derating threshold and the V_{IN} threshold for open LED fault detect.
4	NTC	Connect the NTC resistor divider to set the temperature threshold for the LED string temperature monitor. As long as the temperature exceeds the threshold, the reference voltage will be derated linearly according to NTC pin voltage.
5	TAIL	Connect to an external DC voltage below 3.7V for internal PWM mode to adjust operating duty cycle. Connect TAIL pin to VDD for external PWM mode. PWM duty cycle is controlled by the PWM signal on PWMIN pin.
6	ADJR	Connect a proper value resistor from this pin to GND to set the Internal reference voltage.
7	GND	Ground pin.
8	PWMIN	In internal PWM mode (TAIL pin voltage < 3.7V), the frequency of PWM is set by a resistor from PWMIN to GND. In external PWM mode (TAIL pin is connected to VDD), PWM frequency and duty cycle are determined by external PWM signal on PWMIN pin.
9	PWMOUT	PWM signal output pin. In internal PWM mode, the output PWM signal is internal PWM generator. In external PWM mode, the output PWM signal is sync with PWMIN pin.
10	FAULTB	Open drain I/O diagnostic pin. Active low output driven by the device when it detects a fault condition. As an input (MODE pin high), this pin will accept an externally generated FAULTB signal to disable the device output to satisfy the “One-Fail-All-Fail” function. Note this pin requires an external pull up resistor (R_{FAULTB}).
11	PWMB	Full brightness mode select input. When PWMB pin is low, the device is in PWM dimming mode and the output is dimming by the internal or external PWM signal. When PWMB pin is high, the device is in full brightness mode, NMOS FET current 100% duty cycle operation. And the internal and external PWM signal are overridden.
12	VIN	Power input for the IC.
24,19,18,13	DET1/2/3/4	Detect NMOS FET drain voltage for channel 1/2/3/4 LED string open/short faults. If any channel is unused, connect its DET pin to used DET pin. For example, if channel 1/2 are used and channel 3/4 are not used. DET1/2 is connected to the drain of their NMOS FETs. DET3/4 can be connected to DET1 or DET2.
23,20,17,14	GATE1/2/3/4	Gate driver for external NMOS FET1/2/3/4.
22,21,16,15	FB1/2/3/4	Current sense for channel 1/2/3/4. Connect sense resistors to independently set current level of channel 1/2/3/4.
	Thermal Pad	Must be connected to GND with sufficient copper plate for heat sink.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3123-ZLA3-TR	eTSSOP-24, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage at VIN	-0.3V ~ +42V
Voltage at PWMB, FAULTB, DET1~4, PWMIN	-0.3V ~ +V_{IN}+0.3V
Voltage at GATE1~4, FB1~4, PWMOUT	-0.3V ~ +20V
Voltage at VDD, VTH, ADJR, NTC, TAIL, MODE	-0.3V ~ +7V
Operating temperature, T_A=T_J	-40°C ~ +150°C
Storage temperature, T_{STG}	-65°C ~ +150°C
Junction temperature, T_{JMAX}	+150°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	28.1°C/W
Package thermal resistance, junction to thermal PAD (4 layer standard test PCB based on JESD 51-8), θ_{JP}	8.55°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Valid at V_{IN}= 7V ~ 19V

"●" symbol indicates specifications across the full operating temperature range with T_A= T_J= -40°C to +125°C, other specifications are at T_A= T_J= 25°C; unless noted otherwise.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Input Supply							
V_{IN}	Operating input voltage range		●	5.0		40	V
V_{IN_UV}	V_{IN} undervoltage release	VIN rising			4.5		V
V_{IN_UVHY}	V_{IN} undervoltage lockout hysteresis	IC disabled			0.15		V
I_{IN}	VIN operational current	V_{NTC}=V_{VTH}=V_{TAIL}=V_{DD}, PWMB=High	●			13	mA
t_{ON}	Startup time	V_{IN}>7V, C_{VDD}= 10μF, V_{FB}= 20mV, PWMB=High			200		μs
Current Regulation							
V_{REFMAX}	Maximum reference voltage on FB pins	V_{VTH}=V_{NTC}=V_{ADJR}=V_{DD}	●	192	200	208	mV
		V_{VTH}=V_{NTC}=V_{ADJR}=V_{DD}		194	200	206	
V_{REFDR}	VIN over voltage derating for reference voltage	V_{VTH}= 2V, V_{NTC}=V_{ADJR}=V_{DD} V_{IN}≥ 26V			51		%
Err_{VREF}	Matching between FB voltage (Note 2)	V_{VTH}=V_{NTC}=V_{ADJR}=V_{DD}				2	%
$V_{REFADJR}$	Reference voltage adjusted by ADJR pin	V_{VTH}=V_{NTC}=V_{DD}, R_{ADJR}=2kΩ	●	122	132	142	mV
V_{DD}	VDD pin voltage output	I_{VDD}= 10mA	●	5.0	5.25	5.5	V
I_{DD_LIM}	VDD pin output current limit		●	14			mA

ELECTRICAL CHARACTERISTICS (CONTINUE)

Valid at V_{IN}= 7V ~ 19V

"●" symbol indicates specifications across the full operating temperature range with T_A= T_J= -40°C to +125°C, other specifications are at T_A= T_J= 25°C; unless noted otherwise.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Gate Driver							
V_{GATEH}	GATE high-level output	V_{IN}= 12V, PWMIN=High, V_{FB}= 150mV, V_{TAIL}= V_{DD}		6		8	V
V_{GATEL}	GATE low-level output	PWMIN= Low, PWMB=Low				0.2	V
V_{GATED}	GATE driver dropout	V_{IN}= 7V, V_{FB}= 150mV, measured as (V_{IN} - V_{GATE})			1.65		V
I_{GPU}	Gate pull-up current	V_{FB}= 180mV, V_{GATE}= 0V, V_{IN}= 7V			-0.92		mA
I_{GPD}	Gate pull-down current	V_{FB}= 220mV, V_{GATE}= 7V, V_{IN}= 7V			8.8		mA
C_{GISS}	External NMOS FET gate capacitance range (Note 5)	For stable operation		250		2000	pF
t_{PD}	Propagation delay (Note 5)	Delay from PWMIN to PWMOUT pin, TAIL connected to VDD			0.1		µs
f_{PWM}	Internal PWM signal frequency	External R_{FPWM}= 30kΩ, across PWMIN to GND	●	180	200	220	Hz
D_{PWM7}	PWM duty cycle	V_{TAIL} driven by resistor divider from VDD, V_{TAIL}/V_{DD}= 0.093, R_{FPWM}= 30kΩ		6.3	7	7.7	%
D_{PWM90}		V_{TAIL} driven by resistor divider from VDD, V_{TAIL}/V_{DD}= 0.612, R_{FPWM}= 30kΩ		87	90	93	
t_{DPWM}	Delay time between PWMIN rising edge to 20% of FB	Delay time between PWM rising edge to 20% of FB			23		us
t_{SR}	Current slew time	FB rising from 20% to 90% levels, for internal reference ramp		49	70	91	µs
t_{SF}	Current slew time	FB falling from 90% to 20% levels, for internal reference ramp		49	70	91	µs
t_{SRMS}	Rise time and fall time mismatch between four strings (Note 3,4)	Rise and fall time mismatch between 20% and 90% levels in all strings				5	%

ELECTRICAL CHARACTERISTICS (CONTINUE)

Valid at V_{IN}= 7V ~ 19V

"●" symbol indicates specifications across the full operating temperature range with T_A= T_J= -40°C to +125°C, other specifications are at T_A= T_J= 25°C; unless noted otherwise.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Logic Pins							
V_{IL}	MODE, PWMIN, FAULTB pins input low voltage	Below V_{IL} level, input voltage considered as logic LOW	●			0.8	V
V_{IH}	MODE, PWMIN, FAULTB pins input high voltage	Above V_{IH} level, input voltage considered as logic HIGH	●	2			V
V_{OL}	FAULTB, PWMOUT pins output low voltage	I_{OL}= 1mA	●			0.4	V
V_{OH}	PWMOUT pin output high voltage	I_{OH}= –1mA	●	4			V
V_{ILF}	PWMB pin input low voltage	Below V_{ILF} level, input voltage on PWMB pin will disable PWM dimming mode	●	0.85		1.15	V
V_{IHF}	PWMB pin input high voltage	Above V_{IHF} level, input voltage on PWMB pin will enable PWM dimming mode	●	1.06		1.44	V
Protection							
$V_{INth(L)}$	Input over voltage derates V_{FB} by 10%	V_{VTH}= 2V		19.7	20.7	21.7	V
V_{INthd}	Input over voltage derating range (V_{IN_180mV} to V_{IN_120mV})	V_{REF} drops from 180mV to 120mV			2.16		V
V_{SCV}	V_{IN} to drain short detect voltage	Measured as (V_{IN} - V_{DET})	●	0.5	0.8	1.1	V
V_{OCV}	Open LED fault detect voltage	Measured at DET, V_{IN}>V_{OCVEN}	●	0.2	0.25	0.3	V
V_{OCVEN}	Open LED detect enable voltage	V_{VTH}= 2V			10		V
V_{NTC10}	NTC derates V_{FB} by 10%			1.9	2.0	2.12	V
V_{NTC90}	NTC derates V_{FB} by 90%				0.43		V
T_{JH}	Thermal rolloff activation temperature (Note 5)	V_{FB} derated by 10%			148		°C
T_{JL}	Thermal rolloff low-current temperature (Note 5)	V_{FB} derated by 65%			163		°C
T_{SD}	Over temperature shutdown (Note 5)	Temperature increasing			170		°C
T_{SDHY}	Over temperature hysteresis (Note 5)	Recovery= T_{SD} -T_{SDHY}			30		°C

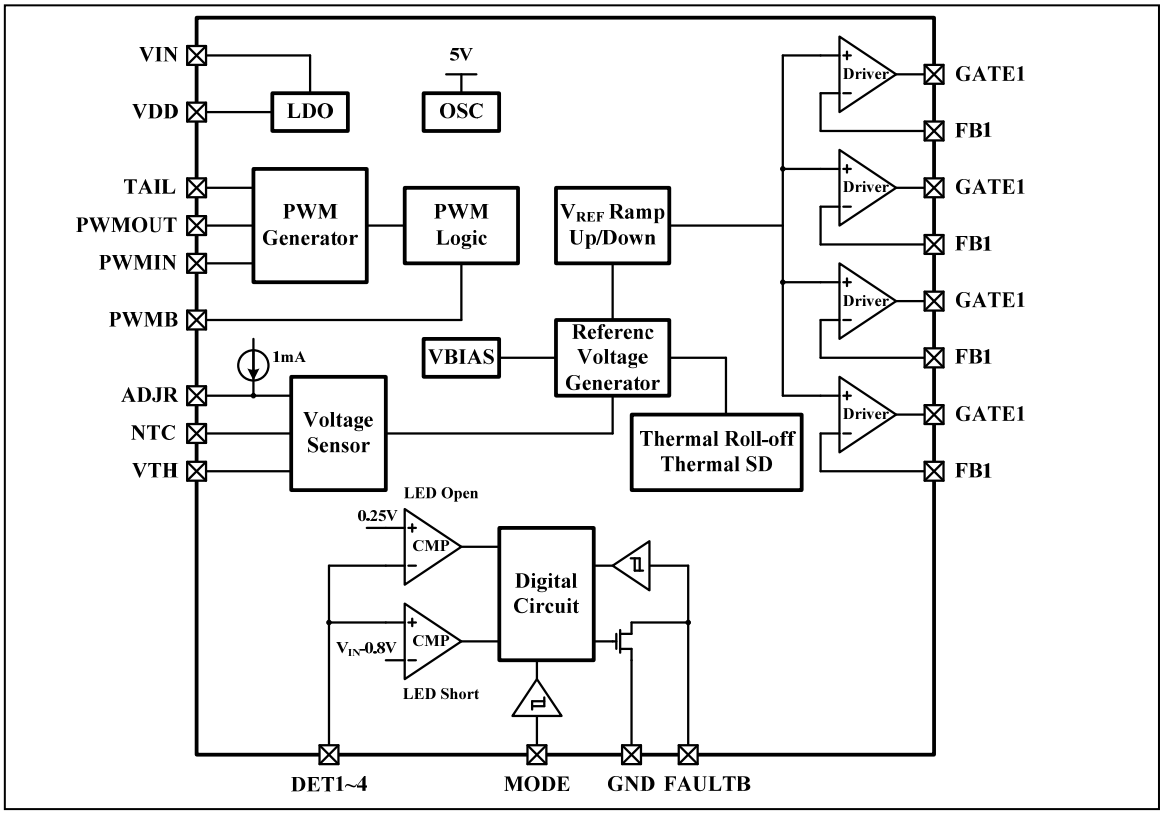
Note 2: Reference matching is defined as: ($V_{FB(max)}$ – $V_{FB(min)}$) / $V_{FB(AVG)}$. Where $V_{FB(AVG)}$ is the average of all V_{FB}.

Note 3: Rise Time to Fall Time Matching is defined as the maximum difference between the rise time and the fall time of the same string.

Note 4: Rise Time to Fall Time Mismatch between all strings is defined as the maximum ratio of the difference between either the rise time or the fall time to the average of the rise time or fall times between all strings.

Note 5: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

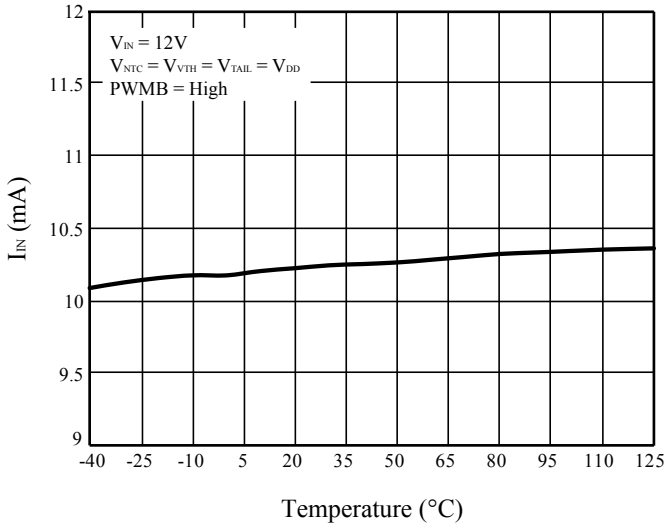


Figure 5 I_{IN} vs. Temperature

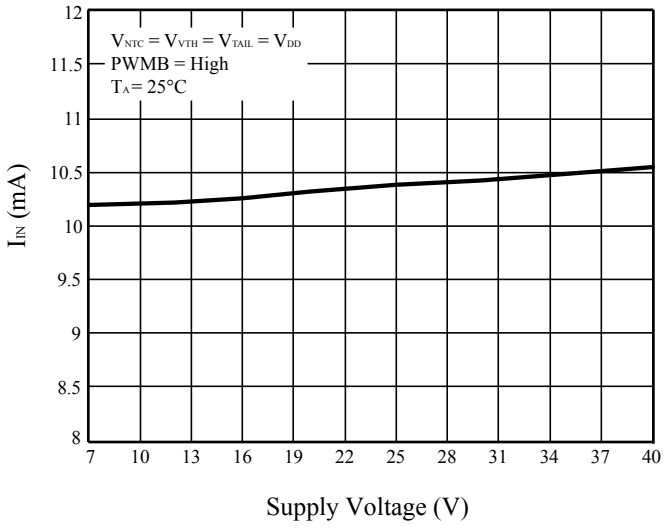


Figure 6 I_{IN} vs. Supply Voltage

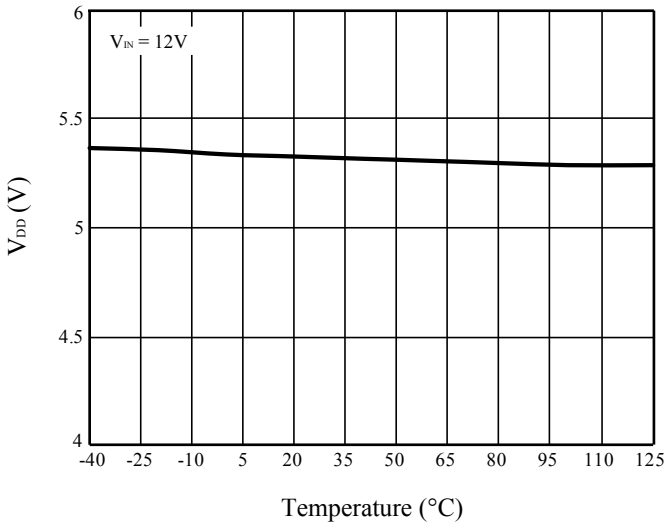


Figure 7 V_{DD} vs. Temperature

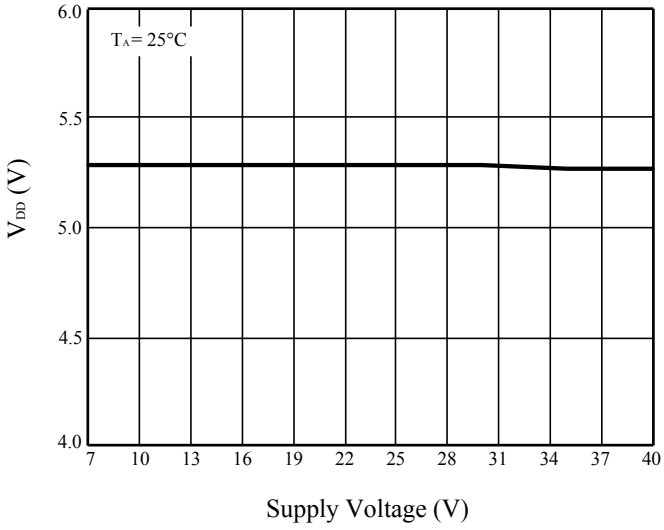


Figure 8 V_{DD} vs. Supply Voltage

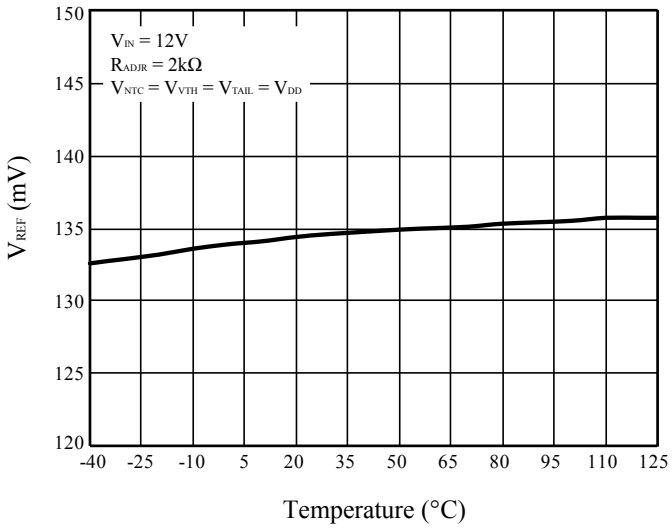


Figure 9 V_{REF} vs. Temperature

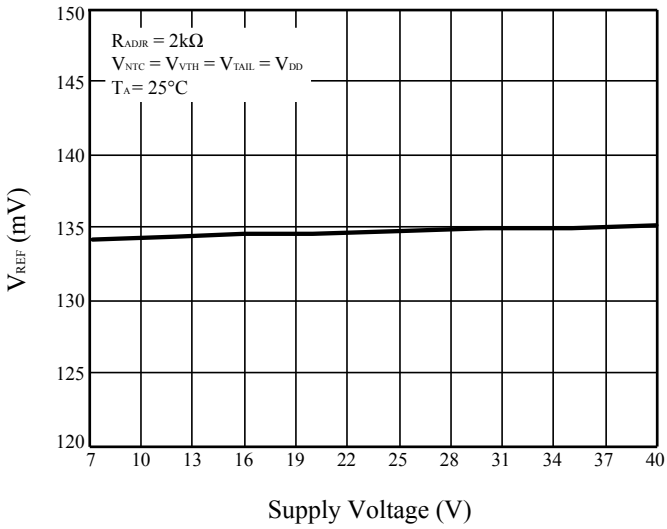


Figure 10 V_{REF} vs. Supply Voltage

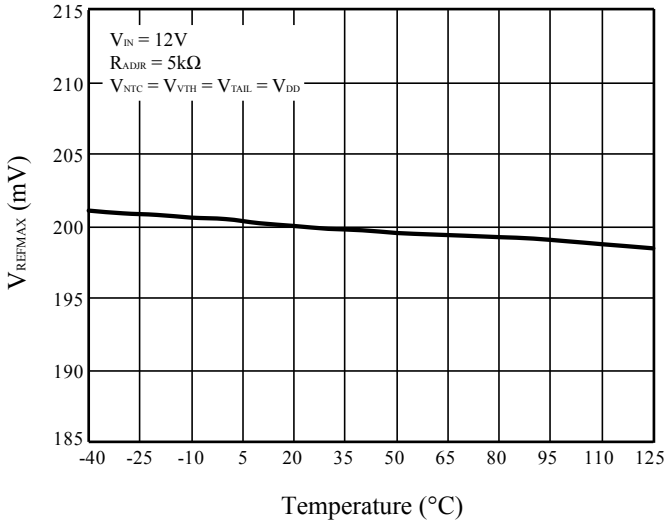


Figure 11 V_{REFMAX} vs. Temperature

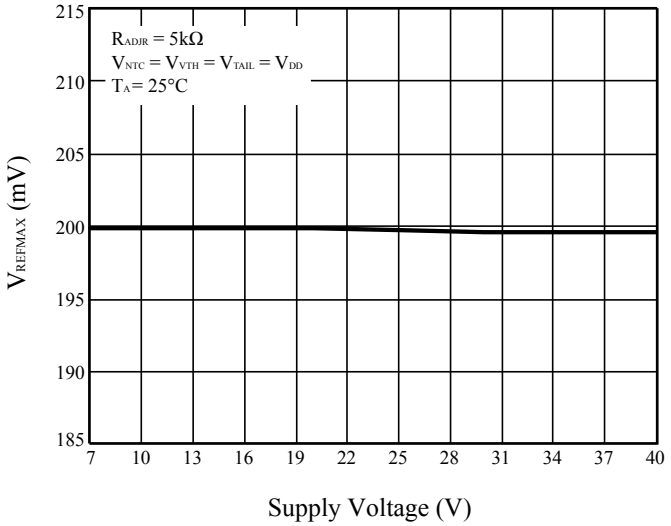


Figure 12 V_{REFMAX} vs. Supply Voltage

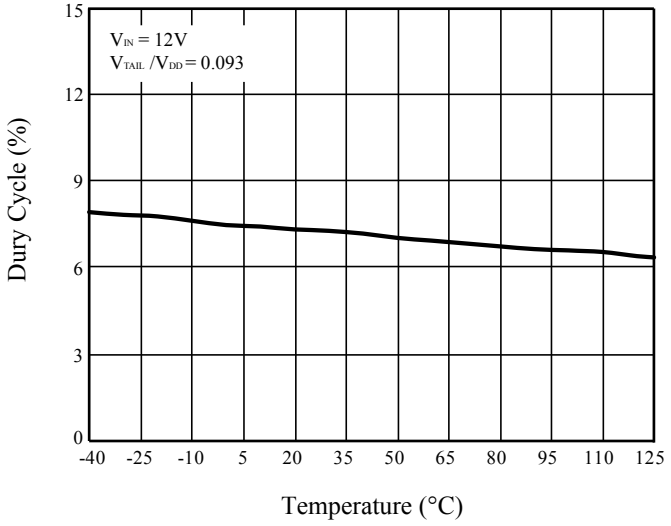


Figure 13 Duty Cycle vs. Temperature (Internal PWM)

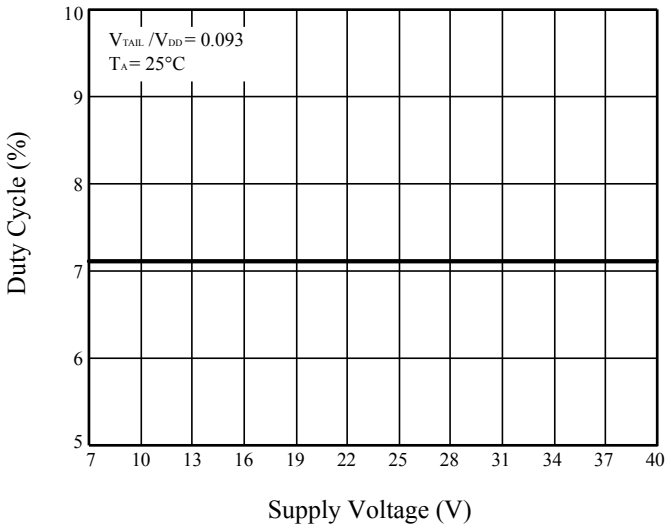


Figure 14 Duty Cycle vs. Supply Voltage (Internal PWM)

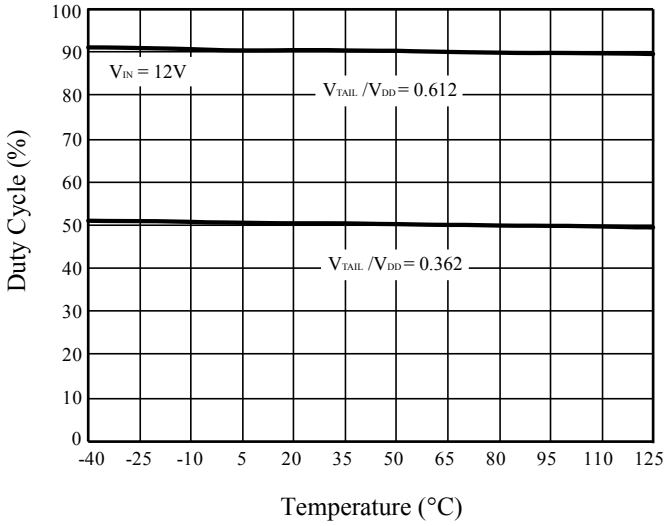


Figure 15 Duty Cycle vs. Temperature (Internal PWM)

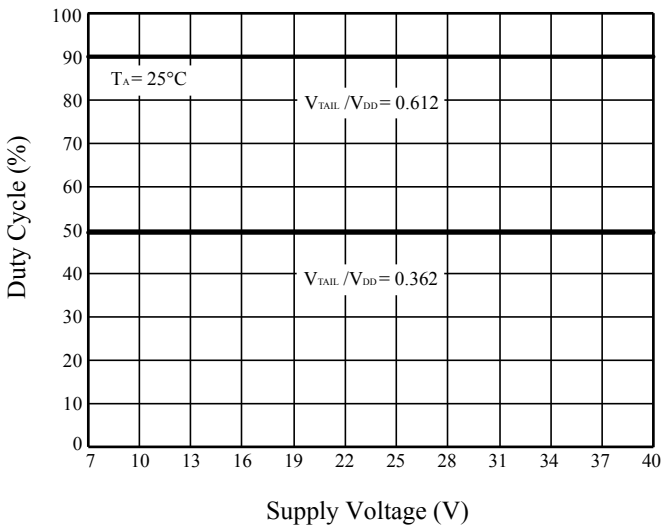


Figure 16 Duty Cycle vs. Supply Voltage (Internal PWM)

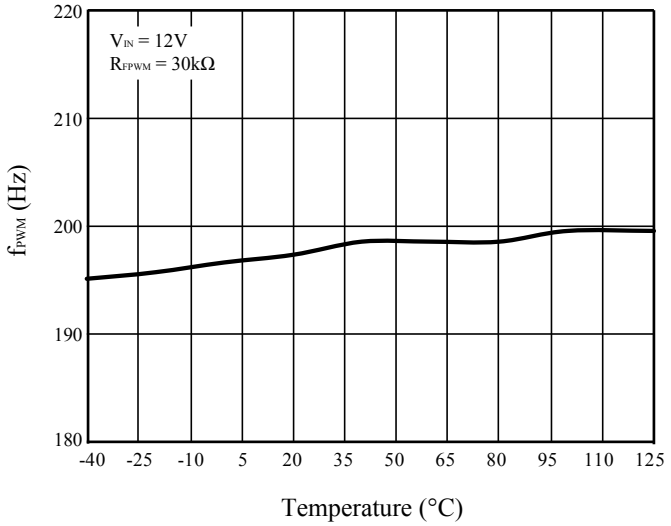


Figure 17 f_{PWM} vs. Temperature (Internal PWM)

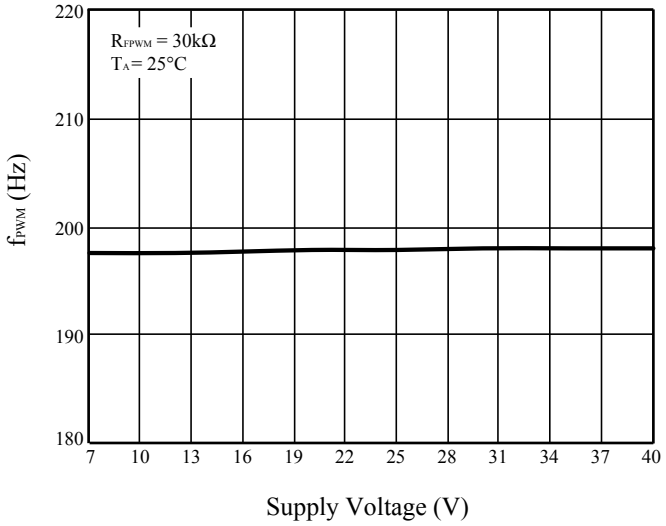


Figure 18 f_{PWM} vs. Supply Voltage (Internal PWM)

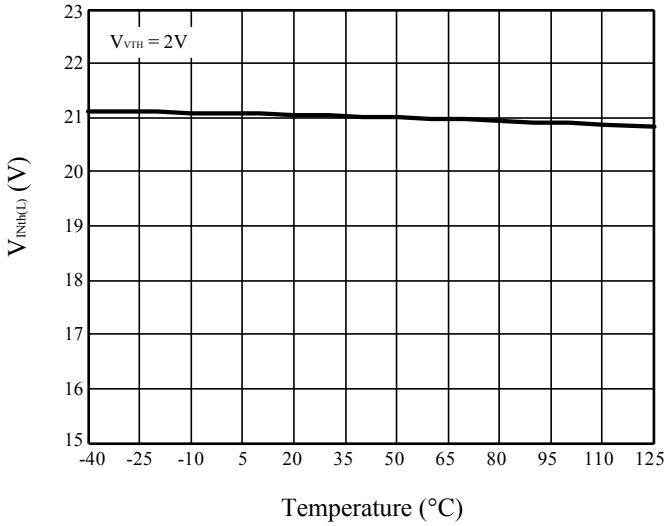


Figure 19 $V_{INth(L)}$ vs. Temperature

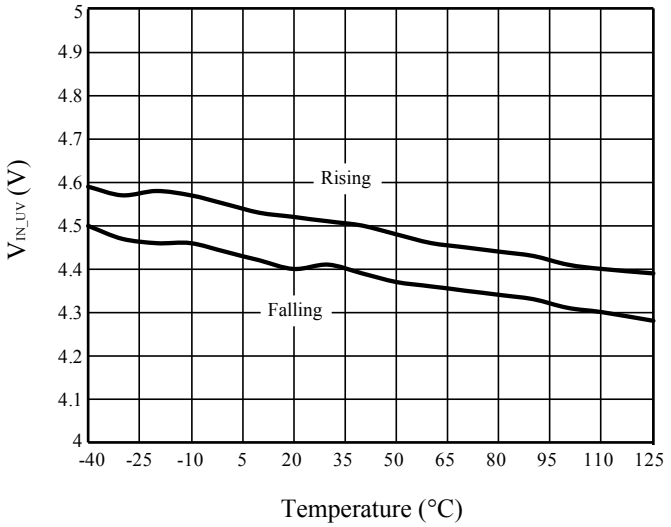


Figure 20 V_{IN_UV} vs. Temperature

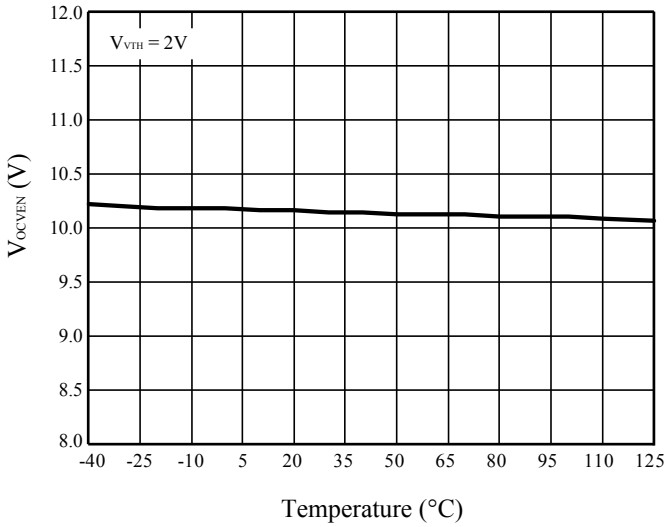


Figure 21 V_{OCVEN} vs. Temperature

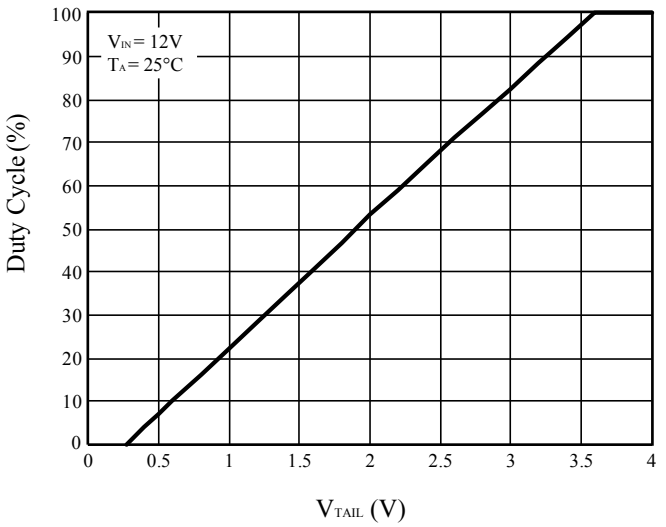


Figure 22 Duty Cycle vs. V_{TAIL} (Internal PWM)

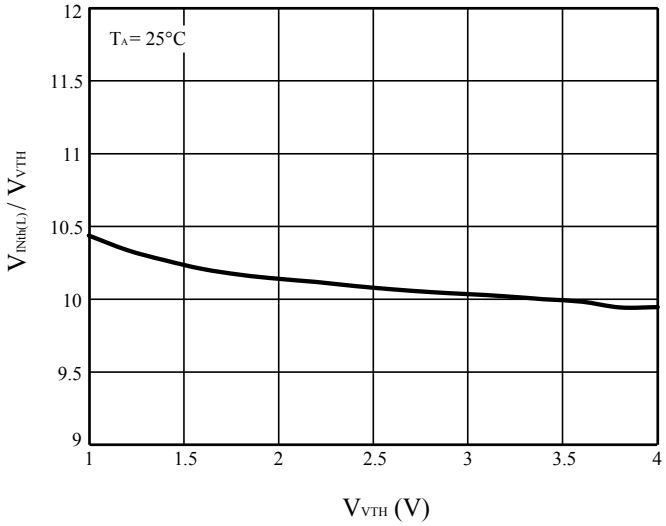


Figure 23 $V_{INth(L)}/V_{VTH}$ vs. V_{VTH}

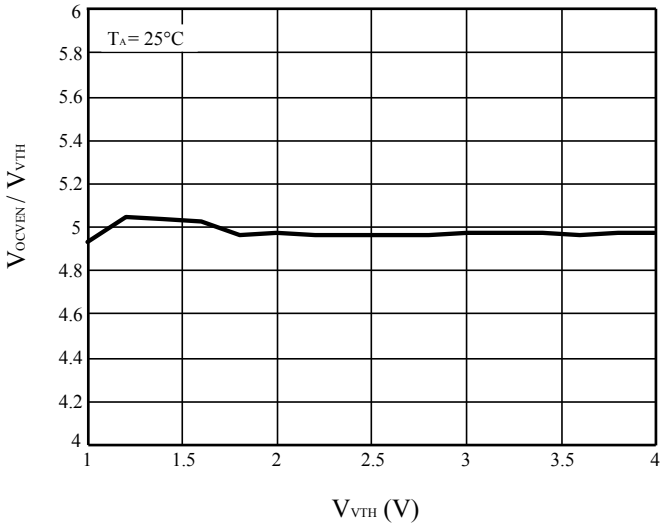


Figure 24 V_{OCVEN}/V_{VTH} vs. V_{VTH}

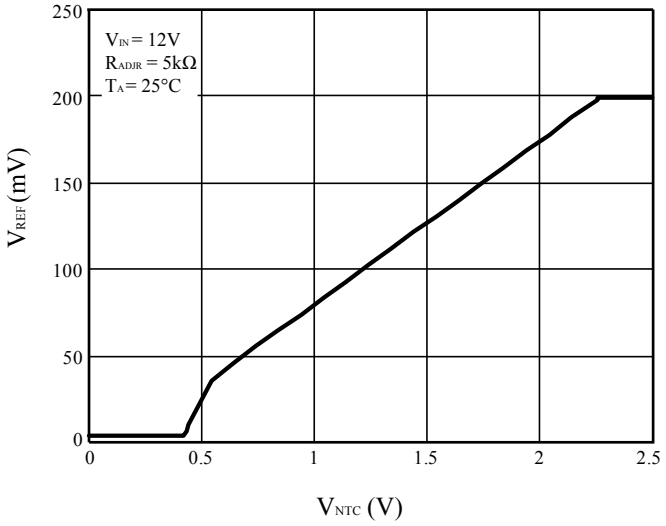


Figure 25 V_{REF} vs. V_{NTC}

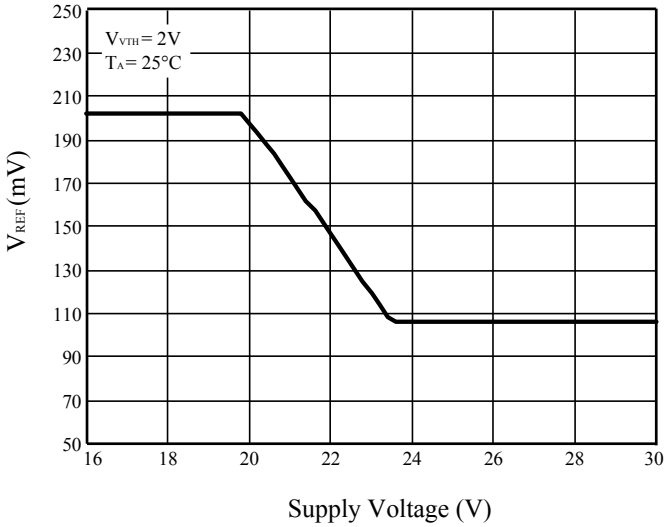


Figure 26 VIN OVP

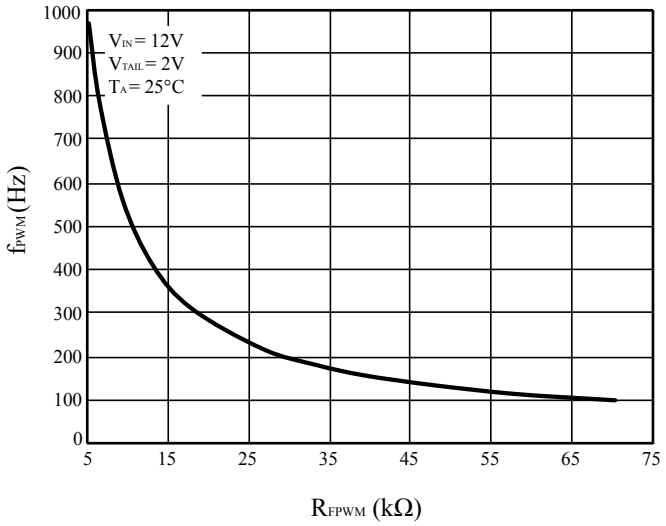


Figure 27 f_{PWM} vs. R_{FPWM} (Internal PWM)

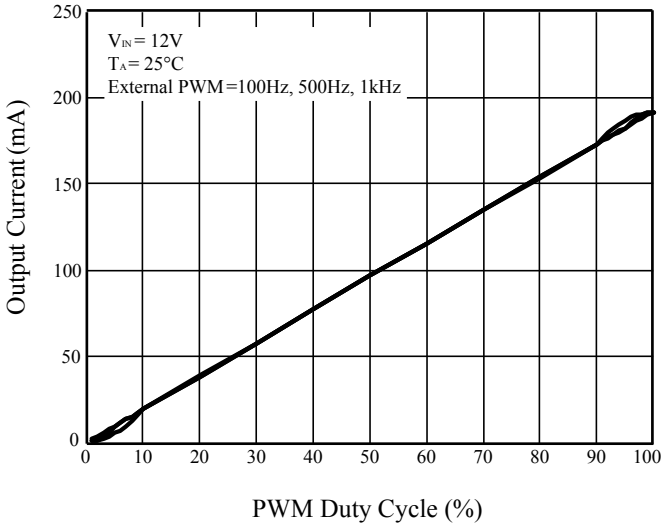


Figure 28 External PWM Dimming

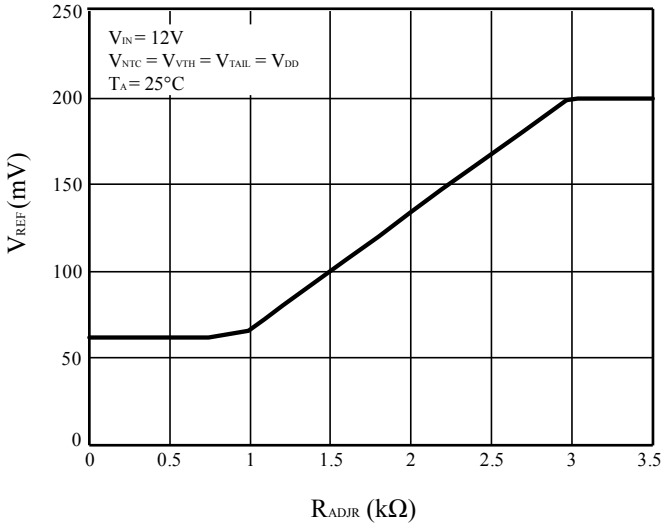


Figure 29 V_{REF} vs. R_{ADJR}

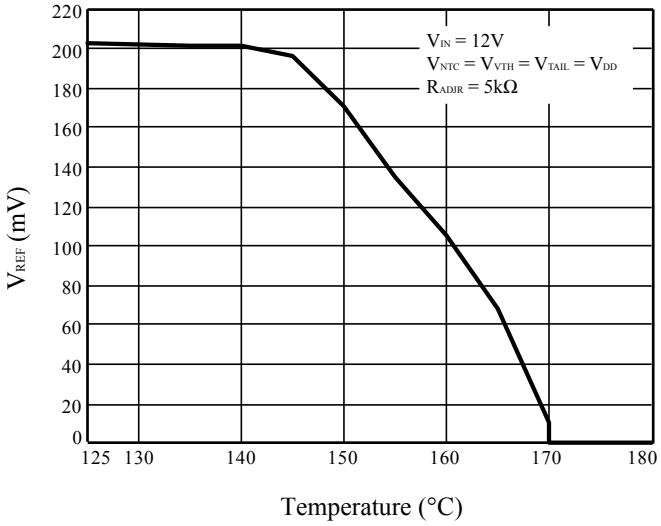


Figure 30 Thermal Rolloff

APPLICATION INFORMATION

The IS32LT3123 is a programmable linear controller capable of regulating high constant current in four LED strings with external NMOS FETs. A dedicated pin (PWMB) is able to switch the output current between full brightness mode (high current) and PWM dimming mode (low current) by an external logic level. In the PWM dimming mode, the PWM dimming can be either the internal PWM generator, whose duty cycle and frequency are programmed by TAIL and PWMIN pins, or an external PWM signal fed on PWMIN pin. Mounting different value resistors on ADJR pin can fine tune the output peak current for binning purpose. With a NTC resistor divider placed close to LED strings, IS32LT3123 can monitor the temperature of the LED strings and realize current derating if the temperature exceeds the setting thermal threshold, which effectively prevents the LED strings from thermal runaway damage. A settable input over voltage detection is provided to sense the input voltage and reduce the output current if the input voltage exceeds the targeted threshold. IS32LT3123 also integrates fault detection and protection circuitry for the LED string open/short and over temperature fault conditions and reports fault conditions by a dedicated pin (FAULTB). In the case of fault conditions, the MODE pin can control the action to be either “one fail all fail” or “one fail all on”. The FAULTB pins of multiple devices can be tied together for fault condition sharing to achieve simultaneous “one fail all fail”.

UNDER VOLTAGE LOCKOUT (UVLO)

IS32LT3123 features an under voltage lockout (UVLO) function on the VIN pin to prevent misoperation at too low input voltages. UVLO threshold is an internally fixed value and cannot be adjusted. The device is enabled when the V_{IN} voltage exceeds V_{IN_UV} (Typ. 4.5V), and disabled when the V_{IN} voltage falls below (V_{IN_UV}-V_{IN_UVHY}) (Typ. 4.35V).

LINEAR REGULATOR VDD

The device incorporates a linear regulator (VDD) output with a minimum 14mA current capability to power external circuitry. It requires a low ESR, X7R type ceramic capacitor from VDD pin to GND for proper operation; this capacitor must be placed as close to VDD pin as possible. To drive the external circuitry, the recommended capacitor value is 1μF.

OUTPUT CURRENT SETTING

The IS32LT3123 provides 4 channels of low-side current drive via 4 external NMOS FETs. The negative feedback loops drive the GATEs of NMOS FETs to maintain the current feedback voltage of FB pins equal to the internal reference voltage, V_{REF}. All channels share the same reference voltage source. So V_{REF} decides the output current. The regulated maximum LED current of each NMOS FET is individually set by its corresponding feedback resistor (R_{FB}). As Figure 31.

V_{REF} can be controlled by ADJR resistor (R_{ADJR}), NTC thermal rolloff protection, input over voltage protection and thermal rolloff protection actions. If R_{ADJR}≥3kΩ and no protection actions, V_{REF} is maximum value, V_{REFMAX} (Typ. 0.2V). The feedback resistor value can be computed using the following:

$$R_{FB} = \frac{V_{REFMAX}}{I_{OUT\_FULL}} \qquad (1)$$

Where I_{OUT_FULL} is output current of full brightness mode (without PWM dimming) in Amp and R_{FB} is in Ω.

It is recommend that R_{FB} be a 1% accuracy resistor with good temperature characteristic to ensure stable and precise output current.

When the desired current is high, the power rating also should be considered. The maximum power dissipation on the R_{FB} resistor is calculated by:

$$P_{RFB} = V_{REFMAX} \times I_{OUT\_FULL} \qquad (2)$$

A single high wattage resistor or several small wattage resistors in parallel can be used to sustain the power dissipation.

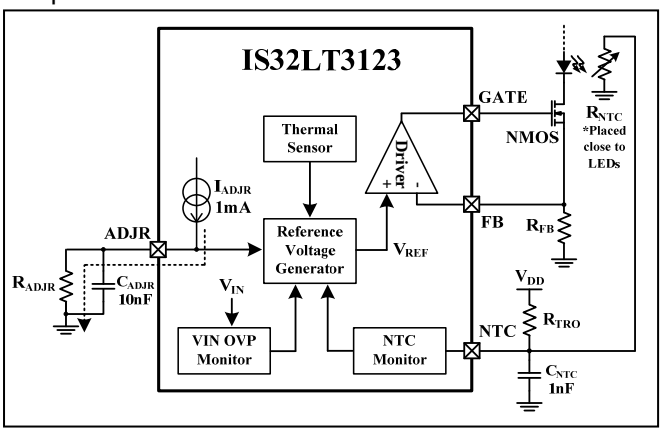


Figure 31 Constant Current Regulation

If any channel is unused, connect its FB pin to GND and leave its GATE pin floating. To avoid false protection triggering, its DET pin must be tied to one of the used channel’s DET pin as Figure 32.

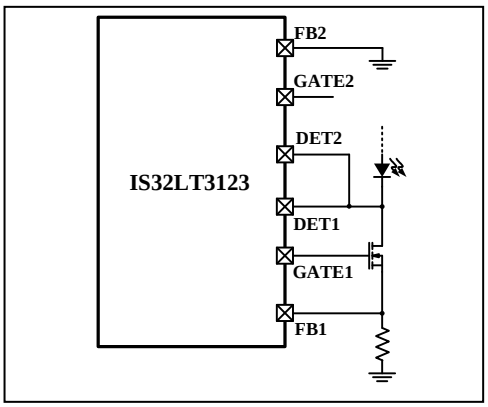


Figure 32 Unused Channel (CH1 Used and CH2 Unused)

CURRENT ADJUSTMENT BY ADJR

The ADJR pin is a dedicated pin for output current fine tuning. Connecting a proper range value resistor, R_{ADJR}, from this pin to GND can adjust the output current, which can be used for LED binning or output power ranking purpose. As Figure 31, there is a precise constant current source, I_{ADJR} (typ. 1mA), inside ADJR pin. When R_{ADJR} is connected, I_{ADJR} going through this resistor creates a voltage drop on AJDR pin which is detected by the internal Reference Voltage Generator circuit to generate the internal reference voltage, V_{REF}, for output current regulation.

If R_{ADJR} value is greater than or equal to 3kΩ, the V_{REF} is clamped at maximum value, V_{REFMAX} (typ. 0.2V). The output current will be the maximum setting value, I_{OUT_FULL} in Equation (1).

If R_{ADJR} value is between 1kΩ and 3kΩ, the V_{REF} is decided by:

$$V_{REF} = \left(\frac{R_{ADJR} \times 1mA}{3V} \right) \times 0.2V \quad (3)$$

So the output current can be adjusted by this resistor:

$$I_{OUT\_ADJR} = \frac{\left(\frac{R_{ADJR} \times 1mA}{3V} \right) \times 0.2V}{R_{FB}} \quad (4)$$

Where R_{ADJR} is in kΩ and R_{FB} is in Ω.

If the R_{ADJR} value is smaller than or equal to 1kΩ, the V_{REF} is clamped at 0.067V (Typ.). Then the output current will be:

$$I_{OUT\_ADJR} = \frac{0.067V}{R_{FB}} \quad (5)$$

It is recommend that R_{ADJR} be a 1% accuracy resistor with good temperature characteristics to ensure stable and precise output current. R_{ADJR} could be placed on LED board and connected to ADJR pin via a long hardness. To prevent external EMI noise interference from the harness, a 10nF X7R type ceramic capacitor, C_{ADJR}, must be added and placed as close to ADJR pin as possible to prevent noise interference.

All above equations are apply only if there are no protection actions.

LED THERMAL ROLLOFF PROTECTION BY NTC

IS32LT3123 is capable to implement LED over temperature current roll off protection in conjunction with an external NTC thermistor placed close to the LEDs. As Figure 31, NTC pin voltage, V_{NTC}, is monitored and feedback to the Reference Voltage Generator circuits to adjust the internal reference voltage, V_{REF}. V_{NTC} will not affect V_{REF} until dropping below NTC pin's voltage threshold, V_{NTC_TH} (typ. 2.2V). If $V_{NTC} \geq V_{NTC\_TH}$, the V_{REF} is clamped at the value set by R_{ADJR}. Once $V_{NTC} < V_{NTC\_TH}$, the internal reference voltage is decided by V_{NTC}:

$$V_{REF\_NTC} = V_{REF} - \frac{2.2V - V_{NTC}}{10} \quad (6)$$

Where, V_{REF} is set by R_{ADJR} value, as Equation (3) ~ (5). So the output current with NTC pin's adjustment will be:

$$I_{OUT\_NTC} = \frac{V_{REF\_NTC}}{R_{FB}} \quad (7)$$

In the application, a resistor divider containing a NTC thermistor (R_{NTC}) derives a voltage on NTC pin from V_{DD}. The NTC pin voltage is:

$$V_{NTC} = \frac{V_{DD} \times R_{NTC}}{R_{TRO} + R_{NTC}} \quad (8)$$

Due to the negative temperature coefficient characteristic of the NTC thermistor, the V_{NTC} gradually reduces following the temperature ramping up. The output current is constant until $V_{NTC} = V_{NTC\_TH}$. As shown in Figure 33, assume that the desired temperature point of current rolloff start is T_{ROSP}. With a given NTC thermistor, the NTC resistance (R_{NTC_ROSP}) at T_{ROSP} temperature point can be found in its datasheet. Put into Equation (8) to decide R_{TRO} value:

$$R_{TRO} = \frac{V_{DD} \times R_{NTC\_ROSP}}{V_{NTC\_TH}} - R_{NTC\_ROSP} \quad (9)$$

Choose a 1% accuracy resistor with good temperature characteristics for R_{TRO} to ensure stable and precise temperature threshold.

When the temperature ramps above T_{ROSP}, V_{NTC}'s reduction gradually derates the output current. The rolloff rate is decided by NTC's characteristics. The output current in rolloff range is:

$$I_{OUT\_TRO} = \frac{V_{REF} + 0.1 \times \frac{V_{DD} \times R_{NTC\_TRO}}{R_{TRO} + R_{NTC\_TRO}} - 0.22V}{R_{FB}} \quad (10)$$

Where, R_{NTC_TRO} is the NTC resistance at the temperature over T_{ROSP} which can be found in NTC's datasheet.

The R_{NTC} thermistor has to be placed close to LEDs which may be connected to IS32LT3123 driver board via long PCB traces or hardness. To prevent external EMI noise interference from these traces/harness, a 1nF X7R type ceramic capacitor, C_{NTC}, must be added and placed close to the NTC pin. If this LED protection is unused, connect the NTC pin to the VDD pin via a 10kΩ resistor.

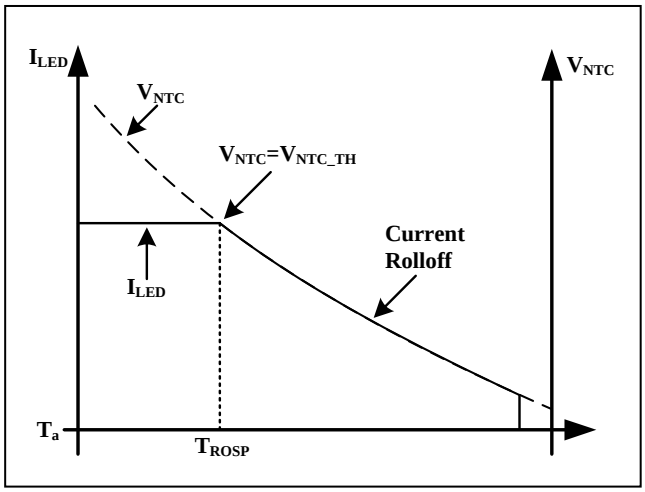


Figure 33 LED Thermal Rolloff Protection

If the current rolloff slew rate is too steep for the application, adding an optional resistor, R_{TRO1}, in series with R_{NTC} can slow down the slew rate as Figure 34.

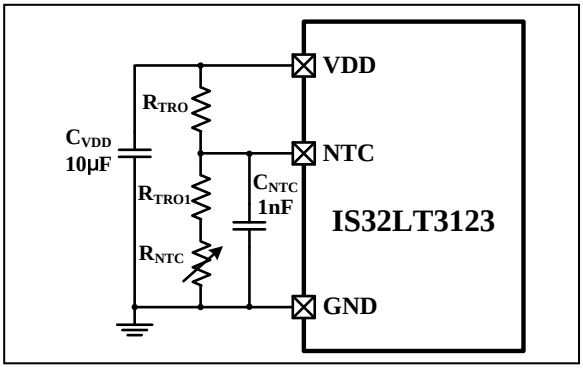


Figure 34 R_{TRO1} Slows Down Slew Rate

EXTERNAL NMOS FET

The IS32LT3123 uses the NMOS FETs as constant current sources operating in the "linear mode" as shown in the current saturation region in the output characteristic graph. As shown in the graph, the drain current (I_{DS}) is independent of the drain to source voltage (V_{DS}) it depends on the V_{GS} gate voltage of the NMOS FET. Therefore, since the NMOS FET is used as a constant current source, the current flow through the LED string is controlled by the V_{GS} voltage at the NMOS FET gate.

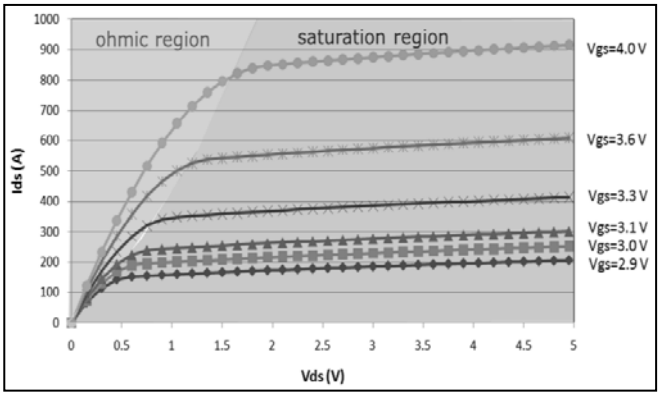


Figure 35 NMOS FET Operating Mode

The NMOS FET must be chosen with its drain voltage rating greater than the Transient Voltage Suppressor (TVS) clamp voltage of the load dump protection. And its current rating should be greater than the desired maximum current. To ensure constant current regulation, the voltage drop on drain to source (V_{DS}) of NMOS FET must be larger than its saturation voltage of desired current level, V_{DS_SAT}, which can be found from the "I_{DS} vs. V_{DS}" output characteristic graph in NMOS FET datasheet. Basically, larger current rating NMOS FET gets lower saturating voltage at same current level. As Figure 36. The minimum VIN voltage is decided by:

$$V_{IN\_MIN} = V_{LED} + V_{DS\_SAT} + V_{FB} \qquad (11)$$

Where V_{LED} is the LED string forward voltage.

So the larger V_{DS_SAT} will slightly affect the minimum VIN voltage.

All NMOS FET datasheets include a Safe Operating Area (SOA) diagram to be used as a tool to show the limits where the NMOS FET can be safely operated in linear mode. The SOA diagram is only valid for a given condition, different conditions require derating calculations.

In addition, because the NMOS FET doesn't have an over temperature protection mechanism, the power rating of the NMOS FET should be carefully considered to sustain the maximum power dissipation on it. When the LED string forward voltage is fixed, a higher input supply voltage will result in a larger V_{DS} voltage which results in more power dissipation on NMOS FET. Because the NMOS FET is operated in linear mode, the $R_{DS(on)}$ value of the MOSFET is not used when calculating power dissipation. The power dissipation in the NMOS FET depends only on the voltage drop V_{DS} and the current flow: $P_{NMOS} = V_{DS} \times I_{DS}$. So the maximum power dissipation at full brightness mode can be calculated by:

$$P_{NMOS\_MAX} = (V_{IN\_MAX} - V_{LED\_MIN} - V_{FB}) \times I_{OUT\_FULL} \qquad (12)$$

Where V_{IN_MAX} is the maximum input voltage in the application and V_{LED_MIN} is the LED string minimum forward voltage.

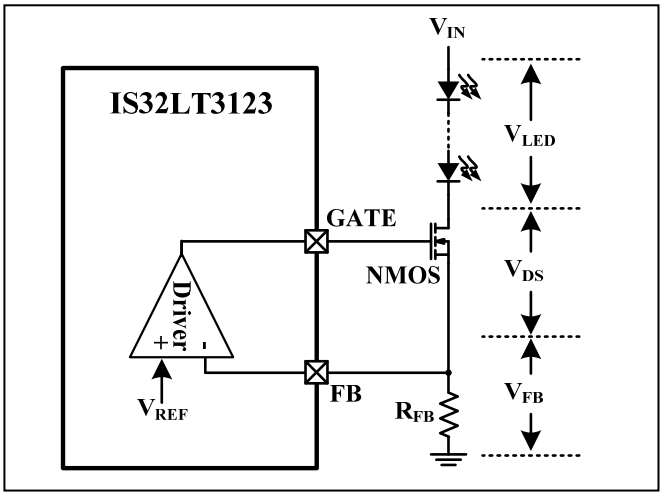


Figure 36 Voltage Drop

After calculating the maximum power dissipation, the junction temperature increase of the NMOS FET can be estimated. Make sure the junction temperature in worst case should not exceed the maximum operating junction temperature of the NMOS FET.

$$(P_{NMOS\_MAX} \times R_{\theta JA\_NMOS} + T_{A\_MAX}) < T_{J(MAX)\_NMOS} \quad (13)$$

Where, $T_{J(MAX)\_NMOS}$ is the maximum operating junction temperature limit of the NMOS FET. $R_{\theta JA\_NMOS}$ is the junction to ambient thermal resistance of the NMOS FET. T_{A_MAX} is the highest operating ambient temperature of the system.

A NMOS FET with a big thermal PAD and low thermal resistance is preferred, such as a SOT-223 or D-PAK package. When designing the Printed Circuit Board (PCB) layout, a double-sided PCB with a large copper area on each side of the board directly under these NMOS FETs must be used. Multiple thermal vias under the exposed pad will help conduct heat from the pad of NMOS FET to the copper on each side of the board. The thermal resistance can be further be reduced by using a metal substrate or by adding a heat sink. To avoid heat buildup, these power components should be spread out on the PCB board with some distance.

PWM DIMMING

IS32LT3123 supports two modes: full brightness mode and PWM dimming mode. When PWMB pin is pulled low, the IS32LT3123 will enable PWM dimming mode, which supports both internal and external PWM dimming modes. If PWMB pin is pulled high, the PWM dimming signal will be overridden to get full brightness mode (100% duty cycle) and its output current is as Equation (1)/(4)/(5). Note that both PWM dimming modes will simultaneously dim all output channels.

INTERNAL PWM DIMMING MODE

When the TAIL pin is connected to a voltage below 3.7V (typ.), the IS32LT3123 will be in internal PWM dimming mode. As in Figure 1. The integrated PWM generator is enabled and the voltage on TAIL pin determines the PWM duty cycle. The PWM duty cycle can be calculated as follows:

$$D_{PWM} = 160 \times \frac{V_{TAIL}}{V_{DD}} - 7.9 \quad (14)$$

Where, D_{PWM} is PWM duty cycle in %. V_{DD} and V_{TAIL} are in Volts.

To get better accuracy, recommend to derive V_{TAIL} by a precise resistor divider from V_{DD} (as R_{TAIL1} and R_{TAIL2} in Figure 1, 1% accuracy resistor is recommended to be used) and the recommended duty cycle setting range is 5%~95%. The lower duty cycle results in lower output current accuracy. A 1nF X7R type ceramic capacitor, C_{TAIL}, should be added and placed close to TAIL pin for noise decoupling. The output current is modulated by the PWM duty cycle:

$$I_{OUT\_PWM} = I_{OUT\_FULL} \times D_{PWM} \quad (15)$$

If R_{ADJR}<3KΩ, the output current will be:

$$I_{OUT\_PWM} = I_{OUT\_ADJR} \times D_{PWM} \quad (16)$$

When the duty cycle is set by the TAIL pin, the PWM frequency is programmed by a single resistor, R_{FPWM}, connected from PWMIN pin to GND. The PWM frequency can be set in a range of 100Hz~1kHz. Since the output current has slew rate control for EMI consideration, the lower PWM frequency will get better output accuracy. The resistor value can be calculated as follows:

$$R_{FPWM} = \frac{5380}{f_{PWM} - 20.7} \quad (17)$$

Where, f_{PWM} is desired PWM frequency in Hz and R_{FPWM} is in kΩ.

An external voltage on the TAIL pin instead of the resistor divider can be used for analog input PWM dimming. As in Figure 3. The PWM duty cycle and frequency are identical as Equation (14) and (17). A 1nF X7R type ceramic capacitor, C_{TAIL}, must be added and placed close to TAIL pin for noise decoupling.

EXTERNAL PWM DIMMING MODE

When the TAIL pin is tied to V_{DD} directly, the IS32LT3123 will be in external PWM dimming mode. As in Figure 2. The integrated PWM generator is disabled. An external PWM signal on PWMIN pin can modulate the output current based on the duty cycle. The recommended frequency range of the external PWM signal is 100Hz~1kHz and the duty cycle can be from 0 to 100%. Since the output current has slew rate control for EMI consideration, a lower frequency PWM will get better dimming contrast ratio. The calculation of output current is identical as Equation (15) and (16). Note that the PWMIN pin is high impedance input in

external PWM dimming mode.

PWM DIMMING SYNCHRONIZATION

When PWMB pin is pulled low (PWM dimming mode), the PWMOUT pin is able to output a PWM signal to drive other slave devices for PWM dimming synchronization. When the device is configured as internal PWM dimming mode (PWMB pin pulled low and V_{TAIL}<3.7V), the output of the PWMOUT pin is the internal PWM generator. When the device is configured as external PWM dimming mode (PWMB pin pulled low and TAIL pin tied to VDD), the output of the PWMOUT pin is synchronized with the signal on PWMIN pin. For lighting systems with multiple IS32LT3123 controllers, one controller can be configured as internal PWM dimming mode to be a master and output a PWM signal. Other controllers can be configured as external PWM dimming mode to be slaves. Connect all PWMIN pins of the slaves to the PWMOUT pin of the master to implement PWM dimming synchronization. As in Figure 4. If the PWMOUT pin is unused, leave it floating.

FAULT PROTECTION AND REPORTING

For robust system reliability, the IS32LT3123 integrates the detection circuitry to protect various fault conditions and report the fault conditions on the FAULTB pin which can be monitored by an external host. The fault protections include LED string open/short, VIN over voltage, controller junction thermal rolloff, LED thermal rolloff and thermal shutdown. Refer to Table 1. The FAULTB pin is open drain structure with both input and output function. The FAULTB pin is not allowed to float. An external resistor, R_{FAULTB}, must be added to pull up FAULTB pin above 2V for normal operation. The recommended resistor value is 47kΩ. The FAULTB pin will go low when the device enables fault detection and detects a fault condition.

As an input pin (MODE pin high), externally pulling FAULTB pin low will disable the output. For lighting systems with multiple IS32LT3123 controllers which require the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection as shown in Figure 4. A fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn them off. This satisfies the “one fail all fail” operating requirement.

VIN OVER VOLTAGE CURRENT DERATING PROTECTION

According to Equation (12), the input voltage will significantly affect the power dissipation on the NMOS FET. With given LED strings and output current, the higher input voltage the large power dissipation on NMOS FET. In automotive applications, the nominal battery voltage range is about 9V to 16V. However, electrical and radio-frequency disturbance frequently occur in vehicle environment that results in the supply voltage jumping over 16V. Such as load dump case, it could raise up the supply voltage over 40V. Since the NMOS FET doesn’t have over temperature protection mechanism, the IS32LT3123 integrates a power supply over voltage current derating protection to avoid thermal runaway on the NMOS FET.

As Figure 31, the VIN voltage is monitored and fedback to the Reference Voltage Generator circuit to adjust the internal reference voltage, V_{REF}, thereby the output current is changed accordingly. In case the VIN voltage exceeds a setting over voltage threshold, the device will start to gradually reduce the internal reference voltage (V_{REF}) down by 49%*V_{REFMAX}, following the increasing V_{IN}. The VIN over voltage threshold, V_{INOV_TH}, is set by an external resistor divider (R_{TH1} and R_{TH2}) from VIN pin connected to VTH pin:

$$V_{INOV\_TH} = 10 \times V_{VTH} = 10 \times \frac{V_{DD} \times R_{TH2}}{R_{TH1} + R_{TH2}} \quad (18)$$

Where, V_{VTH} is VTH pin voltage. Choose proper R_{TH1} and R_{TH2} to make sure V_{VTH} is within 1V to 4V. R_{TH1} and R_{TH2} must be 1% accuracy resistor with good temperature characteristics to ensure stable and precise voltage threshold.

When V_{IN}>V_{INOV_TH} before V_{REF} being reduced by 49%*V_{REFMAX}, the internal reference voltage is decided by:

$$V_{REF\_OV} = V_{REF} - 0.0286 \times (V_{IN} - V_{INOV\_TH}) \quad (19)$$

$$I_{OUT\_OV} = \frac{V_{REF\_OV}}{R_{FB}} \quad (20)$$

Where, V_{REF} is set by R_{ADJR} value, as Equation (3) and (5). Assume V_{VTH}=2V, the V_{REF} will drop down by 49%*V_{REFMAX} at around V_{IN}=23.4V and stay at this level for higher VIN voltage.

If the NTC thermistor LED thermal rolloff also kicks in, the internal reference voltage would be:

$$V_{REF\_OV} = V_{REF\_NTC} - 0.0286 \times (V_{IN} - V_{INOV\_TH}) \quad (21)$$

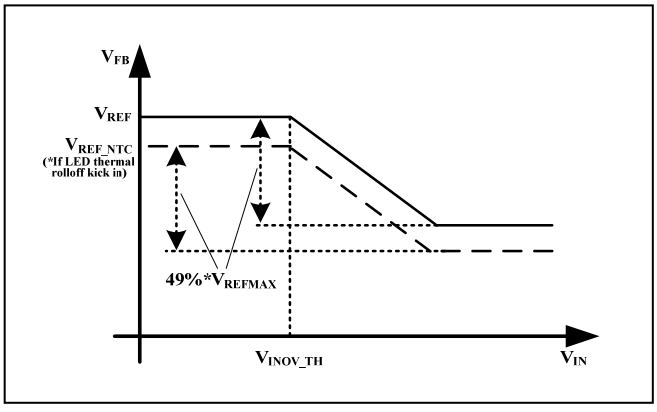


Figure 37 V_{IN} Over Voltage Protection

VIN over voltage protection won't be reported via FAULTB pin.

LED STRING OPEN PROTECTION

The LED string open detection is enabled after VIN voltage rising above a setting threshold, V_{INOC_TH}, which is to prevent insufficient V_{IN} falsely triggering LED string open detection. The threshold is programmed by the external resistor divider (R_{TH1} and R_{TH2}) from VIN pin connected to VTH pin as well:

$$V_{INOC\_TH} = 5 \times V_{VTH} = 5 \times \frac{V_{DD} \times R_{TH2}}{R_{TH1} + R_{TH2}} \quad (22)$$

If any LED string is open, the corresponding DET pin connected to NMOS FET's drain is pulled down by NMOS FET. If $V_{IN}>V_{INOC\_TH}$ and the DET pin voltage drops below the open LED detect voltage, V_{OCV}, the LED string open protection will be triggered and FAULTB pin will go low to report the fault condition. The MODE pin decides the fault protection mode. If the MODE pin is high, the fault protection mode is "one fail all fail". So that the GATE pins of all normal channels will go low to turn off all LED strings. The GATE pin of the faulty channel will remain high for recovery detection, but the corresponding LED string will be off due to LED open. If the MODE pin is low, the fault protection mode is "one fail all on" which means that all normal channels will keep normal operation, however the LED string of the faulty channel will be off due to LED open. No matter in which fault mode, the device will recover to normal operation and FAULTB pin will go back to high impedance once the open condition is removed.

LED STRING SHORT PROTECTION

The LED string short condition is detected if the voltage across VIN pin to any one of DET pins is lower than short detect voltage, V_{SCV}. Once short condition occurs, the FAULTB pin will go low to report the fault condition. If the MODE pin is high, the fault protection mode is "one fail all fail". So that the GATE pins of all normal channels will go low to turn off all LED strings. The GATE pin of the faulty channel will remain high for recovery detection, but the corresponding LED string will be off due to LED open. If the MODE pin is low, the fault protection mode is "one fail all on" which means that all normal channels will keep normal operation, however the LED string of the faulty channel will be off due to LED short. No matter in which fault mode, the device will recover to normal operation and FAULTB pin will go back to high impedance once the short condition is removed.

CONTROLLER JUNCTION THERMAL ROLLOFF

This feature is to protection the controller itself. The output current will be equal to the set value as long as the junction temperature of the controller remains below 145°C (typ.). If the junction temperature exceeds this threshold, the V_{REF} of the controller will begin to reduce toward zero at a rate of about -7.34mV/°C following the temperature ramping up. controller thermal rolloff protection won't be reported via FAULTB pin.

CONTROLLER THERMAL SHUTDOWN

In the event that the junction temperature exceeds 170°C, the output channels will go to the 'OFF' state and FAULTB pin will pull low to report the fault condition. At this point, the IC presumably begins to cool off. Any attempt to toggle the channel back to the source condition before the IC cooled to <140°C will be blocked and the IC will not be allowed to restart, and FAULTB pin will recover to high impedance.

Table 1 Fault Condition

Protection Type	Detect Condition	FAULTB	MODE=V_{DD} (one fail all fail)				MODE=GND (one fail all on)			
			PWMOUT	Faulty String	Other Strings	Recover	PWMOUT	Faulty String	Other Strings	Recover
Short LED	(V_{IN}-V_{DETx})<V_{SCV}	Pulled low	Pulled low	Keep on with 100% duty cycle irrespective of any PWM mode.	Turn off	Fault condition removed	Normal	The LEDs will be off due to shorted, however the current in the NMOS FET will be normal.	Normal	Fault condition removed
		This fault is detected after all GATEx high and completion of reference ramp. When detected, the fault remains active independent of GATE status.								
Open LED	$V_{IN}>V_{INOC\_TH}$ and $V_{DETx}<V_{OCV}$	Pulled low	Pulled low	Keep on with 100% duty cycle irrespective of any PWM mode.	Turn off	Fault condition removed	Normal	The LEDs will be off due to open, however the corresponding GATE pin will be high.	Normal	Fault condition removed
Controller Thermal Rolloff	T_J exceeds 145°C	Normal	Normal	All string current derates based on junction temperature.		T_J drops below 145°C	Normal	All string current derates based on junction temperature.		T_J drops below 145°C

V_{IN} Over Voltage	$V_{IN}>V_{INOV\_TH}$	Normal	Normal	All string current derates based on supply voltage.	$V_{IN}\leq V_{INOV\_TH}$	Normal	All string current derates based on supply voltage.	$V_{IN}\leq V_{INOV\_TH}$
Thermal Shutdown	T_J exceeds 170°C	Pulled low	Pulled low	All string turn off	T_J drops below 140°C	Normal	All string turn off	T_J drops below 140°C
LED String Thermal Rolloff	$V_{NTC}<V_{NTC\_TH}$	Normal	Normal	All string current derates based on NTC pin voltage.	$V_{NTC}\geq V_{NTC\_TH}$	Normal	All string current derates based on NTC pin voltage.	$V_{NTC}\geq V_{NTC\_TH}$

CONTROLLER THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, θ_{JA}, as in Equation (23):

$$P_D = V_{IN} \times I_{IN} \qquad (23)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \qquad (24)$$

When operating the chip at high ambient temperatures, or when the supply voltage is high, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (25):

$$P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \qquad (25)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{28.1°C/W} \approx 3.56W \qquad (26)$$

for eTSSOP-24 package.

Figure 38, shows the power derating of the IS32LT3123 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

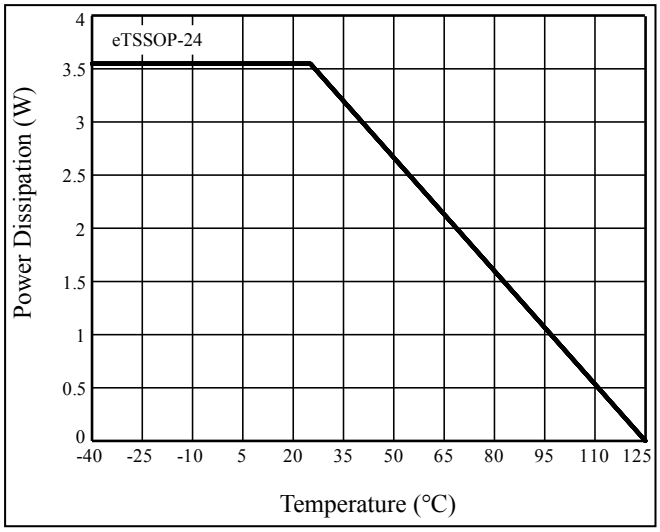


Figure 38 Dissipation Curve (eTSSOP-24)

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a large copper area on each side of the board directly under the IS32LT3123. Multiple thermal vias, as shown in Figure 39, will help to conduct heat from the exposed pad of the IS32LT3123 to the copper on each side of the board.

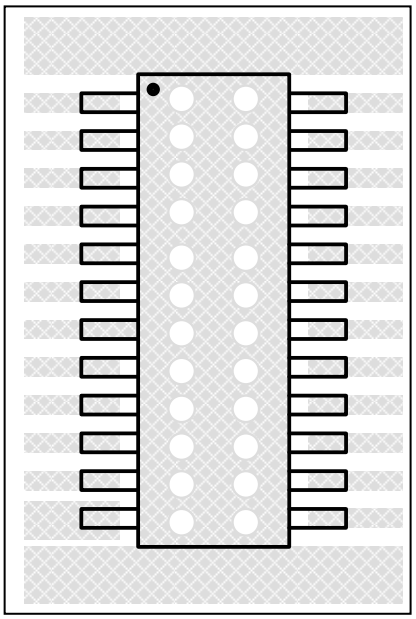


Figure 39 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

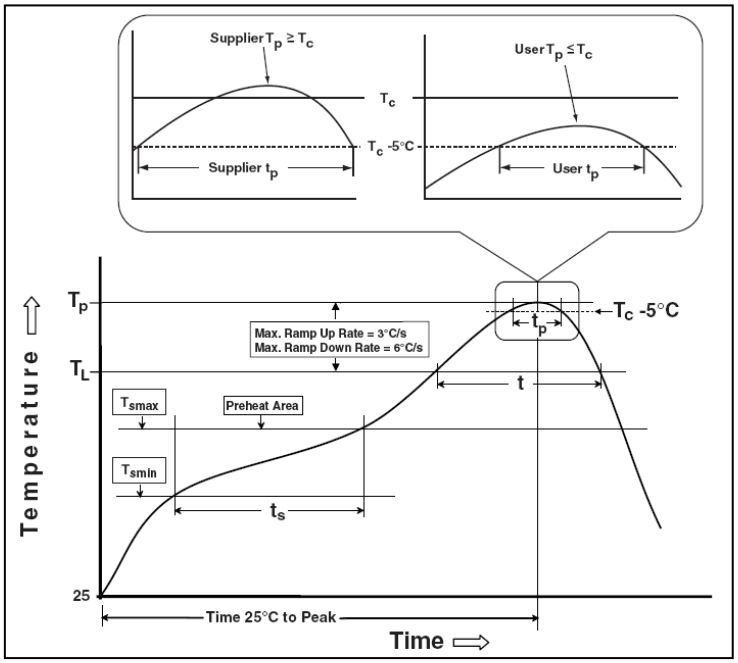
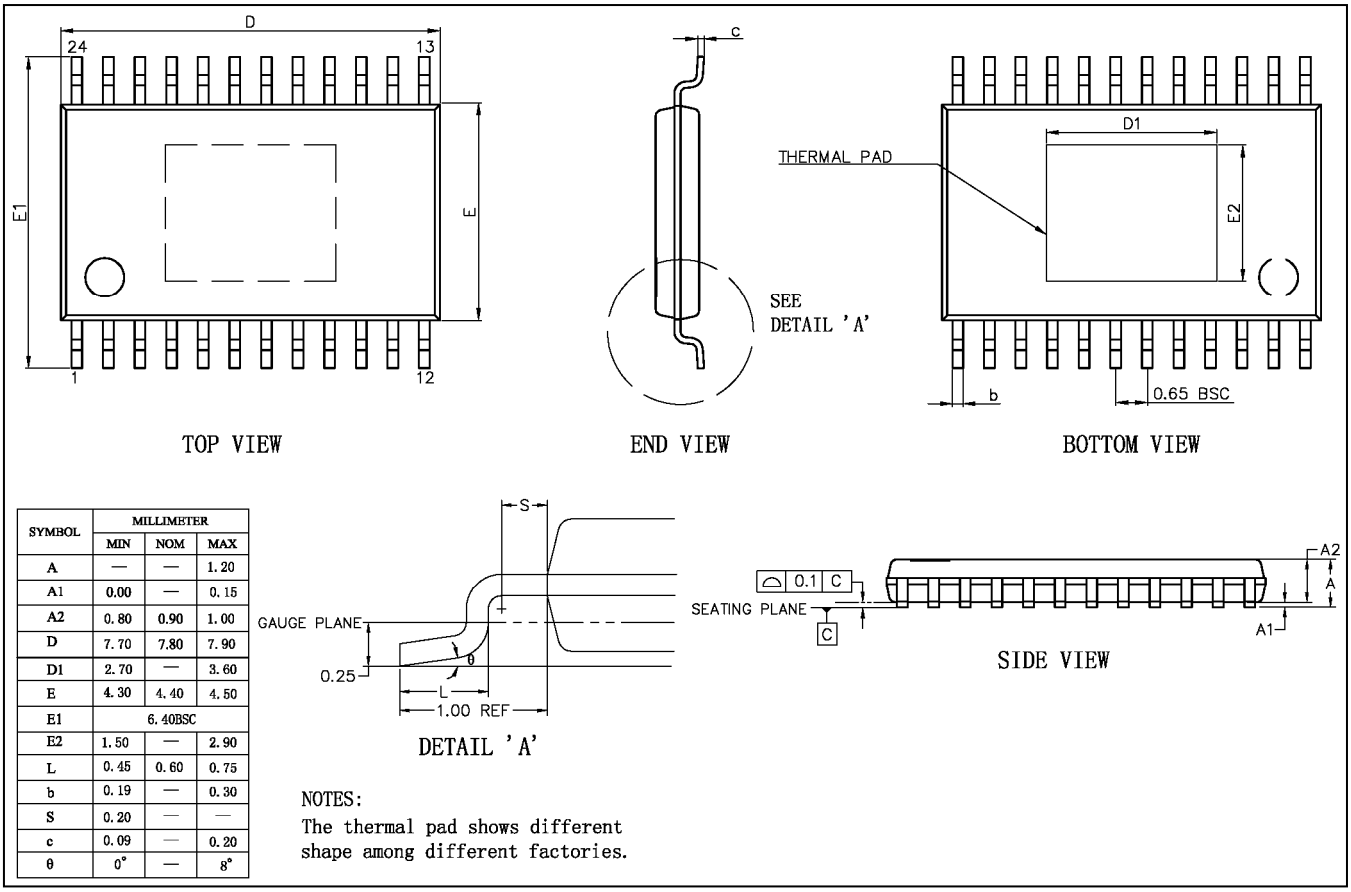


Figure 40 Classification Profile

PACKAGE INFORMATION

eTSSOP-24

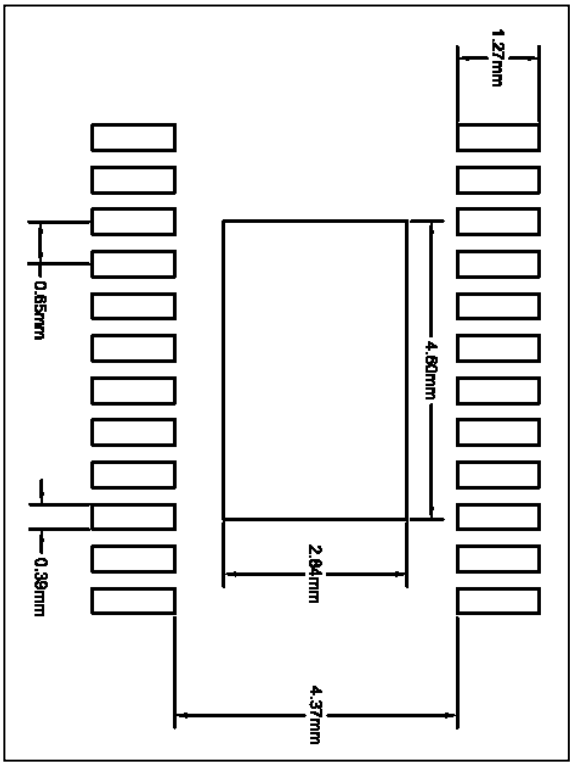


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.00
D	7.70	7.80	7.90
D1	2.70	—	3.60
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	2.90
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN

eTSSOP-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0C	Initial release.	2020.03.19
A	1. Update EC table 2. Remove Tube packing	2020.05.06