

General Description

The AOZ1363DI is a high-side load switch intended for applications that require circuit protection. The device operates from voltages between 5V and 16V, and capable of supplying 6A of continuous current. The internal current limiting circuit protects the input supply voltage from large load current. The AOZ1363DI provides thermal protection function that limits excessive power dissipation. The device employs an externally programmable soft-start circuitry to control inrush current due to highly capacitive loads associated with hot-plug events. It features low quiescent current of 400 μ A and the supply current reduces to less than 10 μ A in shutdown.

The device can output current monitoring information with an accuracy of 10% at a specified load current of 3A. The device can detect the over-current fault condition and execute the switch power down within a maximum delay time of 100ns. It features an input overvoltage protection where the device powers down when the power input voltage exceeds 19V.

The AOZ1363DI is available in a 3mm x 3mm DFN-12L package and can operate over -40 °C to +85 °C temperature range.

Features

- 5V to 16V operating input voltage
- 40m Ω maximum on resistance
- Fast 100ns switch turn off time during OCP
- Current monitoring with 10% accuracy (3A)
- Externally programmable soft-start
- Low quiescent current
- Under-voltage lockout
- Thermal shutdown protection
- Input over-voltage protection
- 2.0kV ESD rating
- Small 3mm x 3mm DFN-12L package

Applications

- Notebook PCs
- Hot swap supplies
- Micro-servers



Typical Application

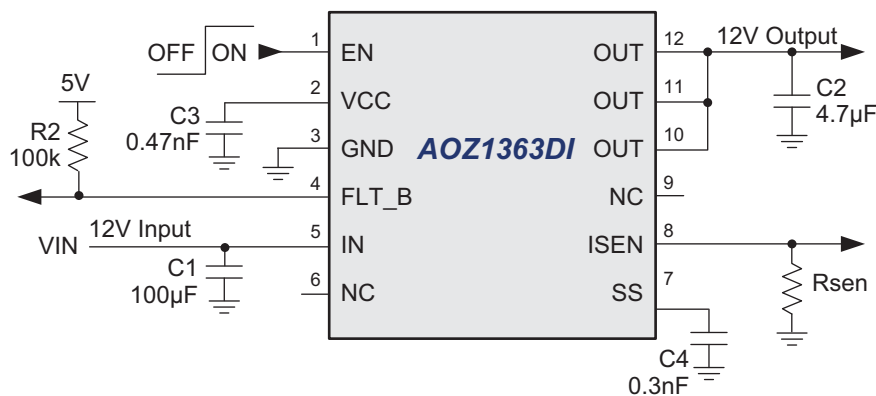


Figure 1. Typical Application Circuit (with Current Monitoring)

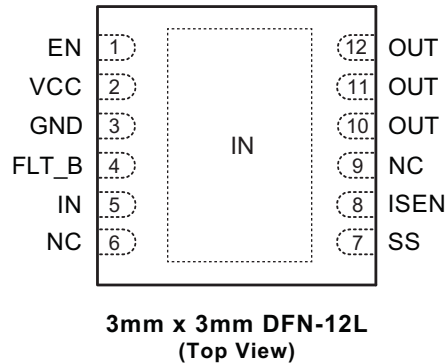
Ordering Information

| Part Number | Ambient Temperature Range | Package | Environmental |
|-------------|---------------------------|-------------------|----------------|
| AOZ1363DI | -40°C to +85°C | 3mm x 3mm DFN-12L | RoHS Compliant |



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|----------|--|
| 1 | EN | Enable Input. Active high. For automatic enabling, this pin is highly recommended to connect to VCC. |
| 2 | VCC | VCC is a bypass pin. Connect a 0.47nF capacitor from VCC to GND. |
| 3 | GND | Ground. |
| 4 | FLT_B | Fault Output pin. This is an open drain output that is externally pulled high with a pull-up resistor. Drain is internally pulled down to GND to indicate a fault condition. Connect to 5V, 3.3V, or VCC through a 100kΩ pull-up resistor. |
| 5, EPAD | IN | N-channel MOSFET Drain. Connect a 100μF capacitor from IN to GND |
| 6, 9 | NC | No Connection. |
| 7 | SS | Externally Programmable Soft-Start pin. |
| 8 | ISEN | Current Sense Information Output. See Figure 3 for Rsen value. |
| 10, 11, 12 | OUT | N-channel MOSFET Source. Connect a 4.7μF capacitor from OUT to GND. |

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

| Parameter | Rating |
|--|---------------|
| IN, OUT, ISEN to GND | -0.3V to +24V |
| VCC, EN, SS, FLAG | -0.3V to 6V |
| Maximum Continuous Current | 6A (25°C) |
| Maximum Junction Temperature (T _J) | +150°C |
| ESD Rating (HBM) | 2.0kV |

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

| Parameter | Rating |
|------------------------------|--------|
| Thermal Resistance (DFN 3x3) | 40°C/W |

Electrical Characteristics

V_{IN} = 12V, T_A = 25°C unless otherwise stated.

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|----------------------|---|---|------|------|-------------------|-------|
| V _{IN} | Input Supply Voltage | | 5 | | 16 | V |
| V _{UVLO} | Undervoltage Lockout Threshold | IN rising | | 4.1 | 4.4 | V |
| V _{UVHYS} | Undervoltage Lockout Hysteresis | | | 400 | | mV |
| V _{UVP} | Input Overvoltage Protection | IN rising | | 19 | | V |
| V _{UVHYS} | Input Overvoltage Protection Hysteresis | | | 1.5 | | V |
| I _{IN_ON} | Input Quiescent Current | EN = 4V, no load | | 400 | 600 | μA |
| I _{IN_OFF} | Input Shutdown Current | EN = GND, no load | | | 10 | μA |
| I _{LEAK} | Output Leakage Current | EN = GND, no load | | | 10 | μA |
| R _{DS(ON)} | Switch On Resistance | V _{IN} = 12V | | 23 | 40 | mΩ |
| I _{LIM} | Current Limit | | -25% | 11 | +25% | A |
| I _{OFF} | Offset Current in ISEN | I _{IN} = 0A | | 2 | | μA |
| A _{IF} | Current Monitor Gain | I _{IN} = 1A~6A | | 5 | | μA/A |
| I _{MON} | Current Monitor Accuracy | I _{IN} = 3A | | 10 | | % |
| V _{LOW} | Fault Low Voltage | I _{FLT} = 1mA | | | 0.5 | V |
| I _{LK_FLT} | Fault Leakage Current | | | | 1 | μA |
| t _{FLT} | Fault Flag Delay Time | | | | 100 | ns |
| t _{SS} | Soft-Start Time | C _{SS} = 300pF | | 100 | | μs |
| V _{EN_L} | Enable Input Low Voltage | | | | 0.8 | V |
| V _{EN_H} | Enable Input High Voltage | | 2 | | | V |
| V _{EN_HYS} | Enable Input Hysteresis | | | 100 | | mV |
| I _{EN_BIAS} | Enable Input Bias Current | | | | 1 | μA |
| Td_on | Turn-On Delay Time EN_50% to OUT_10% | R _L = 120Ω, C _L = 1μF | | 220 | | μs |
| t _{ON} | Turn-On Rise Time OUT_10% to 90% | R _L = 120Ω, C _L = 1μF | | 160 | | μs |
| T _{SD} | Thermal Shutdown Threshold | | | 130 | | °C |
| T _{SD_HYS} | Thermal Shutdown Hysteresis | | | 30 | | °C |
| T _{CL} | Current Limit Detection Delay | | | | 50 ⁽¹⁾ | ns |
| T _{FDP} | N-Channel Turn Off Delay | | | | 50 ⁽¹⁾ | ns |

Note: 1. Guaranteed by design.

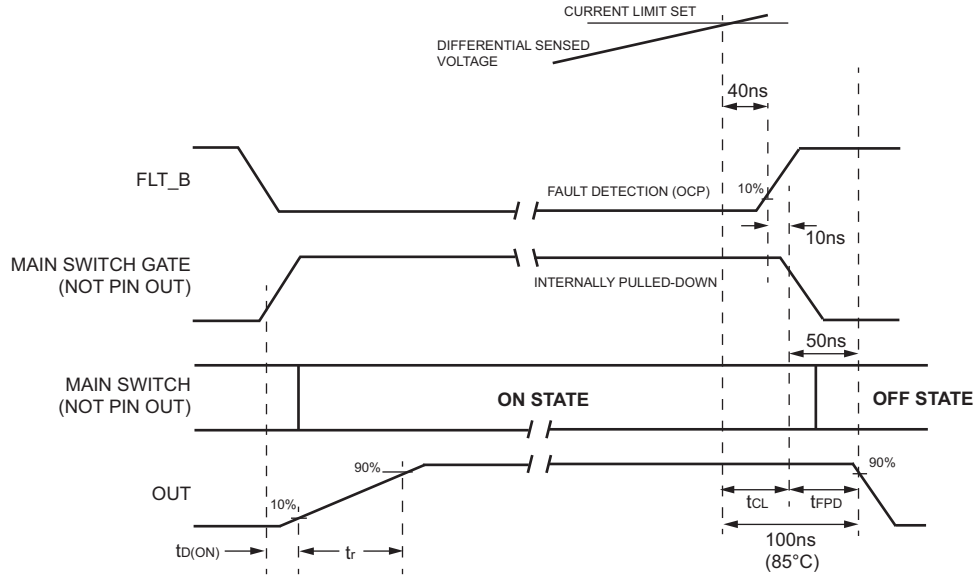


Figure 2. Over Current Limit Timing Diagram

$$V(I_{SEN}) = (A_{IF} * I_{DC} + I_{OFF}) * R_{SEN}$$

$$V(I_{SEN}) = (5\mu A/A * 6A + 2\mu A) * 100k\Omega = 3.2V$$

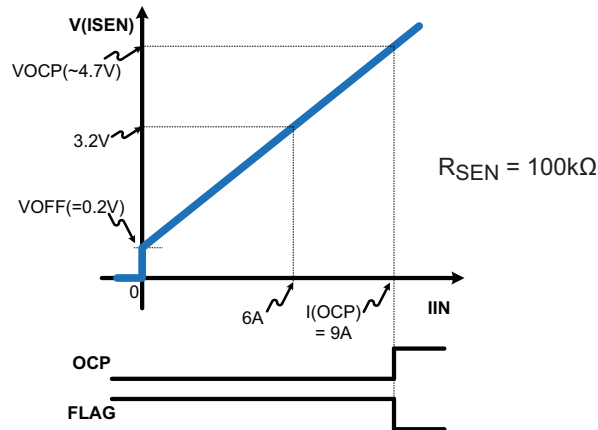
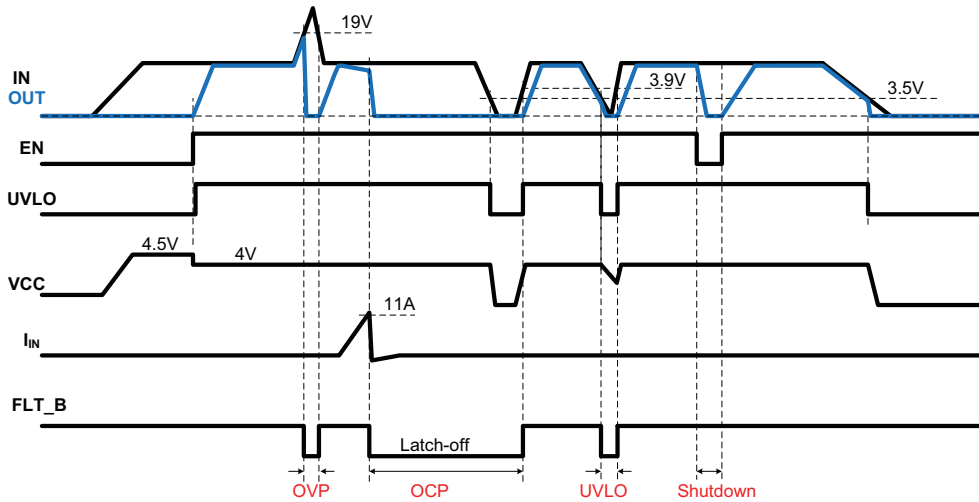


Figure 3. Current Monitoring and Reverse Current

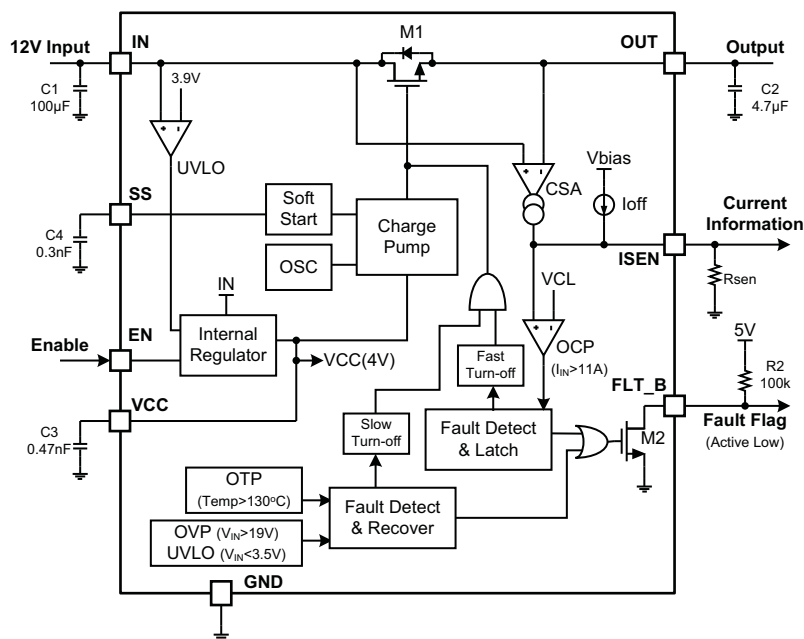
Protection Table

| Fault Condition | LSW Position | Fault Flag | System State | Comparator Add-on |
|-----------------|--------------|------------|--------------|-----------------------|
| UVLO (falling) | Open | Low | Stand-by | Hysteresis + Deglitch |
| OCP | Open | Low | Latch-off | Deglitch |
| OTP | Open | Low | Stand-by | Hysteresis |
| EN (low) | Open | H-Z | Shutdown | Deglitch |

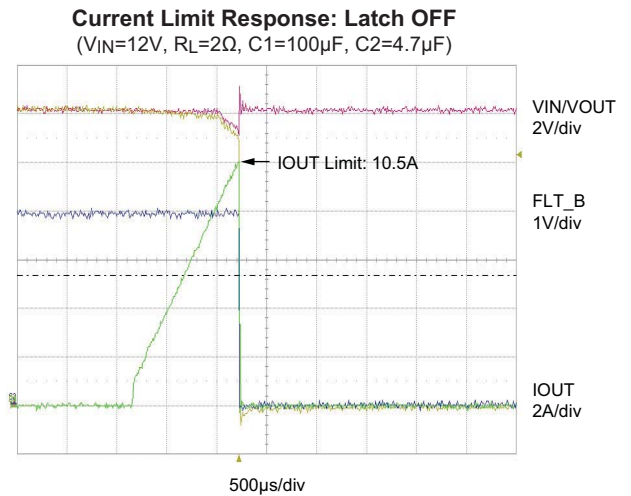
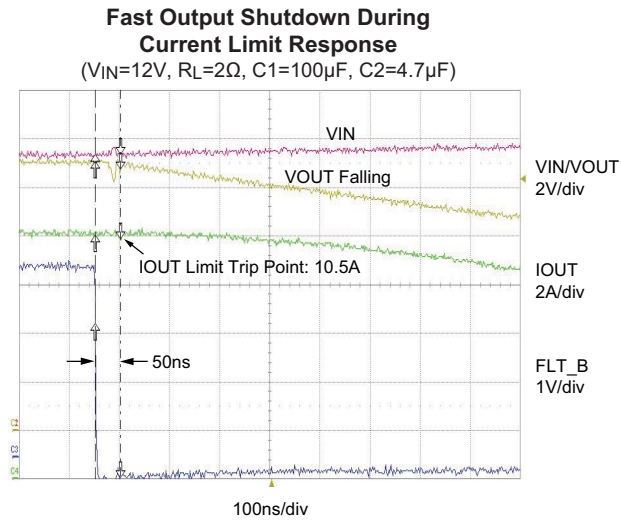
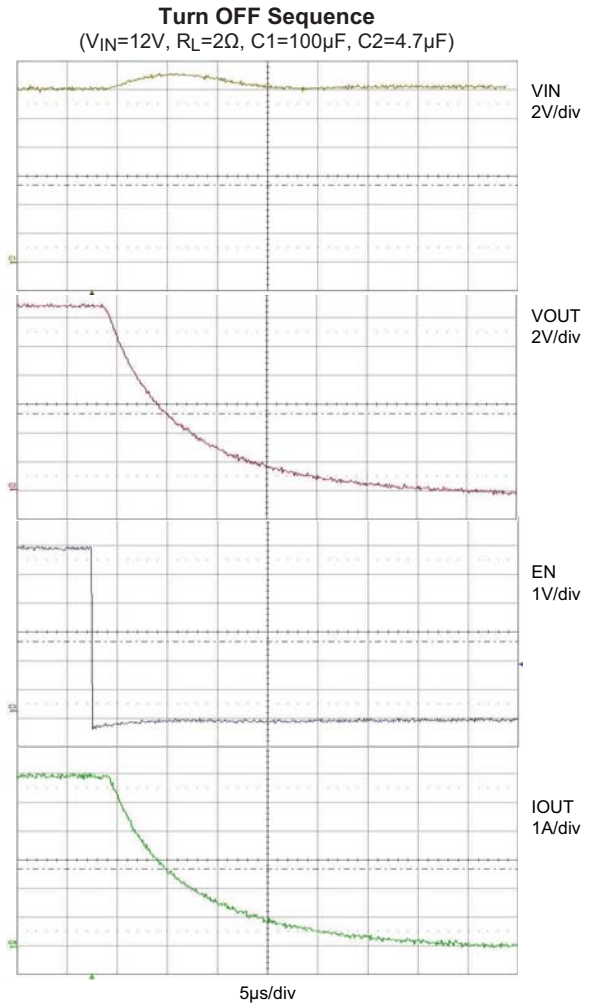
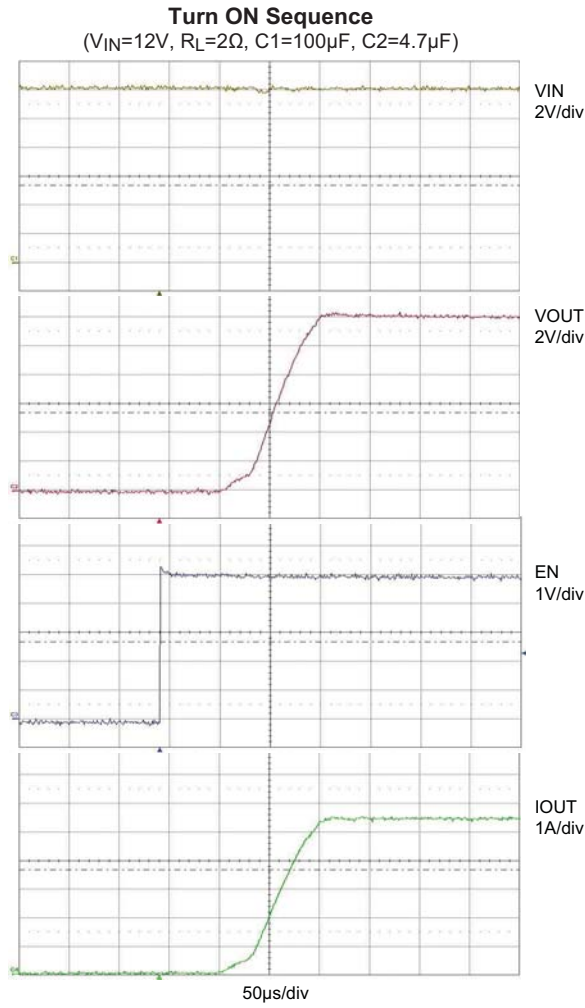
Protection Diagram



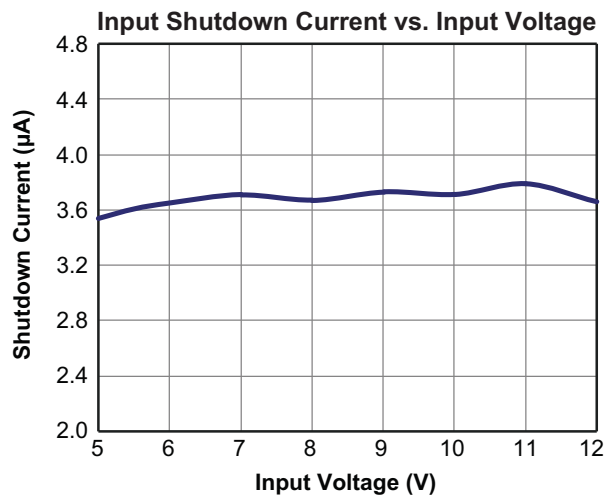
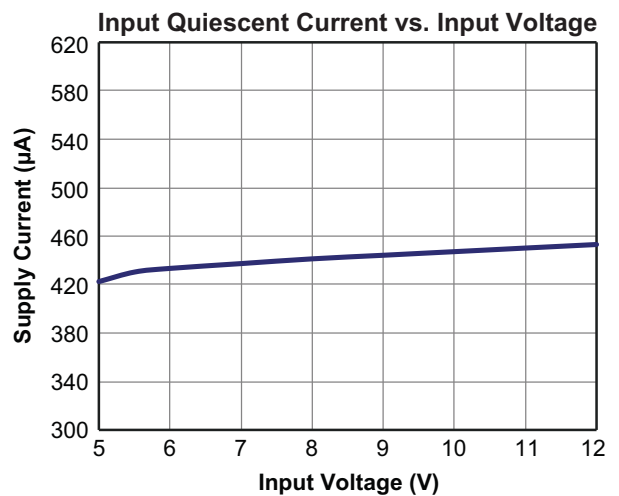
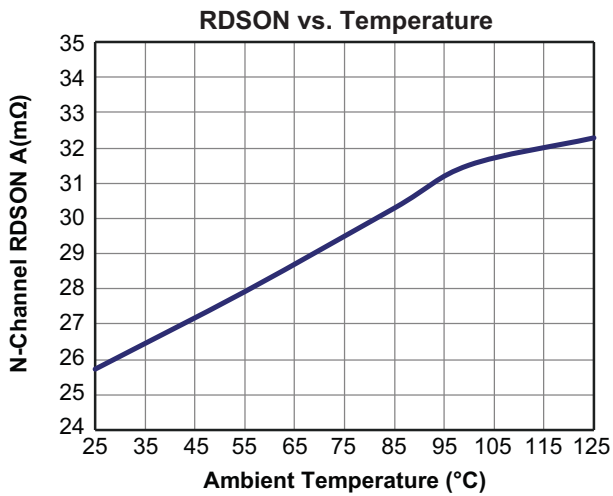
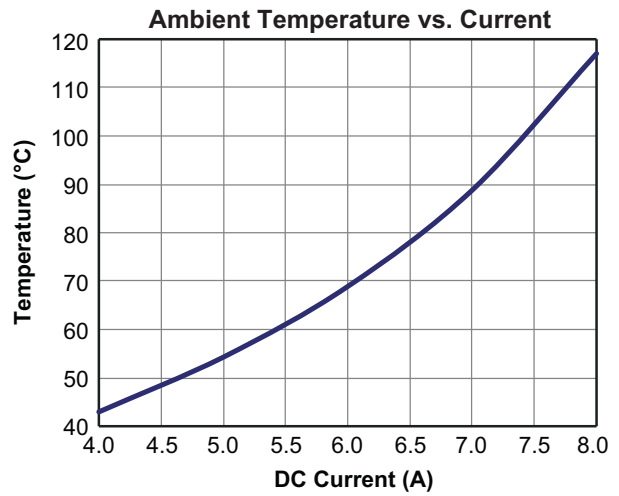
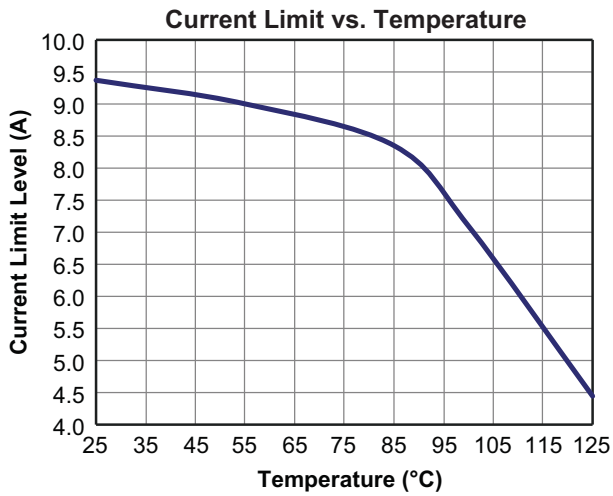
Functional Block Diagram



Functional Characteristics



Typical Characteristics



Application Information

Parallel Load Switch Configuration

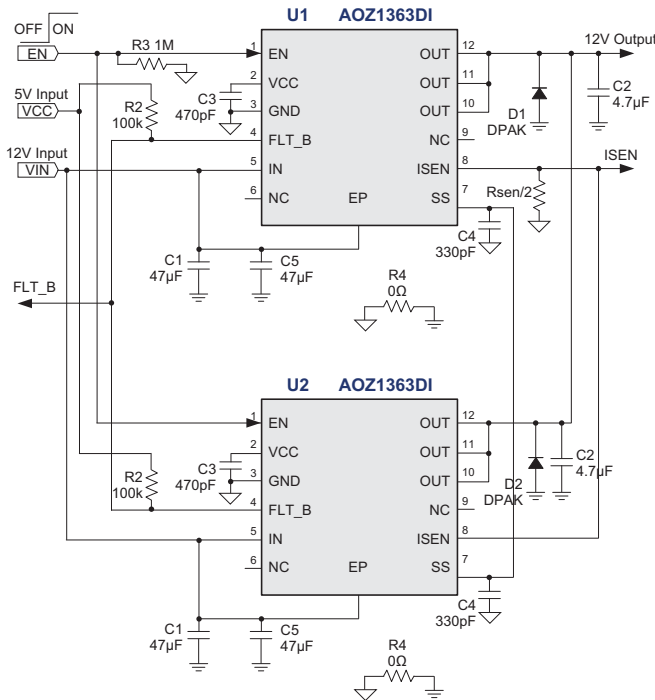


Figure 4. Parallel Configuration Application Schematic

The AOZ1363DI fast load switch can also be parallel configured in applications that require efficiency optimization. Overall conduction losses during the ON cycle can be reduced in half by mounting two load switches, as shown above. The EN pins can be tied together and a common rising edge signal enables both devices simultaneously. Each load switch device must have a 470pF surface mounted ceramic capacitor across VCC and GND (pin 2 and pin 3) – see PCB floor plan in the Layout Guidelines. The VCC pin then connected together onto a common 5V VCC rail. A 100kΩ resistor tied between each of the devices' VCC pin and FLT_B pin for user flag function. Both FLT_B pins will be tied together to a single trace for easy user access. Each device will employ its own pair of 47µF capacitor next to the IN (pin 5 and EP) and PGND. Both VIN pins will be tied together through a wide track, connecting to the 12V supply rail.

The SS cap of 330pF will be mounted next to each device's SS pin and each respective GND. Both SS pins will be tied to a common trace on the PCB. The ISEN resistor should be configured such that the typical value ISEN resistor, $R_{sen} = 100k\Omega$ will be divided by the same amount of AOZ1363DI devices used.

A 4.7µF capacitor will be mounted between the Output (pins 10,11 and 12) and EP of each AOZ1363DI load switch. All output pins of load switch devices will be tied together through a wide track on the top layer for optimize cooling. This common Output track will lead to the Load downstream.

The same techniques and methodology previously explained should be applied to any Multi-Load Switch parallel configuration. Layout techniques for multi-load switch topology should be referenced to the Recommended Layout Guidelines section.

Short Protection

AOZ1363 has the protection function against the destructive output short current thanks to the ultra fast turn-off feature as long as the short phenomenon takes place in the upper switch of the totem pole. In Figure 5A, when the short phenomenon happens in the upper MOSFET(M2) of the totem pole type load the excessive short current starts ramping up speedily but since AOZ1363 can detect it, turn off MOSFET quickly within 100ns and flag the fault signal to main controller the whole system can be protected safely.

However, in case the output is short to the GND like Figure 5B, AOZ1363 needs a diode(D1) between OUT and GND to clamp the excessive negative voltage in the output due to parasitic inductance.

The C1 and C2 capacitor should be located in nearest point to IN and OUT each other and the C2 should be lower than 4.7µF for the fast short detection.

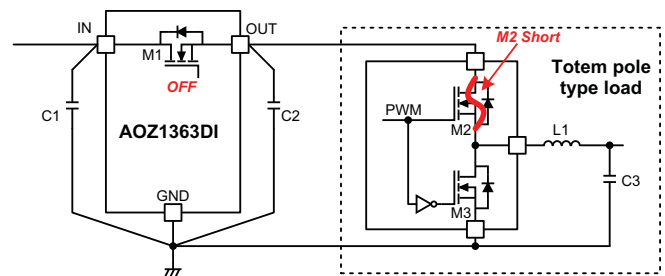


Figure 5A. Application Against Totem Pole Load Short

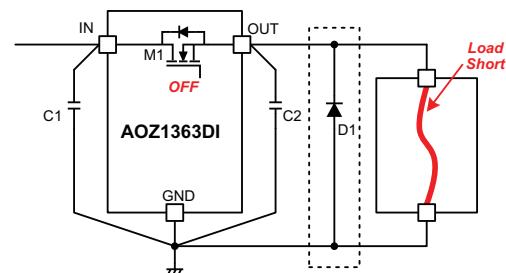
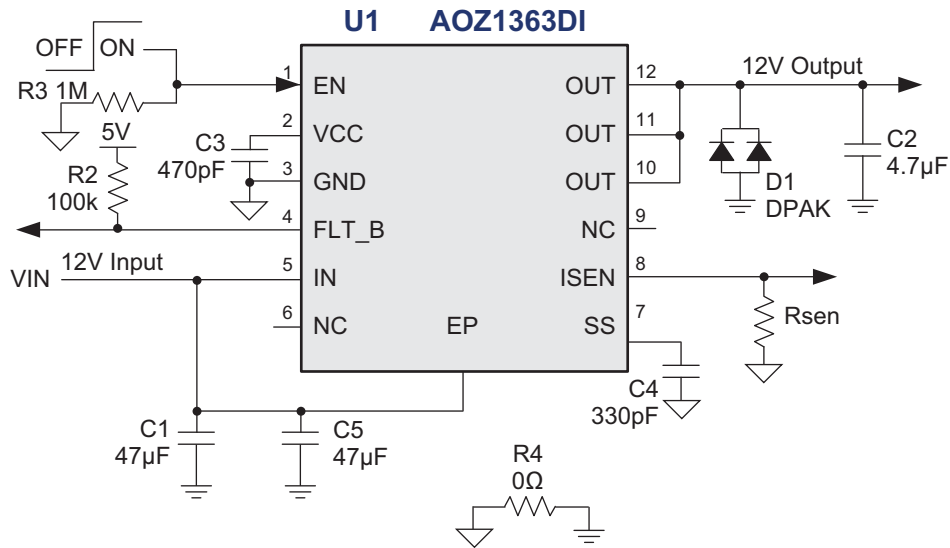


Figure 5B. Application Against Load Rail Short to Ground

Recommended Bill of Materials



| Component | Value | Description / Rating | Vendor | Part # |
|-----------|-------|--------------------------------|-----------------|--------------------|
| U1 | -- | -- | Alpha Omega | AOZ1363DI |
| C1, C5 | 4.7µF | CAP CER 47UF 16V 20% X5R 1210 | Taiyo Yuden | EMK325BJ476MM-T |
| C2 | 4.7µF | CAP CER 4.7UF 50V 10% X5R 1206 | Taiyo Yuden | UMK316BJ475KL-T |
| C3 | 470pF | CAP CER 470PF 50V 10% X7R 0603 | Murata Elec. | GRM188R71H471KA01J |
| C4 | 330pF | CAP CER 330PF 50V 10% X7R 0603 | Murata Elec. | GRM188R71H331KA0ID |
| RSEN | 100kΩ | 1/10W 1% JUMP 0603 SMD | Panasonic (ECG) | ERJ-3GEYJ104V |
| R2 | 100kΩ | 1/10W 1% JUMP 0603 SMD | Panasonic (ECG) | ERJ-3GEYJ104V |
| R3 | 1MΩ | 1/10W 1% JUMP 0603 SMD | Yaged | RC0603FR-071ML |
| R4 | 0Ω | 1/10W 1% JUMP 0603 SMD | Yaged | RC0603JR-070RL |
| D1 | CQ714 | CQ 5D CQ714 B2535G | AKA | CQ714B2535G |

Recommended Layout Guidelines

The AOZ1363DI load switch is a device that is capable of delivering a steady flow of DC current. It provides up to 6A of continuous current into two DrMos modules for step-down conversion in continuous conduction mode. The floor plan in Figure 6 is focused on providing the IN (pin 5 and exposed pad) and the OUT (pins 10,11 and 12) with plenty of top layer exposed copper for thermal relief, thus, transferring most of the power dissipated as heat down to the PCB. The top layer layout diagram in Figure 6 shows an optimal method for cooling.

Furthermore, the input bypass capacitors CIN1 and CIN2 are surface mounted ceramic capacitors mounted directly to the exposed VIN paddle. The 4.7µF MLCC should be located as close as physically possible to the output pins 10-12 with return path star power grounded with the input capacitors. The AOZ1363DI employs an extremely fast 100ns turn off mechanism during an over-current event. When the DC current through the large internal NMOS switch exceeds its maximum threshold of 11.2A at 25°C, a fast gate discharging circuit is deployed causing the output to decay to zero. The layout configuration of Figure 6 enables the fast discharging of the 4.7µF output capacitor very effectively through the load downstream.

Please note the GND (upside down triangle) and PGND (earth ground) symbols in Figure 7. The PGND symbols should only be connected to the Input and Output capacitors and nowhere else. All GND symbols should be used for the rest of the external components including the IC's pin 3. All GND connections should be star grounded together separate from the PGND connections. Bottom layer has been allocated for PGND use only so the Input and the Output capacitors are directly tied to the bottom layer through via connectors. Only a single point will be used to connect both AGND and PGND for optimal noise isolation. Please refer to Figure 6 for R4 valued at 0Ω.

All Input (pin 5 and Exposed Pad) and Output (pins 10, 11 and 12) traces should be at top layer for optimal trace resistances. Current going through vias is not acceptable. Traces on top layer may be duplicated to the second layer (bottom layer) and via connecting both the top and bottom traces as near as possible to the IC region is advisable to provide thermal relief.

All of the above details must be applied when considering to implement a multi-device parallel configuration (2 or 3 devices).

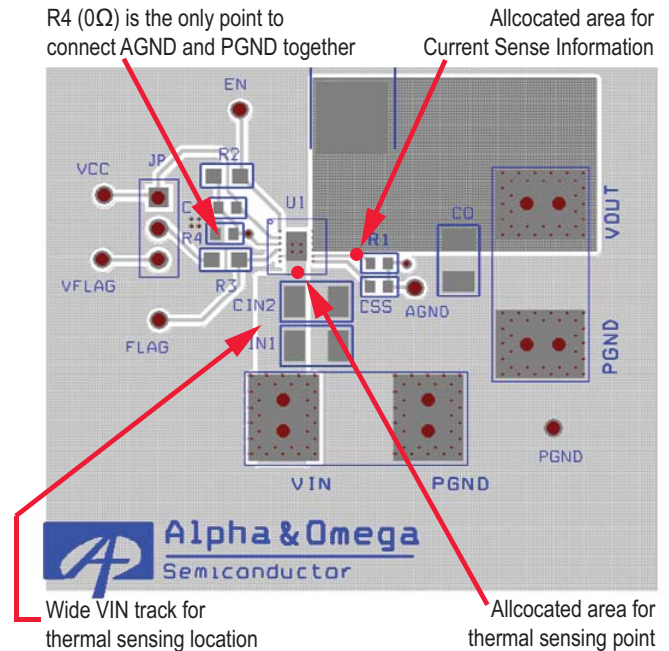


Figure 7. Top Layer Floor Plan

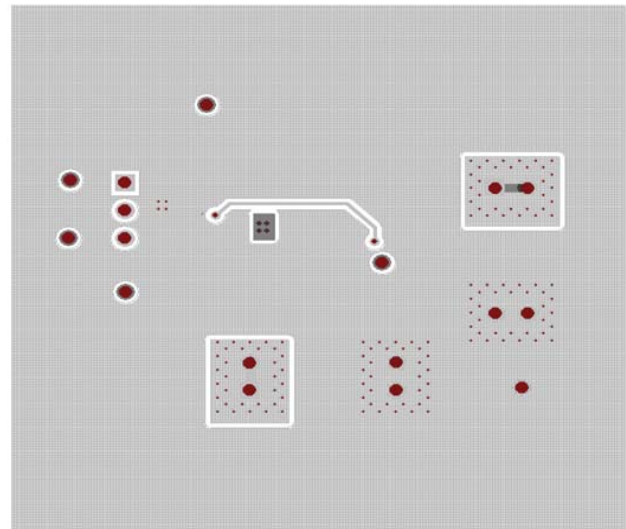
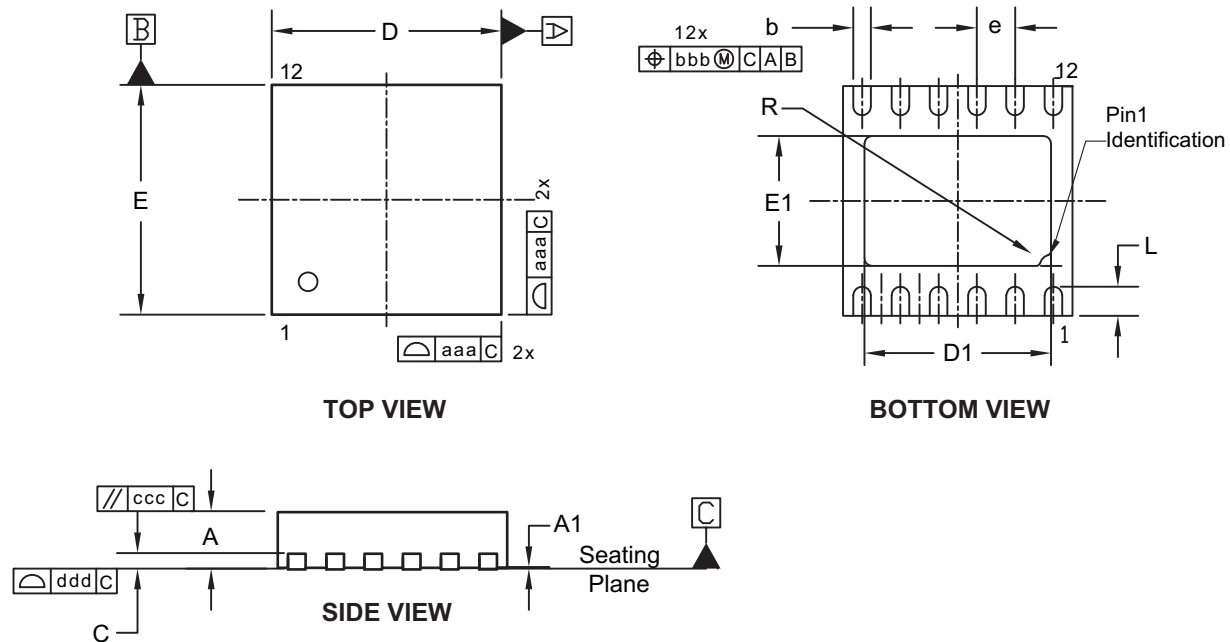
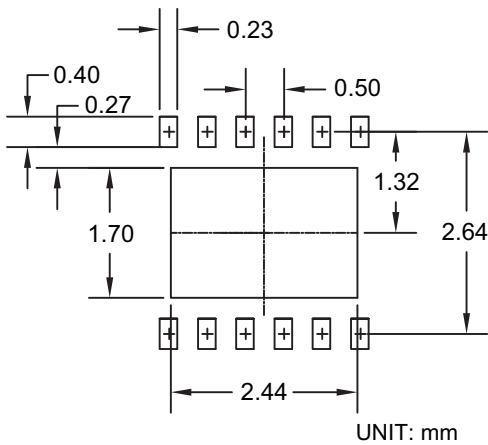


Figure 8. Bottom Layer Floor Plan

Package Dimensions, DFN 3x3, 12L



RECOMMENDED LAND PATTERN



Dimensions in millimeters

| Symbols | Min. | Nom. | Max. |
|---------|----------|-------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.23 | 0.28 |
| c | --- | 0.203 | --- |
| D | 3.00 BSC | | |
| D1 | 2.39 | 2.44 | 2.54 |
| E | 3.00 BSC | | |
| E1 | 1.55 | 1.70 | 1.80 |
| e | 0.50 BSC | | |
| L | 0.28 | 0.38 | 0.48 |
| R | 0.20 | | |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.08 | | |

Dimensions in inches

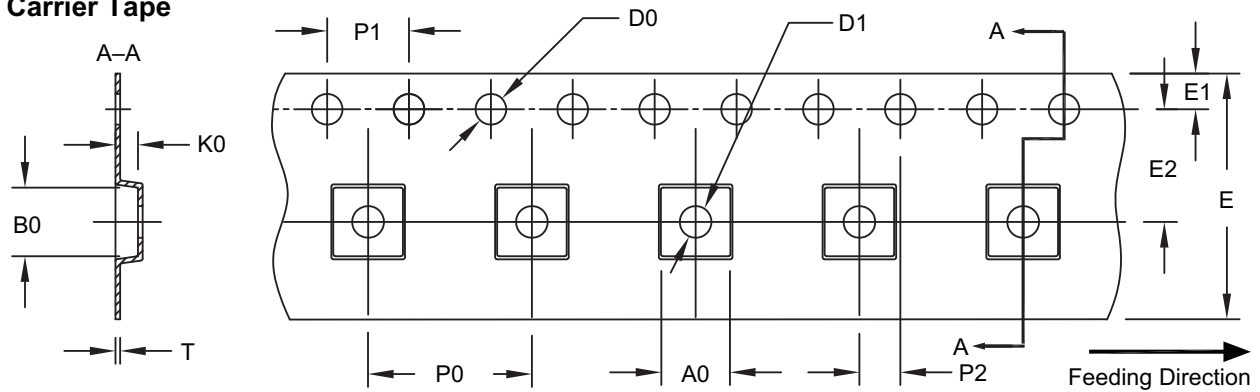
| Symbols | Min. | Nom. | Max. |
|---------|-----------|-------|-------|
| A | 0.028 | 0.030 | 0.031 |
| A1 | 0.000 | 0.001 | 0.002 |
| b | 0.007 | 0.009 | 0.011 |
| c | --- | 0.008 | --- |
| D | 0.118 BSC | | |
| D1 | 0.094 | 0.096 | 0.010 |
| E | 0.118 BSC | | |
| E1 | 0.061 | 0.067 | 0.071 |
| e | 0.020 BSC | | |
| L | 0.011 | 0.015 | 0.019 |
| R | 0.008 | | |
| aaa | 0.006 | | |
| bbb | 0.004 | | |
| ccc | 0.004 | | |
| ddd | 0.003 | | |

Notes:

1. Dimensions and tolerances conform to ASME Y14.5M-1994.
2. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
3. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, dimension b should not be measured in that radius area.
4. Coplanarity ddd applies to the terminals and all other bottom surface metallization.

Tape and Reel Dimensions, DFN 3x3, 12L

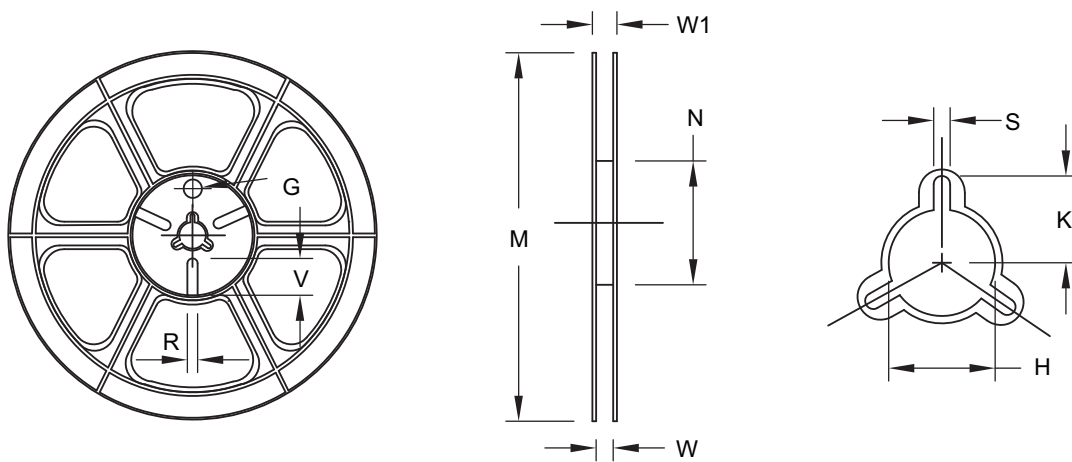
Carrier Tape



UNIT: mm

| Package | A0 | B0 | K0 | D0 | D1 | E | E1 | E2 | P0 | P1 | P2 | T |
|------------|---------------|---------------|---------------|--------------------|--------------------|----------------|---------------|---------------|---------------|---------------|---------------|---------------|
| DFN 3x3_EP | 3.40 ±0.10 | 3.35 ±0.10 | 1.10 ±0.10 | 1.50 +0.10/-0.0 | 1.50 +0.10/-0.0 | 12.00 ±0.30 | 1.75 ±0.10 | 5.50 ±0.05 | 8.00 ±0.10 | 4.00 ±0.10 | 2.00 ±0.05 | 0.30 ±0.05 |

Reel

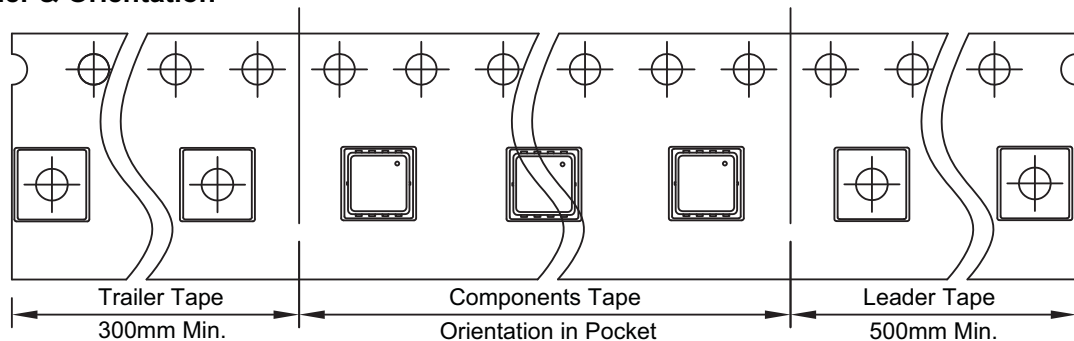


UNIT: mm

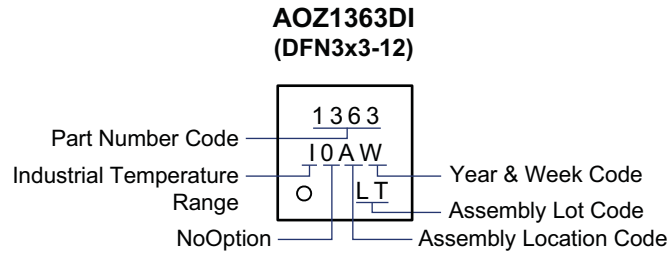
| Tape Size | Reel Size | M | N | W | W1 | H | K | S | G | R | V |
|-----------|-----------|------------------|-----------------|----------------|----------------|---------------------|-------|---------------|-----|-----|-----|
| 12mm | ø330 | ø330.00 ±0.50 | ø97.00 ±0.10 | 13.00 ±0.30 | 17.40 ±1.00 | ø13.00 +0.5/-0.2 | 10.60 | 2.00 ±0.50 | N/A | N/A | N/A |

Leader / Trailer & Orientation

Unit Per Reel:
5000pcs



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.