

Double channel high-side driver with analog current sense

Datasheet – production data



Features

Max transient supply voltage	V_{CC}	58 V
Operating voltage range	V_{CC}	8 to 36 V
Typ on-state resistance (per ch.)	R_{ON}	35 m Ω
Current limitation (typ)	I_{LIM}	42 A
Off-state supply current	I_S	2 μ A

- General
 - Very low standby current
 - 3.0 V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - Fault reset standby pin (FR_Stby)
- Diagnostic functions
 - Proportional load current sense
 - High current sense precision for wide range currents
 - Off-state open load detection
 - Output short to V_{CC} detection
 - Overload and short to ground latch off
 - Thermal shutdown latch-off
 - Very low current sense leakage
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients

- Protection against loss of ground and loss of V_{CC}
- Thermal shutdown
- Electrostatic discharge protection

Application

All types of resistive, inductive and capacitive loads

Description

The VPS2535H is a monolithic device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

The device integrates an analog current sense which delivers a current proportional to the load current.

Fault conditions such as overload, overtemperature or short to V_{CC} are reported via the current sense pin.

Output current limitation protects the device in overload conditions. The device latches off in case of overload or thermal shutdown.

The device is reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and on the fault reset standby pins disables all outputs and sets the device in standby mode.

Contents

- 1 Block diagram and pin description 5**
- 2 Electrical specifications 7**
 - 2.1 Absolute maximum ratings 7
 - 2.2 Thermal data 8
 - 2.3 Electrical characteristics 9
 - 2.4 Electrical characteristics curves 17
- 3 Application information 19**
 - 3.1 Maximum demagnetization energy ($V_{CC} = 24\text{ V}$) 20
- 4 Package and PCB thermal data 21**
 - 4.1 PowerSSO-24 thermal data 21
- 5 Package and packing information 24**
 - 5.1 PowerSSO-24 package information 24
 - 5.2 PowerSSO-24 packing information 27
- 6 Order codes 28**
- 7 Revision history 29**

List of tables

Table 1.	Pin function	5
Table 2.	Suggested connections for unused and not connected pins	6
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data	8
Table 5.	Power section	9
Table 6.	Switching ($V_{CC} = 24\text{ V}$; $T_j = 25\text{ °C}$)	9
Table 7.	Logic inputs	10
Table 8.	Protections and diagnostics	11
Table 9.	Current sense ($8\text{ V} < V_{CC} < 36\text{ V}$)	12
Table 10.	Open-load detection ($V_{FR_Stby} = 5\text{ V}$)	13
Table 11.	Truth table	16
Table 12.	Thermal parameters	23
Table 13.	PowerSSO-24 mechanical data	25
Table 14.	Device summary	28
Table 15.	Document revision history	29

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram PowerSSO-24 (top view)	6
Figure 3.	Current and voltage conventions	7
Figure 4.	Treset definition	10
Figure 5.	T_{STBY} definition	11
Figure 6.	Current sense delay characteristics	13
Figure 7.	Open-load off-state delay timing	13
Figure 8.	Switching characteristics	14
Figure 9.	Output stuck to V_{CC} detection delay time at FR_{STBY} activation	14
Figure 10.	Delay response time between rising edge of output current and rising edge of current sense	15
Figure 11.	Output voltage drop limitation	15
Figure 12.	Device behavior in overload condition	16
Figure 13.	Off-state output current	17
Figure 14.	High-level input current	17
Figure 15.	Input clamp voltage	17
Figure 16.	High-level input voltage	17
Figure 17.	Low-level input voltage	17
Figure 18.	Input hysteresis voltage	17
Figure 19.	On-state resistance vs T_{case}	18
Figure 20.	On-state resistance vs V_{CC}	18
Figure 21.	I_{LIMH} vs T_{case}	18
Figure 22.	Turn-on voltage slope	18
Figure 23.	Turn-off voltage slope	18
Figure 24.	Application schematic	19
Figure 25.	Maximum turn-off current versus inductance (with no diodes connected in anti-parallel to inductive load)	20
Figure 26.	PowerSSO-24 PC board	21
Figure 27.	$R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)	21
Figure 28.	PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)	22
Figure 29.	Thermal fitting model of a double channel HSD in PowerSSO-24	22
Figure 30.	PowerSSO-24 package dimensions	24
Figure 31.	PowerSSO-24 tube shipment (no suffix)	27
Figure 32.	PowerSSO-24 tape and reel shipment (suffix "TR")	27

1 Block diagram and pin description

Figure 1. Block diagram

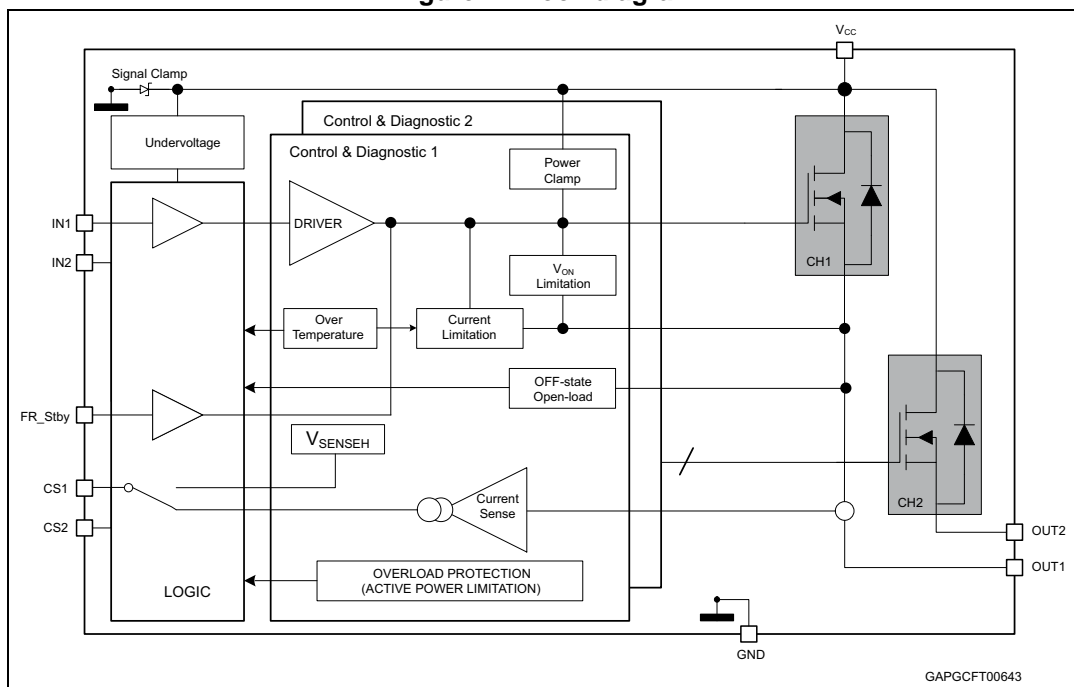


Table 1. Pin function

Name	Function
V _{CC}	Bus voltage connection
OUT _{1,2}	Power outputs
GND	Ground connection
IN _{1,2}	Voltage controlled input pins with hysteresis, CMOS compatible. They Control output switch state
CS _{1,2}	Analog current sense pins, they deliver a current proportional to the load current
FR_Stby	In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low.

Figure 2. Configuration diagram PowerSSO-24 (top view)

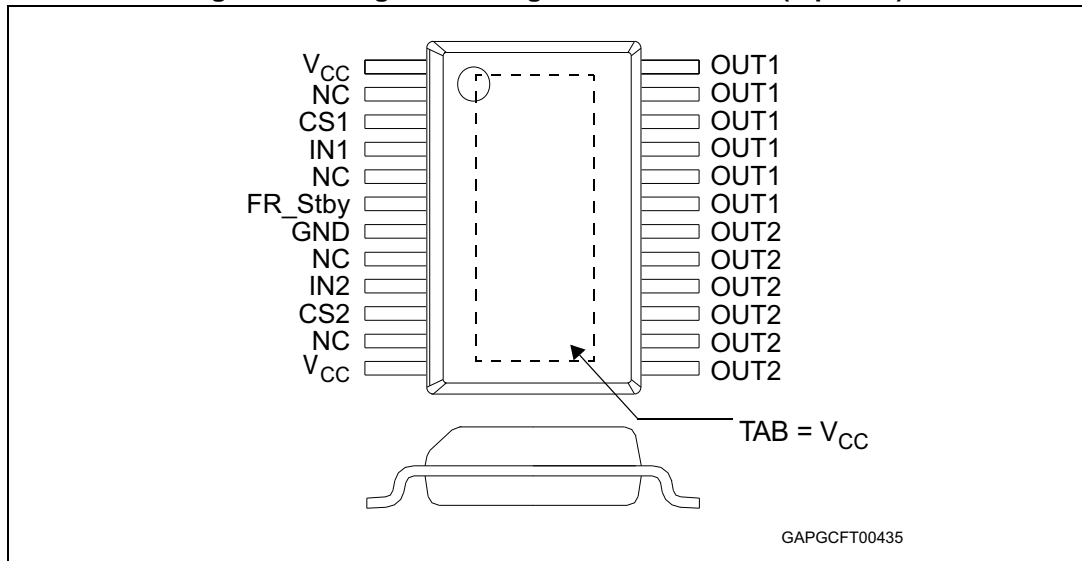


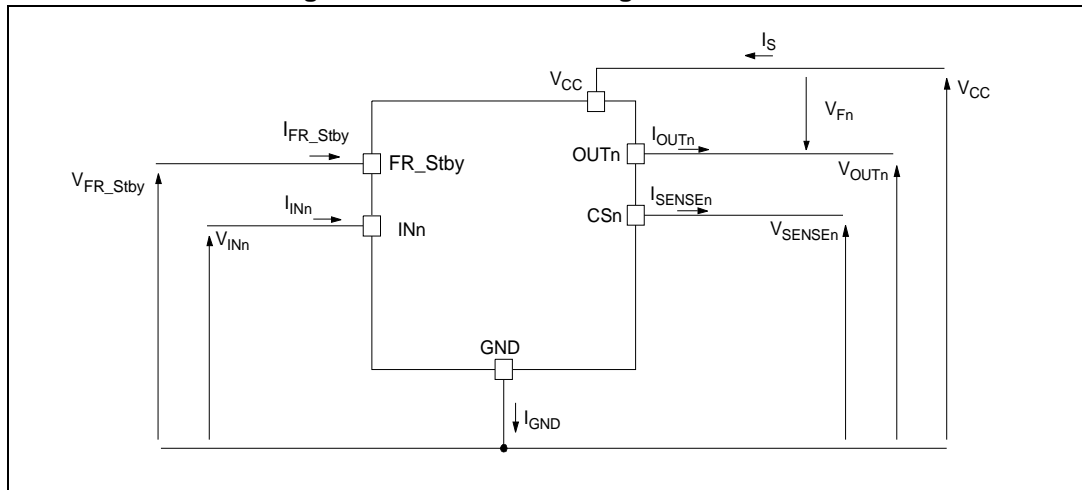
Table 2. Suggested connections for unused and not connected pins

Connection / pin	CurrentSense	N.C.	Output	Input	FR_Stby
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 10 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ

1. X: do not care.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	58	V
I_{OUT}	DC output current	Internally limited	A
I_{IN}	DC input current	-1 to 10	mA
I_{FR_Stby}	Fault reset standby DC input current	-1 to 1.5	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC} - 58$ to $+V_{CC}$	V
E_{MAX}	Maximum switching energy ⁽¹⁾ ($L = 10$ mH; $V_{BAT} = 32$ V; $T_{jstart} = 25$ °C; $I_{OUT} = I_{limL}$ (typ))	1000	mJ
L_{smax}	Maximum strain inductance in short circuit condition ⁽¹⁾ $R_L = 300$ mΩ; $V_{CC} = 32$ V; $T_{jstart} = 25$ °C; $I_{OUT} = I_{LMHmax}$	40	μH

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V _{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 kΩ; C = 100 pF)		
	– IN _{1,2}	4000	V
	– CS _{1,2}	2000	V
	– FR_Stby	4000	V
	– OUT _{1,2}	5000	V
	– V _{CC}	5000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

1. In case no diode are connected in anti-paralled to load.

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case (max) (with one channel ON)	2	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (max)	See Figure 27	°C/W

2.3 Electrical characteristics

$8\text{ V} < V_{CC} < 36\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		8	24	36	V
V_{USD}	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance ⁽¹⁾	$I_{OUT} = 3\text{ A}$; $T_j = 25\text{ °C}$		35		mΩ
		$I_{OUT} = 3\text{ A}$; $T_j = 150\text{ °C}$			70	
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$	58	64	70	V
I_S	Supply current	Off-state; $V_{CC} = 24\text{ V}$; $T_j = 25\text{ °C}$; $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		2 ⁽²⁾	5 ⁽²⁾	μA
		On-state; $V_{CC} = 24\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		4.2	6	mA
$I_{L(off)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $T_j = 125\text{ °C}$	0		5	
V_F	Output - V_{CC} diode voltage	$-I_{OUT} = 3\text{ A}$; $T_j = 150\text{ °C}$			0.7	V

1. For each channel
2. PowerMOS leakage included

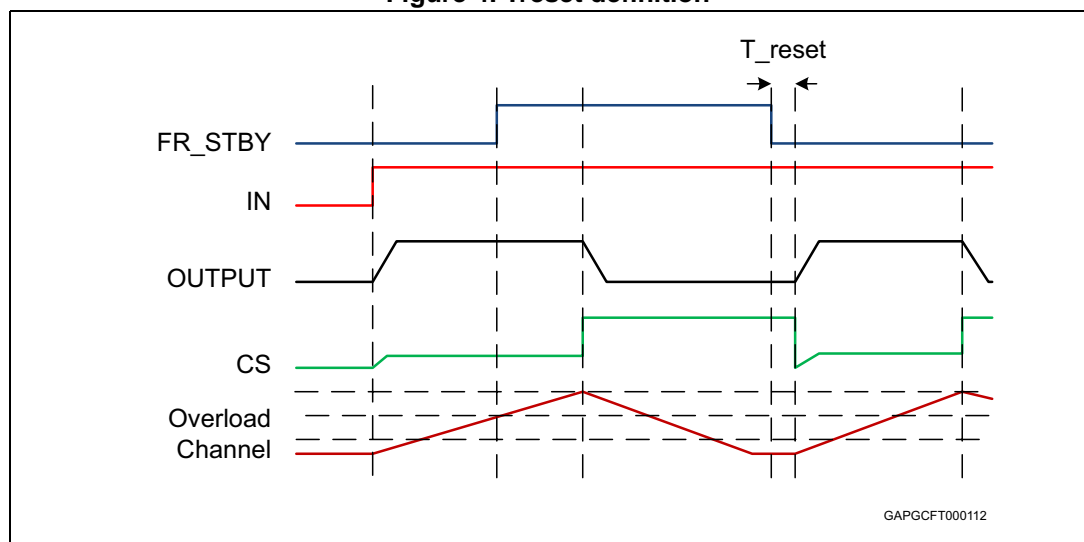
Table 6. Switching ($V_{CC} = 24\text{ V}$; $T_j = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 8\text{ Ω}$		46		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 8\text{ Ω}$		54		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 8\text{ Ω}$		0.55		V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 8\text{ Ω}$		0.46		V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 8\text{ Ω}$		1		mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 8\text{ Ω}$		0.65		mJ
dV_{OUTOFF}/dt	Max negative dV/dt on the output to prevent device from spuriously turning-on	$V_{CC} = 28\text{ V}$		0.3		V/μs

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
$V_{FR_Stby_L}$	Fault_reset_standby low level voltage				0.9	V
$I_{FR_Stby_L}$	Low level fault_reset_standby current	$V_{FR_Stby} = 0.9\text{ V}$	1			μA
$V_{FR_Stby_H}$	Fault_reset_standby high level voltage		2.1			V
$I_{FR_Stby_H}$	High level fault_reset_standby current	$V_{FR_Stby} = 2.1\text{ V}$			10	μA
$V_{FR_Stby(hyst)}$	Fault_reset_standby hysteresis voltage		0.25			V
$V_{FR_Stby_CL}$	Fault_reset_standby clamp voltage	$I_{FR_Stby} = 15\text{ mA (10 ms)}$	11		15	V
		$I_{FR_Stby} = -1\text{ mA}$		-0.7		V
t_{reset}	Overload latch-off reset time	See Figure 4	2		24	μs
t_{stby}	Standby delay	See Figure 5	120		1200	μs

Figure 4. Treset definition



GAPGCF000112

Figure 5. T_{STBY} definition

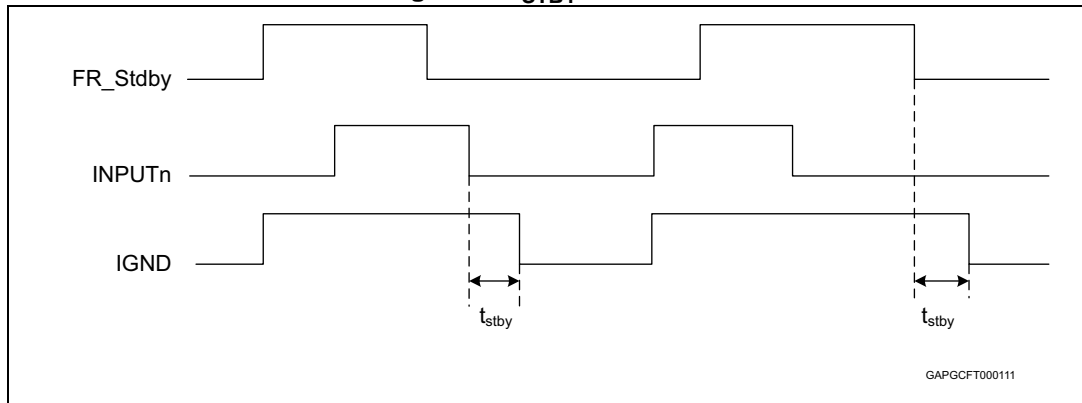


Table 8. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{limH}	DC short circuit current	V _{CC} = 24 V	30	42	55	A
		5 V < V _{CC} < 36 V			55	A
I _{limL}	Short circuit current during thermal cycling	V _{CC} = 24 V; T _R < T _j < T _{TSD}		10.5		A
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature		T _{RS} + 1	T _{RS} + 5		°C
T _{RS}	Thermal reset of status		135			°C
T _{HYST}	Thermal hysteresis (T _{TSD} -T _R)			7		°C
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 3 A; V _{IN} = 0; L = 6 mH	V _{CC} - 58	V _{CC} - 64	V _{CC} - 70	V
V _{ON}	Output voltage drop limitation	I _{OUT} = 150 mA; T _j = -40 °C to 150 °C		25		mV

Table 9. Current sense (8 V < V_{CC} < 36 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 1 A; V _{SENSE} = 2 V; T _J = -40 °C to 150 °C T _J = 25 °C to 150 °C	1952 2080	2960	4150 3840	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 1 A; V _{SENSE} = 2 V; T _J = -40 °C to 150 °C	-15		15	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 3 A; V _{SENSE} = 4 V; T _J = -40 °C to 150 °C T _J = 25 °C to 150 °C	2490 2585	2930	3440 3265	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 3 A; V _{SENSE} = 4 V; T _J = -40 °C to 150 °C	-10		+10	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 12 A; V _{SENSE} = 4 V; T _J = -40 °C to 150 °C T _J = 25 °C to 150 °C	2770 2755	2900	3125 3045	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 12 A; V _{SENSE} = 4 V; T _J = -40 °C to 150 °C	-5		5	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{IN} = 0 V; T _J = -40 °C to 150 °C	0		1	μA
		I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{IN} = 5 V; T _J = -40 °C to 150 °C	0		2	μA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 12 A; R _{SENSE} = 3.9 kΩ	5			V
V _{SENSEH}	Analog sense output voltage in fault condition ⁽²⁾	V _{CC} = 24 V; R _{SENSE} = 3.9 kΩ	7.5	8.5	9.5	V
I _{SENSEH}	Analog sense output current in fault condition ⁽²⁾	V _{CC} = 24 V; V _{SENSE} = 5 V	4.9	9	12	mA
t _{DSENSE2H}	Delay response time from rising edge of INPUT pins	V _{SENSE} < 4 V; 0.2 A < I _{OUT} < 12 A; I _{SENSE} = 90 % of I _{SENSE max} ; (see Figure 6)		200	400	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4 V; I _{SENSE} = 90 % of I _{SENSEMAX} ; I _{OUT} = 90 % of I _{OUTMAX} ; I _{OUTMAX} = 3 A (see Figure 10)			250	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pins	V _{SENSE} < 4 V; 0.2 A < I _{OUT} < 12 A; I _{SENSE} = 10 % of I _{SENSE max} ; (see Figure 6)		5	20	μs

1. Parameter guaranteed by design; it is not tested.

2. Fault condition includes: power limitation, overtemperature and open load in off-state condition.

Table 10. Open-load detection ($V_{FR_Stby} = 5\text{ V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}; 8\text{ V} < V_{CC} < 36\text{ V}$	2		4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	See Figure 7	180		1800	μs
$I_{L(off2)}$	Off-state output current at $V_{OUT} = 4\text{ V}$	$V_{IN} = 0\text{ V}; V_{SENSE} = 0\text{ V}; V_{OUT}$ rising from 0 V to 4 V	-120		0	μA
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in openload	$V_{OUT} = 4\text{ V}; V_{IN} = 0\text{ V}; V_{SENSE} = 90\% \text{ of } V_{SENSEH}; R_{SENSE} = 3.9\text{ K}$			20	μs
t_{DFRSTK_ON}	Output short circuit to V_{CC} detection delay at FRSTBY activation	See Figure 9 ; Input _{1,2} = low			50	μs

Figure 6. Current sense delay characteristics

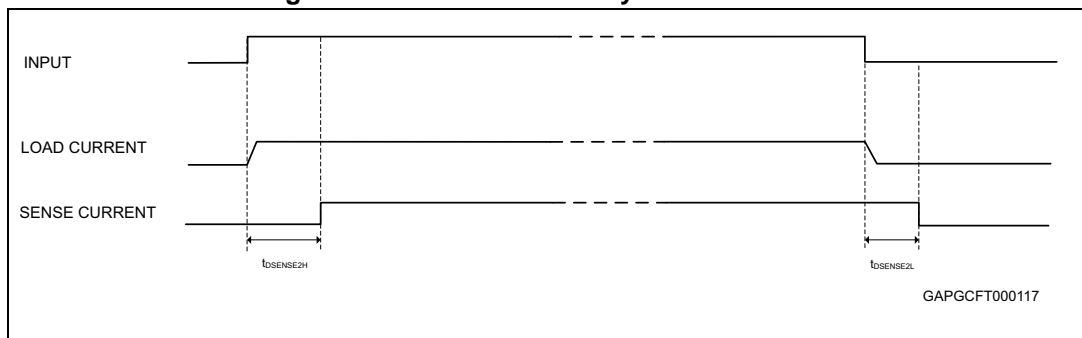
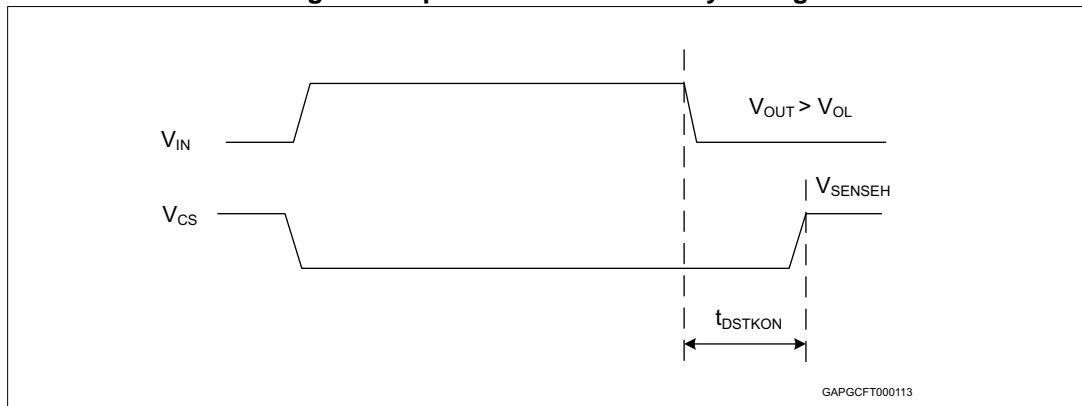


Figure 7. Open-load off-state delay timing



Note: $V_{fr_stby} = \text{high}$

Figure 8. Switching characteristics

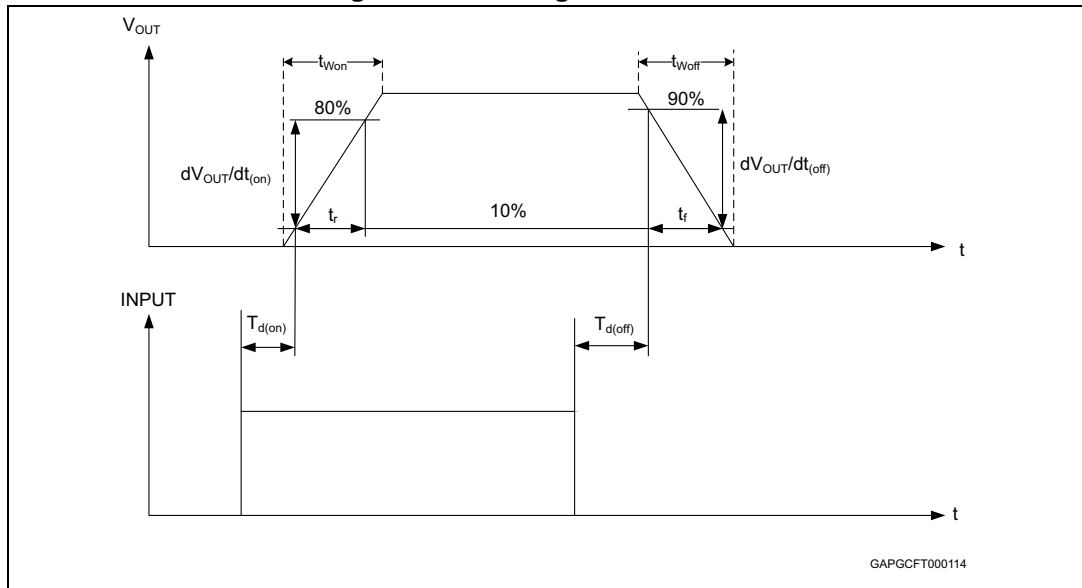


Figure 9. Output stuck to V_{CC} detection delay time at FR_{STBY} activation

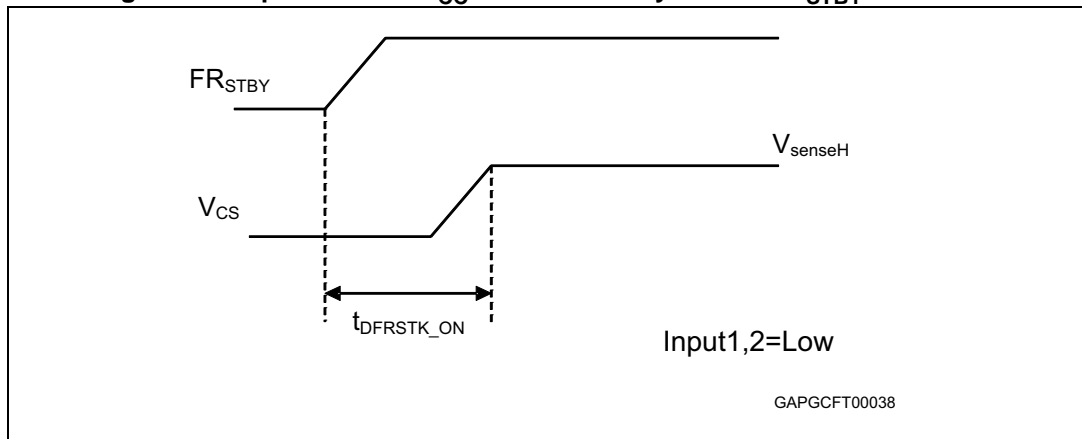


Figure 10. Delay response time between rising edge of output current and rising edge of current sense

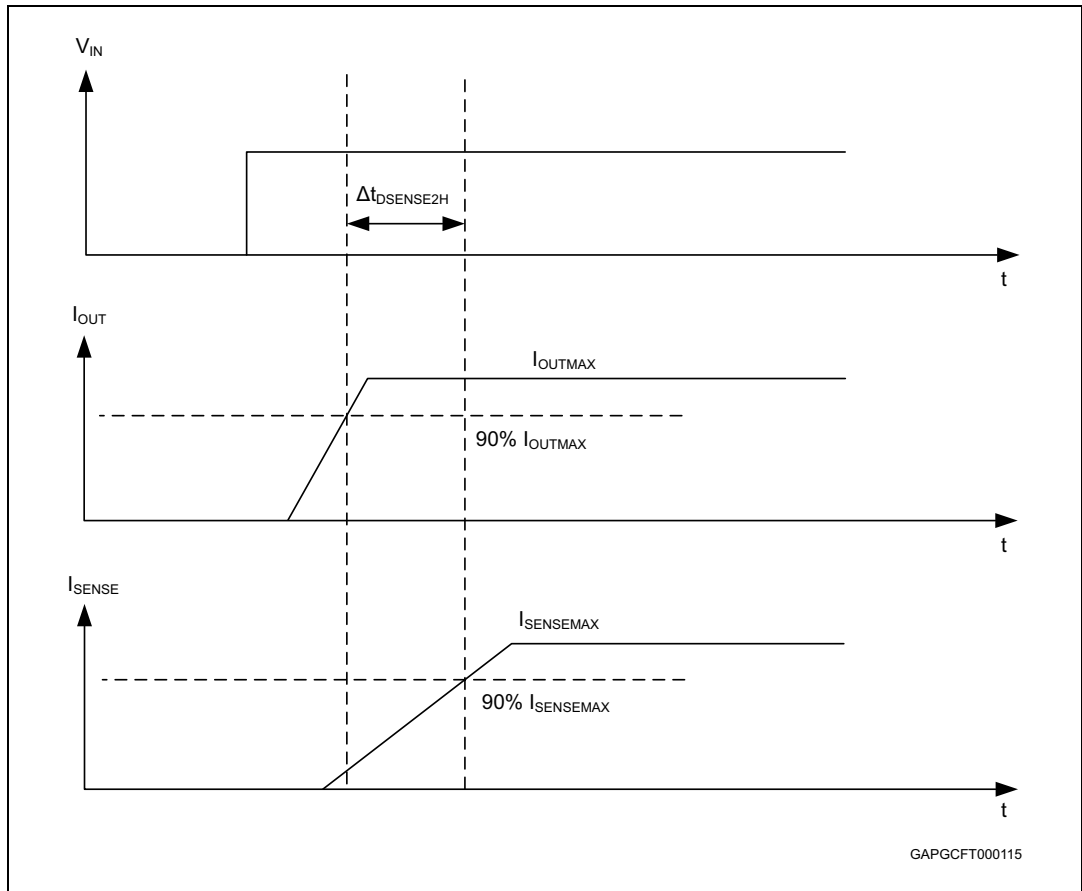


Figure 11. Output voltage drop limitation

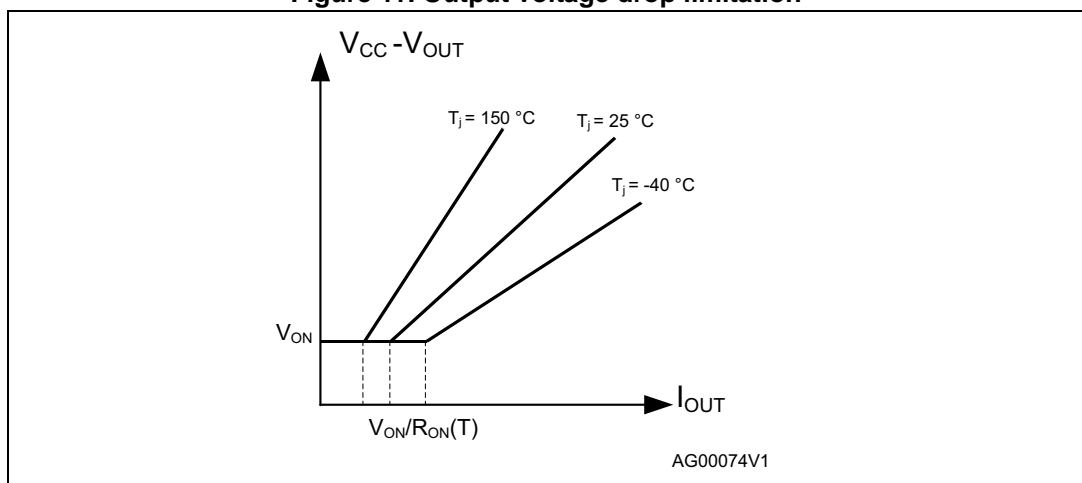


Figure 12. Device behavior in overload condition

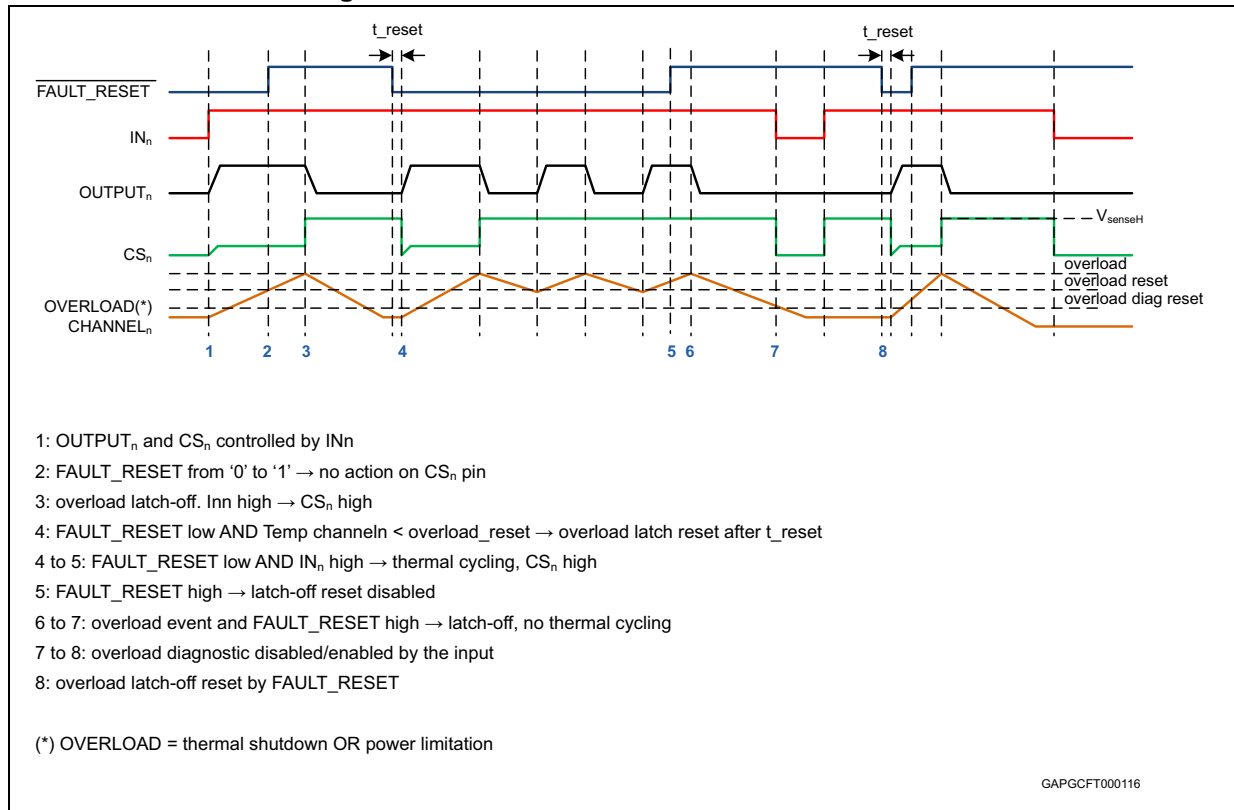


Table 11. Truth table

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	L	0
Normal operation	X	L	L	0
	X	H	H	Nominal
Overload	X	L	L	0
	X	H	H	> Nominal
Overtemperature / short to ground	X	L	L	0
	L	H	Cycling	V _{SENSEH}
	H	H	Latched	V _{SENSEH}
Undervoltage	X	X	L	0
Short to V _{CC}	L	L	H	0
	H X	L H	H H	V _{SENSEH} < Nominal
Open load off-state (with pull-up)	L	L	H	0
	H X	L H	H H	V _{SENSEH} 0
Negative output voltage clamp	X	L	Negative	0

2.4 Electrical characteristics curves

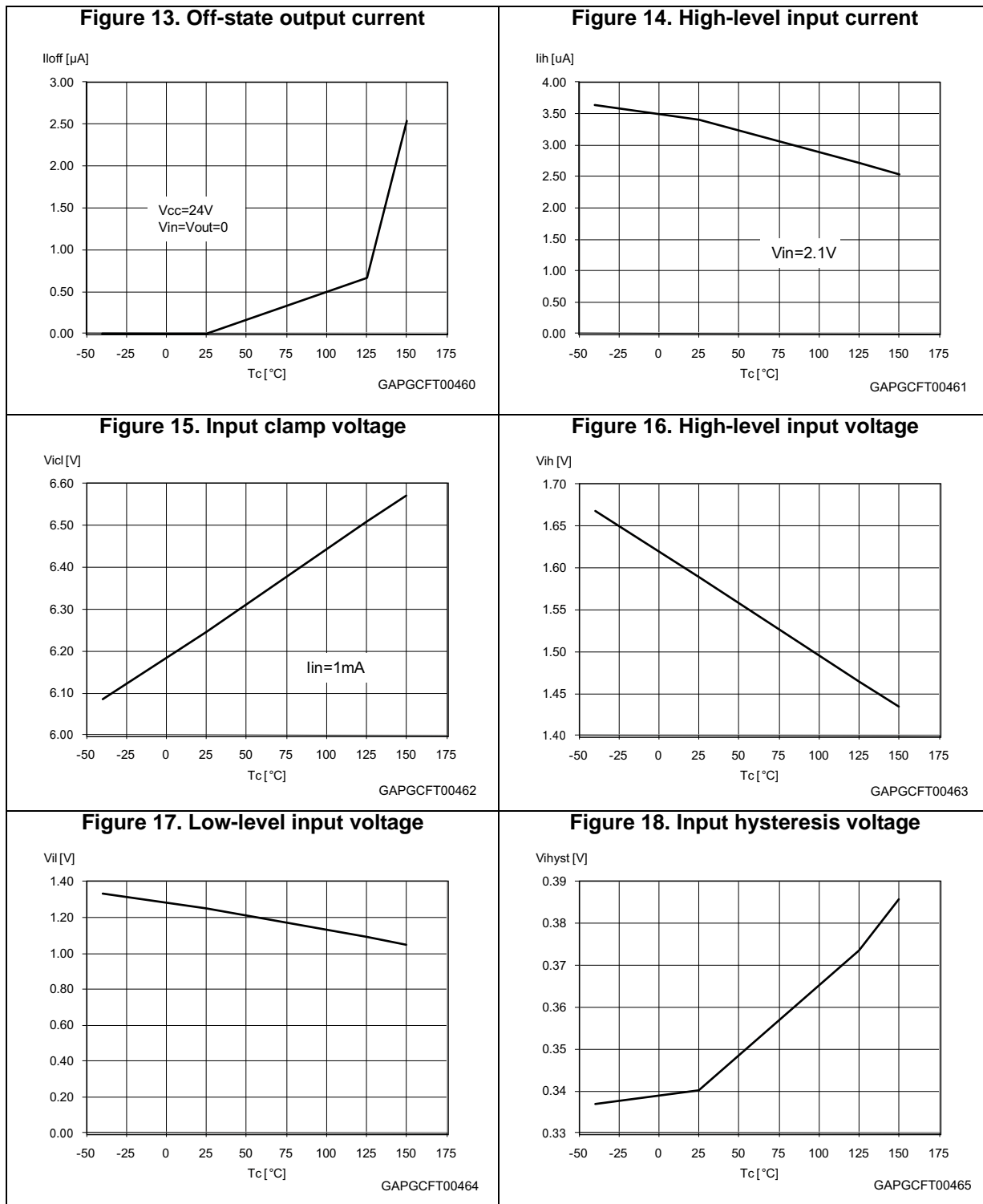


Figure 19. On-state resistance vs T_{case}

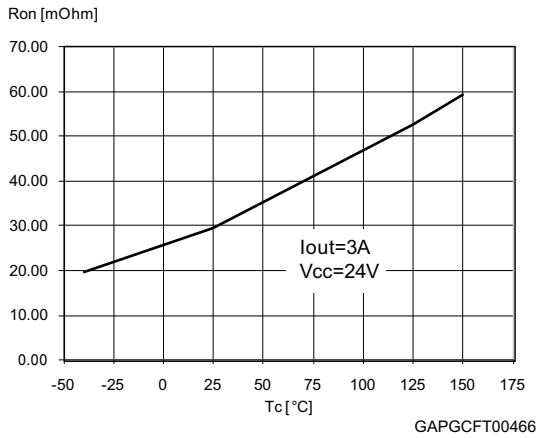


Figure 20. On-state resistance vs V_{CC}

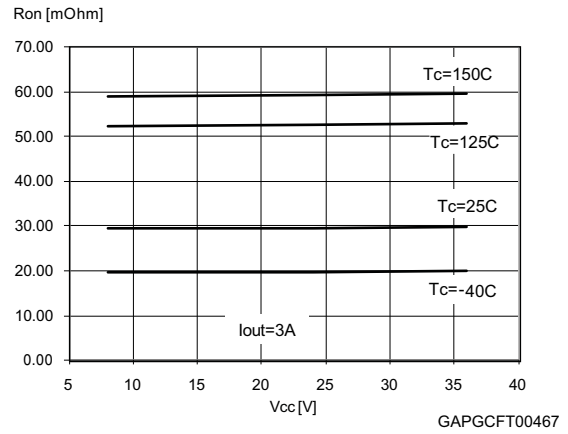


Figure 21. I_{LIMH} vs T_{case}

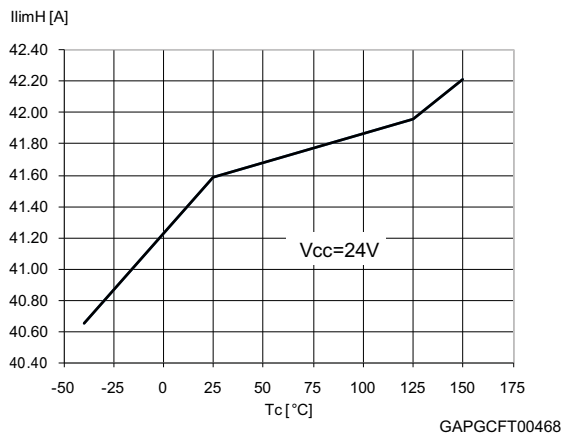


Figure 22. Turn-on voltage slope

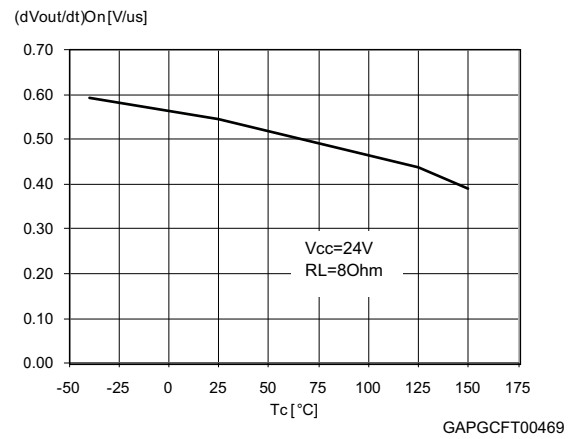
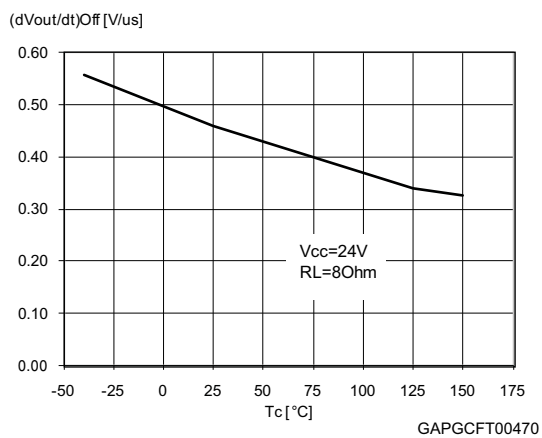
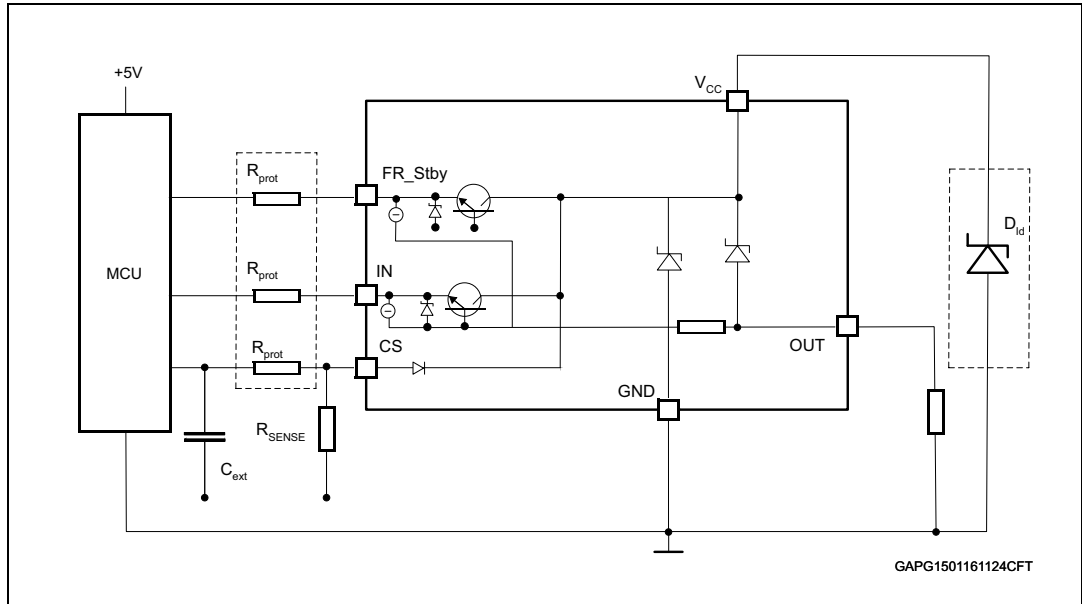


Figure 23. Turn-off voltage slope



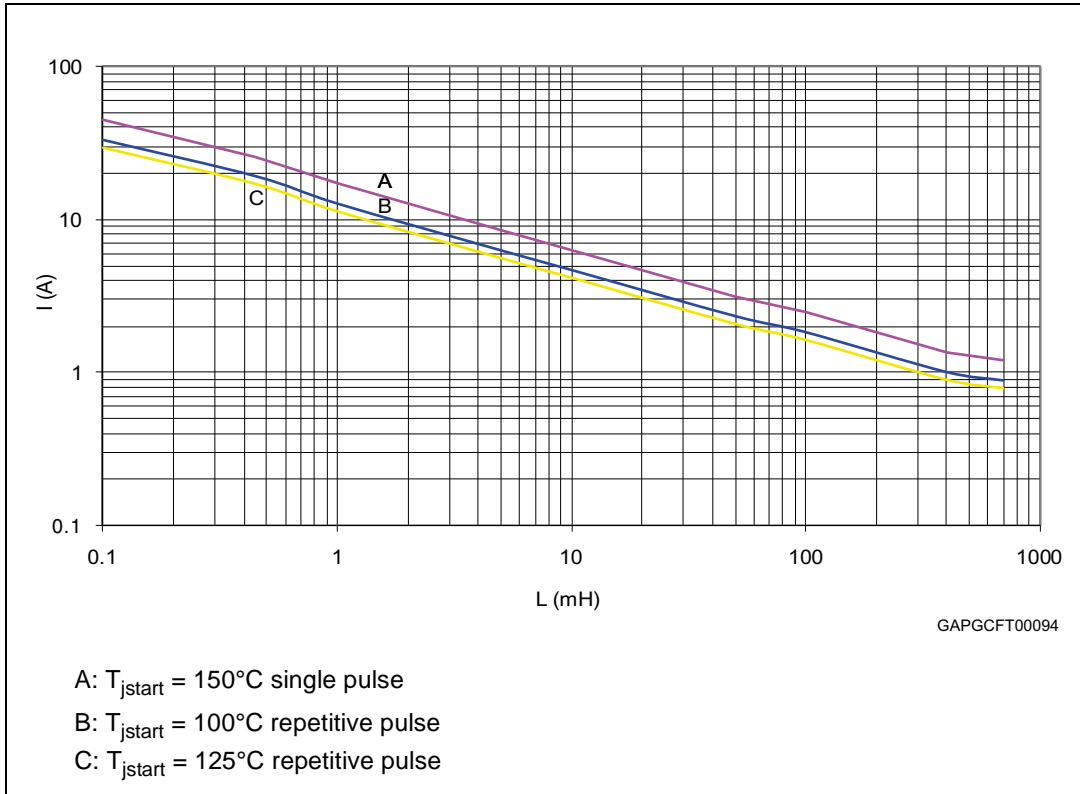
3 Application information

Figure 24. Application schematic



3.1 Maximum demagnetization energy ($V_{CC} = 24\text{ V}$)

Figure 25. Maximum turn-off current versus inductance (with no diodes connected in anti-parallel to inductive load)

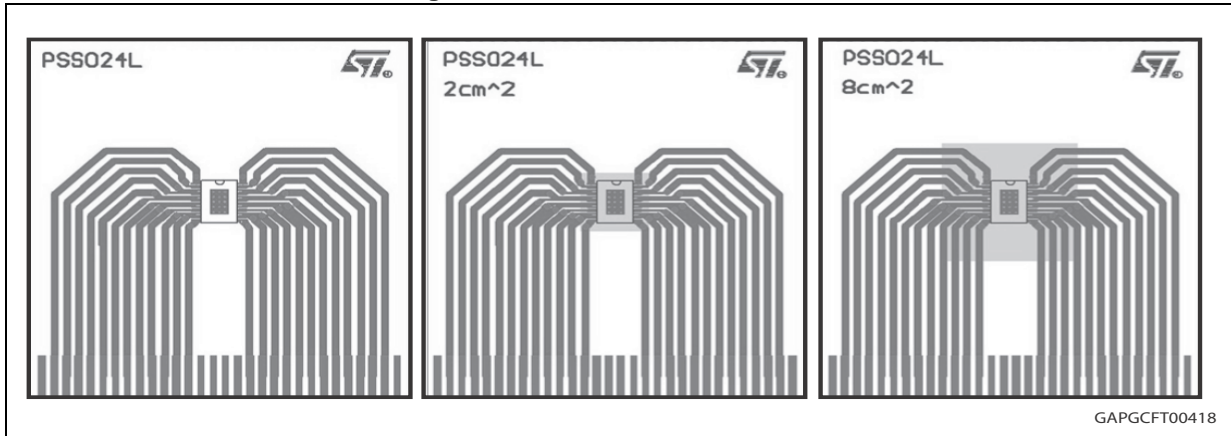


Note: Values are generated with $R_L = 0\ \Omega$. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-24 thermal data

Figure 26. PowerSSO-24 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 μ m (front and back side), Copper areas: from minimum pad lay-out to 8 cm²).

Figure 27. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

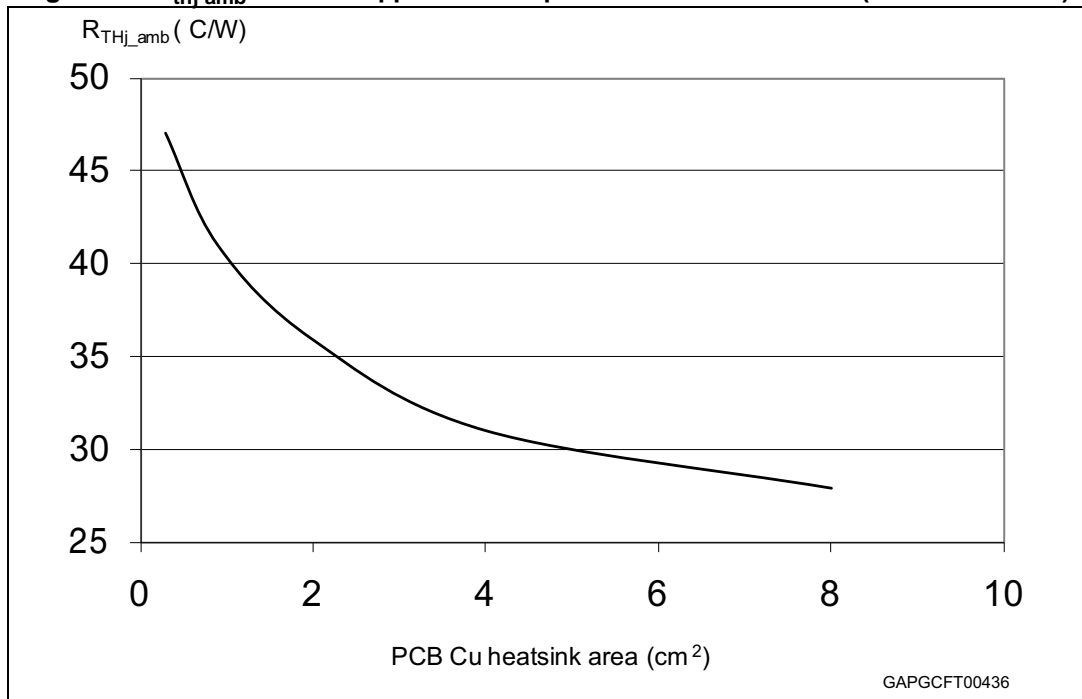


Figure 28. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

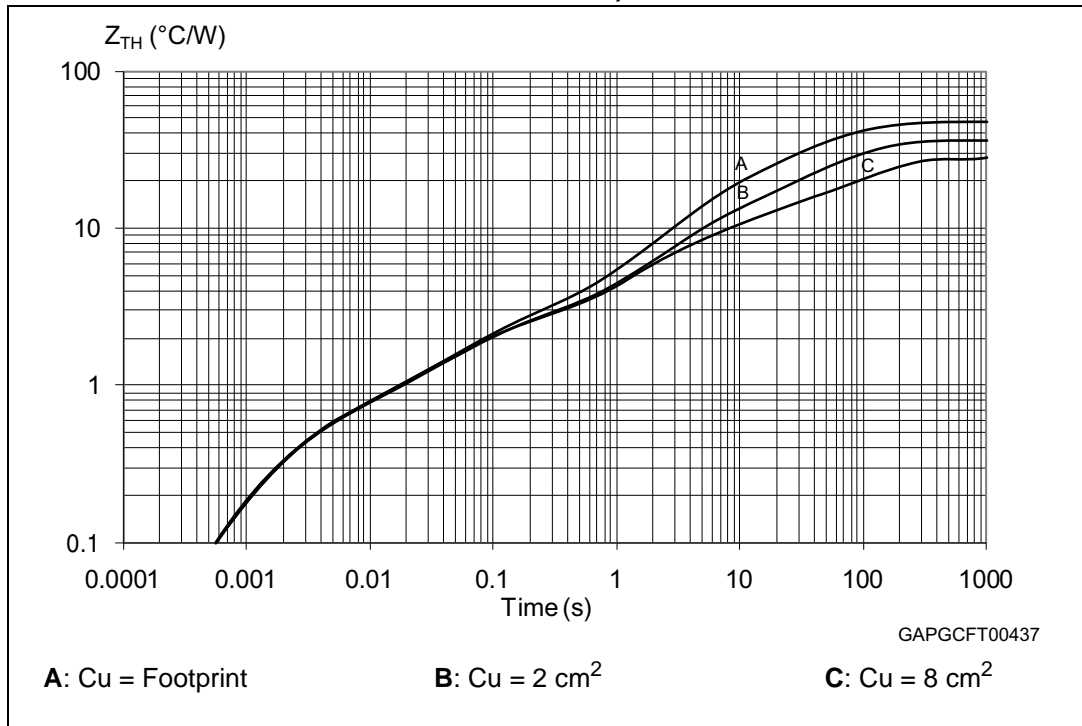
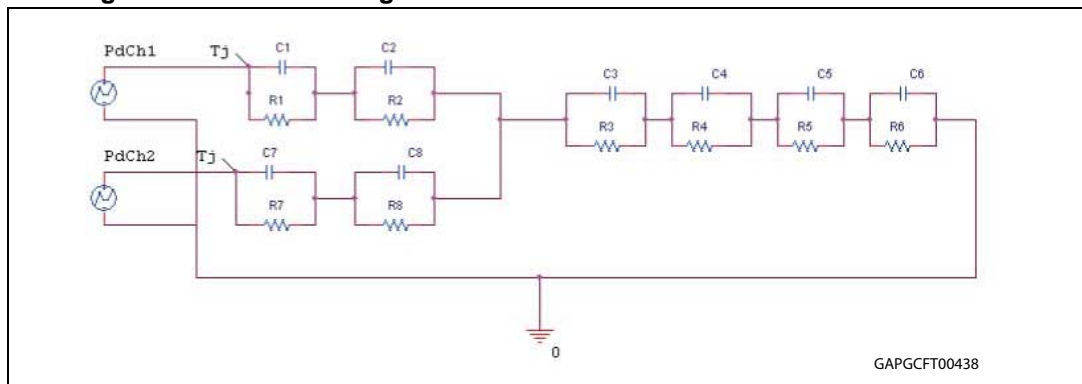


Figure 29. Thermal fitting model of a double channel HSD in PowerSSO-24



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered

Equation 1: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 12. Thermal parameters

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0,5	—	—
R2 (°C/W)	0.75	—	—
R3 (°C/W)	1	—	—
R4 (°C/W)	7.7	—	—
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
R7 (°C/W)	0,5	—	—
R8 (°C/W)	0.75	—	—
C1 (W.s/°C)	0,005	—	—
C2 (W.s/°C)	0,05	—	—
C3 (W.s/°C)	0,1	—	—
C4 (W.s/°C)	0,5	—	—
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17
C7 (W.s/°C)	0,005	—	—
C8 (W.s/°C)	0,05	—	—

5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 PowerSSO-24 package information

Figure 30. PowerSSO-24 package dimensions

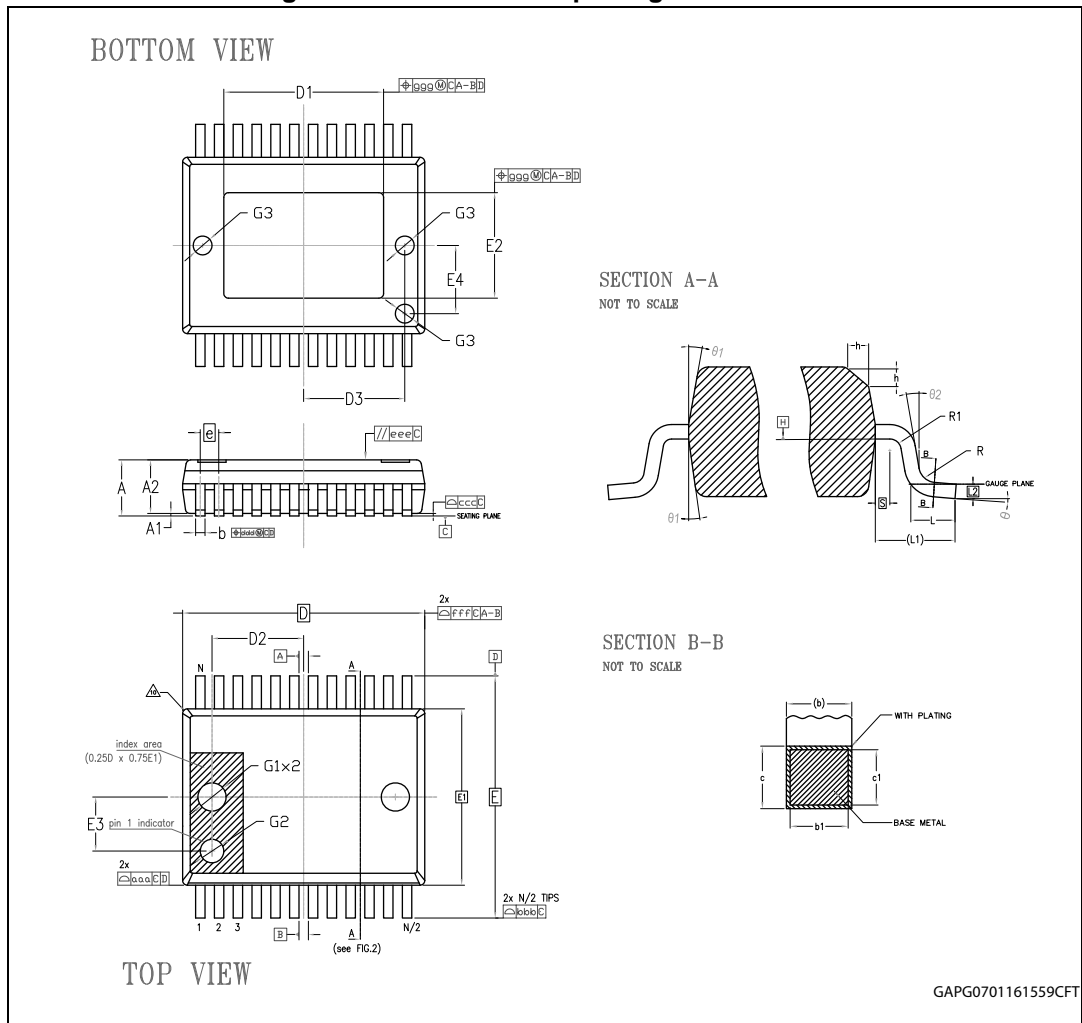


Table 13. PowerSSO-24 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
$\Theta 1$	5°		10°
$\Theta 2$	0°		
A			2.45
A1	0.00		0.10
A2	2.15		2.35
b	0.33		0.51
b1	0.28	0.40	0.48
c	0.23		0.32
c1	0.20	0.20	0.30
D	10.30 BSC		
D1	6.50		7.10
D2		3.65	
D3		4.30	
e	0.80 BSC		
E	10.30 BSC		
E1	7.50 BSC		
E2	4.10		4.70
E3		2.30	
E4		2.90	
G1		1.20	
G2		1.00	
G3		0.80	
h	0.30		0.40
L	0.55	0.70	0.85
L1	1.40		
L2	0.25 BSC		
N	24		
R	0.30		
R1	0.20		
S	0.25		
Tolerance of form and position			
aaa	0.20		

Table 13. PowerSSO-24 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
bbb		0.20	
ccc		0.10	
ddd		0.20	
eee		0.10	
fff		0.20	
ggg		0.15	

5.2 PowerSSO-24 packing information

Figure 31. PowerSSO-24 tube shipment (no suffix)

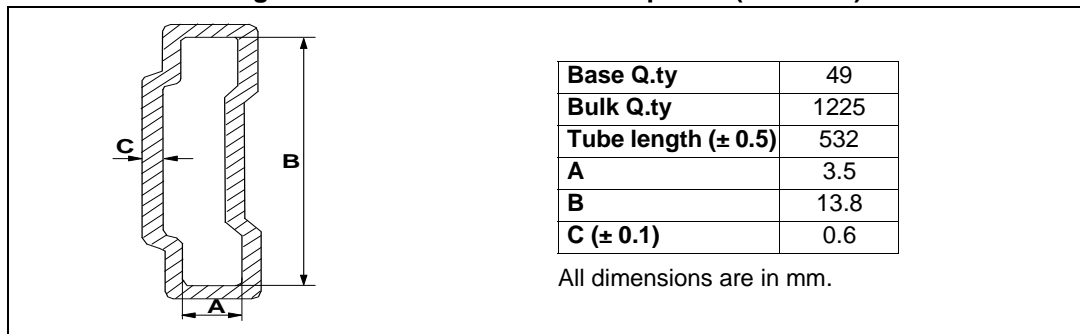
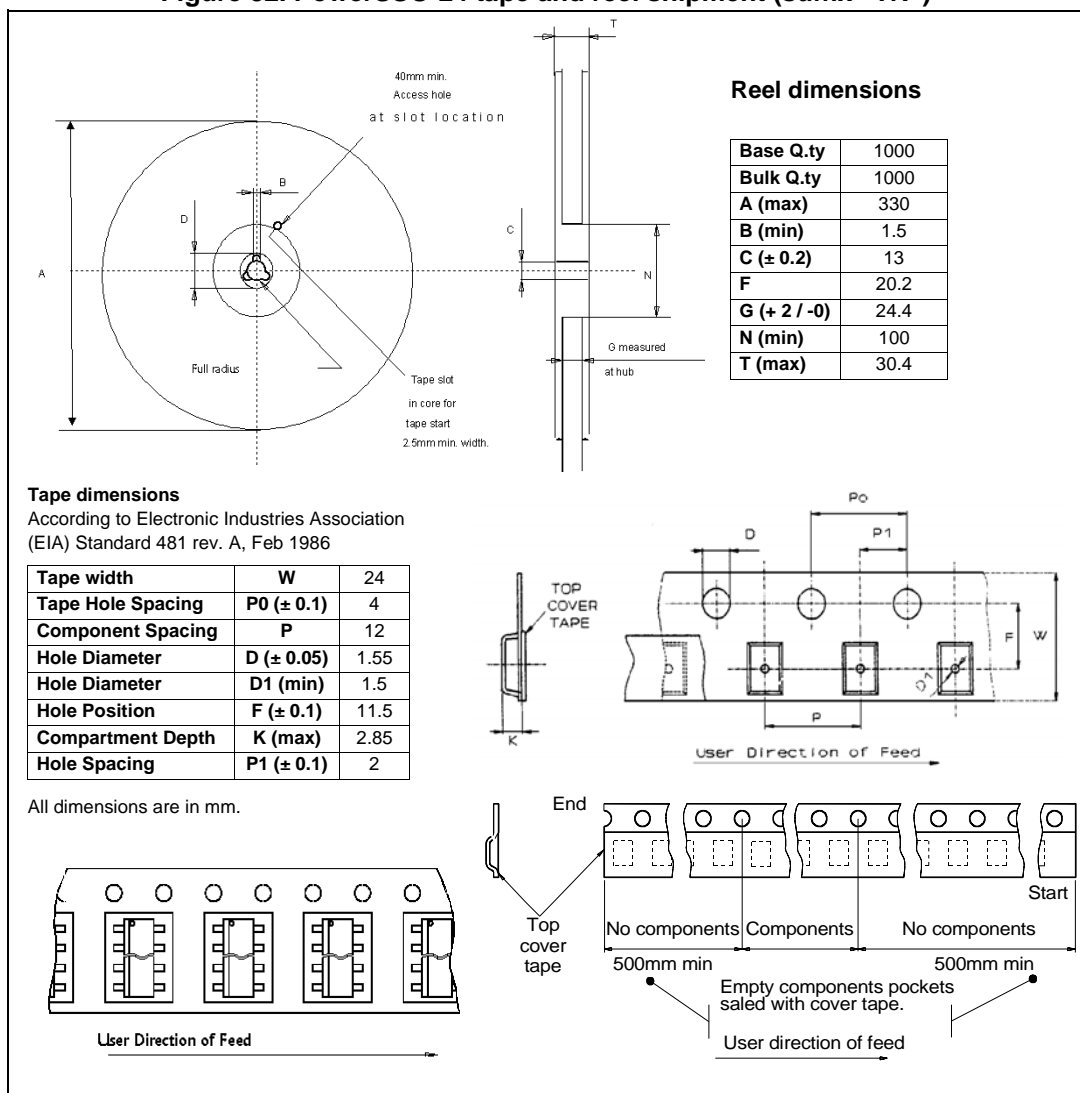


Figure 32. PowerSSO-24 tape and reel shipment (suffix "TR")



6 Order codes

Table 14. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VPS2535H	VPS2535HTR

7 Revision history

Table 15. Document revision history

Date	Revision	Changes
22-Jan-2016	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved