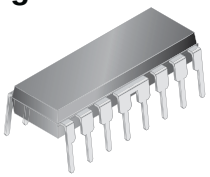
Protected Quad Power Driver

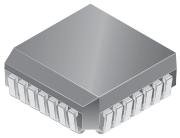
Features and Benefits

- 700 mA output current per channel
- Independent overcurrent protection for each driver
- Thermal protection for device and each driver
- Low output-saturation voltage
- Integral output flyback diodes
- TTL and 5 V CMOS-compatible inputs

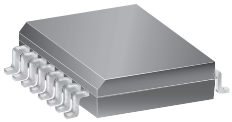
Packages:



16-pin DIP
with exposed thermal tabs
(B package)



28-pin PLCC
(Package EB)



16-pin SOICW
with internally fused pins
(LB package)

Not to scale

Description

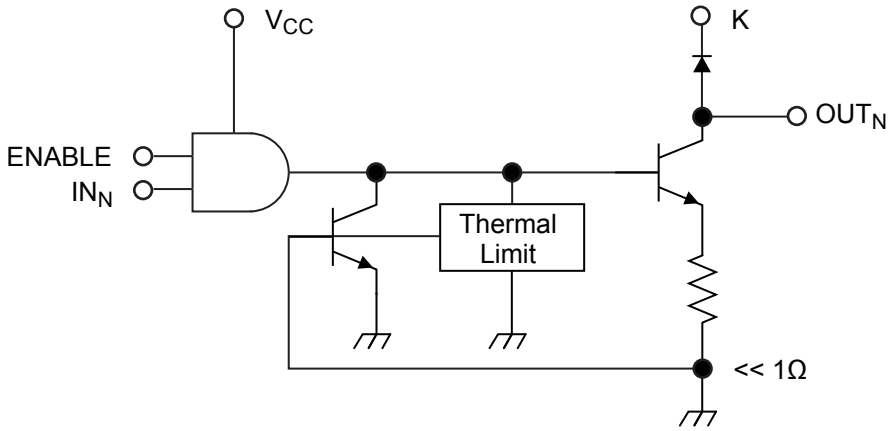
Providing improved output current limiting, the UDK, UDN, and UDQ2559B, EB, and LB quad power drivers combine AND logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs sink 700 mA in the on state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems.

Overcurrent protection for each channel has been designed into these devices and is activated at approximately 1 A. It protects each output from short circuits with supply voltages up to 25 V. When an output current trip point is reached, that output stage is driven linearly resulting in a reduced output current level. If an over-current or short-circuit condition continues, the thermal-limiting circuits will first sense the rise in junction temperature and then the rise in chip temperature, further decreasing the output current. Under worst-case conditions, these devices will tolerate short circuits on all outputs, simultaneously.

These devices can be used to drive various loads including incandescent lamps (without warming or limiting resistors) or inductive loads such as relays, solenoids, or dc stepping motors.

The packages offer fused leads for enhanced thermal dissipation. Package B is a 16-pin power DIP with exposed tabs, EB is a 28-lead power PLCC, and LB is a 16-lead power wide-body SOIC for surface-mount applications. The lead (Pb) free versions have 100% matte tin leadframe plating.

Functional Block Diagram
(1 of 4 Channels)



Selection Guide

Part Number	Pb-free	Package	Packing	Ambient Temperature (°C)
UDN2559B-T	Yes	16-pin DIP, exposed tabs	25 per tube	–20 to 85
UDN2559EBTR-T	Yes	28-lead PLCC	800 per reel	
~~UDN2559LBTR-T*~~	Yes	16-lead SOIC	1000 per reel	
~~UDQ2559B-T*~~	Yes	16-pin DIP, exposed tabs	25 per tube	–40 to 85
UDQ2559LBTR-T	Yes	16-lead SOIC	1000 per reel	
UDK2559B-T	Yes	16-pin DIP, exposed tabs	25 per tube	–40 to 125
~~UDK2559EBTR*~~	–	28-lead PLCC	800 per reel	
UDK2559EBTR-T	Yes	28-lead PLCC	800 per reel	
~~UDK2559LBTR*~~	–	16-lead SOIC	1000 per reel	
UDK2559LBTR-T	Yes	16-lead SOIC	1000 per reel	

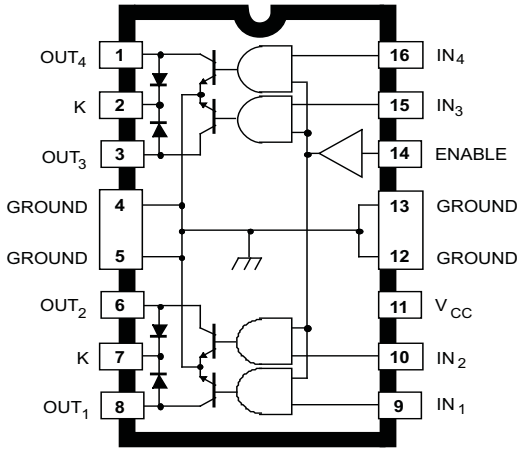
*Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change November 2, 2009. Deadline for receipt of LAST TIME BUY orders is April 30, 2010.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		7	V
Input Voltage Range	V_{IN}, V_{EN}		7	V
Output Voltage	V_{OUT}		60	V
Overcurrent-Protected Output Voltage	$V_{OUT(P)}$		25	V
Output Current	I_{OUT}	Outputs are peak current limited at approximately 1.0 A per driver. See Circuit Description and Application section for further information.	1.0	A
Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
		Range N	–20 to 85	°C
		Range Q	–40 to 85	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

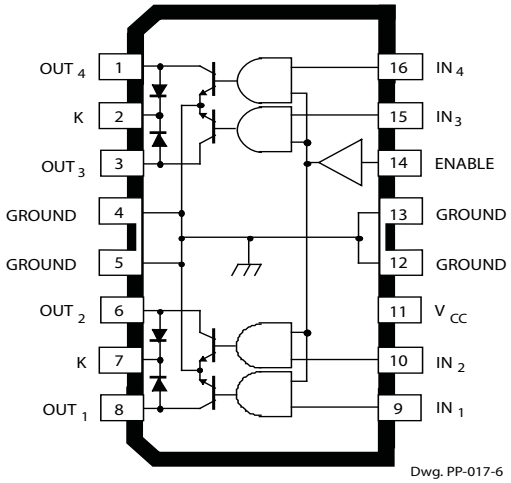
Pin-out Diagrams

Package B



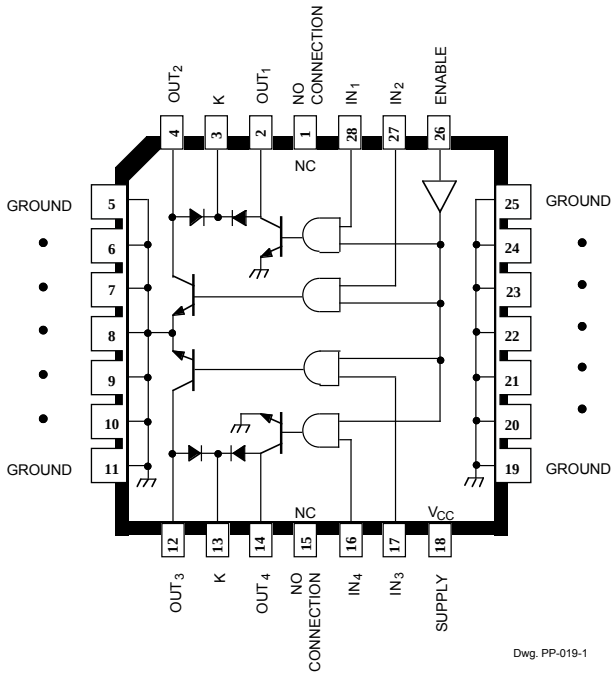
Dwg. PP-017-1

Package LB



Dwg. PP-017-6

Package EB

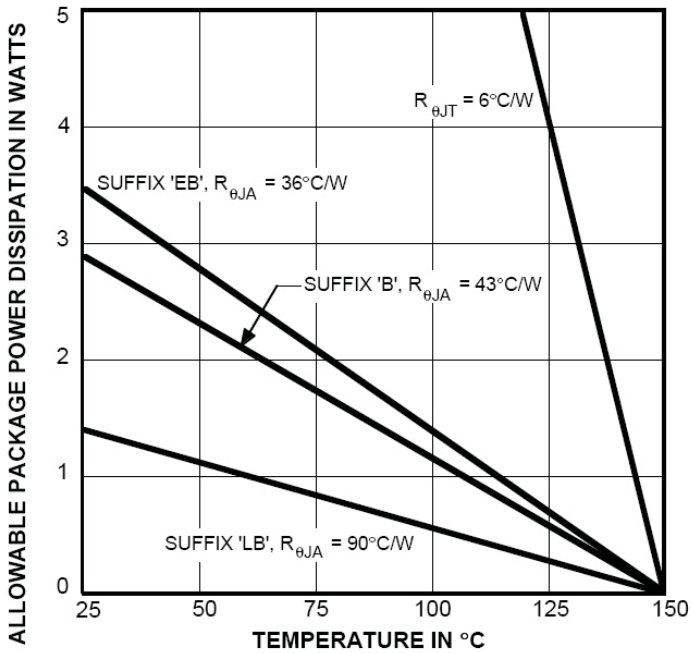


Dwg. PP-019-1

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package B, 2-layer PCB with 0.5 in.^{2} exposed copper each side	43	°C/W
		Package EB, 1-layer PCB with copper limited to solder pads	36	°C/W
		Package LB, 1-layer PCB with copper limited to solder pads	90	°C/W

*Additional thermal information available on the Allegro website



Dwg. GP-004-2B

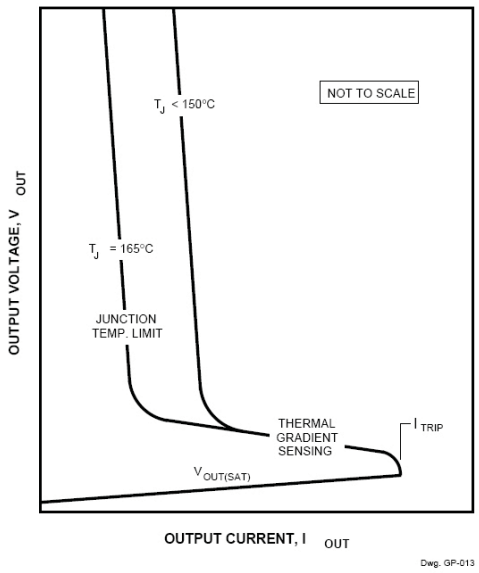
$$P_D = (V_{OUT1} \times I_{OUT1} \times dc) + \ldots + (V_{OUTn} \times I_{OUTn} \times dc) + (V_{CC} \times I_{CC}) = (T_J - T_A)/R_{\theta JA}$$

ELECTRICAL CHARACTERISTICS at T_A = +25°C (prefix 'UDN') or over operating temperature range (prefix 'UDK' or 'UDQ'), V_{CC} = 4.75 V to 5.25 V

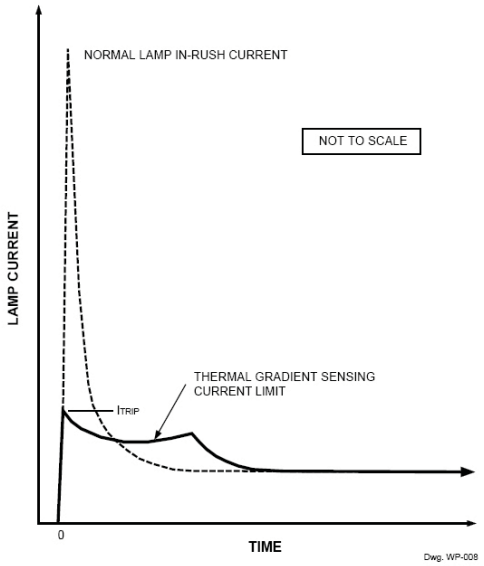
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V, V_{IN} = 0.8 V, V_{EN} = 2.0 V	—	<1.0	100	µA
		V_{OUT} = 50 V, V_{IN} = 2.0 V, V_{EN} = 0.8 V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 0.8 V	40	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	All Devices, I_{OUT} = 100 mA	—	—	300	mV
		All Devices, I_{OUT} = 400 mA	—	—	500	mV
		B or EB package only, I_{OUT} = 600 mA	—	—	700	mV
Over-Current Trip	I_{TRIP}		—	1.0	—	A
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.0 V	—	—	40	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	—	-10	µA
Total Supply Current*	I_{CC}	All Outputs ON, V_{IN} = V_{EN} = 2.0 V	—	—	80	mA
		All Outputs OFF	—	—	5.0	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	—	1.7	V
		I_F = 1.5 A	—	—	2.1	V
Clamp Diode Leakage Current	I_R	V_R = 50 V, D_1 + D_2 or D_3 + D_4	—	—	50	µA
Turn-On Delay	t_{PHL}	I_{OUT} = 500 mA	—	—	20	µs
	t_{PLH}	I_{OUT} = 500 mA	—	—	20	µs
Thermal Limit	T_J		—	165	—	°C

Typical Data is for design information only.
Negative current is defined as coming out of (sourcing) the specified terminal.
As used here, -100 is defined as greater than +10 (absolute magnitude convention) and the minimum is implicitly zero.
* All inputs simultaneously, all other tests are performed with each input tested separately.

TYPICAL OUTPUT CHARACTERISTIC



TYPICAL OUTPUT BEHAVIOR



CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON/in-rush currents can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warming or current-limiting resistors protect both driver and lamp but use significant power either when the lamp is OFF or when the lamp is ON, respectively. Lamps with steady-state current ratings up to 700 mA can be driven by these devices without the need for warming (parallel) or current-limiting (series) resistors.

When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current. With these drivers, during turn-ON, the high in-rush current is sensed by the internal low-value sense resistor. Drive current to the output stage is then diverted by the shunting transistor, and the load current is momentarily limited to approximately 1.0 A. During this short transition period, the output current is reduced to a value dependent on supply voltage and filament resistance. During lamp warmup, the filament resistance increases to its maximum value, the output stage goes into saturation and applies maximum rated voltage to the lamp.

INDUCTIVE LOAD DRIVER

Bifilar (unipolar) stepper motors, relays, or solenoids can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes that occur when turning OFF an inductive load.

For rapid current decay (fast turn-OFF speeds), the use of Zener diodes will raise the flyback voltage and inprove performance. However, the peak voltage must not exceed the specified minimum sustaining voltage (V_{SUPPLY} + V_Z + V_F $V_{OUT(SUS)}$).

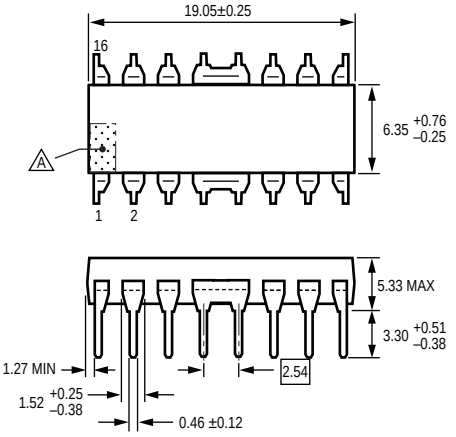
FAULT CONDITIONS

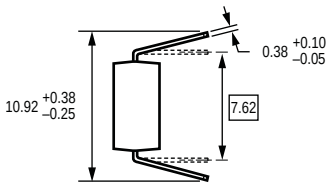
In the event of a shorted load, the load current will attempt to increase. As described above, the drive current to the affected output stage is reduced, causing the output stage to go linear, limiting the peak output current to approximately 1 A. As the power dissipation of that output stage increases, a thermal gradient sensing circuit will become operational, further decreasing the drive current to the affected output stage and reducing the output current to a value dependent on supply voltage and load resistance.

Continuous or multiple overload conditions causing the chip temperature to reach approximately 165°C will result in an additional reduction in output current to maintain a safe level.

If the fault condition is corrected, the output stage will return to its normal saturated condition.

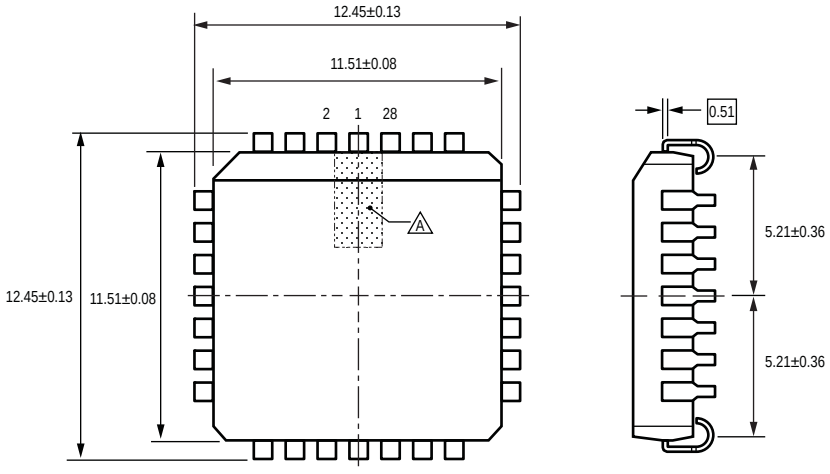
B Package, 16-pin DIP
with internally fused pins 4, 5, 12, and 13 and external thermal tabs

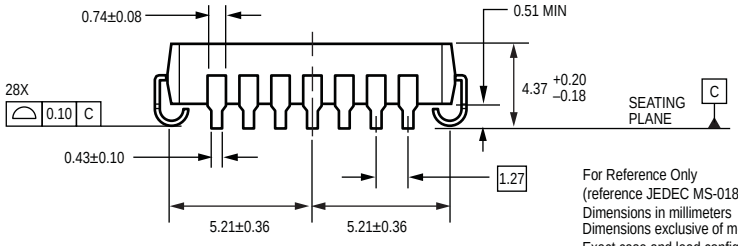




For Reference Only
(reference JEDEC MS-001 BB)
Dimensions in inches, metric dimensions (mm) in brackets, for reference only
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

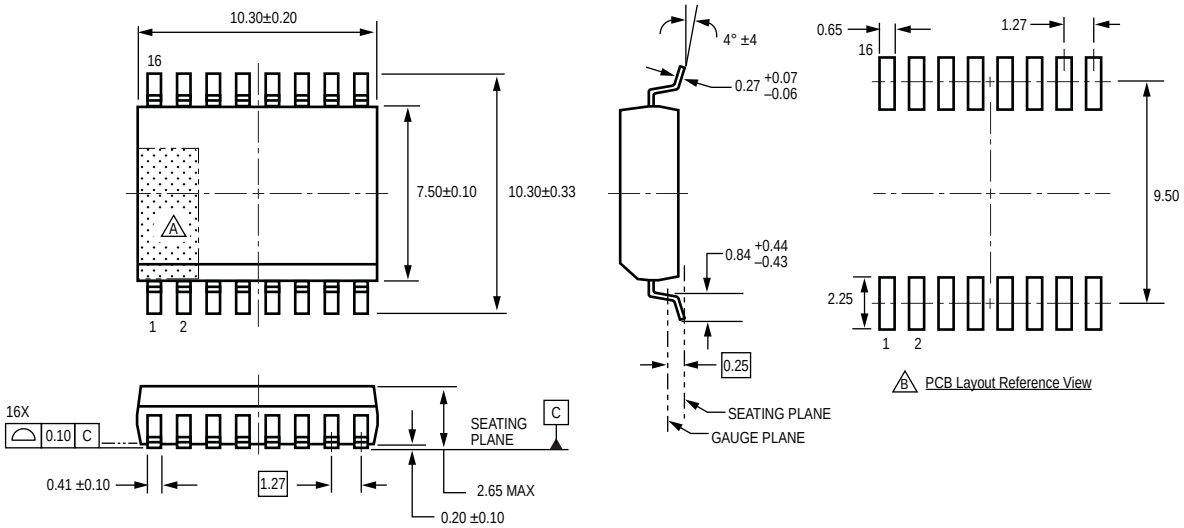
EB Package, 28-pin PLCC
with internally fused pins 5 through 11 and 19 through 25





For Reference Only
(reference JEDEC MS-018 AB)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

LB Package, 16-pin SOICW
with internally fused pins 4 and 5, and 12 and 13



For Reference Only
Pins 4 and 5, and 12 and 13 internally fused
Dimensions in millimeters
(reference JEDEC MS-013 AA)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Reference pad layout (reference IPC SOIC127P1030X265-16M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

For the latest version of this document, visit our website:
www.allegromicro.com