

NCP436, NCP437

3A Ultra-Small Controlled Load Switch with Auto-Discharge Path

The NCP436 and NCP437 are very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail for the NCP437 part only.

Proposed in a wide input voltage range from 1.0 V to 3.6 V, in a small 1 x 1.5 mm WLCSP6, pitch 0.5 mm.

Features

- 1.0 V – 3.6 V Operating Range
- 20 mΩ P MOSFET at 3.6 V
- DC Current Up to 3 A
- Output Auto-discharge
- Active High EN Pin
- WLCSP6 1 x 1.5 mm
- These are Pb-Free Devices

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices



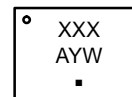
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM

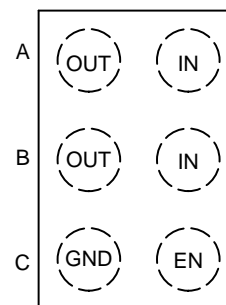


WLCSP6
CASE 567FH



- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

PIN DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

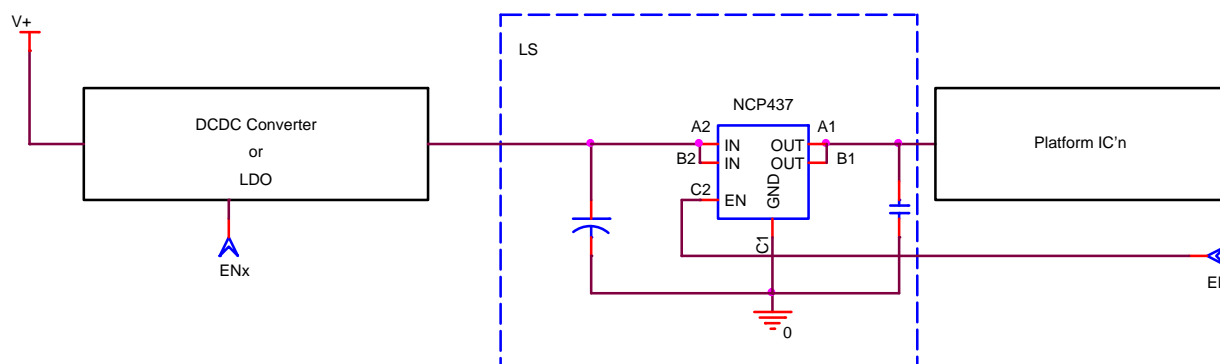


Figure 1. Typical Application Circuit

NCP436, NCP437

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2, B2	POWER	Load-switch input voltage; connect a 1 μ F or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	C1	POWER	Ground connection.
EN	C2	INPUT	Enable input, logic high turns on power switch.
OUT	A1, B1	OUTPUT	Load-switch output; connect a 1 μ F ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

BLOCK DIAGRAM

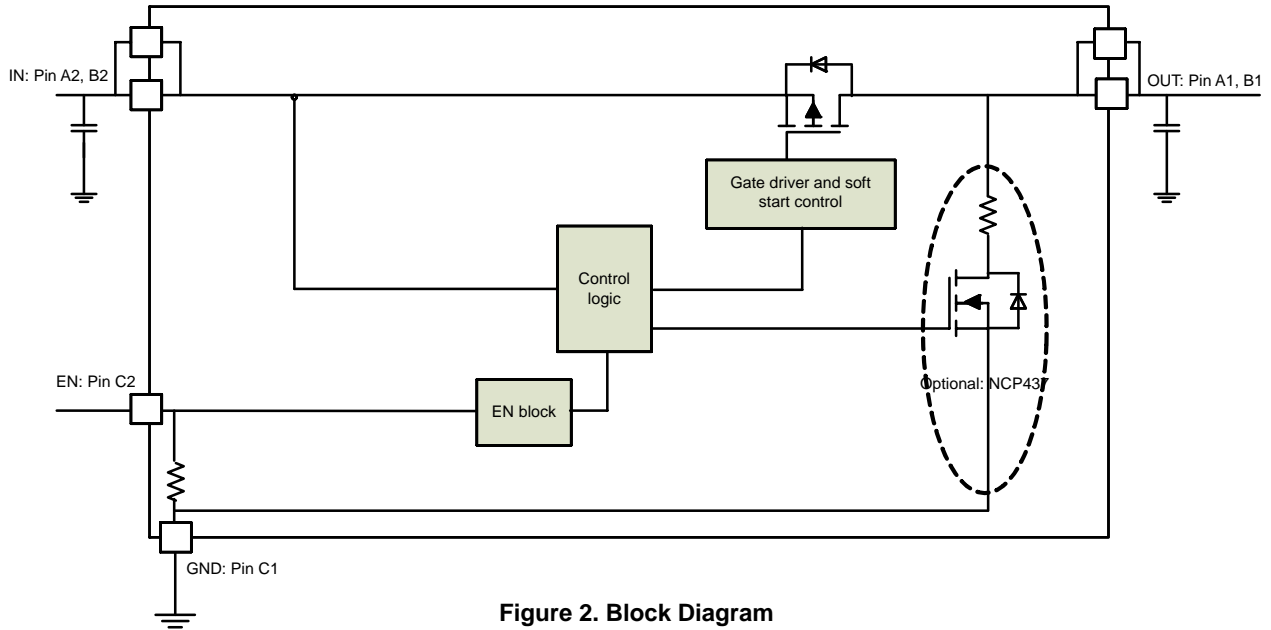


Figure 2. Block Diagram

NCP436, NCP437

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{EN}, V_{IN}, V_{OUT}	IN, OUT, EN, Pins: (Note 1)	-0.3 to + 4	V
V_{IN}, V_{OUT}	From IN to OUT Pins: Input/Output (Note 1)	0 to + 4	V
T_J	Maximum Junction Temperature	-40 to + 125	°C
ESD HBM	Human Body Model (HBM) ESD Rating are (Notes 2 and 3)	8000	V
ESD MM	Machine Model (MM) ESD Rating are (Notes 2 and 3)	250	V
ESD CDM	Charge Device Model (CDM) ESD Rating are (Notes 2 and 3)	2000	V
LU	Latch-up Protection (Note) - Pins IN, OUT, EN	100	mA
T_{STG}	Storage Temperature Range	-40 to + 150	°C
MSL	Moisture Sensitivity (Note 2)	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. According to JEDEC standard JESD22-A108.
2. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.
3. This device series contains ESD protection and passes the following tests
Human Body Model (HBM) ± 8.0 kV per JEDEC standard: JESD22-A114 for all pins.
Machine Model (MM) ± 250 V per JEDEC standard: JESD22-A115 for all pins.
Charge Device Model (CDM) ± 2.0 kV per JEDEC standard: JESD22-C101 for all pins.
4. Latch-up Current Maximum Rating: ± 100 mA per JEDEC standard: JESD78 Class II.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{IN}	Operational Power Supply		1.0		3.6	V	
V_{EN}	Enable Voltage		0		3.6		
T_A	Ambient Temperature Range		-40	25	+85	°C	
T_J	Junction Temperature Range		-40	25	+125	°C	
C_{IN}	Decoupling input capacitor		1			μF	
C_{OUT}	Decoupling output capacitor		1			μF	
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 5)		100		°C/W	
I_{OUT}	Maximum DC current				3	A	
P_D	Power Dissipation Rating (Note 6)	$T_A \leq 25^\circ C$	WLCSP package		0.66		W
		$T_A = 85^\circ C$	WLCSP package		0.26		W

5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

NCP436, NCP437

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ for V_{IN} between 1.0 V to 3.6 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$ and $V_{IN} = 3.3\text{ V}$ (Unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
POWER SWITCH							
$R_{DS(on)}$	Static drain-source on-state resistance	$V_{IN} = 3.6\text{ V}$	$I = 200\text{ mA}, 25^{\circ}\text{C}$		15	26	m Ω
			$I = 200\text{ mA}, T_A = 85^{\circ}\text{C}$			28	
			$T_J = 125^{\circ}\text{C}$			29	
		$V_{IN} = 2.5\text{ V}$	$I = 200\text{ mA}, 25^{\circ}\text{C}$		18	30	
			$I = 200\text{ mA}, T_A = 85^{\circ}\text{C}$			32	
			$T_J = 125^{\circ}\text{C}$			35	
		$V_{IN} = 1.8\text{ V}$	$I = 200\text{ mA}, 25^{\circ}\text{C}$		23	40	
			$I = 200\text{ mA}, \text{Full } T_a$			42	
			$T_J = 125^{\circ}\text{C}$			44	
		$V_{IN} = 1.2\text{ V}$	$I = 200\text{ mA}, 25^{\circ}\text{C}$		45	80	
			$I = 200\text{ mA}, \text{Full } T_a$			84	
			$T_J = 125^{\circ}\text{C}$			85	
$V_{IN} = 1.1\text{ V}$	$I = 200\text{ mA}, 25^{\circ}\text{C}$		62				
R_{dis}	Output discharge path	$V_{IN} = 3.3\text{ V}$	$EN = \text{low}$	50	65	90	Ω
V_{IH}	High-level input voltage			1.1			V
V_{IL}	Low-level input voltage					0.5	

QUIESCENT CURRENT

I_{std}	Standby current	$V_{IN} = 3.3\text{ V}$	$EN = \text{low}, \text{No load}$		0.01	0.6	μA
I_q	Quiescent current	$V_{IN} = 3.3\text{ V}$	$EN = \text{high}, \text{No load}$		0.2	0.6	

TIMINGS

T_{EN}	Enable time	$V_{IN} = 3.6\text{ V}$ (Note 8)	$R_L = 25\ \Omega, C_{OUT} = 1\ \mu\text{F}$	20	39	55	μs
T_R	Output rise time		$R_L = 25\ \Omega, C_{OUT} = 1\ \mu\text{F}$	10	25	40	
T_{ON}	ON time ($T_{EN} + T_R$)		$R_L = 25\ \Omega, C_{OUT} = 1\ \mu\text{F}$	30	64	95	
T_{DIS}	Disable time		$R_L = 25\ \Omega, C_{OUT} = 1\ \mu\text{F}$		20		
T_F	Output fall time		NCP437. $R_L = 25\ \Omega,$ $C_{OUT} = 1\ \mu\text{F}$	20	55	80	

7. Guaranteed by design and characterization

8. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

NCP436, NCP437

TIMINGS

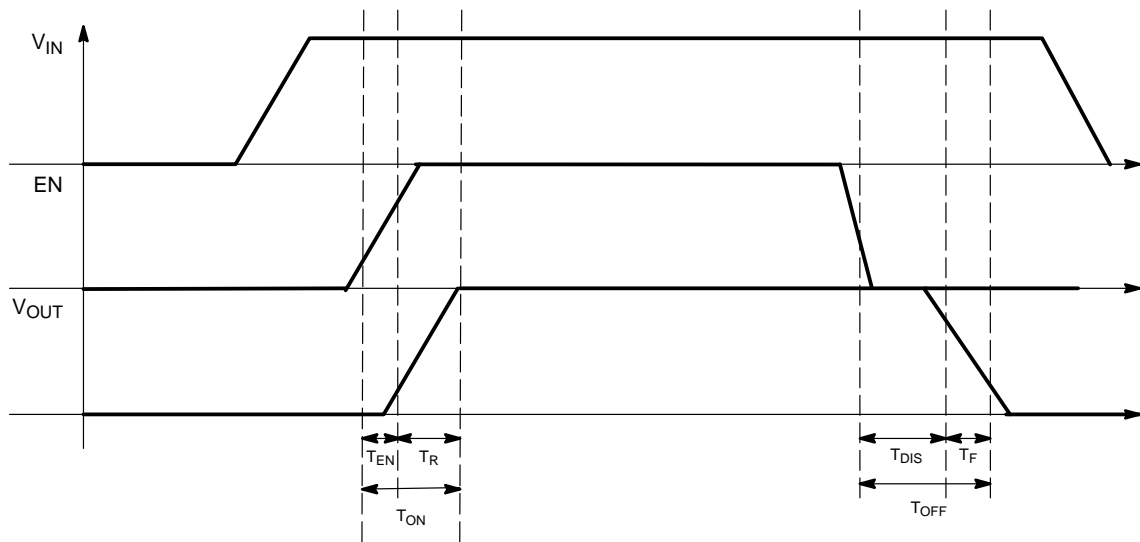


Figure 3. Enable, Rise and Fall Time

FUNCTIONAL DESCRIPTION

Overview

The NCP437 is a high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 1.0 V to 3.6 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of V_{IN} of 1.2 V and EN forced to high level.

Auto Discharge

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto-discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and $V_{IN} > 1.2$ V.

In order to limit the current across the internal discharge N-MOSFET, the typical value is set at 65Ω .

C_{IN} and C_{OUT} Capacitors

IN and OUT, 1 μ F, at least, capacitors must be placed as close as possible the part to for stability improvement.

NCP436, NCP437

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times (I_{OUT})^2$$

P_D = Power dissipation (W)
 $R_{DS(on)}$ = Power MOSFET on resistance (Ω)
 I_{OUT} = Output current (A)

$$T_J = R_{\theta JA} \times P_D + T_A$$

T_J = Junction temperature ($^{\circ}\text{C}$)
 $R_{\theta JA}$ = Package thermal resistance ($^{\circ}\text{C}/\text{W}$)
 T_A = Ambient temperature ($^{\circ}\text{C}$)

PCB Recommendations

The NCP437 integrates an up to 3 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

Routing example: 2 oz, 4 layers with vias across two internal inners.

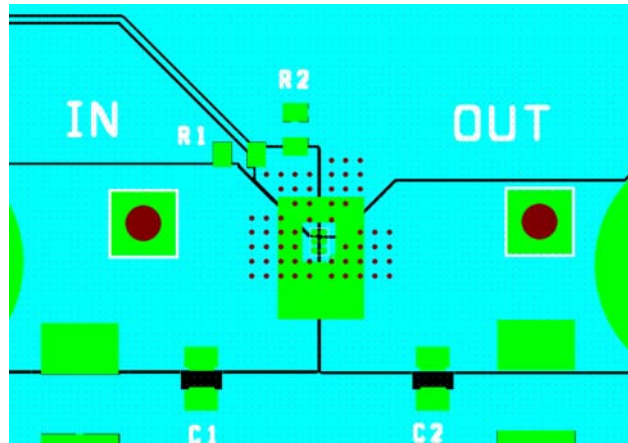


Figure 4.

Example of application definition.

$$T_J - T_A = R_{\theta JA} \times P_D = R_{\theta JA} \times R_{DS(on)} \times I^2$$

T_J : Junction Temperature.

T_A : Ambient Temperature.

R_{θ} = Thermal resistance between IC and air, through PCB.

$R_{DS(on)}$: Intrinsic resistance of the IC MOSFET.

I: Load DC current.

Taking into account of R_{θ} obtain with:

- 1 oz, 2 layers: 100 $^{\circ}\text{C}/\text{W}$.

At 3 A, 25 $^{\circ}\text{C}$ ambient temperature, $R_{DS(on)}$ 20 m Ω @ V_{IN} 5 V, the junction temperature will be:

$$T_J = R_{\theta JA} \times P_D = 25 + (0.02 \times 3^2) \times 100 = 43^{\circ}\text{C}$$

Taking into account of R_{θ} obtain with:

- 2 oz, 4 layers: 60 $^{\circ}\text{C}/\text{W}$.

At 3 A, 65 $^{\circ}\text{C}$ ambient temperature, $R_{DS(on)}$ 24 m Ω @ V_{IN} 5 V, the junction temperature will be:

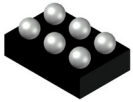
$$T_J = T_A + R_{\theta} \times P_D = 65 + (0.024 \times 3^2) \times 60 = 78^{\circ}\text{C}$$

ORDERING INFORMATION

Device	Marking	Option	Package	Shipping†
NCP437FCT2G	AR	Auto discharge	WLCSP 1 x 1.5 mm (Pb-Free)	3000 / Tape & Reel
NCP436FCT2G	AQ	Without Auto discharge	WLCSP 1 x 1.5 mm (Pb-Free)	3000 / Tape & Reel

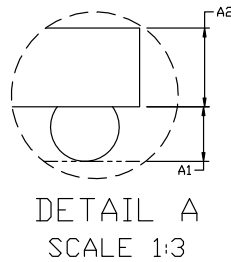
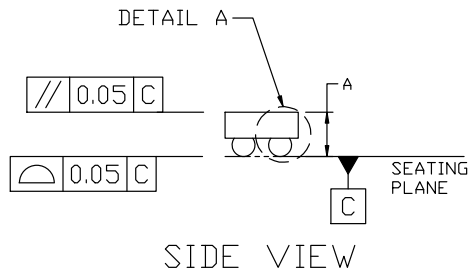
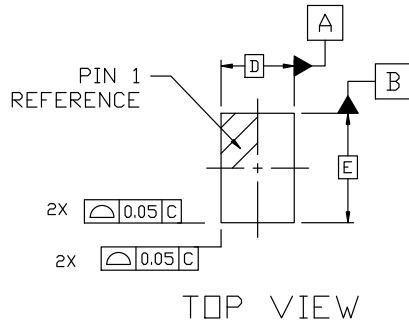
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



WLCSP6 1.0x1.5x0.609
CASE 567FH
ISSUE A

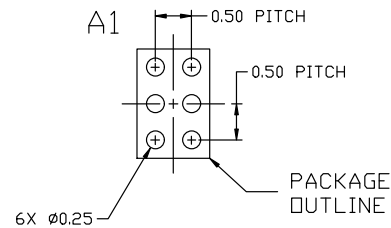
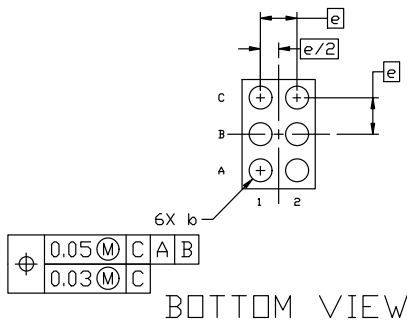
DATE 21 JUN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

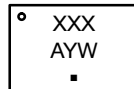
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.554	0.609	0.664
A1	0.219	0.249	0.279
A2	0.335	0.360	0.385
b	0.282	0.312	0.342
D	1.00 BSC		
E	1.50 BSC		
e	0.50 BSC		



RECOMMENDED
MOUNTING FOOTPRINT*

- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON79918E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WLCSP6 1.0x1.5x0.609	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative