

0257526 ADV MICRO PLA/PLE/ARRAYS

96D 27162 D

Programmable Polarity

Each flip-flop has individually programmable polarity. The unprogrammed state is active low.

Product Term Steering

Product term steering allows each pair of outputs to share its product terms with one output or the other (not both). Each pair has a total of sixteen product terms; thus, one output can use zero to sixteen terms while the other has sixteen to zero. Product terms can only be shared mutually exclusively. If both outputs need the same term, it must be created twice, once for each output.

Preload and Power-Up Reset

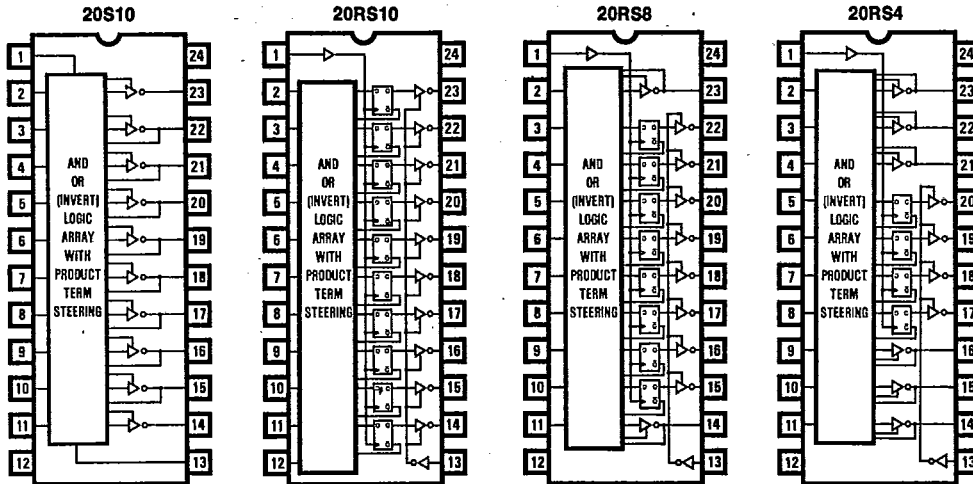
The 20RS10 Series offers register preload for device testability. The registers can be preloaded from the outputs by using super-voltages in order to simplify functional testing. The 20RS10 Series also offers Power-Up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

Packages

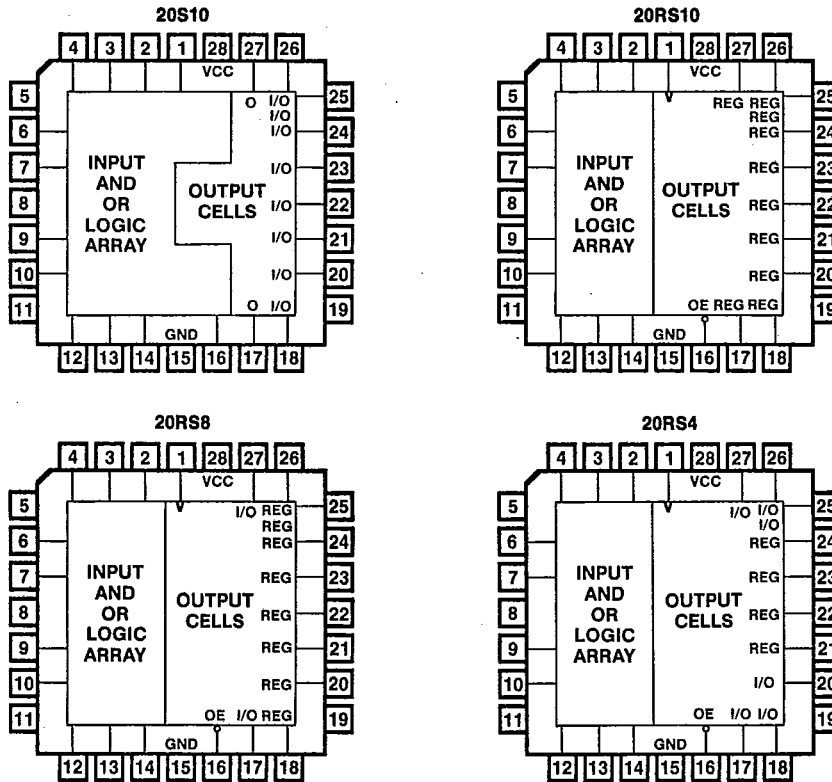
The commercial PAL20RS10 Series is available in the plastic SKINNYDIP (NS), ceramic SKINNYDIP (JS), plastic leaded chip carrier (NL), and small outline (SG) packages.

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DIP/SO Pinouts



PLCC Pinouts



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Absolute Maximum Ratings

	Operating	Programming
Supply voltage VCC	-0.5 V to 7.0 V	-0.5 V to 12.0 V
Input voltage	-1.5 V to 5.5 V	-1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature		-65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			UNIT	
		MIN	TYP	MAX		
V _{CC}	Supply voltage	4.75	5	5.25	V	
t _w	Width of clock	Low	15	10	ns	
		High	15	10		
t _{su}	Set up time from input or feedback to clock	20RS10, 20RS8, 20RS4	35	25	ns	
t _h	Hold time		0	-10	ns	
T _A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IL} ¹	Low-level input voltage					0.8	V
V _{IH} ¹	High-level input voltage			2			V
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		-0.8	-1.5	V
I _{IL} ²	Low-level input current	V _{CC} = MAX	V _I = 0.4 V		-0.02	-0.25	mA
I _{IH} ²	High-level input current	V _{CC} = MAX	V _I = 2.4 V			25	μA
I _I	Maximum input current	V _{CC} = MAX	V _I = 5.5 V			100	μA
V _{OL}	Low-level output voltage	V _{CC} = MIN	I _{OL} = 24 mA		0.3	0.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA	2.4	2.8		V
I _{OZL} ²	Off-state output current	V _{CC} = MAX	V _O = 0.4 V			-100	μA
I _{OZH} ²			V _O = 2.4 V			100	μA
I _{OS} ³	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30	-70	-130	mA
I _{CC}	Supply current	V _{CC} = MAX			175	240	mA

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

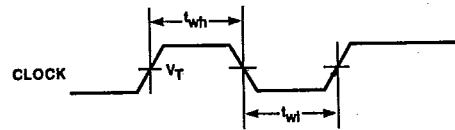
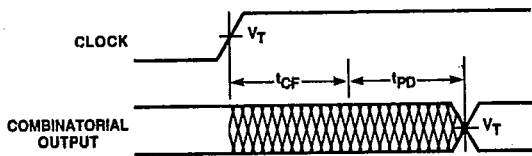
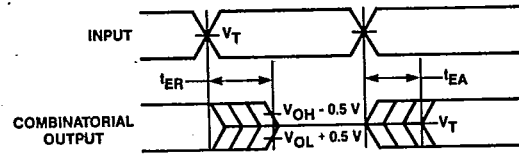
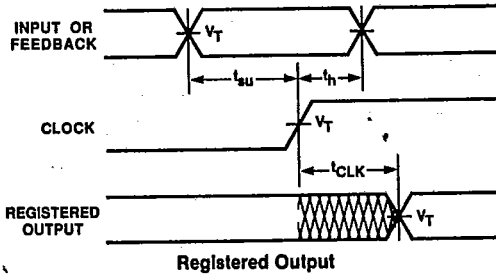
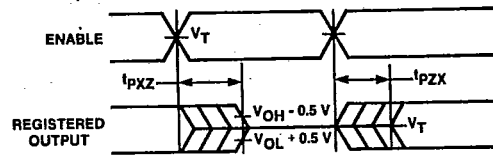
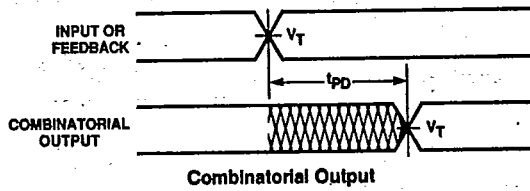
SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PD}	Input or feedback to output 20S10, 20RS8, 20RS4	Polarity fuse intact	R ₁ = 200 Ω R ₂ = 390 KΩ	25	35	ns	
		Polarity fuse programmed		30	40		
t _{CLK}	Clock to output or feedback	12		17	ns		
t _{CF}	Clock to feedback	10		15	ns		
t _{PZX}	Pin 13 to output enable except 20S10	10		20	ns		
t _{PXZ}	Pin 13 to output disable except 20S10	11		20	ns		
t _{EA}	Input to output enable	20S10, 20RS8, 20RS4		25	35	ns	
t _{ER}	Input to output disable	20S10, 20RS8, 20RS4		13	25	ns	
t _{MAX}	Maximum frequency	External			19	27	MHz
		Internal			20	28	
		No feedback	33		50		

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Switching Waveforms

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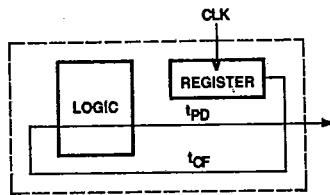


Clock to Feedback to Combinatorial Output (See Path Below)

Clock Width

Key to Timing Diagrams

WAVEFORM	INPUTS	OUTPUTS
	DONT CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY



- Notes:
 1. $V_T = 1.5\text{ V}$
 2. Input pulse amplitude 0 V to 3.0 V
 3. Input rise and fall times 2-5 ns typical

Switching Test Load

(refer to page 5-164)

Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)

Register Preload Waveform

(refer to page 5-164)

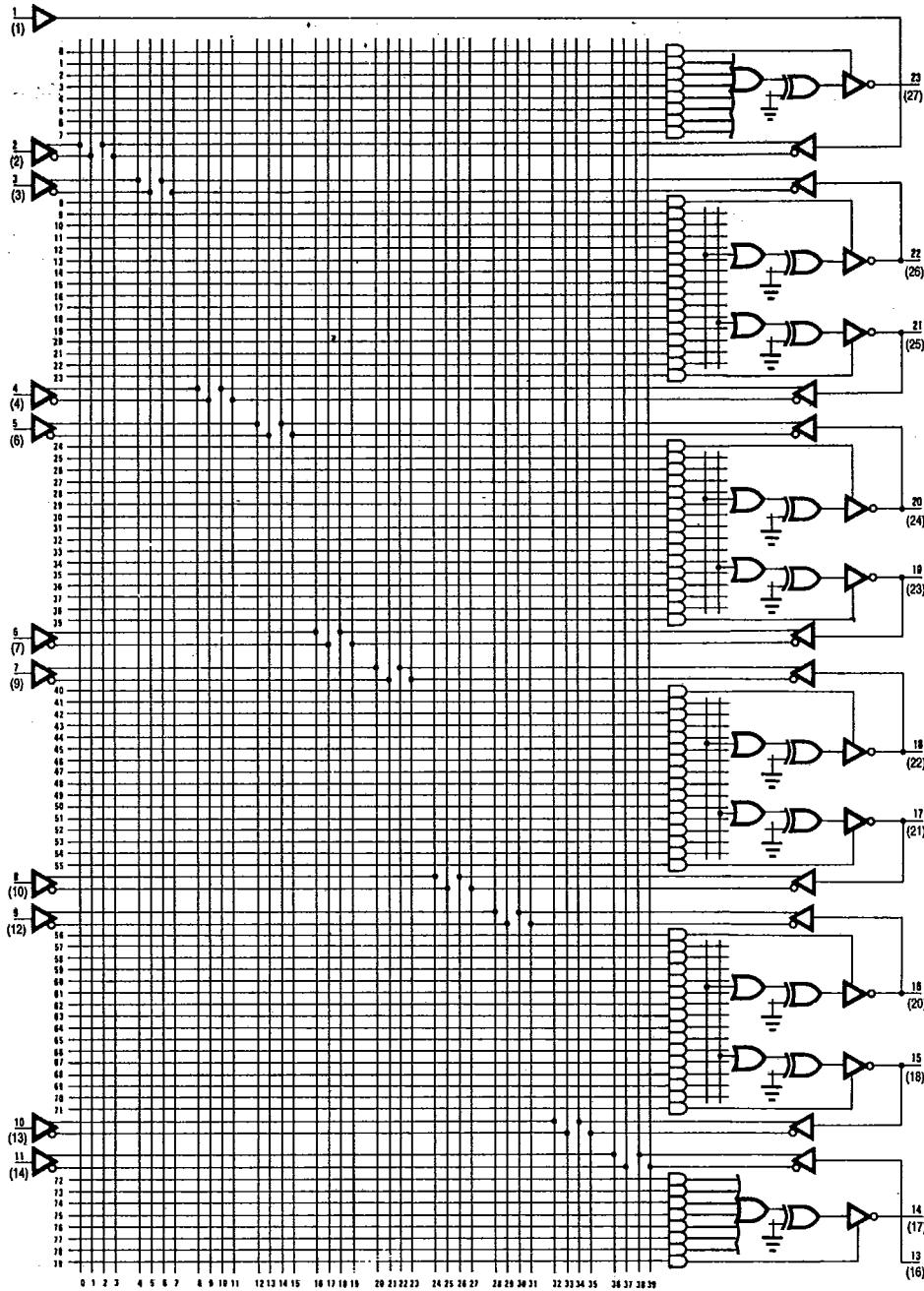
Power-Up Reset Waveform

(refer to page 5-164)

Schematic of Inputs and Outputs

(refer to page 5-164)

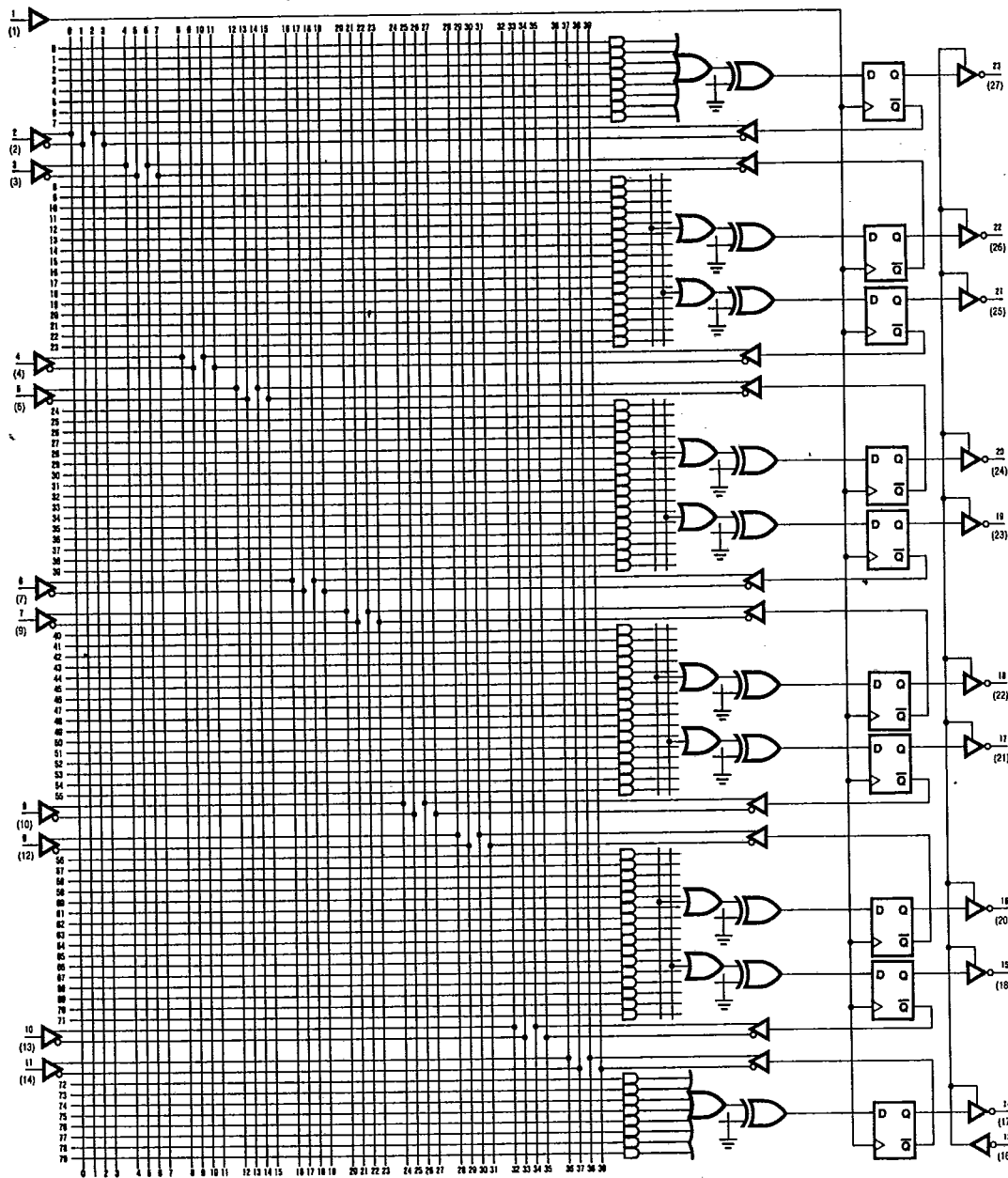
20S10



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20RS10



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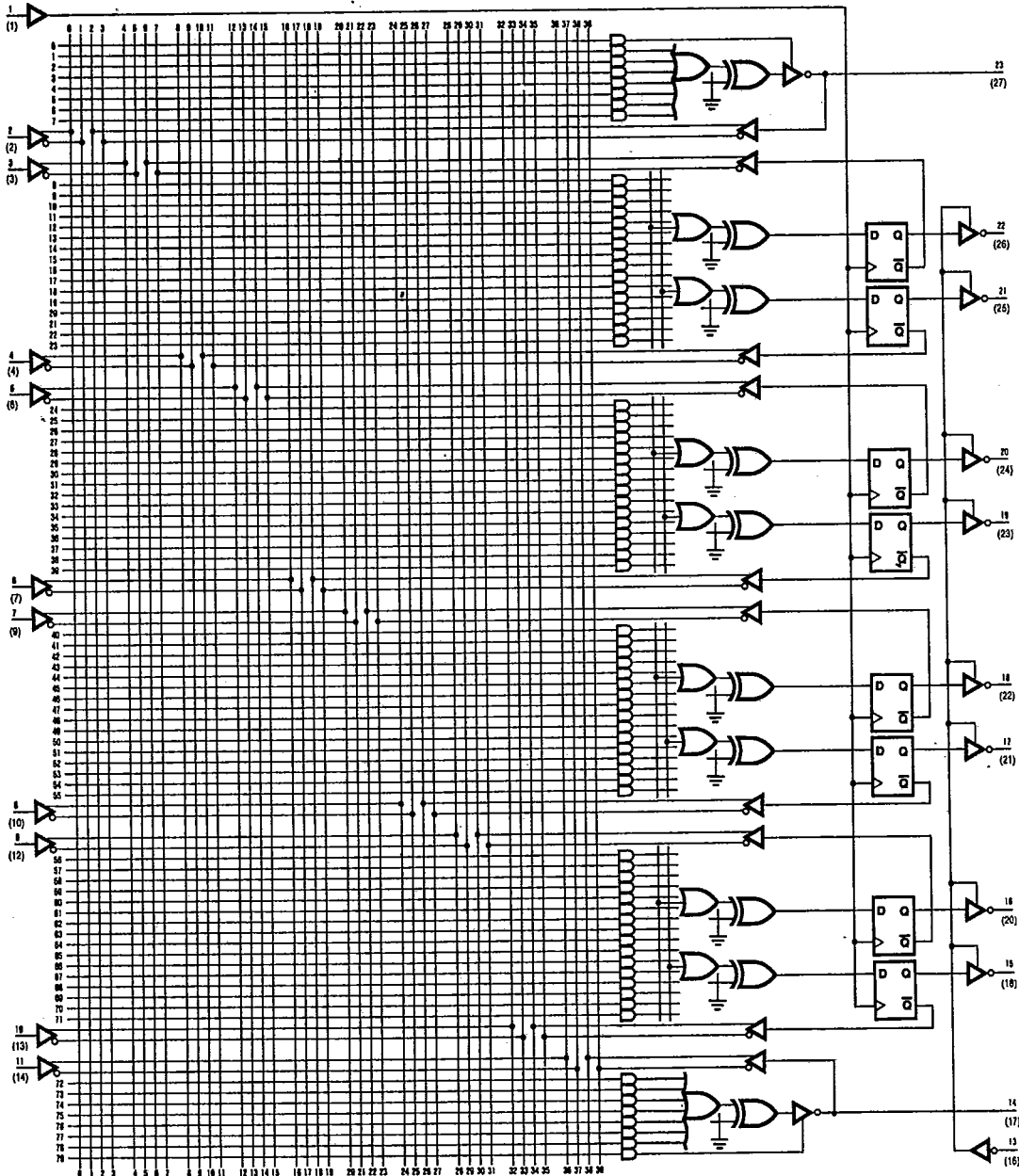
PAL20RS10 Series
20S10, 20RS10, 20RS8, 20RS4

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20RS8

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PAL20RS10 Series
20S10, 20RS10, 20RS8, 20RS4

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96D 27170 D

20RS4

