CY7C330

CMOS Programmable Synchronous State Machine

Features

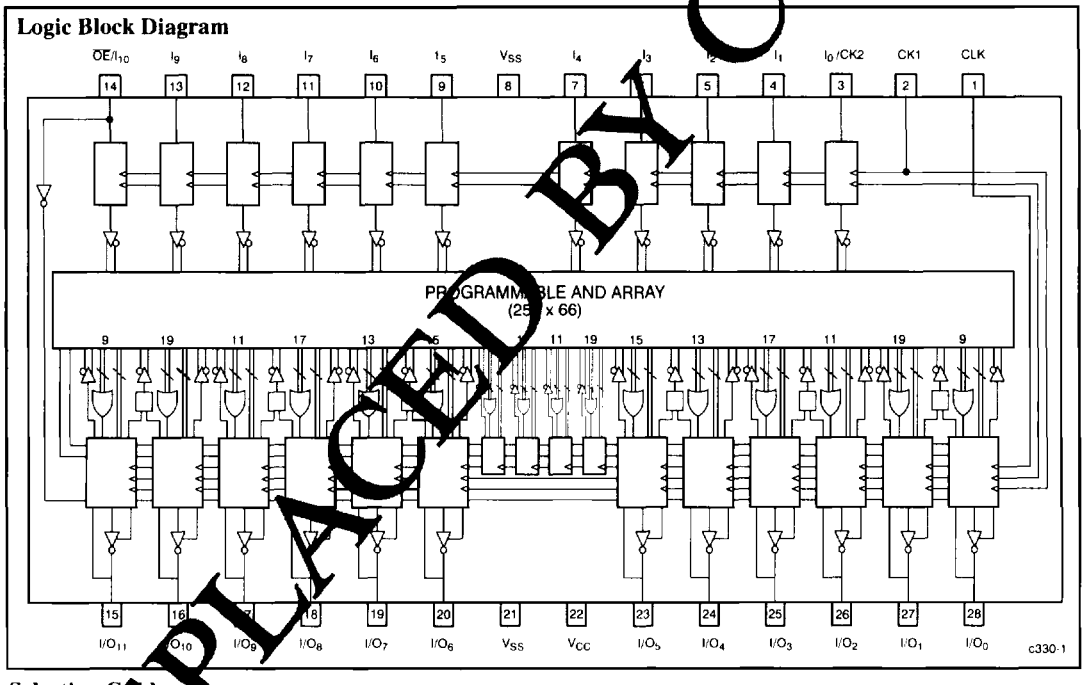
- Twelve I/O macrocells each having:
  - registered, three-state I/O pins
  - input register clock select multiplexer
  - feed back multiplexer
  - output enable (OE) multiplexer
- All twelve macrocell state registers can be hidden
- User-configurable state registers—JK, RS, T, or D
- One input multiplexer per pair of I/O macrocells allows I/O pin associated with a hidden macrocell state register to be saved for use as an input
- Four dedicated hidden registers
- Eleven dedicated, registered inputs
- Three separate clocks—two inputs, one output
- Common (pin 14–controlled) or product term–controlled output enable for each I/O pin
- 256 product terms—32 per pair of macrocells, variable distribution
- Global, synchronous, product term–controlled, state register set and reset—inputs to product term are clocked by input clock
- 66-MHz operation
  - 3-ns input set-up and 12-ns clock to output
  - 15-ns input register clock to state register clock
- Low power
  - 130 mA I_{CC}
- 28-pin, 300-mil DIP, LCC
- Erasable and reprogrammable

Functional Description

The CY7C330 is a high-performance, erasable, programmable, logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance synchronous state machines.

The unique architecture of the CY7C330, consisting of the user-configurable output macrocells, bidirectional I/O capability, input registers, and three separate clocks, enables the user to design high-performance state machines that can communicate either with each other or with microprocessors over bidirectional parallel buses of user-definable widths.

Logic Block Diagram



Selection Guide

		7C330–66	7C330–50	7C330–40	7C330–33	7C330–28
Maximum Operating Frequency, f_{MAX} (MHz)	Commercial	66.6	50.0		33.3	
	Military		50.0	40.0		28.5
Power Supply Current I_{CC1} (mA)	Commercial	140	130		130	
	Military		160	150		150

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