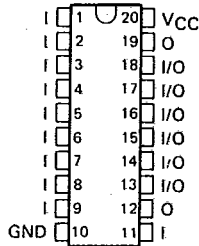


TIBPAL16L8-15M, TIBPAL16R4-15M, TIBPAL16R6-15M, TIBPAL16R8-15M
 TIBPAL16L8-12C TIBPAL16R4-12C TIBPAL16R6-12C TIBPAL16R8-12C
 HIGH-PERFORMANCE **IMPACT™** PAL® CIRCUITS

D3338, JANUARY 1986—REVISED AUGUST 1989

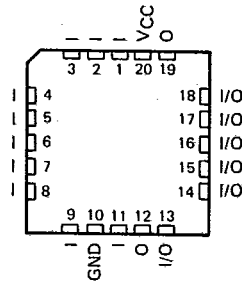
- High-Performance Operation
 Propagation Delay
 M Suffix . . . 15 ns Max
 C Suffix . . . 12 ns Max
- Functionally Equivalent, but Faster than
 PAL16L8B, PAL16R4B, PAL16R6B, and
 PAL16R8B
- Power-Up Clear on Registered Devices
 (All Registered Outputs are Set High but
 Voltage Levels at the Output Pins Go Low)
- Package Options Include Both Plastic and
 Ceramic Chip Carriers in Addition to Plastic
 and Ceramic DIPs
- Dependable Texas Instruments Quality and
 Reliability

TIBPAL16L8'
 M SUFFIX . . . J OR W PACKAGE
 C SUFFIX . . . J OR N PACKAGE
 (TOP VIEW)



T-46-13-47

TIBPAL16L8'
 M SUFFIX . . . FK PACKAGE
 C SUFFIX . . . FN PACKAGE
 (TOP VIEW)



Pin assignments in operating mode

| DEVICE | INPUTS | 3-STATE O OUTPUTS | REGISTERED Q OUTPUTS | I/O PORTS |
|---------|--------|----------------------|-------------------------|-----------|
| PAL16L8 | 10 | 2 | 0 | 6 |
| PAL16R4 | 8 | 0 | 4 (3-state) | 4 |
| PAL16R6 | 8 | 0 | 6 (3-state) | 2 |
| PAL16R8 | 8 | 0 | 8 (3-state) | 0 |

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These **IMPACT™** circuits combine the latest Advanced Low-Power Schottky[†] technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C. The TIBPAL16' C series is characterized for operation from 0°C to 75°C.

TEXAS INSTR (ASIC/MEMORY) 25E D

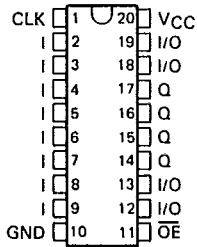
IMPACT is a trademark of Texas Instruments Incorporated.
 PAL is a registered trademark of Monolithic Memories, Inc.
[†]Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

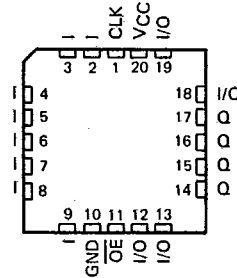


TIBPAL16R4-15M, TIBPAL16R6-15M, TIBPAL16R8-15M
TIBPAL16R4-12C, TIBPAL16R6-12C, TIBPAL16R8-12C
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

TIBPAL16R4'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)

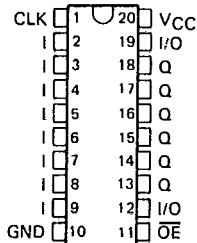


TIBPAL16R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)

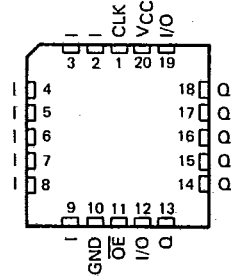


TEXAS INSTR (ASIC/MEMORY) 25E D

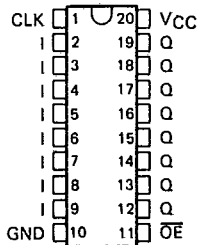
TIBPAL16R6'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



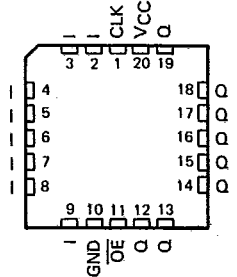
TIBPAL16R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)

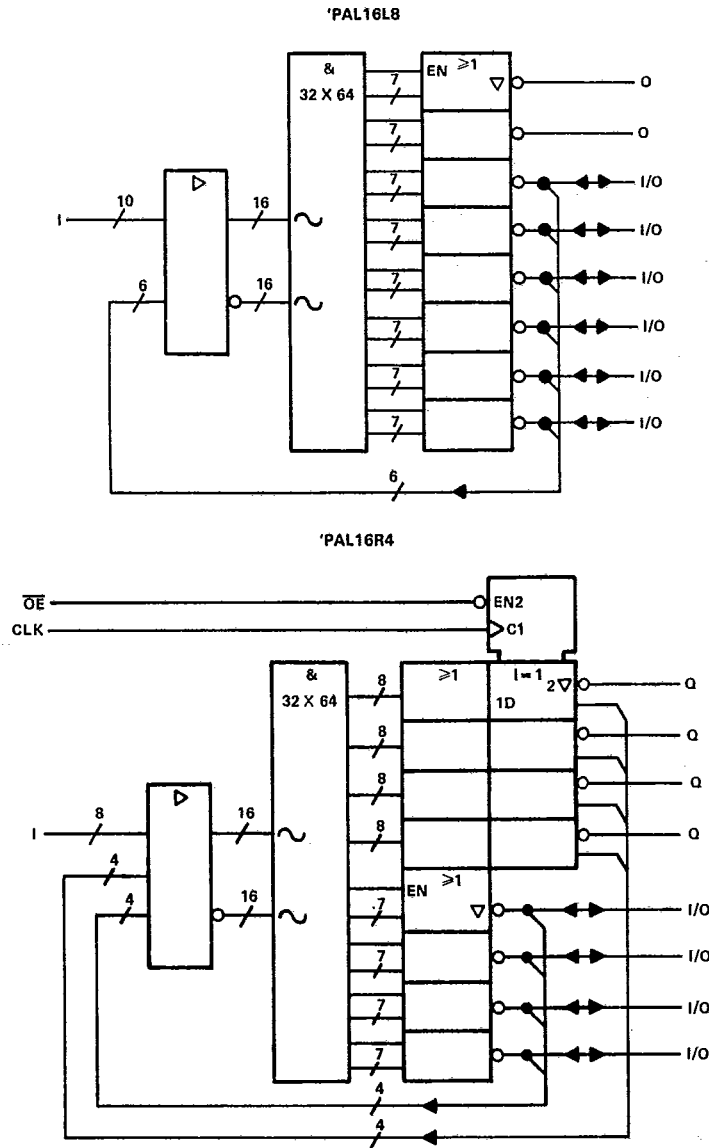


TIBPAL16R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

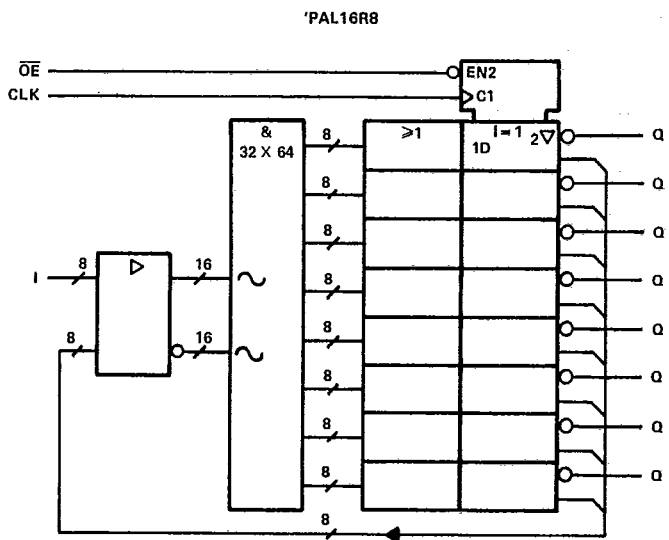
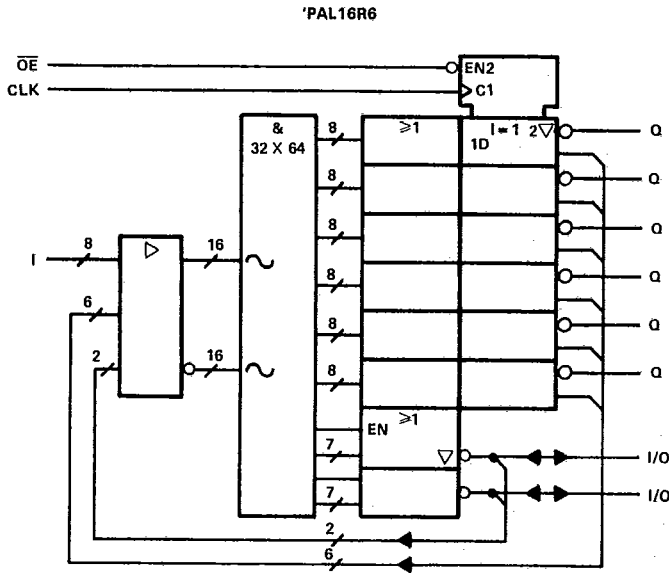
functional block diagrams (positive logic)



~ denotes fused inputs

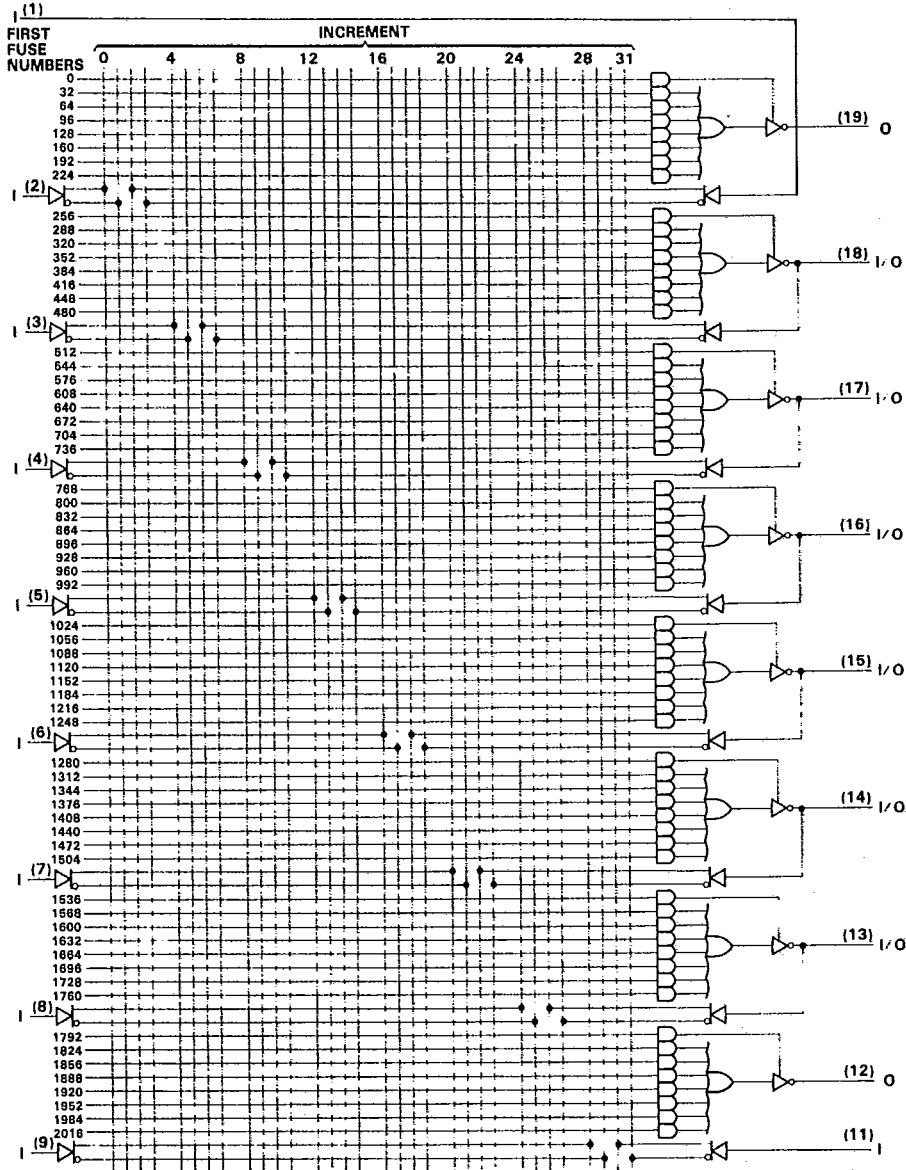
TIBPAL16R6-15M, TIBPAL16R6-12C, TIBPAL16R8-15M, TIBPAL16R8-12C
 HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D
 functional block diagrams (positive logic)



~ denotes fused inputs

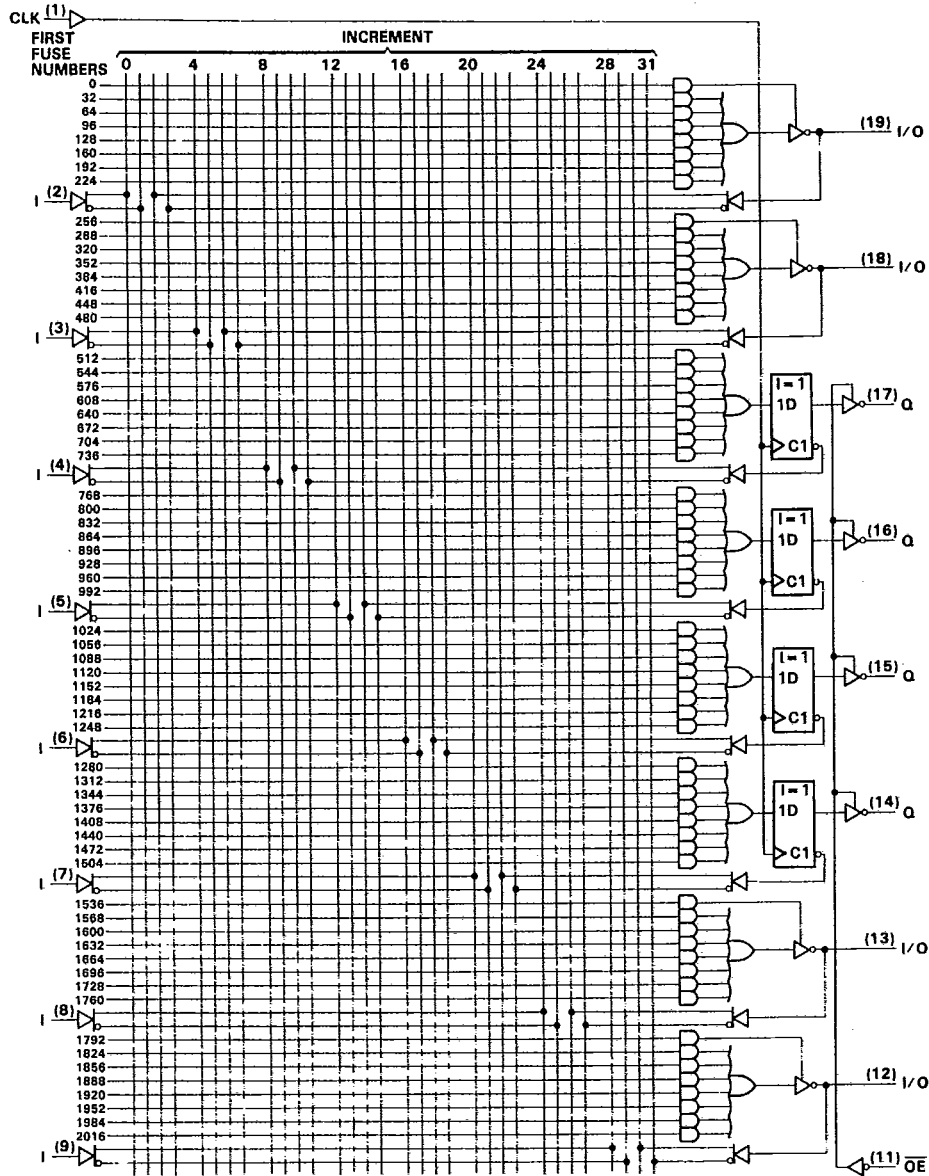
TEXAS INSTR (ASIC/MEMORY) 25E D



Fuse number = First Fuse number + Increment

TIBPAL16R4-15M, TIBPAL16R4-12C
HIGH-PERFORMANCE IMPACT™ PAL® CIRCUITS

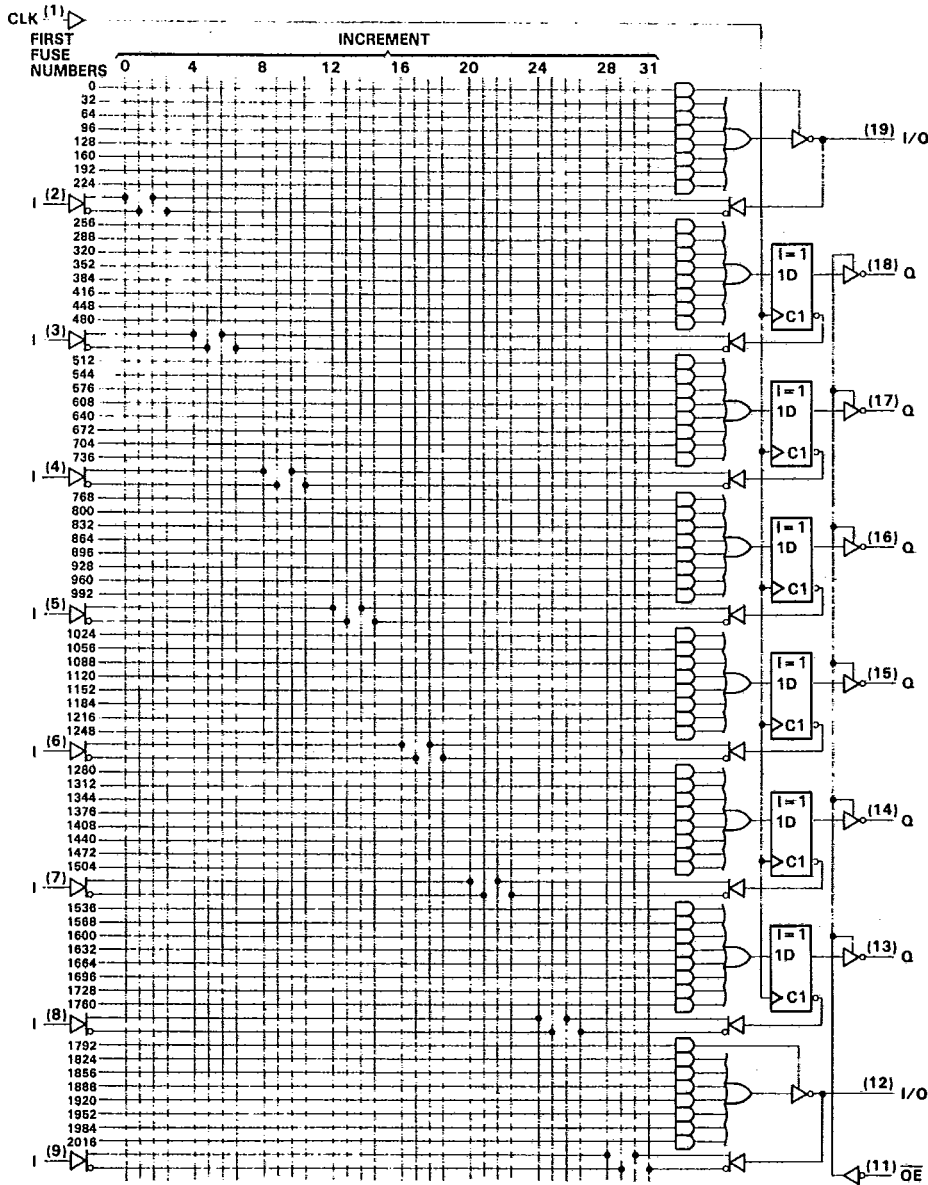
TEXAS INSTR (ASIC/MEMORY) 25E D



Fuse number = First Fuse number + Increment

TIBPAL16R6-15M, TIBPAL16R6-12C
HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

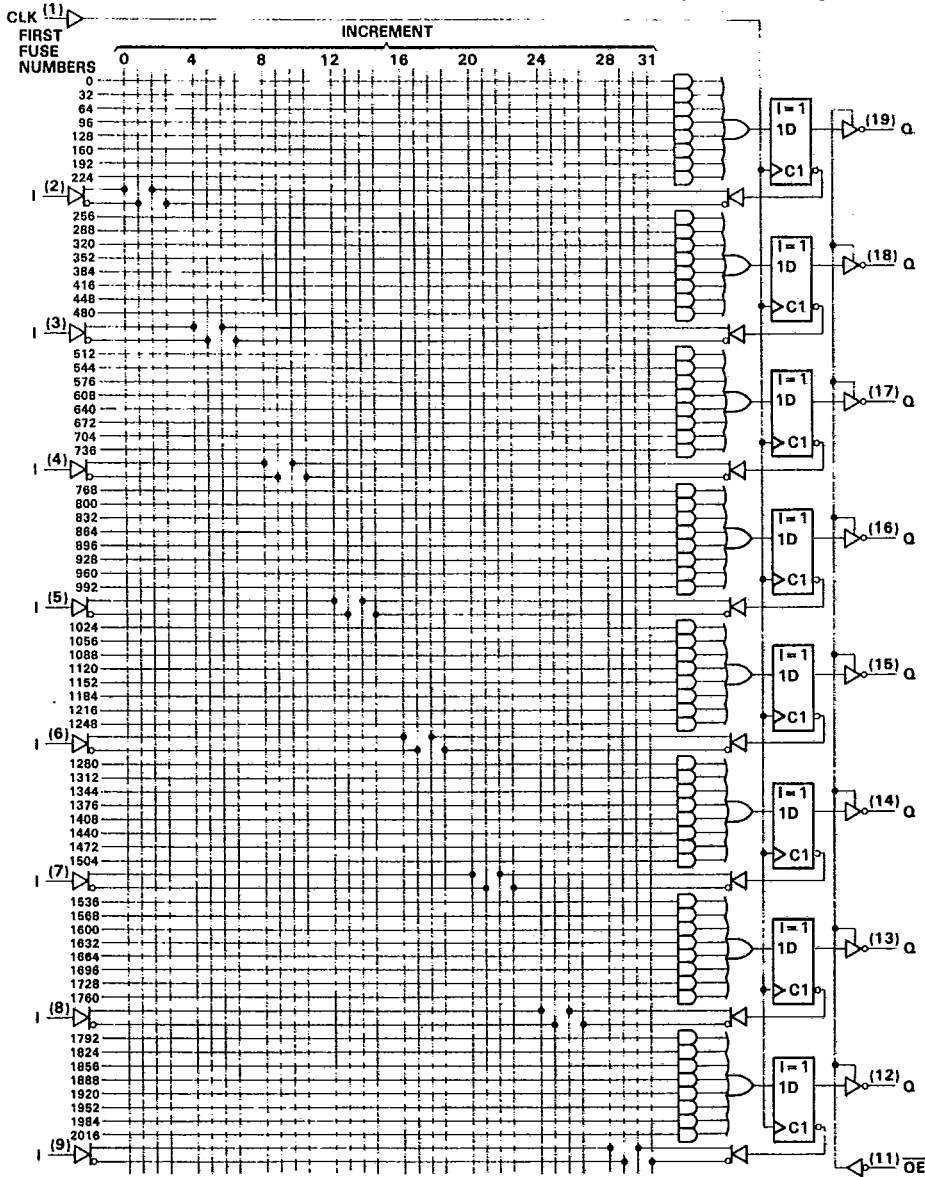
TEXAS INSTR (ASIC/MEMORY) 25E D



Fuse number = First Fuse number + Increment

TIBPAL16R8-15M, TIBPAL16R8-12C
HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D



Fuse number = First Fuse number + Increment

■ 8961725 0076206 9 ■ T-46-13.47

TIBPAL16L8-15M, TIBPAL16R4-15M, TIBPAL16R6-15M, TIBPAL16R8-15M
HIGH-PERFORMANCE IMPACT™ PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V _{CC} (see Note 1) | 7 V |
| Input voltage (see Note 1) | 5.5 V |
| Voltage applied to a disabled output (see Note 1) | 5.5 V |
| Operating free-air temperature | -55°C to 125°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions (see Note 2)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--------------------|---|------|-----|-----|------|
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 5.5 | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{OH} | High-level output current | | | -2 | mA |
| I _{OL} | Low-level output current | | | 12 | mA |
| f _{clock} | Clock frequency | 0 | | 50 | MHz |
| t _w | Pulse duration, clock (see Note 2) | High | 9 | | ns |
| | | Low | 10 | | |
| t _{su} | Setup time, input or feedback before CLK† | 15 | | | ns |
| t _h | Hold time, input or feedback after CLK† | 0 | | | ns |
| T _A | Operating free-air temperature | -55 | | 125 | °C |

NOTE 2: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-------------------|---|---|------|-------|------|
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.5 | V |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -2 mA | 2.4 | 3.3 | | V |
| V _{OL} | V _{CC} = 4.5 V, I _{OL} = 12 mA | | 0.35 | 0.5 | V |
| I _{OZH} | Outputs I/O ports | V _{CC} = 5.5 V, V _O = 2.7 V | | 20 | μA |
| | | | | 100 | |
| I _{OZL} | Outputs I/O ports | V _{CC} = 5.5 V, V _O = 0.4 V | | -20 | μA |
| | | | | -250 | |
| I _I | V _{CC} = 5.5 V, V _I = 5.5 V | Pin 1, 11 | | 0.2 | mA |
| | | All others | | 0.1 | |
| I _{IH} | V _{CC} = 5.5 V, V _I = 2.7 V | Pin 1, 11 | | 50 | μA |
| | | I/O ports | | 100 | |
| | | All others | | 20 | |
| I _{IL} | V _{CC} = 5.5 V, V _I = 0.4 V | I/O ports | | -0.25 | mA |
| | | All others | | -0.2 | |
| I _{OS} ‡ | V _{CC} = 5.5 V, V _O = 0.5 V | -30 | | -250 | mA |
| I _{CC} | V _{CC} = 5.5 V, V _I = 0, Outputs open | | 170 | 220 | mA |

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

8961725 0076207 0 T-46-13-47

TIBPAL16L8-15M, TIBPAL16R4-15M, TIBPAL16R6-15M, TIBPAL16R8-15M
HIGH-PERFORMANCE IMPACT™ PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

| PARAMETER | FROM | TO | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|----------------------|--------|--------|--|-----|------|-----|------|
| f_{max}^{\ddagger} | | | | 50 | | | MHz |
| t_{pd}^{\ddagger} | I, I/O | O, I/O | R1 = 390 Ω, R2 = 750 Ω, See Figure 1 | | 8 | 15 | ns |
| t_{pd}^{\ddagger} | CLK† | Q | | | 7 | 12 | ns |
| t_{en}^{\ddagger} | OEI | Q | | | 8 | 12 | ns |
| t_{dis}^{\ddagger} | OEt | Q | | | 7 | 12 | ns |
| t_{en}^{\ddagger} | I, I/O | O, I/O | | | 8 | 15 | ns |
| t_{dis}^{\ddagger} | I, I/O | O, I/O | | | 8 | 15 | ns |

†All typical values are at VCC = 5 V, TA 25°C.

‡Maximum operating frequency and propagation delay are specified for the basic building block. When using feedback, limits must be calculated accordingly.

8961725 0076208 2 T-46-13-47

TIBPAL16L8-12C, TIBPAL16R4-12C, TIBPAL16R6-12C, TIBPAL16R8-12C
HIGH-PERFORMANCE IMPACT™ PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V _{CC} (see Note 1) | 7 V |
| Input voltage (see Note 1) | 5.5 V |
| Voltage applied to a disabled output (see Note 1) | 5.5 V |
| Operating free-air temperature range | 0°C to 75°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions (see Note 2)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--------------------|---|------|-----|------|------|
| V _{CC} | Supply voltage | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | 2 | | 5.5 | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{OH} | High-level output current | | | -3.2 | mA |
| I _{OL} | Low-level output current | | | 24 | mA |
| f _{clock} | Clock frequency | 0 | | 62 | MHz |
| t _w | Pulse duration, clock (see Note 2) | High | 7 | | ns |
| | | Low | 8 | | |
| t _{su} | Setup time, input or feedback before CLK† | 10 | | | ns |
| t _h | Hold time, input or feedback after CLK† | 0 | | | ns |
| T _A | Operating free-air temperature | 0 | | 75 | °C |

NOTE 2: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|--|------------|------|------|------|
| V _{IK} | V _{CC} = 4.75 V, I _I = -18 mA | | | -1.5 | V |
| V _{OH} | V _{CC} = 4.75 V, I _{OH} = -3.2 mA | 2.4 | 3.3 | | V |
| V _{OL} | V _{CC} = 4.75 V, I _{OL} = 24 mA | 0.35 | 0.5 | | V |
| I _{OZH} | Outputs I/O ports V _{CC} = 5.25 V, V _O = 2.7 V | | 20 | | μA |
| | | | 100 | | |
| I _{OZL} | Outputs I/O ports V _{CC} = 5.25 V, V _O = 0.4 V | | -20 | | μA |
| | | | -250 | | |
| I _I | V _{CC} = 5.25 V, V _I = 5.5 V | Pin 1, 11 | 0.1 | | mA |
| | | All others | 0.1 | | |
| I _{IH} | V _{CC} = 5.25 V, V _I = 2.7 V | Pin 1, 11 | 20 | | μA |
| | | All others | 20 | | |
| I _{IL} | V _{CC} = 5.25 V, V _I = 0.4 V | | | -0.2 | mA |
| I _O ‡ | V _{CC} = 5.25 V, V _O = 0.5 V | -30 | | -125 | mA |
| I _{CC} | V _{CC} = 5.25 V, V _I = 0, Outputs open | | 170 | 200 | mA |

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TIBPAL16L8-12C, TIBPAL16R4-12C, TIBPAL16R6-12C, TIBPAL16R8-12C
HIGH-PERFORMANCE IMPACT™ PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

| PARAMETER | FROM | TO | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|----------------------|--------|--------|--|-----|------|-----|------|
| f_{max}^{\ddagger} | | | | 62 | | | MHz |
| t_{pd}^{\ddagger} | I, I/O | O, I/O | R1 = 500 Ω , R2 = 500 Ω , See Figure 1 | | 8 | 12 | ns |
| t_{pd} | CLK1 | Q | | | 7 | 10 | ns |
| t_{en} | OE1 | Q | | | 8 | 10 | ns |
| t_{dis} | OE1 | Q | | | 7 | 10 | ns |
| t_{en} | I, I/O | O, I/O | | | 8 | 12 | ns |
| t_{dis} | I, I/O | O, I/O | | | 8 | 12 | ns |

†All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

‡Maximum operating frequency and propagation delay are specified for the basic building block. When using feedback, limits must be calculated accordingly.

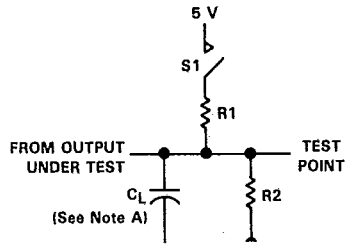
programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

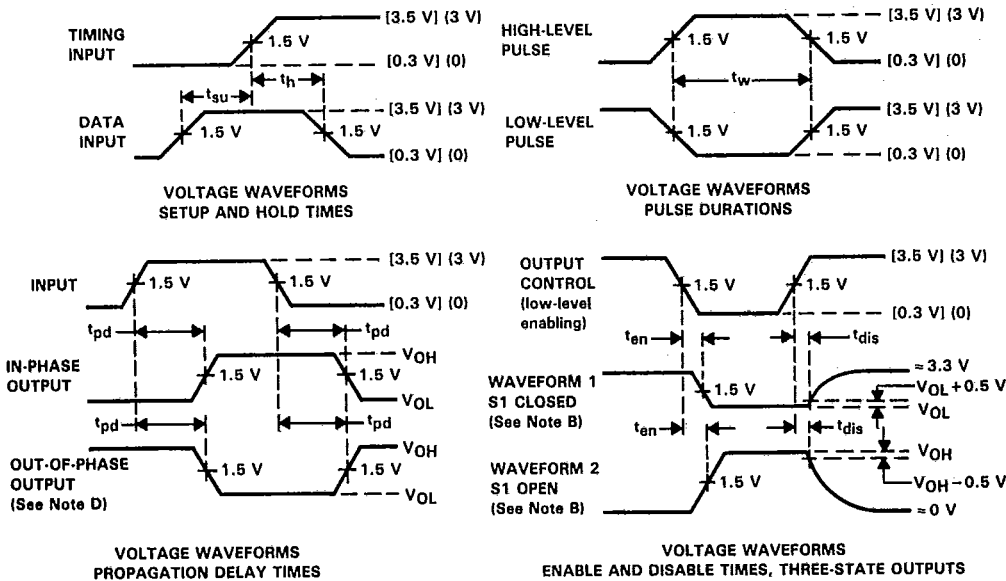
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5666.

TIBPAL16L8-15M, TIBPAL16R4-15M, TIBPAL16R6-15M, TIBPAL16R8-15M
 TIBPAL16L8-12C, TIBPAL16R4-12C, TIBPAL16R6-12C, TIBPAL16R8-12C
 HIGH-PERFORMANCE IMPACT™ PAL® CIRCUITS

PARAMETER MEASUREMENT INFORMATION



TEXAS INSTR (ASIC/MEMORY) 25E D
 LOAD CIRCUIT FOR
 THREE-STATE OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control.
 C. All input pulses have the following characteristics: For M suffix, use voltage levels indicated in parentheses (), $PRR \leq 10$ MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [], $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 E. Equivalent loads may be used for testing.

FIGURE 1