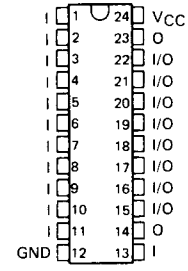
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT*™ *PAL*® CIRCUITS

D2920, OCTOBER 1985—REVISED DECEMBER 1987

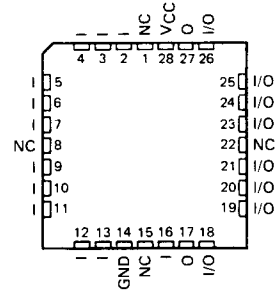
- **High Performance . . . 35 MHz Min**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L10	12	2	0	8
'PAL20X4	10	0	4 (3-state buffers)	6
'PAL20X8	10	0	8 (3-state buffers)	2
'PAL20X10	10	0	10 (3-state buffers)	0

TIBPAL20L10'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L10'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

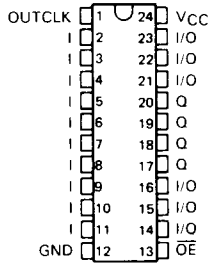
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the registered outputs are set to a low level during power-up. In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

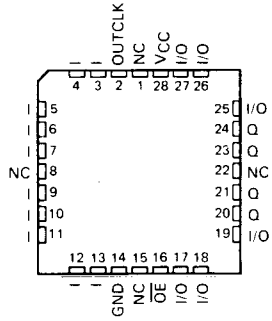
The PAL20' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL20' C series is characterized for operation from 0°C to 75°C.

IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

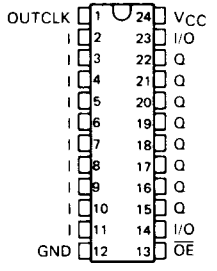
TIBPAL20X4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



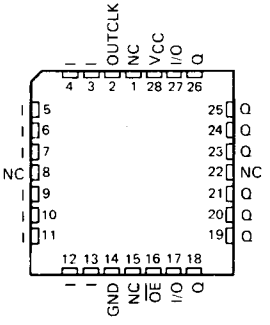
TIBPAL20X4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



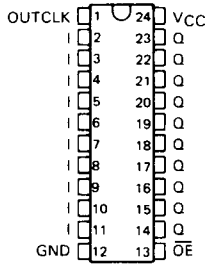
TIBPAL20X8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



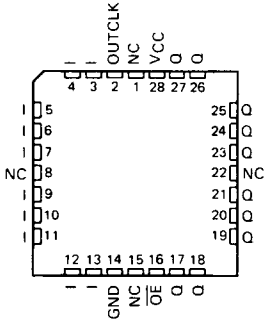
TIBPAL20X8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20X10'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20X10'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



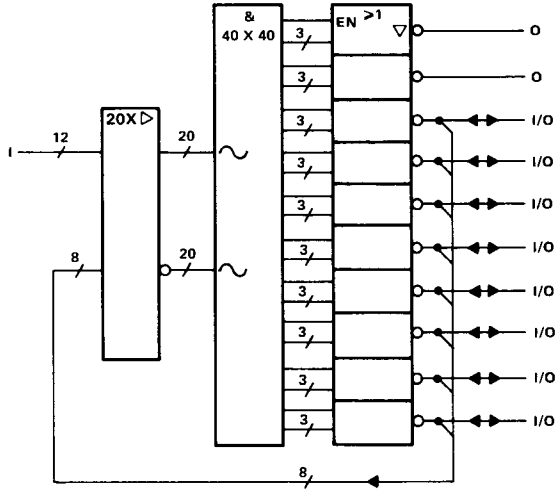
NC—No internal connection

Pin assignments in operating mode

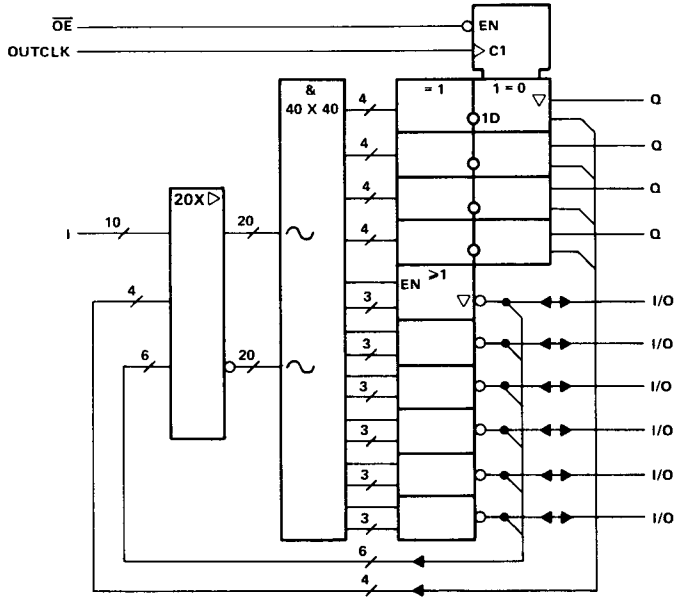
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

functional block diagrams (positive logic)

'PAL20L10



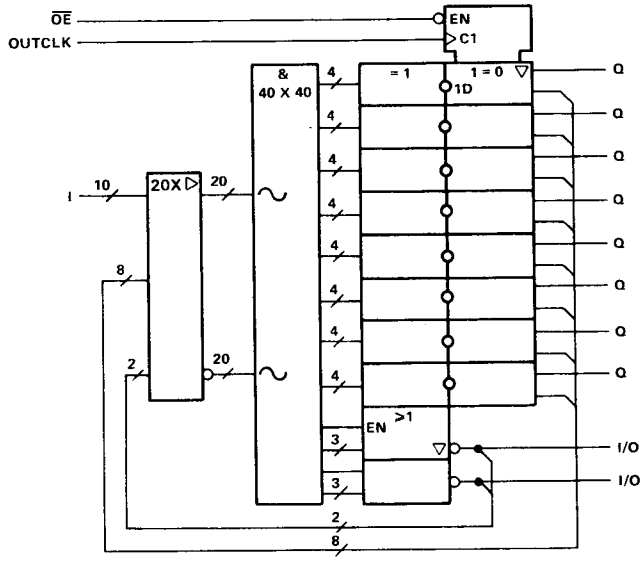
'PAL20X4



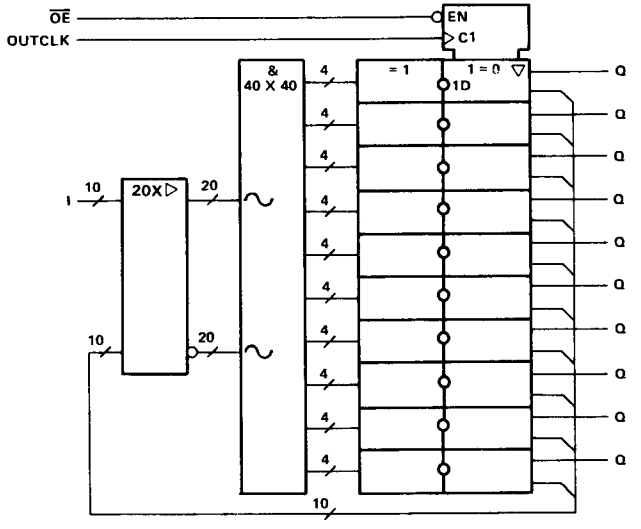
~ denotes fused inputs

functional block diagrams (positive logic)

'PAL20X8

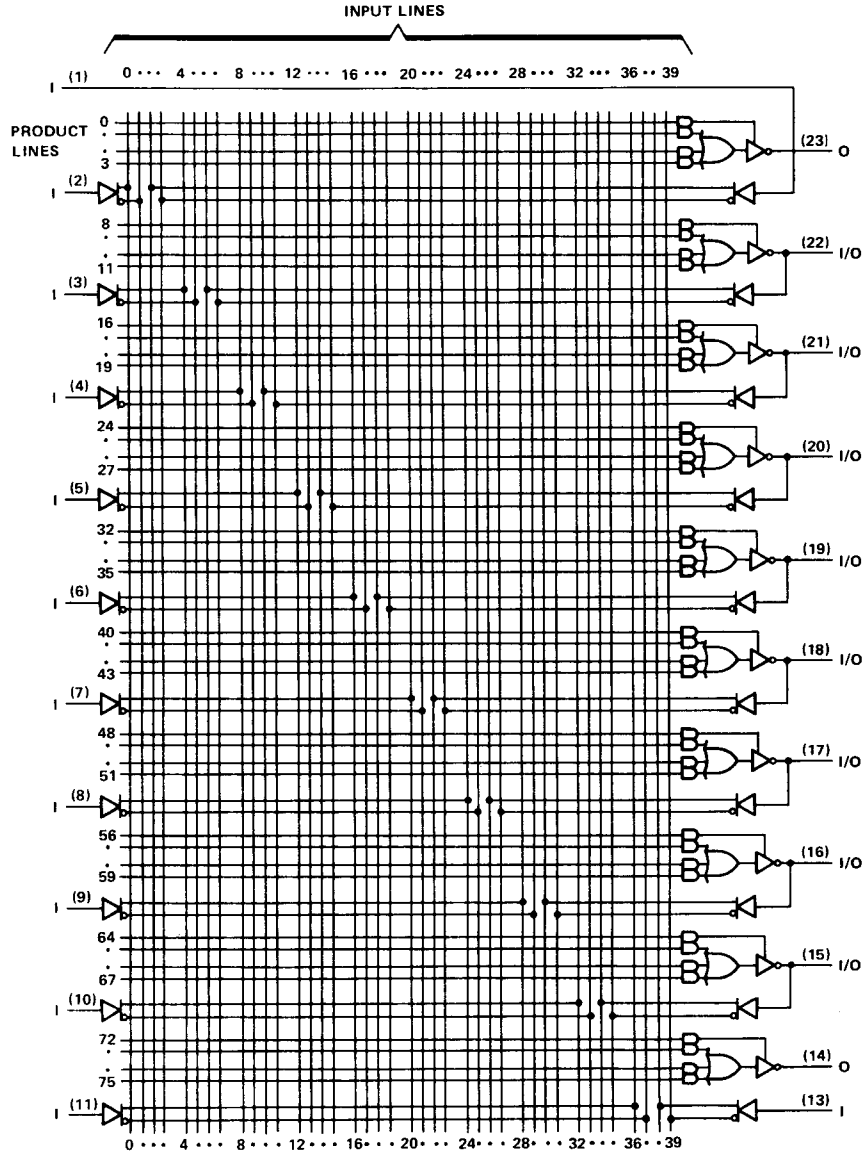


'PAL20X10



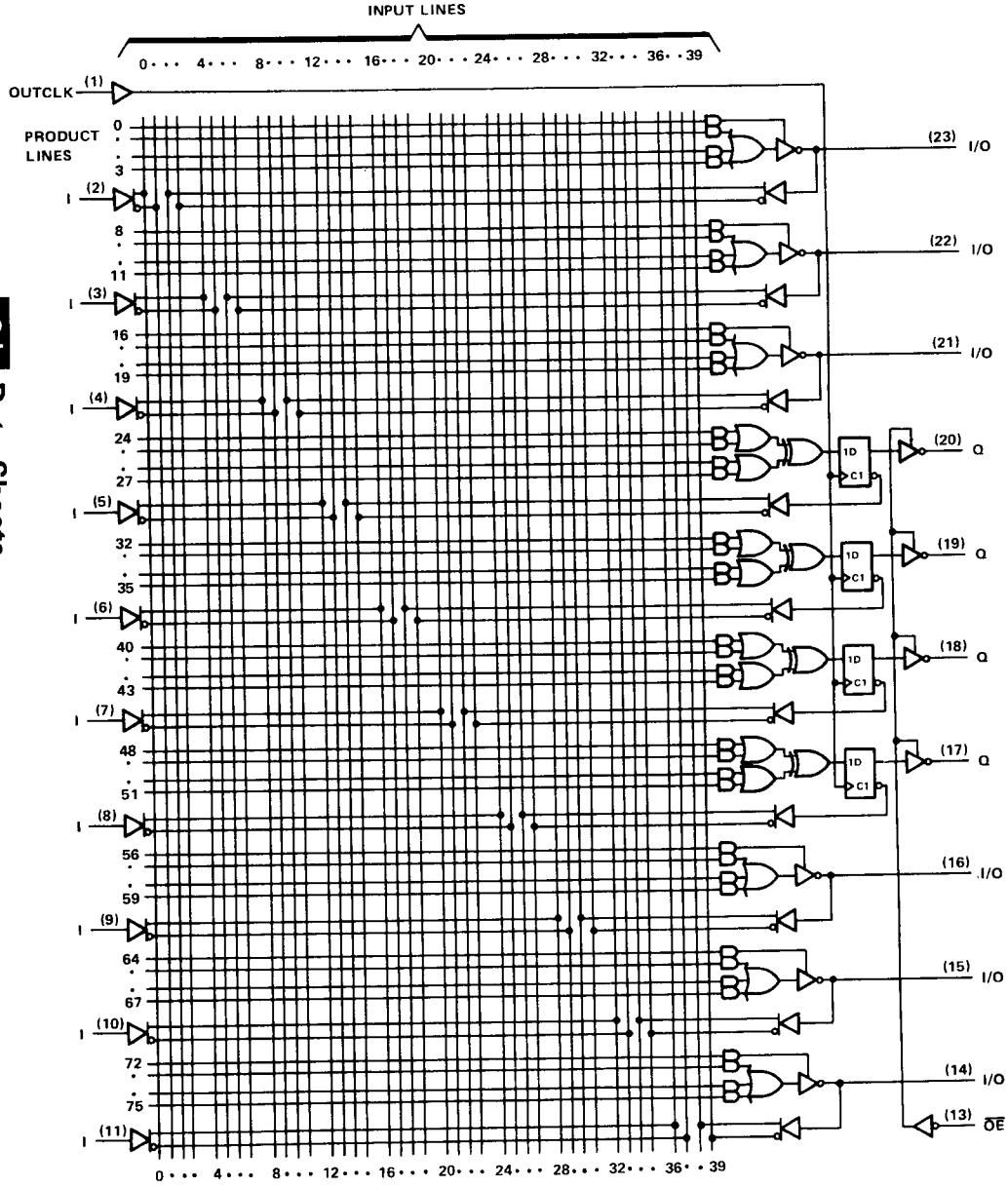
∼ denotes fused inputs

logic diagram (positive logic)



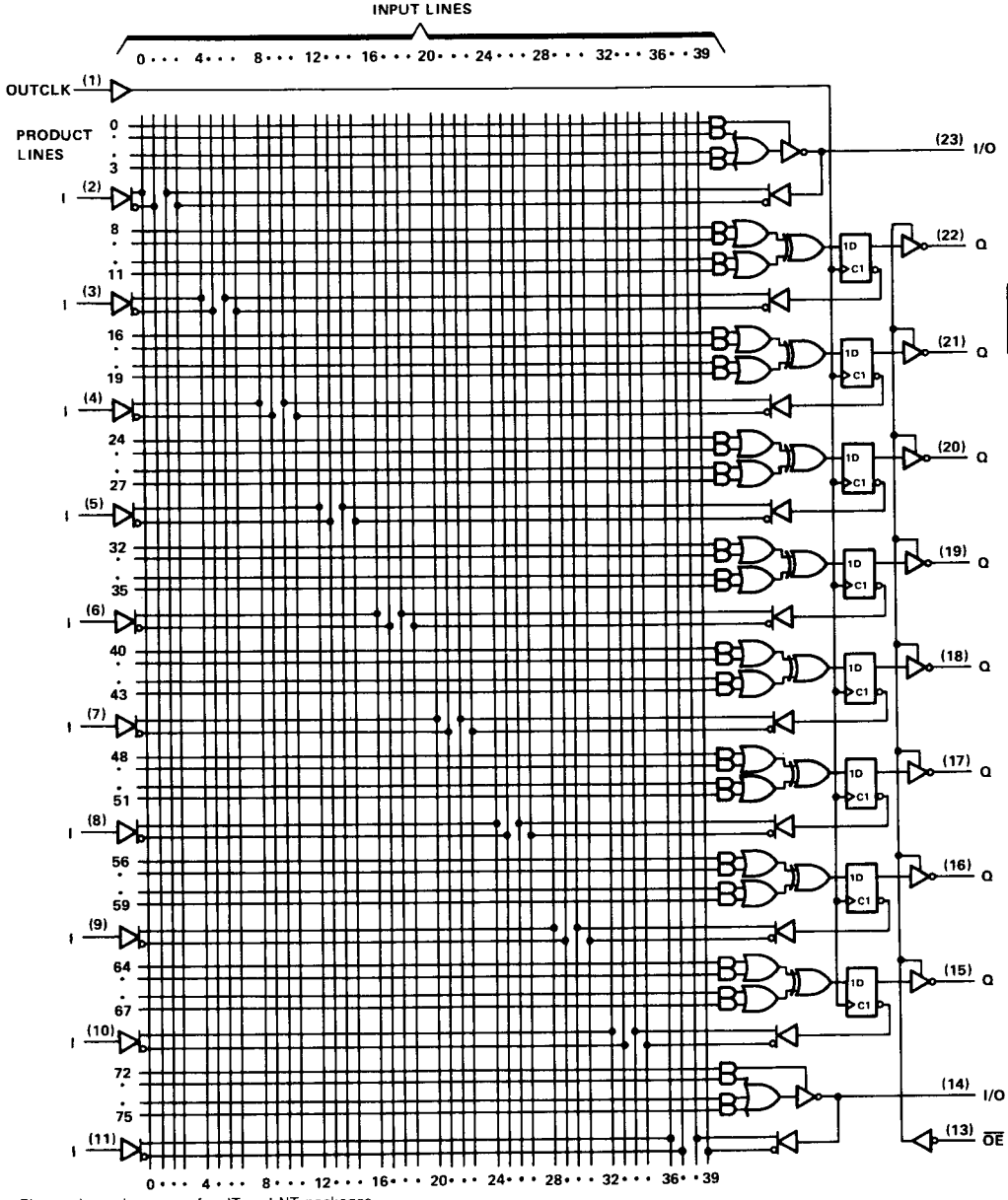
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



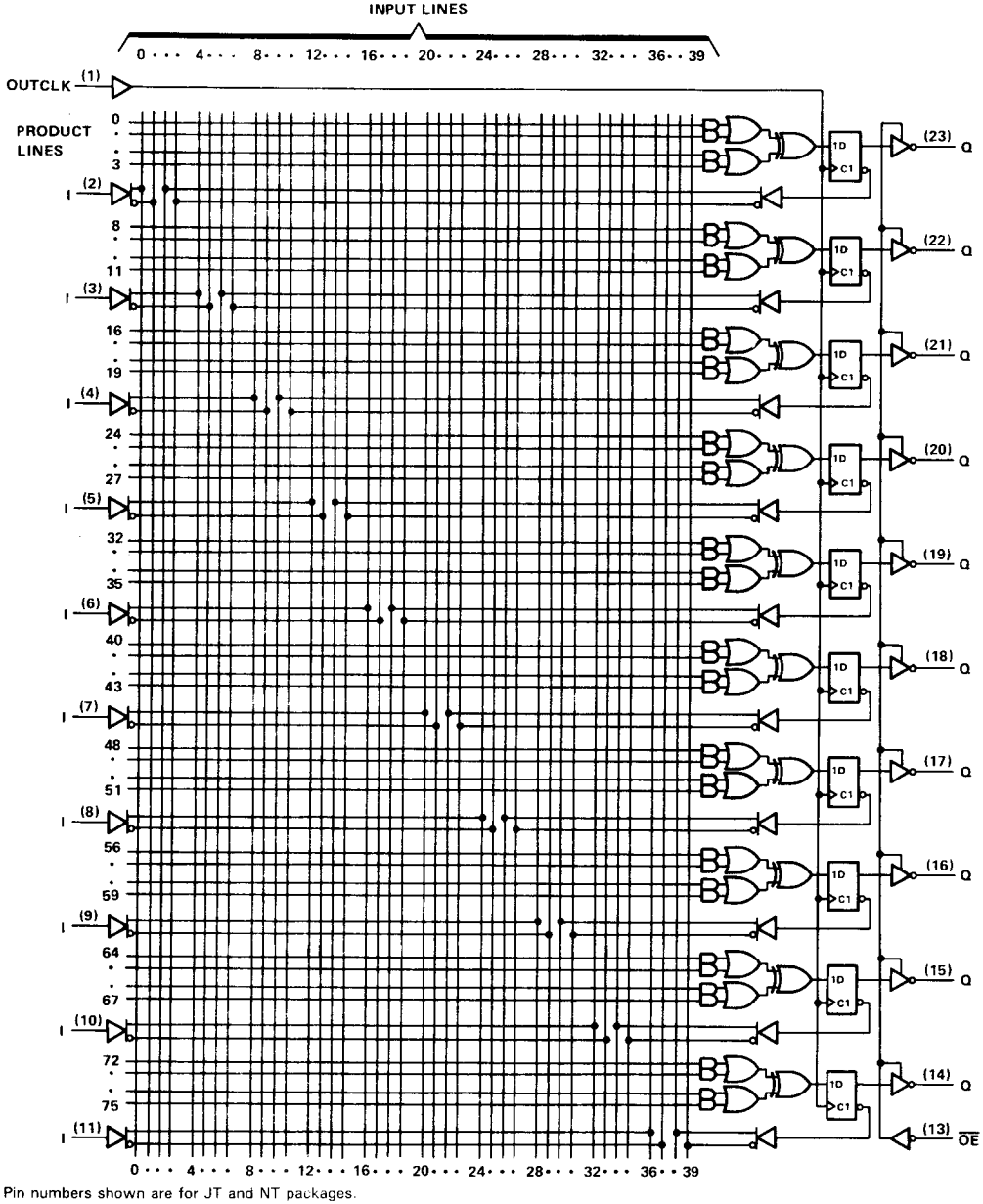
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			−25M			−20C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		35	MHz
t_w	Pulse duration, clock, see Note 2	High	15			10			ns
		Low	20			14			ns
t_{su}	Setup time, input or feedback before OUTCLK↑		25			20			ns
t_h	Hold time, input or feedback after OUTCLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

NOTE 2: The high and low clock pulse durations cannot both be at the minimum values specified. Their sum must be equal to or greater than the minimum clock period, which is the reciprocal of the maximum recommended clock frequency.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	−25M			−20C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX, V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}§		V_{CC} = 5 V, V_O = 0	−30		−130	−30		−130	mA
I_{CC}	'20X4, '20X8, '20X10	V_{CC} = MAX, V_I = 0		120	180		120	180	mA
	'20L10			120	165		120	165	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	−25M			−20C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				25			35			MHz
t_{pd}	I, I/O	O, I/O			12	25		12	20	ns
t_{pd}	OUTCLK↑	Q	R1 = 200 Ω,		10	20		10	15	ns
t_{en}	$\overline{OE}$	Q	R2 = 390 Ω,		7	20		7	15	ns
t_{dis}	$\overline{OE}$↑	Q	C_L = 50 pF		7	20		7	15	ns
t_{en}	I, I/O	O, I/O			15	25		15	20	ns
t_{dis}	I, I/O	O, I/O			15	25		15	20	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

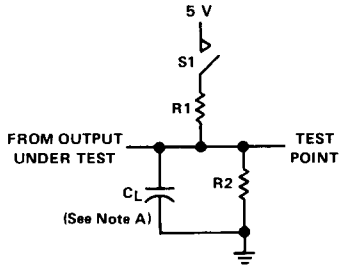
programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

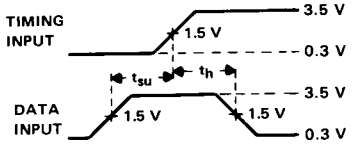
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5762.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

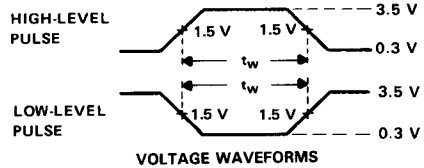
PARAMETER MEASUREMENT INFORMATION



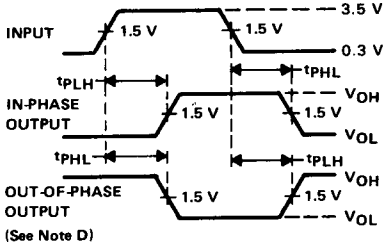
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



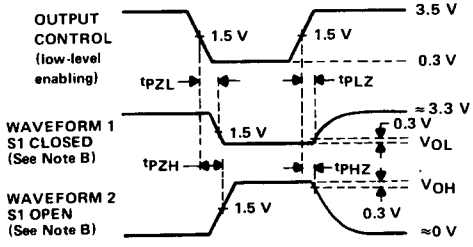
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



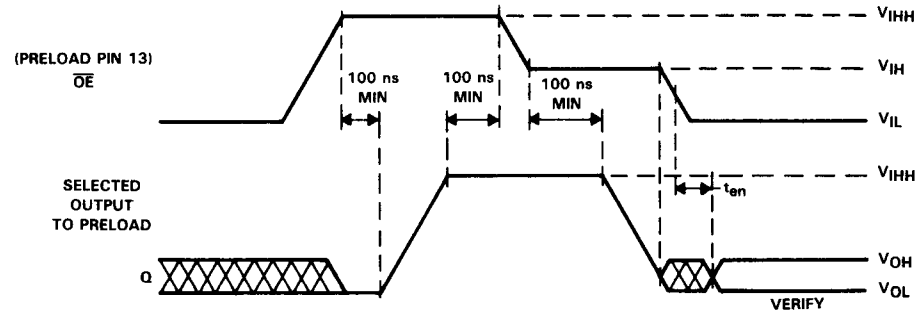
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

preload procedures

preload procedure for registered outputs

Step 1 With V_{CC} at 5 volts, raise Pin 13 ($\overline{OE}$) to V_{IHH} to disable the outputs and clear the registers (output goes low). Since the outputs are low, only high levels need be preloaded.
Step 2 Raise the selected output to be preloaded high to V_{IHH}.
Step 3 Lower Pin 13 to V_{IH}.
Step 4 Remove the voltages applied to the outputs. (At least a 100-ns wait is required between step 3 and step 4)
Step 5 Lower Pin 13 to V_{IL} to verify preload.



PRELOAD WAVEFORMS

security fuse programming

SECURITY FUSE PROGRAMMING WAVEFORMS

NOTE: Pin numbers shown apply only for the DIP package. If a chip carrier socket adaptor is not used, pin numbers must be changed accordingly.