

# TIFPLA839C, TIFPLA840C

## 14 × 32 × 6 FIELD-PROGRAMMABLE LOGIC ARRAYS

D2708, JUNE 1984—REVISED AUGUST 1989

- Input-to-Output Propagation Delay . . . 10 ns Typical
- 24-Pin, 300-mil Slim Line Packages
- Power Dissipation . . . 650 mW Typical
- Programmable Output Polarity

### LOGIC FUNCTION

$f(i) = P_0 + P_1 \dots P_{31}$  for polarity link intact

$f(i) = \overline{P_0} * \overline{P_1} * \dots * \overline{P_{31}}$  for polarity link open

where P<sub>0</sub> through P<sub>31</sub> are product terms

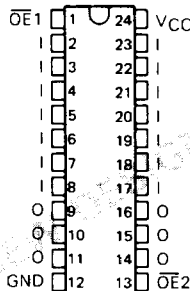
### description

The 'FPLA839 (3-state outputs) and the 'FPLA840 (open-collector outputs) are TTL field-programmable logic arrays containing 32 product terms (AND terms) and six sum terms (OR terms). Each of the sum-of-products output functions can be programmed either high true or low true. The true condition of each output function is activated by the programmed logical minterms of 14 input variables. The outputs are controlled by two chip-enable pins to allow output inhibit and expansion of terms.

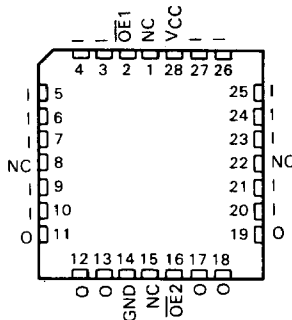
These devices provide high-speed data-path logic replacement where several conventional SSI functions can be designed into a single package.

The 'FPLA839C and 'FPLA840C are characterized for operation from 0°C to 70°C.

### JT OR NT PACKAGE (TOP VIEW)



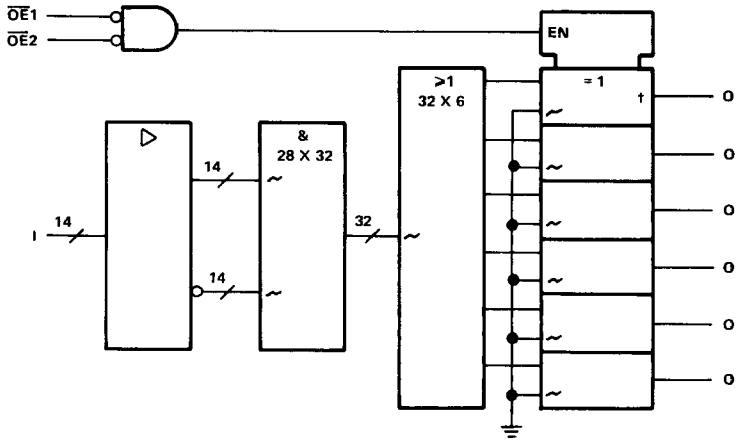
### FN PACKAGE (TOP VIEW)



Pin assignments in operating mode (pin 1 is less positive than V<sub>IHH</sub>)

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functional block diagram (positive logic)



~denotes fused inputs.  
 †FPLA839 has 3-state ( $\nabla$ ) outputs; FPLA840 has open-collector ( $\diamond$ ) outputs.

**absolute maximum ratings**

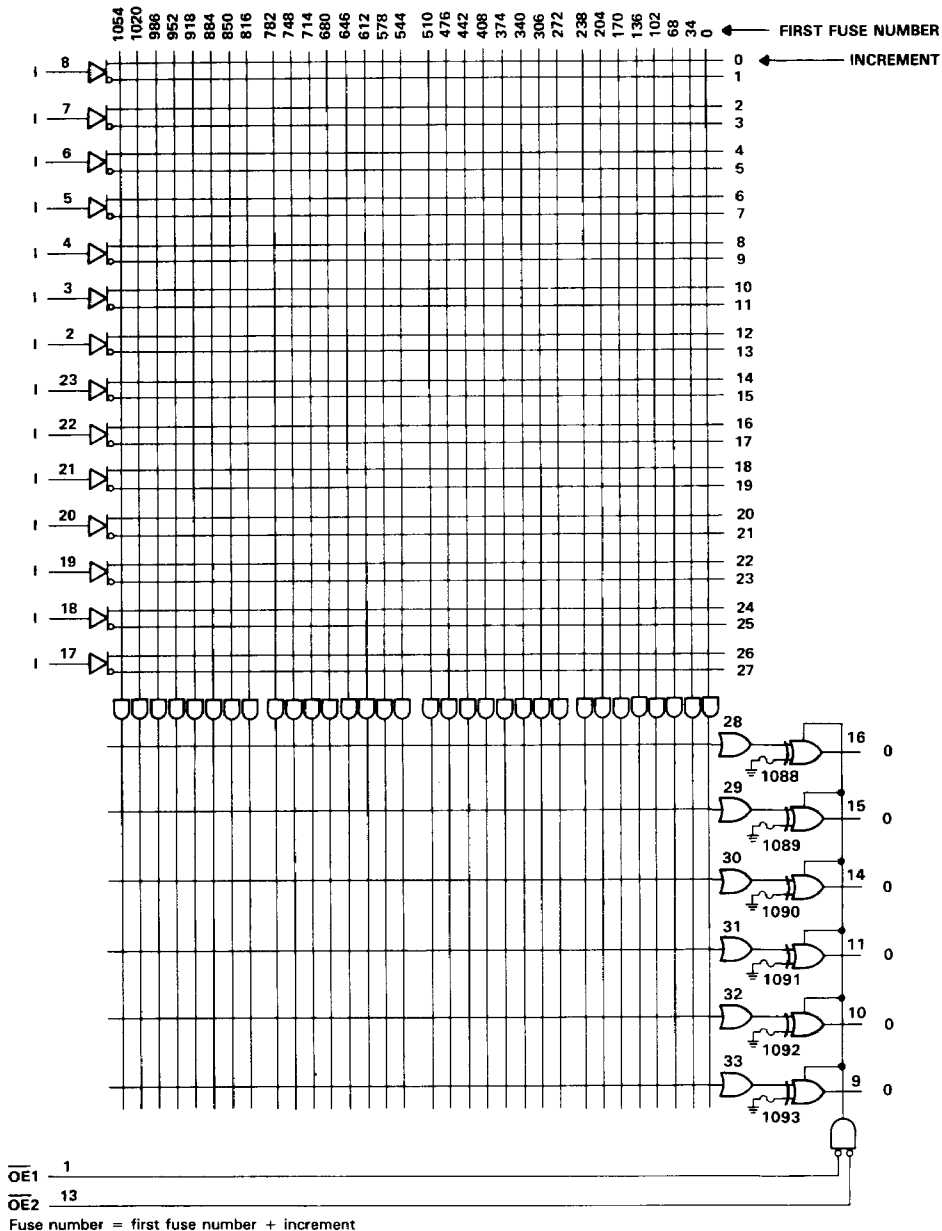
Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage (see Note 1) .....	5.5 V
Off-state output voltage (see Note 1) .....	5.5 V
Operating free-air temperature .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

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logic diagram



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**recommended operating conditions**

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
High-level output voltage, $V_{OH}$		'FPLA840	5.5	V
High-level output current, $I_{OH}$		'FPLA839	-3.2	mA
Low-level output current, $I_{OL}$			24	mA
Operating free-air temperature, $T_A$	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.5	V
$I_{OH}$	'FPLA840 $V_{CC} = 4.75\text{ V}$ ,	$V_{OH} = 5.5\text{ V}$			0.1	mA
$V_{OH}$	'FPLA839 $V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3.2\text{ mA}$	2.4	3		V
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 24\text{ mA}$		0.37	0.5	V
$I_I$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 5.5\text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 0.4\text{ V}$			-0.5	mA
$I_O^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 2.25\text{ V}$	-30		-112	mA
$I_{OZH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 0.4\text{ V}$			-20	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 0\text{ V}$ , $\overline{OE}$ inputs at $V_{IH}$		130	180	mA

**'FPLA839 switching characteristics**

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{pd}$	Input	Output	$R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $C_L = 50\text{ pF}$ , See Figure 1		10	20	ns
$t_{en}$	Pin 1 or Pin 13	Output			10	20	
$t_{dis}$					8	15	ns

**'FPLA840 switching characteristics**

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{pd}$	Input	Output	$R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $C_L = 50\text{ pF}$ , See Figure 1		10	25	ns
$t_{en}$	Pin 1 or Pin 13	Output			10	20	
$t_{dis}$					8	15	ns

†All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current,  $I_{OS}$ .

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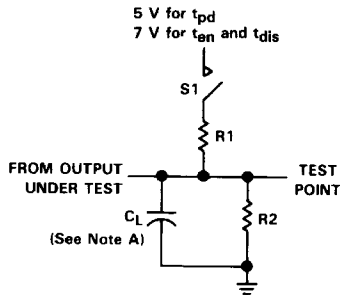
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**programming information**

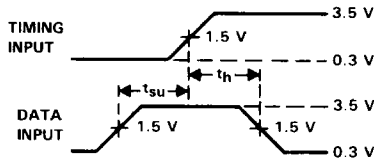
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

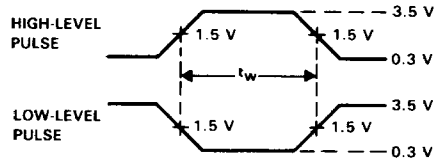
**PARAMETER MEASUREMENT INFORMATION**



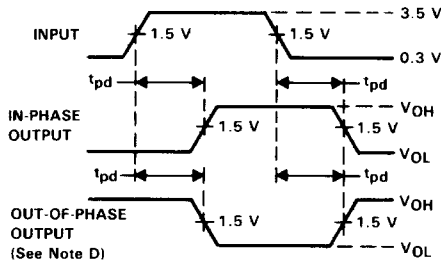
**LOAD CIRCUIT FOR  
THREE-STATE OUTPUTS**



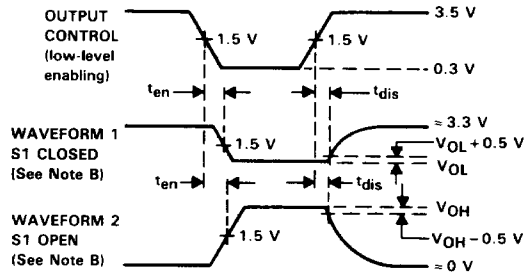
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATIONS**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS**

- NOTES: A.  $C_L$  includes probe and jig capacitance and is 50 pF for  $t_{pd}$  and  $t_{en}$ , 5 pF for  $t_{dis}$ .  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

**FIGURE 1**