REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated document. Added device types 07 thru 10. Added CAGE 18324. Added L package.	94-10-17	M. A. Frye
B	Added device types 11 thru 14. Added device class N option for some devices. Added X package, represents plastic dual-in-line. Editorial changes throughout.	95-12-15	M. A. Frye
C	Updated parameter f_{MAX2} in table I, added new test for devices 07, 08, 11-14, t_{CF}, added footnote 8/ to table I. Changed the measured value in table IIB. Removed cage 65786 as a source.	96-04-30	M. A. Frye

REV																				
SHEET																				
REV	C	C	C	C	C															
SHEET	15	16	17	18	19															
REV STATUS OF SHEETS			REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	
			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
93-01-19

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, BICMOS, ONE TIME PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-91760**

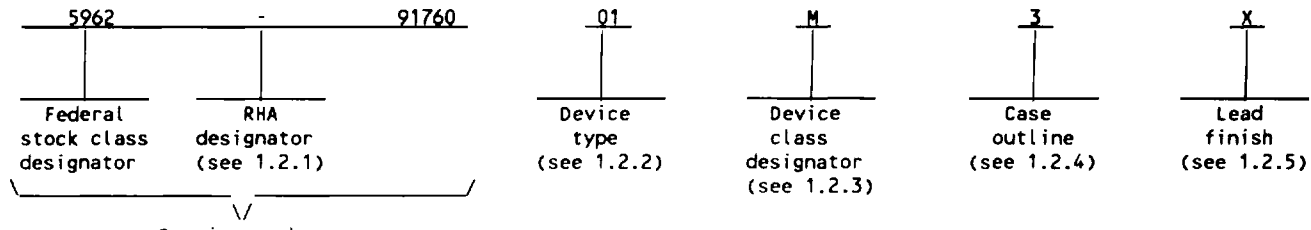
SHEET 1 OF 19

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Three product assurance classes consisting of space application (device class V), military high reliability (device classes M and Q), and non-traditional military (device class N) with a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". For device class N, the user is cautioned to assure that the device is appropriate for the application environment. When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-PRF-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes N, Q, and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	22V10G-15	22-input 10-output and-or-logic array	15 ns
02	22V10G-12	22-input 10-output and-or-logic array	12 ns
03	22V10G-10	22-input 10-output and-or-logic array	10 ns
04	22VP10G-15	22-input 10-output and-or-logic array	15 ns
05	22VP10G-12	22-input 10-output and-or-logic array	12 ns
06	22VP10G-10	22-input 10-output and-or-logic array	10 ns
07	22V10A	22-input 10-output and-or-logic array	10 ns
08	22V10B	22-input 10-output and-or-logic array	8.5 ns
09	22V10G-7.5	22-input 10-output and-or-logic array	7.5 ns
10	22VP10G-7.5	22-input 10-output and-or-logic array	7.5 ns
11	22V10A	22-input 10-output and-or-logic array	10 ns
12	22V10A	22-input 10-output and-or-logic array	10 ns
13	22V10B	22-input 10-output and-or-logic array	8.5 ns
14	22V10B	22-input 10-output and-or-logic array	8.5 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level (see 6.6 herein) as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
N	Certification and qualification to MIL-PRF-38535 with a non-traditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1/ Any device outside the traditional performance environment; e.g., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.2.4 Case outlines. The case outline(s) shall be as designated in MIL-STD-1835, JEDEC Publication 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
3	CQCC1-N28	28	Square leadless chip carrier package	MIL-STD-1835
L	GDIP3-T24	24	Dual-in-line package	MIL-STD-1835
X	MS-001 AF	24	Plastic dual-in-line package	JEP 95

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-PRF-38535 for classes N, Q, and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range to ground potential (V_{CC}) . . . . -0.5 V dc to +7.0 V dc
DC voltage range applied to the outputs in the high-Z state . -0.5 V dc to $+V_{CC}$
Maximum power dissipation . . . . 1.045 W 4/
Lead temperature (soldering, 10 seconds) . . . . +260°C
Thermal resistance, junction-to-case (θ_{JC}):
Cases 3, L . . . . See MIL-STD-1835
Case X . . . . 22°C/W
Junction temperature (T_J) . . . . +175°C
Storage temperature range (T_{STG}) . . . . -65°C to +150°C
Temperature (under bias) range . . . . -55°C to +125°C
Devices 11-14 . . . . -40°C to +85°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) . . . . +4.5 V dc minimum to +5.5 V dc maximum
Supply voltage range (V_{CC}) . . . . +4.75 V dc minimum to +5.25 V dc maximum
(for devices 07,08,11,12,13,14)
Ground voltage (GND) . . . . 0 V dc
Input high voltage (V_{IH}) . . . . 2.0 V dc minimum 5/
Input low voltage (V_{IL}) . . . . 0.8 V dc maximum 5/
Case operating temperature range (T_C) . . . . -55°C to +125°C
(for devices 11-14) . . . . -40°C to +85°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) . . . . xx percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltages referenced to V_{SS}.
4/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
5/ These are absolute values with respect to device ground. Overshoots due to system or tester noise are included.

6/ Values will be added when a qualified source is available.
HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-PRF-38535 for device classes N, Q, and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or quality conformance inspection, groups A, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic cells shall be programmed or at least 25 percent of the total logic cells shall be programmed for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall

apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Verification of programmability. When specified, devices shall be verified as programmed (see 4.6 herein) to the specified pattern. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.6.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.6.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.7 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

3.7.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes N, Q, and V shall be a "QML" as required in MIL-PRF-38535.

3.8 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes N, Q, and V, the requirements of MIL-PRF-38535 and the requirements herein.

3.9 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes N, Q, and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.11 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.12 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 131 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, and function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = V_{IH}, V_{IL}	I_{OH} = -2 mA	1, 2, 3	01-06, 09,10	2.4		V
			I_{OH} = -16 mA,		07,08,11, 12,13,14			
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IN} = V_{IH}, V_{IL}	I_{OL} = 12 mA	1, 2, 3	01-06, 09,10		0.5	V
			I_{OH} = 30 mA		07,08,11, 12,13,14			
Input leakage current	I_{IX}	V_{CC} = 5.5 V, V_{IN} = 2.7 V to 0.4 V		1, 2, 3	01-06, 09,10	-250	50	µA
					07,08,11, 12,13,14	-50	25	
Maximum input current	I_I	V_{CC} = 5.5 V V_{IN} = 5.5 V		1, 2, 3	01-06, 09,10		250	µA
					07,08,11, 12,13,14		30	
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 0.4 V and 2.7 V		1, 2, 3	All	-100	100	µA
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V		1, 2, 3	01-06, 09,10	-30	-120	mA
					07,08, 11-14	-30	-200	
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND		1, 2, 3	All		190	mA
Input capacitance 3/	C_{IN}	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1f)		4	01-06, 09,10		11	pF
					07,08,11, 12,13,14		6	
Output capacitance 3/	C_{OUT}			4	01-06, 09,10		9	pF
					07,08,11, 12,13,14		8	
Functional tests		See 4.4.1c		7,8A,8B	All			
Input or feedback to nonregistered output	t_{PD}	4/ See figures 3 and 4 (circuit A)		9, 10, 11	01,04		15	ns
					02,05		12	
					03,06,07, 11,12		10	
					08,13,14		8.5	
					09,10		7.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5 V \le V_{CC} \le 5.5 V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Clock to output	t_{CO}	See figures 3 and 4 (circuit A) 4/	9, 10, 11	01,04,07, 11,12		10	ns
				02,05		9.5	
				03,06		7.5	
				08,13,14		7.5	
				09,10		6.0	
Input or feedback setup time	t_S		9, 10, 11	01,04	7.5		ns
				02,05	4.5		
				03,06	3.6		
				07,11,12	8.0		
				08,13,14	6.5		
				09,10	3.0		
Hold time 3/	t_h		9, 10, 11	ALL	0		ns
Clock period ($t_S + t_{CO}$)	t_P		9, 10, 11	01,04	17.5		ns
				02,05,08, 13,14	14		
				03,06	11.1		
				07,11,12	18		
				09,10	9		
Clock width high 3/	t_{WH}		9, 10, 11	01,04	6		ns
				02,03, 05,06, 09,10	3		
				07,08,11, 12,13,14	4		
Clock width low 3/	t_{WL}		9, 10, 11	01,04	6		ns
				02,03, 05,06, 09,10	3		
				07,08,11, 12,13,14	4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ 1/ $4.5 V \leq V_{CC} \leq 5.5 V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
External maximum frequency $(1/(t_{CO} + t_S))$	f_{MAX1}		9, 10, 11	01,04	57		MHz
				07,11,12	55		
				02,05,08, 13,14	71		
				03,06	90		
				09,10	111		
Data path maximum frequency $(1/(t_{WH} + t_{WL}))$	f_{MAX2}		9, 10, 11	01,04	83		MHz
				02,03,05, 06,09,10	166		
Internal feedback $1/(t_S + t_{CF})$				07,11,12	90		
				08,13,14	105		
Input to output enable	t_{EA}	See figures 3 and 4 (circuit A) 4/	9, 10, 11	01,04		15	ns
				02,05		12	
				03,06,07, 11,12		10	
				08,13,14		9	
				09,10		7.5	
Input to output disable 3/ 5/	t_{ER}	4/ See figures 3 and 4 (circuit B)	9, 10, 11	01,04		15	ns
				02,05		12	
				03,06,07, 11,12		10	
				08,13,14		9	
				09,10		7.5	
Asynchronous reset pulse width 3/	t_{AW}	4/ See figures 3 and 4 (circuit A)	9, 10, 11	01,04	15		ns
				02,05	12		
				03,06	10		
				07,08,11, 12,13,14	10		
				09,10	8.5		
Clock to feedback 6/	t_{CF}	See figure 3A	9, 10, 11	07-08, 11-14		3	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Asynchronous reset recovery time 3/	t_{AR}	See figures 3 and 4 (circuit A) 4/	9, 10, 11	01,04	10		ns
				02,05	7		
				03,06,07, 08,11,12, 13,14	6		
				09,10	5		
Asynchronous reset to registered output delay 3/	t_{AP}		9, 10, 11	01,04		20	ns
				02,05		14	
				03,06 09,10		12	
				07,08,11, 12,13,14		12.5	
Synchronous preset recovery time 3/	t_{SPR}		9, 10, 11	01,04	10		ns
				02,05	7		
				03,06,07, 08,11,12, 13,14	6		
				09,10	5		
Power-up reset time 3/ 7/	t_{PR}		9, 10, 11	01-06, 09,10	1		µs

1/ Devices 11 and 13 operate and test at -40°C to +85°C temperature range. Devices 07, 08, 11 thru 14; have voltage operate and test range of 4.75 V to 5.25 V.
2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 4.
5/ This delay is measured to the point at which a previous high level has fallen to 0.5 V below V_{OH} minimum or a previous low level has risen to 0.5 V above V_{OL} maximum.
6/ Calculated from f_{MAX} Internal.
7/ The registers in these devices have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic low state. The output will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.6 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the Percent Defective Allowable (PDA) calculation and shall be removed from the lot. The manufacturer as an option may use built-in test circuitry by testing the entire lot to verify programmability and AC performance without programming the user array.

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D); for circuit see 4.2.1c herein.

d. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

d. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7, 8A and 8B tests shall consist of verifying functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available upon request. For device classes N, Q, and V subgroups 7, 8A and 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable: testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, 11, group A testing per MIL-STD-883, method 5005.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

(2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

Device types	1 thru 14	
Case outlines	3	L and X
Terminal number	Terminal symbol	
1	V_{CC}	CLK/I0
2	CP/I	I1
3	I	I2
4	I	I3
5	I	I4
6	I	I5
7	I	I6
8	GND	I7
9	I	I8
10	I	I9
11	I	I10
12	I	GND
13	I	I11
14	GND	F0
15	GND	F1
16	I	F2
17	I/O	F3
18	I/O	F4
19	I/O	F5
20	I/O	F6
21	I/O	F7
22	GND	F8
23	I/O	F9
24	I/O	V_{CC}
25	I/O	
26	I/O	
27	I/O	
28	V_{CC}	

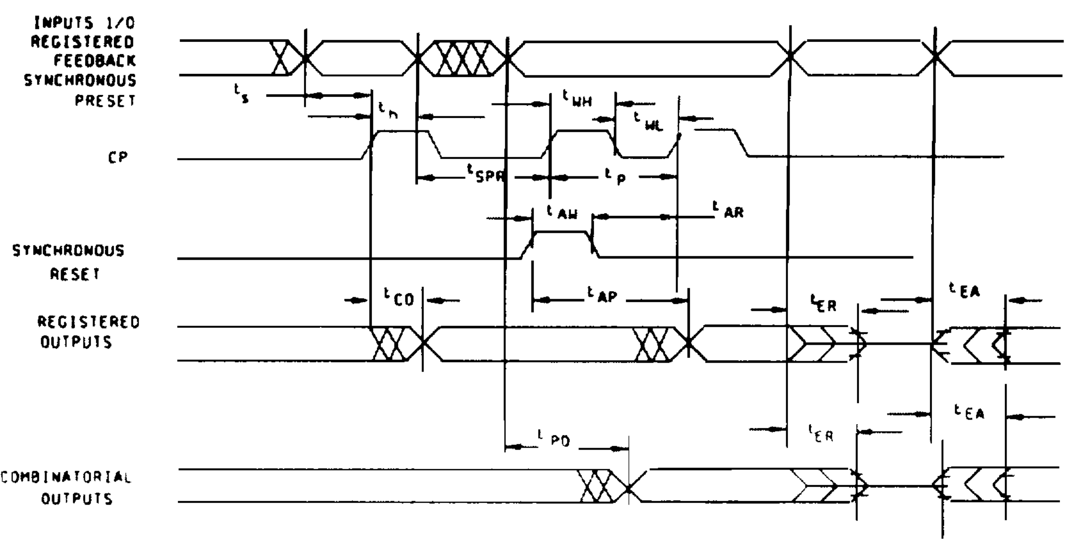
FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
CP/1	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = three-state
2. X = don't care

FIGURE 2. Truth table.

Switching waveform



Power-up reset waveform

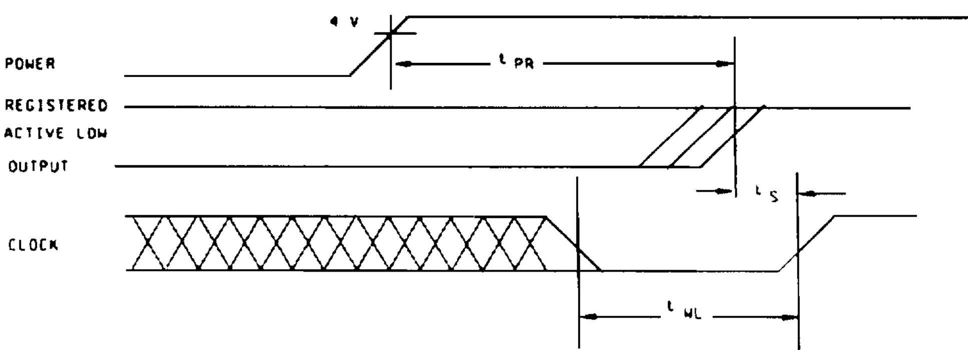
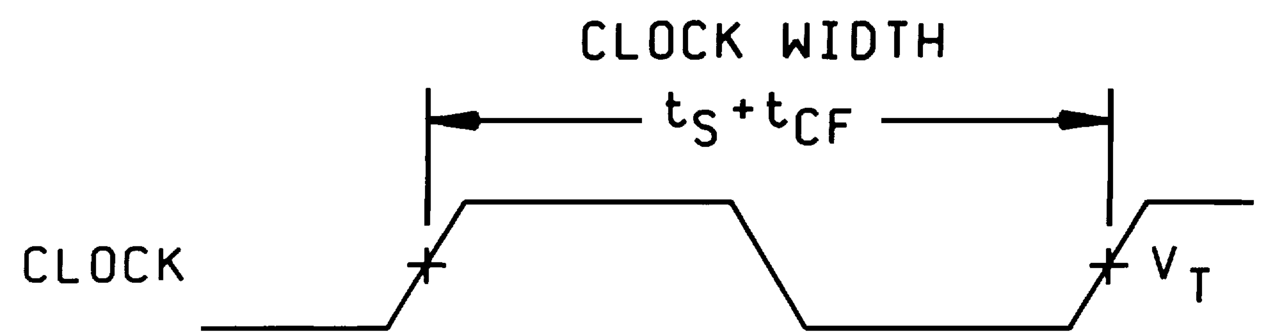


FIGURE 3. Timing waveforms.



INPUT TO OUTPUT DISABLE/ENABLE

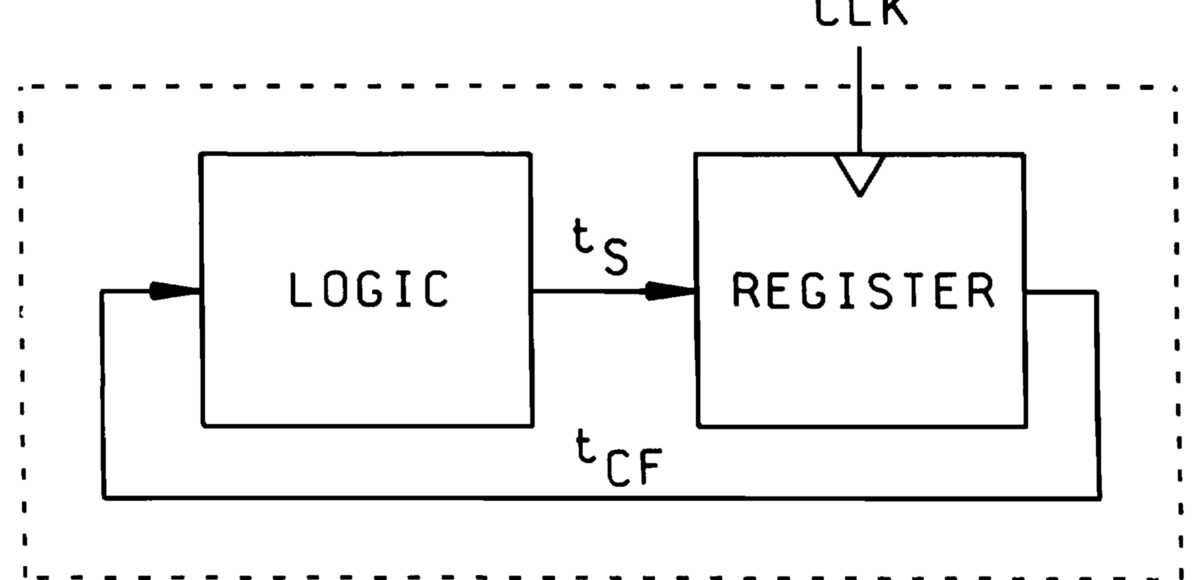
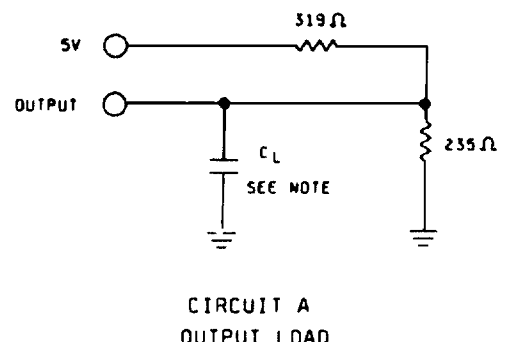
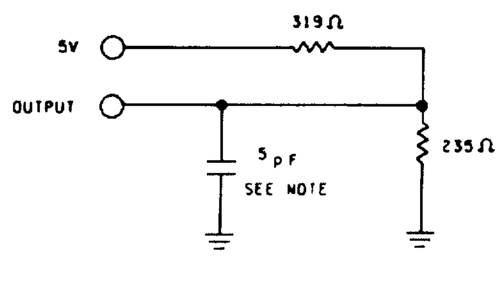


FIGURE 3A. Timing waveforms - Continued.



CIRCUIT A
OUTPUT LOAD



CIRCUIT B
OUTPUT LOAD FOR t_{ER}

NOTE: Including scope and jig (minimum values).

	Package outlines
Load	3,L,X
C_L	50 pF

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuits and tests conditions.

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes N, Q, and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

f. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M . Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes N, Q, and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MMIL-PRF-38535 appendix A, for the RHA level being tested. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line No.	Test Requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class M	Device class N	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)				1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Not required	Required
3	Same as line 1				1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required
5	Same as line 1				1*,7* Δ
6	Final electrical test parameters for unprogrammed devices	1*,2,3,7*,8A,8B	1*,2,3,7*,8A,8B	1*,2,3,7*,8A,8B	1*,2,3,7*,8A,8B
6	Final electrical test parameters for programmed devices	1*,2,3,7*,8A,8B,9	1*,2,3,7*,8A,8B,9	1*,2,3,7*,8A,8B,9	1*,2,3,7*,8A, 8B,9
7	Group A test requirements	1,2,3,4**,7,8A,8B, 9,10, 11	1,2,3,4**,7,8A,8B, 9,10, 11	1,2,3,4**,7,8A,8B, 9,10, 11	1,2,3,4**,7,8A, 8B,9,10, 11
8	Group C test requirements	2,3,7,8A,8B	2,3,7,8A,8B	2,3,7,8A,8B	1,2,3,7,8A, 8B,9,10,11 Δ
9	Group D test requirements	2,3,7,8A,8B	2,3,7,8A,8B	2,3,7,8A,8B	2,3,7,8A,8B
10	Group E test requirements	1,7,9	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1f.
6/ see 4.4.1e.
7/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{OZ}	±4 µA of specified value in table IA
I_{IX}	±1.0 µA of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-PRF-38535 for device classes N, Q, and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and as follows:

C_{IN} Input terminal capacitance.
C_{OUT} Output terminal capacitance.
GND Ground zero voltage potential.
I_{CC} Supply current.
I_{IX} Input current.
I_{OZ} Output current.
T_C Case temperature.
V_{CC} Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
[valid symbol]	MUST BE VALID	WILL BE VALID
[H to L symbol]	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
[L to H symbol]	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
[don't care symbol]	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
[high impedance symbol]		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-H-38534, MIL-PRF-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique part numbers. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique part number. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document
New MIL-PRF-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(N, Q, or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-04-30

Approved sources of supply for SMD 5962-91760 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9176001M3X	3/	PAL22V10G-15LMB
5962-9176002M3X	3/	PAL22V10G-12LMB
5962-9176003M3X	3/	PAL22V10G-10LMB
5962-9176004M3X	3/	PAL22VP10G-15LMB
5962-9176005M3X	3/	PAL22VP10G-12LMB
5962-9176006M3X	3/	PAL22VP10G-10LMB
5962-9176007M3A	18324	ABT22V10A/B3A
5962-9176007MLA	18324	ABT22V10A/BLA
5962-9176008M3A	18324	ABT22V10B/B3A
5962-9176008MLA	18324	ABT22V10B/BLA
5962-9176009M3X	3/	PAL22V10G-7LMB
5962-9176010M3X	3/	PAL22VP10G-7LMB
5962-9176011NXA	18324	ABT22V10A/IN24
5962-9176012NXA	18324	ABT22V10A/CN24
5962-9176013NXA	18324	ABT22V10B/IN24
5962-9176014NXA	18324	ABT22V10B/CN24

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ _Caution_. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source. acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Philips Semiconductors 830 Stewart Dr. Sunnyvale, CA 94088 Point of contact: 811 E Arques Ave. Sunnyvale CA 94088-3409

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.