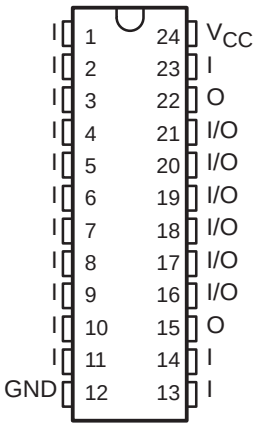
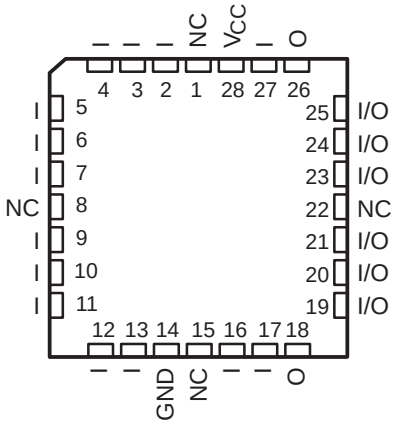
- **High-Performance: f_{max} (w/o feedback)**
  TIBPAL20R' -15C Series . . . 45 MHz
  TIBPAL20R' -20M Series . . . 41.6 MHz
- **High-Performance . . . 45 MHz Min**
- **Reduced I_{CC} of 180 mA Max**
- **Functionally Equivalent, but Faster Than PAL20L8, PAL20R4, PAL20R6, PAL20R8**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Preload Capability on Output Registers Simplifies Testing**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE
(TOP VIEW)



TIBPAL20L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

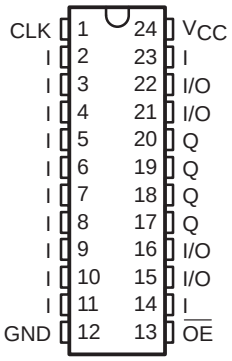
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

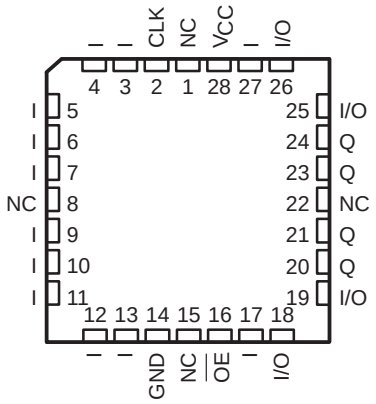
The TIBPAL20' C series is characterized from 0°C to 75°C. The TIBPAL20' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

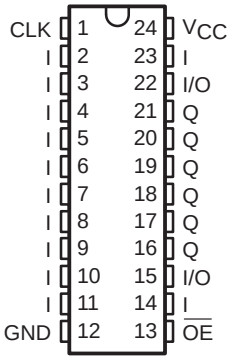
TIBPAL20R4'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE
(TOP VIEW)



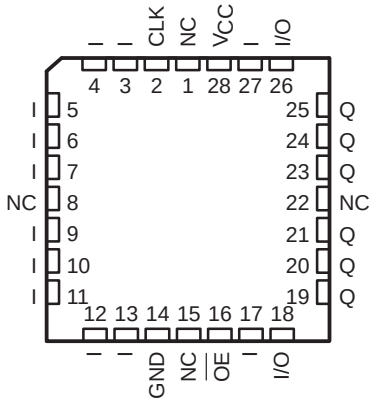
TIBPAL20R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



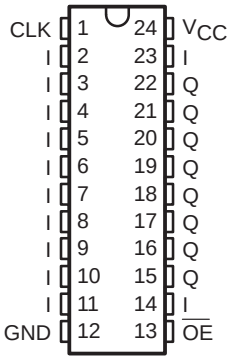
TIBPAL20R6'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE
(TOP VIEW)



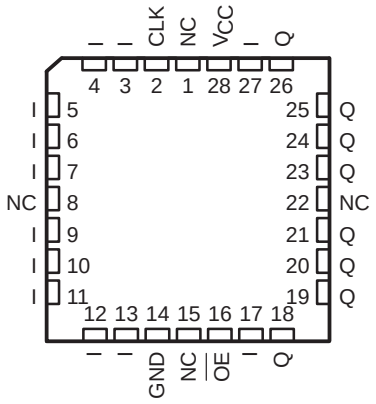
TIBPAL20R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



TIBPAL20R8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE
(TOP VIEW)



TIBPAL20R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)

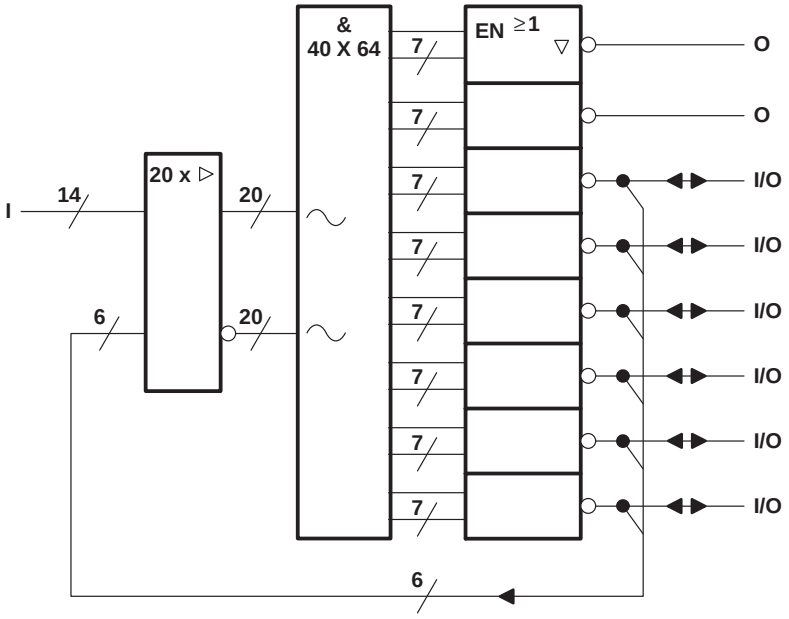


Pin assignments in operating mode

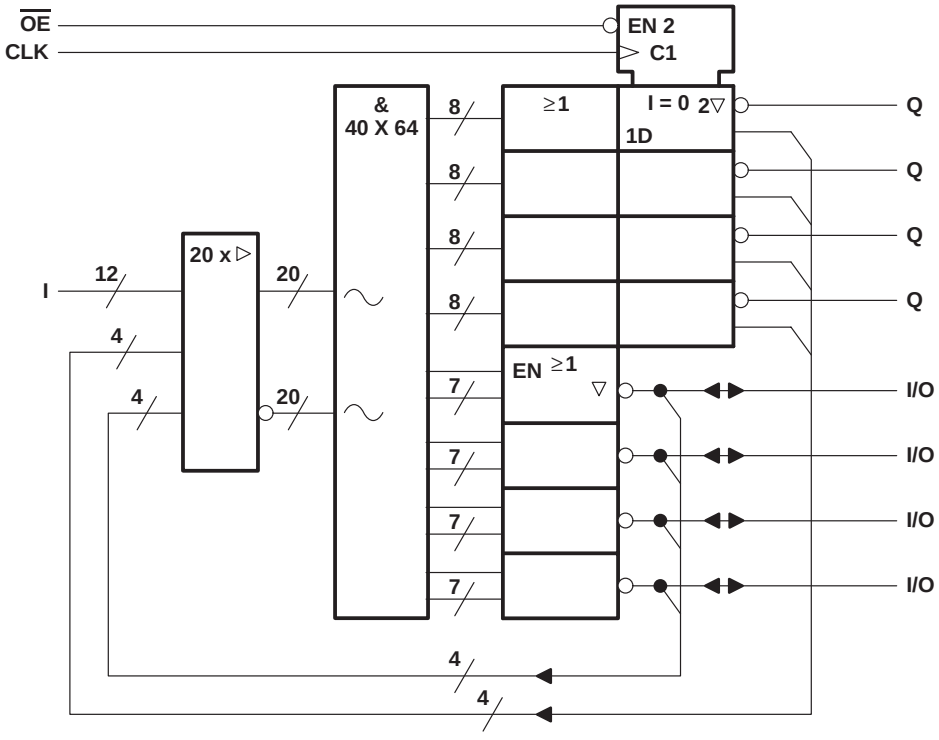
NC – No internal connection

functional block diagrams (positive logic)

TIBPAL20L8'



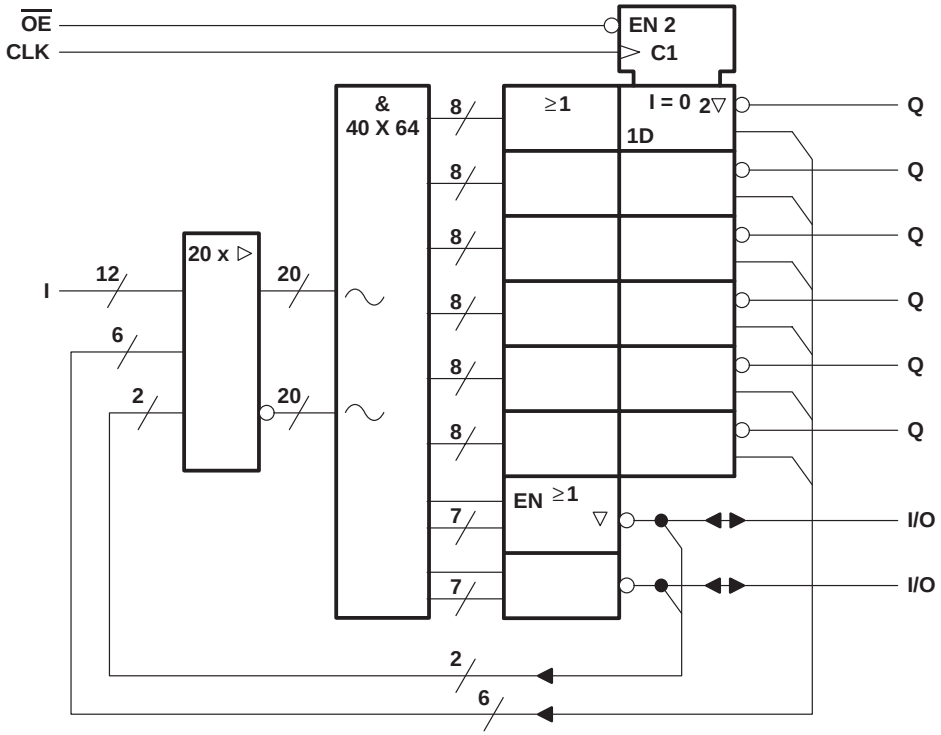
TIBPAL20R4'



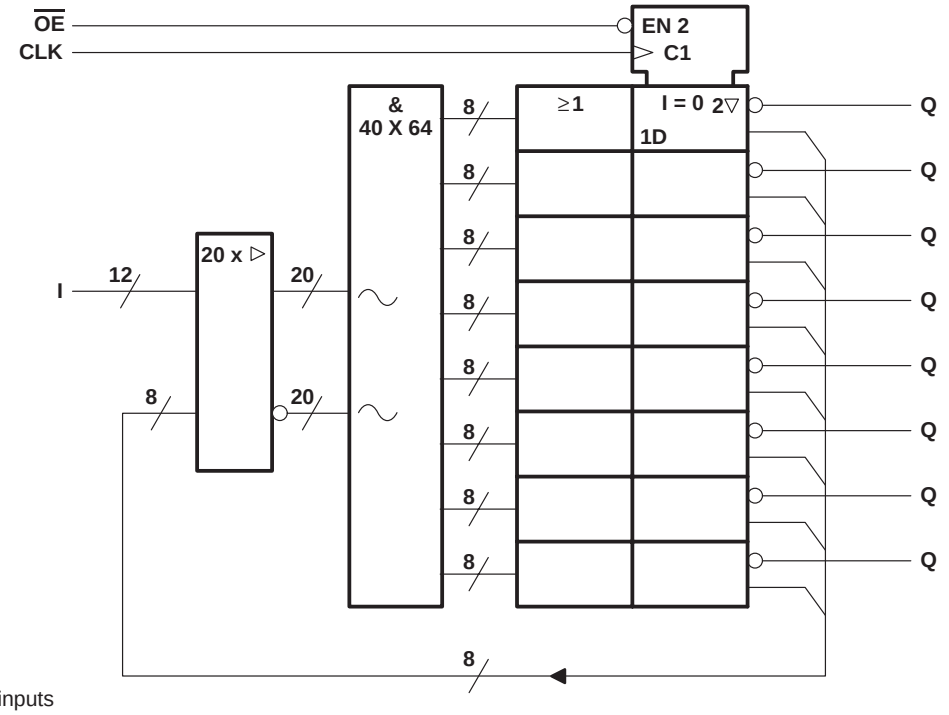
denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

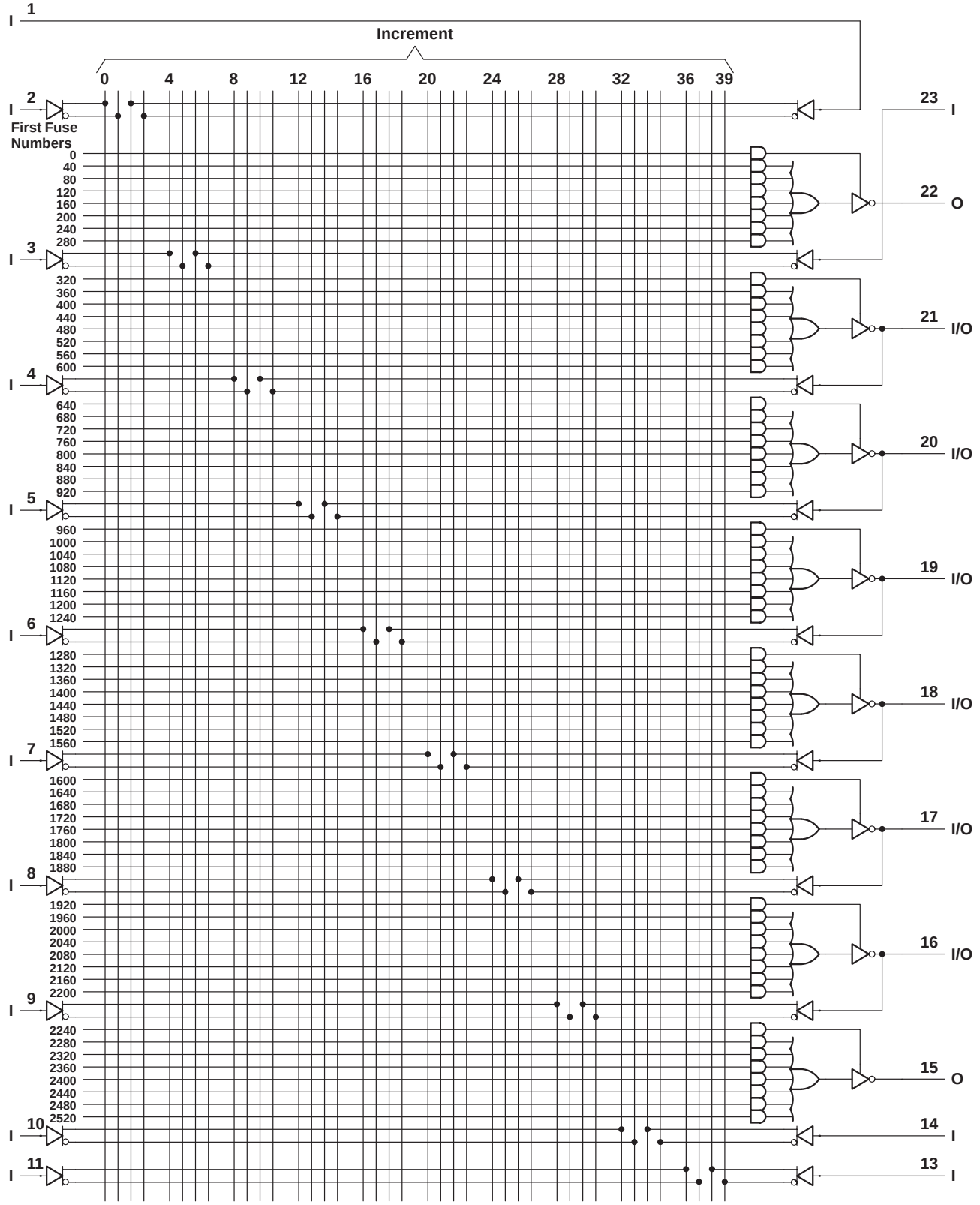


TIBPAL20R8'



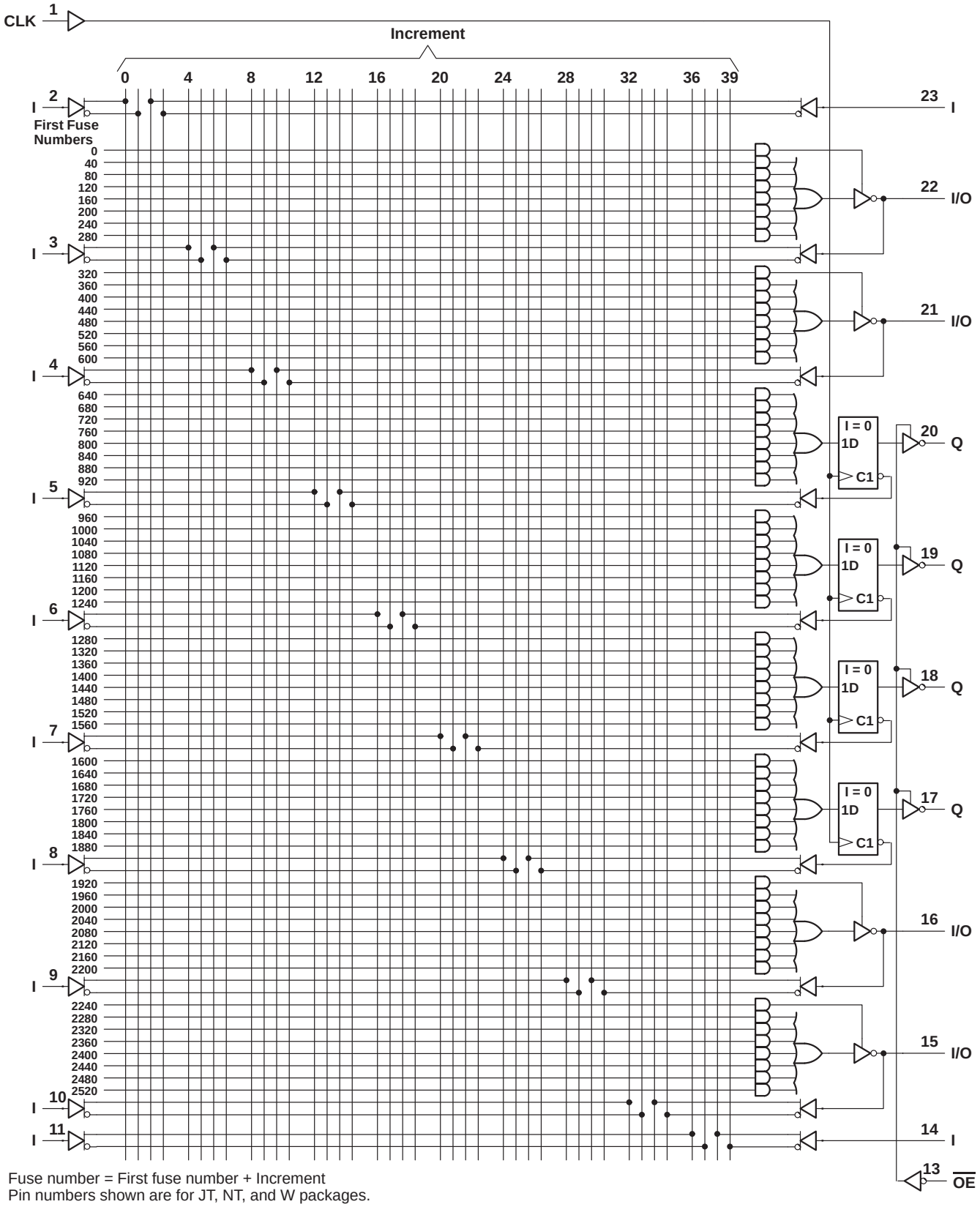
denotes fused inputs

logic diagram (positive logic)



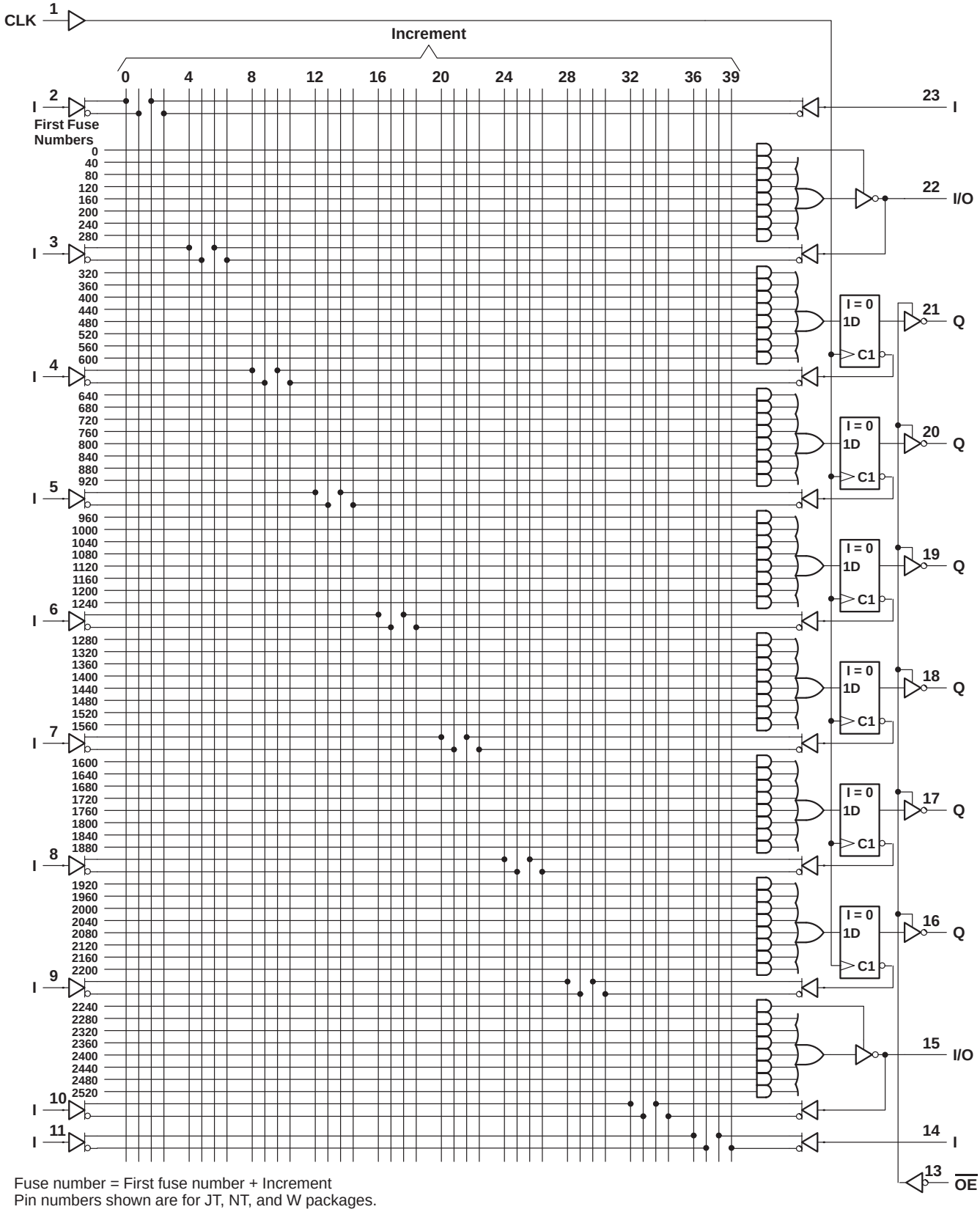
Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

logic diagram (positive logic)



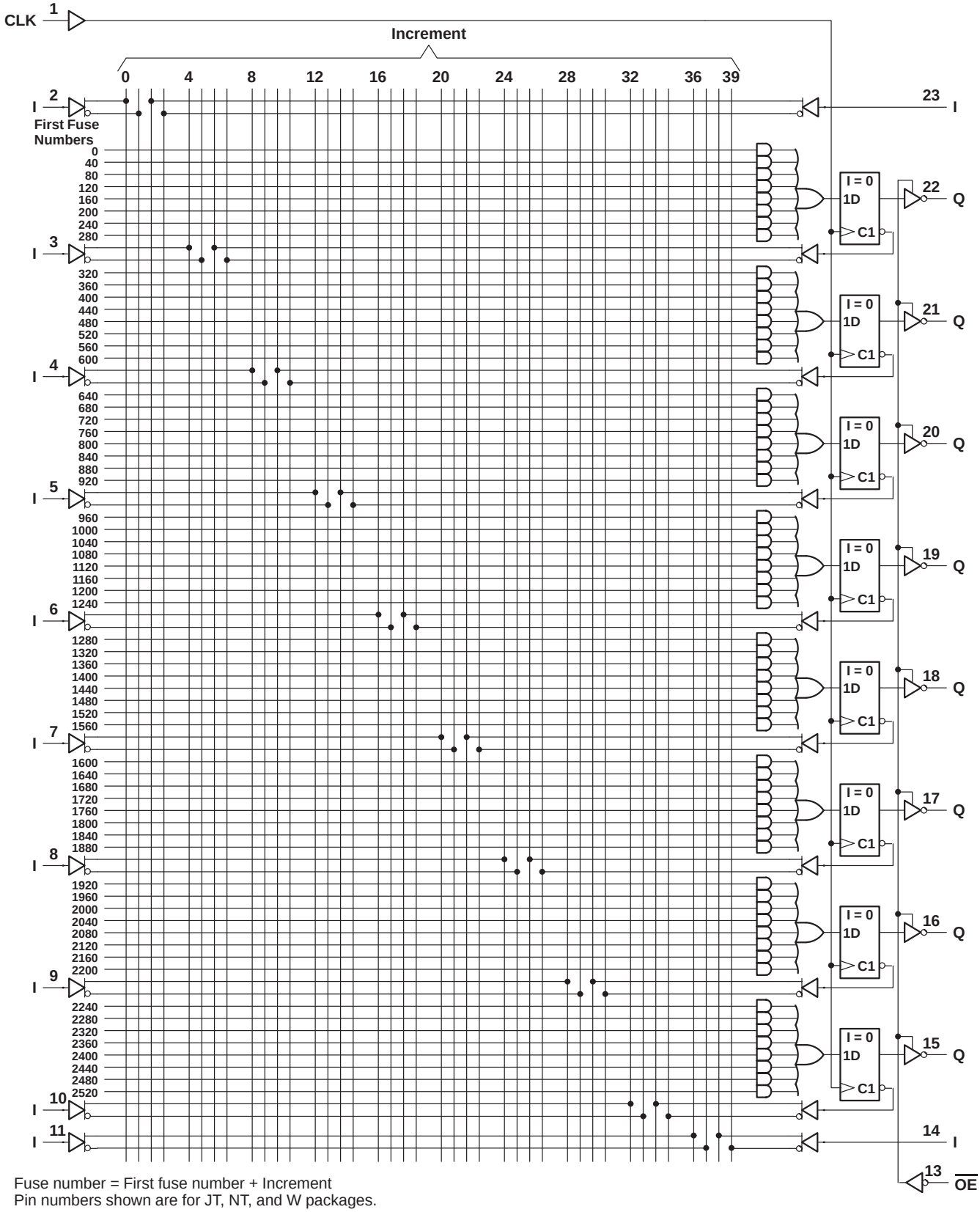
Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}†	Clock frequency		0		45	MHz
t_w†	Pulse duration, clock	High	10			ns
		Low	12			
t_{su}†	Setup time, input or feedback before clock↑		15			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V,	V_O = 2.7 V			20	μA
	I/O ports					100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V,	V_O = 0.4 V			–20	μA
	I/O ports					–250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			25	μA
I_{IL}‡		V_{CC} = 5.25 V,	V_I = 0.4 V			–0.25	mA
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0.5 V	–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open,	V_I = 0, $\overline{OE}$ at V_{IH}		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 3	37	40		MHz
	Without feedback			45	50		
t_{pd}	I, I/O	O, I/O			12	15	ns
t_{pd}	CLK↑	Q			8	12	ns
t_{en}	$\overline{OE}$	Q			10	15	ns
t_{dis}	$\overline{OE}$↑	Q			8	12	ns
t_{en}	I, I/O	O, I/O			12	18	ns
t_{dis}	I, I/O	O, I/O			12	15	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
¶ $f_{max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}$,
f_{max} does not apply for TIBPAL20L8,.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		41.6	MHz
t_w†	Pulse duration, clock	High	12			ns
		Low	12			
t_{su}†	Setup time, input or feedback before clock↑		20			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55	25	125	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA	2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.3	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			100	μA
I_{OZL}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V			–20	μA
	I/O ports					–250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			1	mA
I_{IH}‡	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V			100	μA
	All others					25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.25	mA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0.5 V	–30	–70	–250	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open,	V_I = 0, OE = V_{IH}		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 3	28.5	40		MHz
	Without feedback			41.6	50		
t_{pd}	I, I/O	O, I/O			12	20	ns
t_{pd}	CLK↑	Q			8	15	ns
t_{en}	$\overline{OE}$	Q			10	20	ns
t_{dis}	$\overline{OE}$↑	Q			8	20	ns
t_{en}	I, I/O	O, I/O			12	25	ns
t_{dis}	I, I/O	O, I/O			12	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

¶ $f_{max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}$,

f_{max} does not apply for TIBPAL20L8,.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

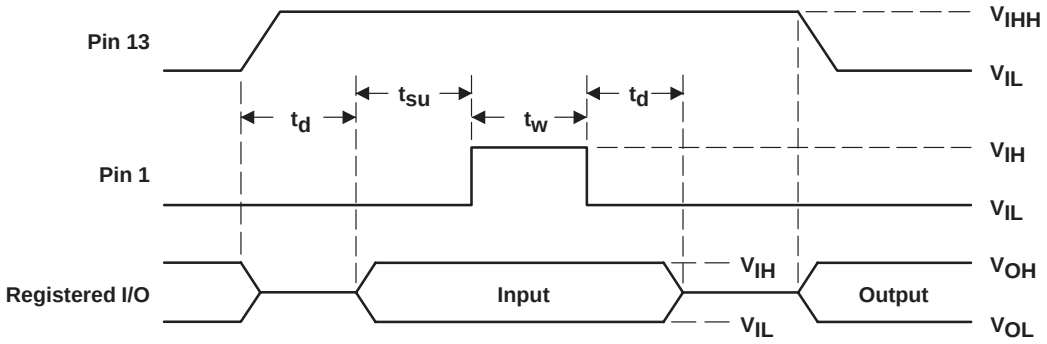
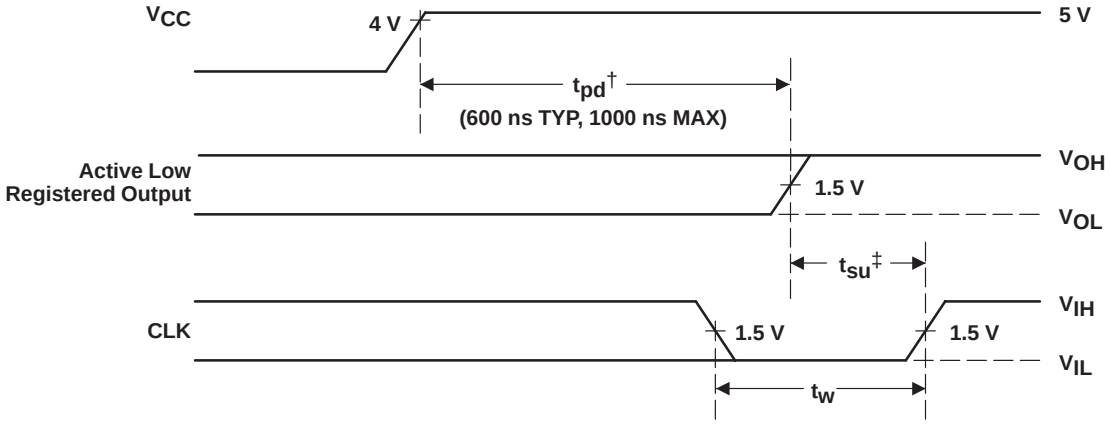


Figure 1. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT, NT, and W packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

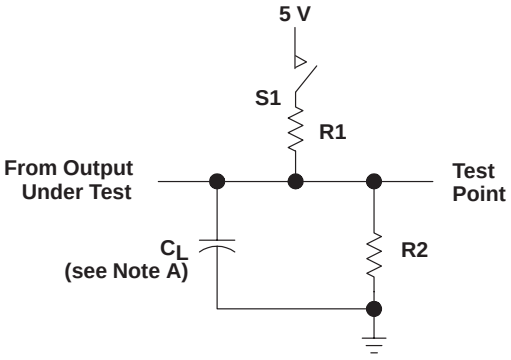
Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



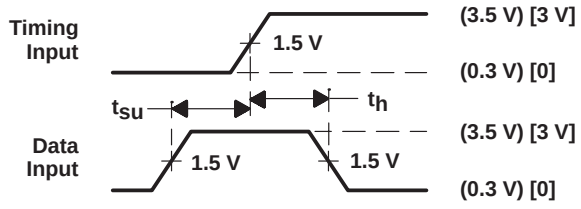
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

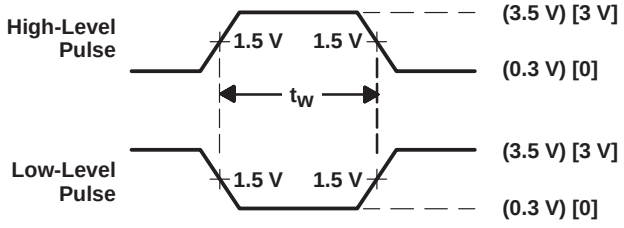
PARAMETER MEASUREMENT INFORMATION



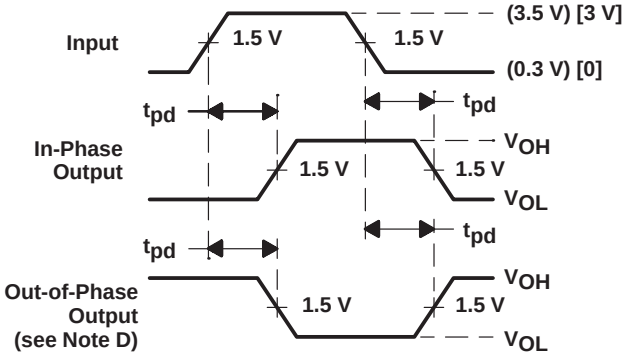
LOAD CIRCUIT FOR 3-STATE OUTPUTS



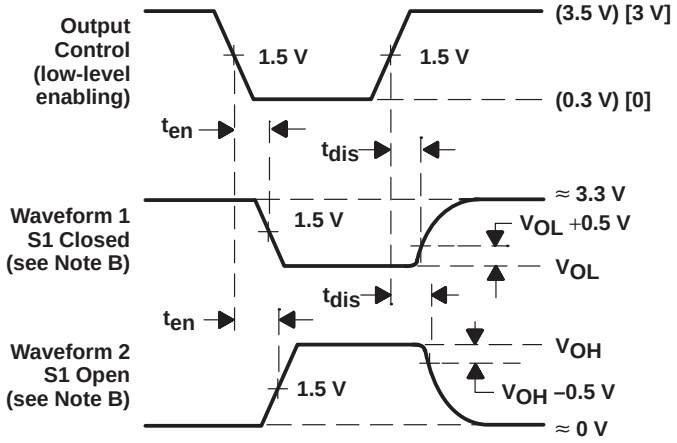
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ). PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets [ ]. PRR ≤ 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

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TEXAS INSTRUMENTS

D0892

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-87671013A	ACTIVE	LCCC	FD	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8767101KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-8767101LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
5962-87671023A	ACTIVE	LCCC	FD	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8767102KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-8767102LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
5962-87671033A	ACTIVE	LCCC	FD	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8767103KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-8767103LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
5962-87671043A	ACTIVE	LCCC	FD	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8767104KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-8767104LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
8412901LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
8412901XA	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
8412902KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
8412902LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
8412902XA	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
8412903KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
8412903LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
8412903XA	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
8412904KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
8412904LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
8412904XA	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/50501BLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
JM38510/50502BLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
JM38510/50503BLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
JM38510/50504BLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20L8-15CFN	ACTIVE	PLCC	FN	28	37	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL20L8-15CNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL20L8-20MFKB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
TIBPAL20L8-20MJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20L8-20MJTB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20L8-20MWB	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R4-15CFN	ACTIVE	PLCC	FN	28	37	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL20R4-15CNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL20R4-20MFKB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
TIBPAL20R4-20MJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R4-20MJTB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R4-20MWB	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R6-15CFN	ACTIVE	PLCC	FN	28	37	TBD	CU SNPB	Level-1-220C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TIBPAL20R6-15CNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL20R6-20MFKB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
TIBPAL20R6-20MJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R6-20MJTB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R6-20MWB	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R8-15CFN	ACTIVE	PLCC	FN	28	37	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL20R8-15CNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL20R8-20MFKB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
TIBPAL20R8-20MJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R8-20MJTB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
TIBPAL20R8-20MWB	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

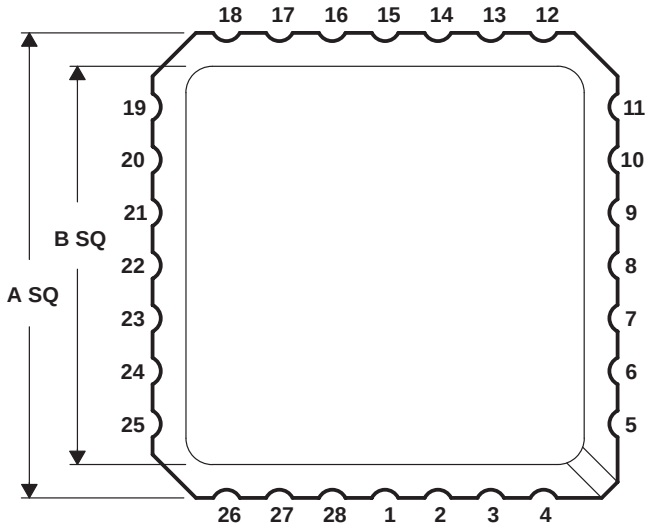
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

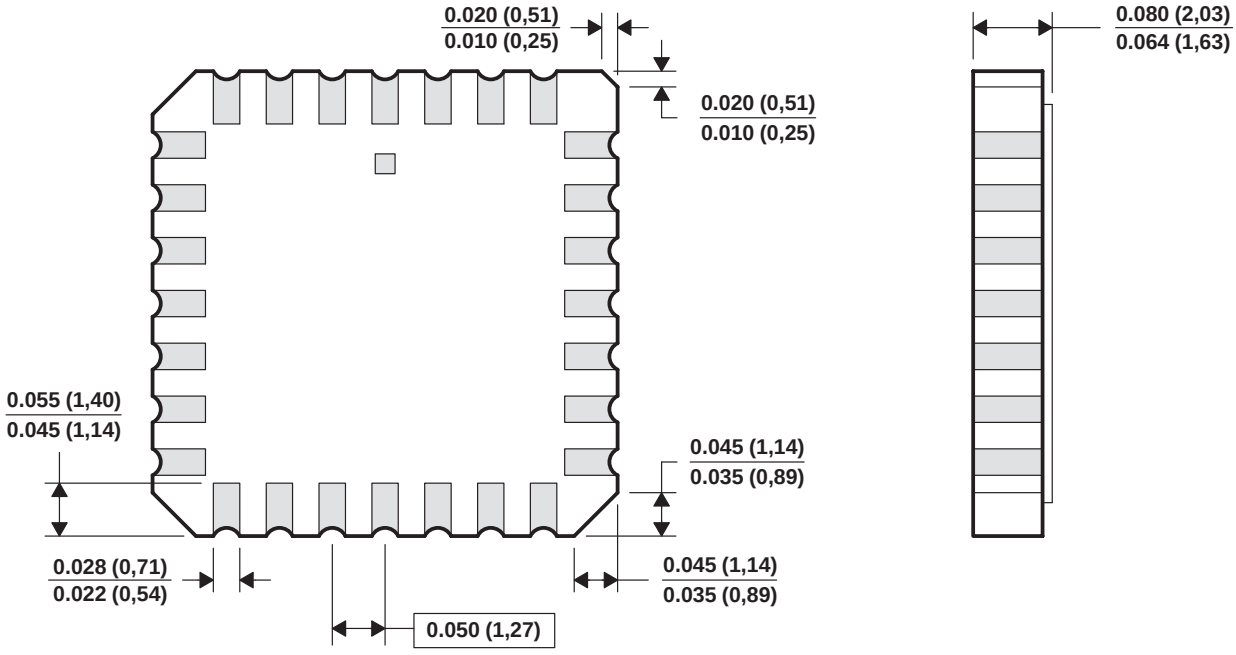
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

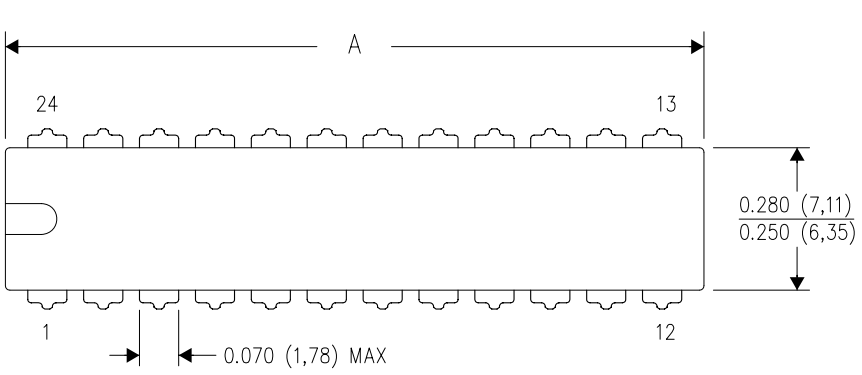


4040140/D 10/96

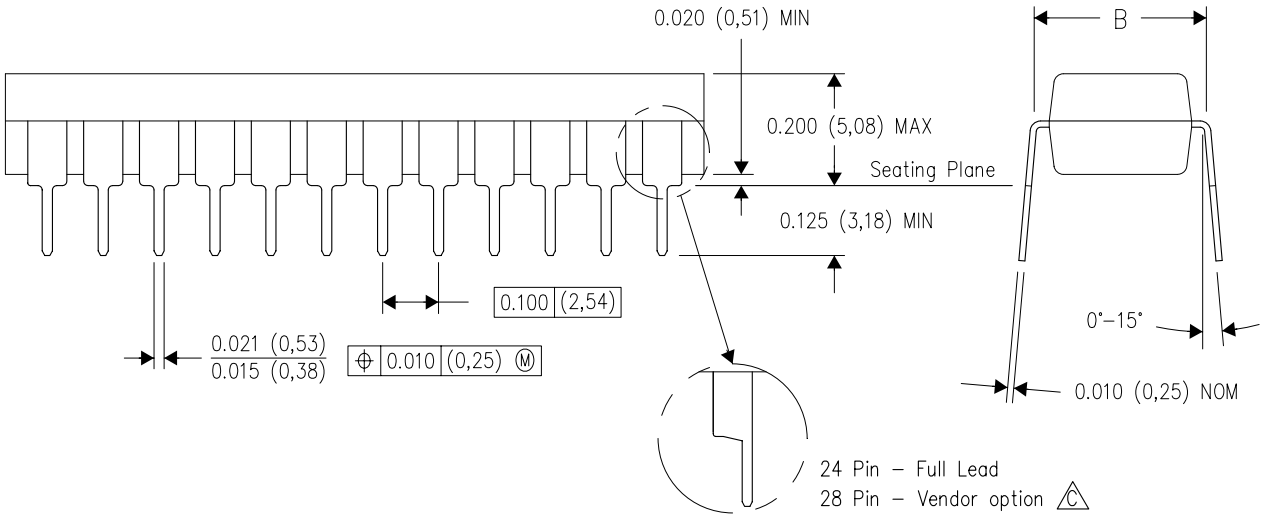
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



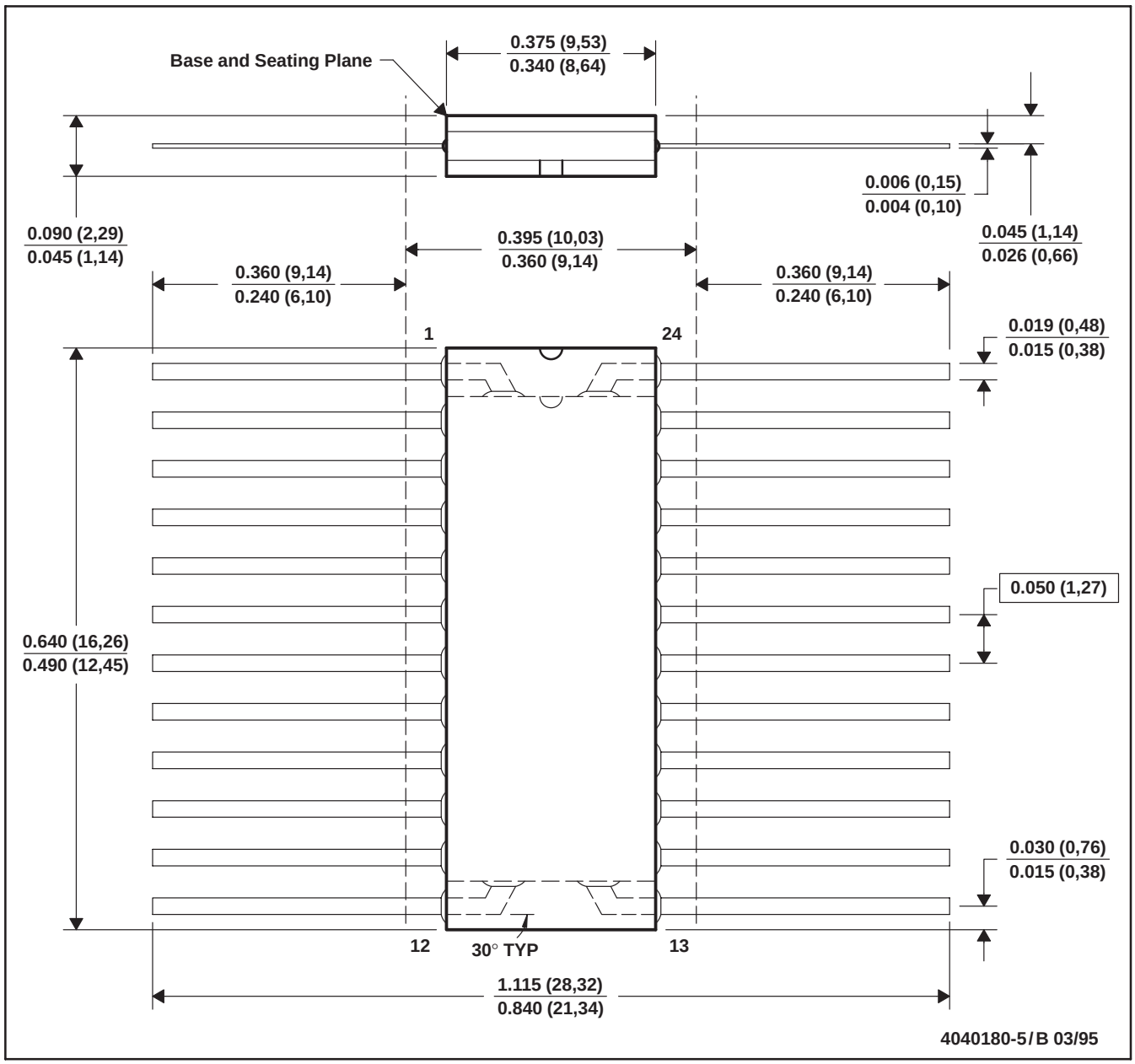
DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/C 04/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

W (R-GDFP-F24) **CERAMIC DUAL FLATPACK**



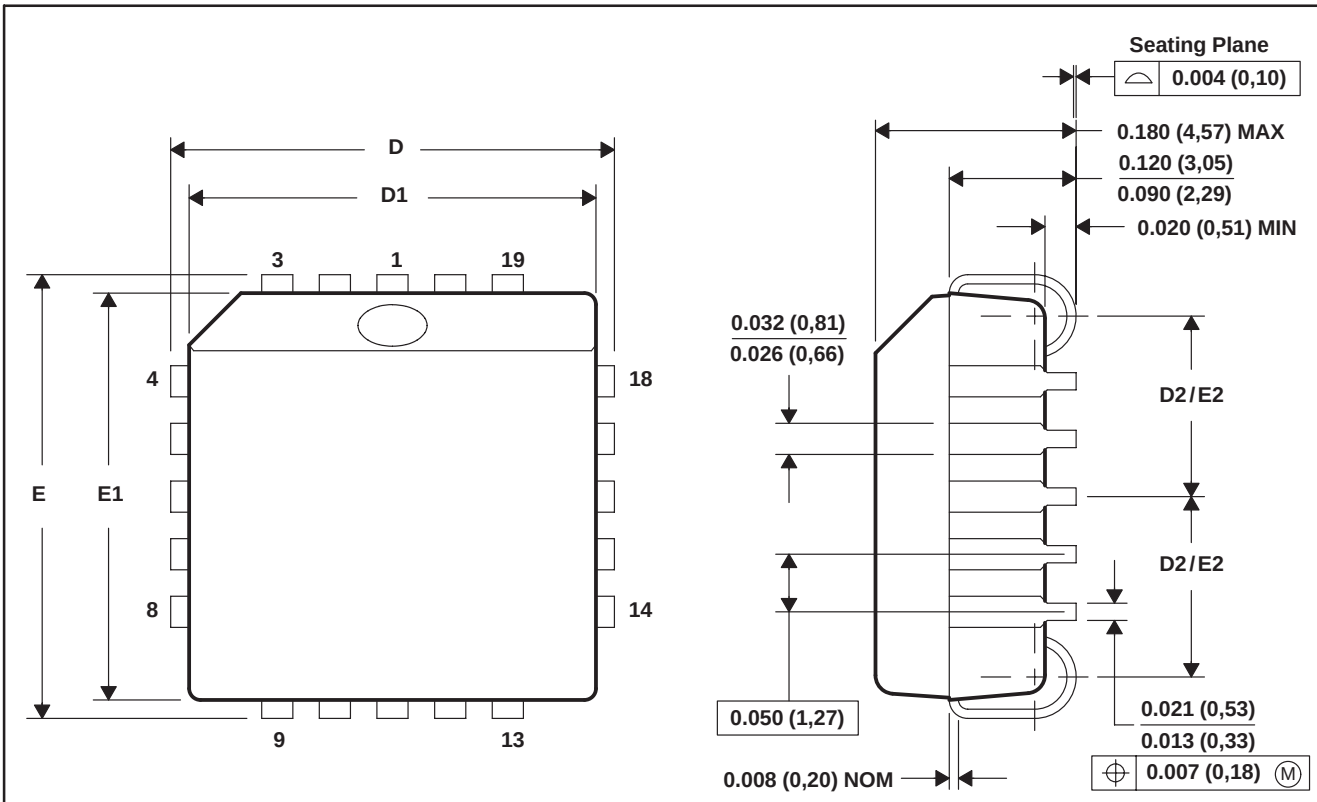
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

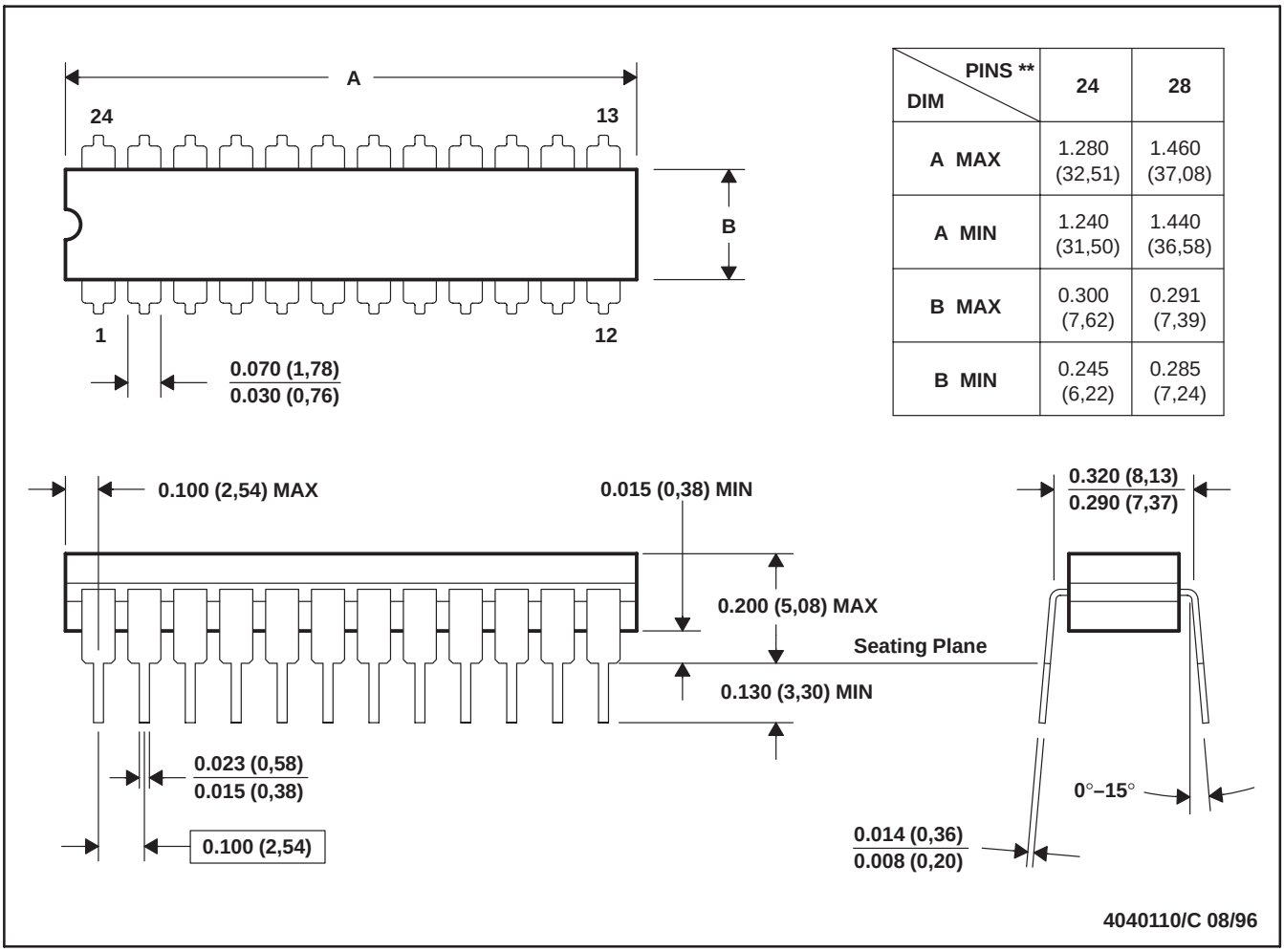
4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

24 LEADS SHOWN



DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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