
Features

- Industry-standard Architecture
 - Emulates Many 20-pin PALs
 - Low-cost Easy-to-use Software Tools
- High-speed Electrically-erasable Programmable Logic Devices
 - 12 ns Maximum Pin-to-pin Delay
- Low-power - 5 μ A (Typ) Standby Current
- CMOS and TTL Compatible Inputs and Outputs
 - Input and I/O Pin Keeper Circuits
- Advanced Flash Technology
 - Reprogrammable
 - 100% Tested
- High-reliability CMOS Process
 - 20 Year Data Retention
 - 100 Erase/Write Cycles
 - 2,000V ESD Protection
 - 200 mA Latchup Immunity
- Commercial and Industrial Temperature Ranges
- Dual-in-line and Surface Mount Packages in Standard Pinouts
- PCI-compliant
- Green (Pb/Halide-free/RoHS Compliant) Package Options Available

1. Description

The ATF16V8CZ is a high-performance EECMOS programmable logic device that utilizes Atmel's proven electrically-erasable Flash memory technology. Speeds down to 12 ns and a 5 μ A (Typ) edge-sensing power-down mode are offered. All speed ranges are specified over the full 5V \pm 10% range for industrial temperature ranges; 5V \pm 5% for commercial range 5-volt devices.

The ATF16V8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

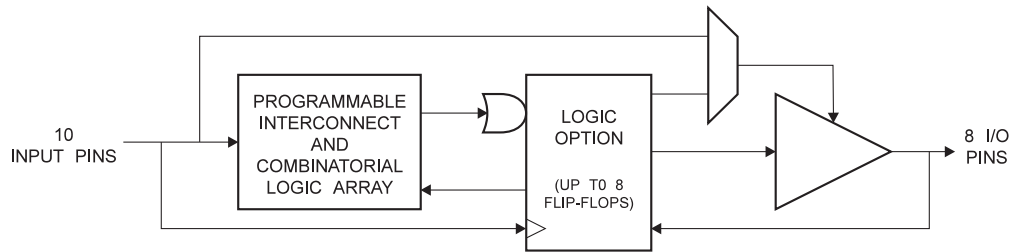
The ATF16V8CZ can significantly reduce total system power, thereby enhancing system reliability and reducing power supply costs. When all the inputs and internal nodes are not switching, supply current drops to less than 5 μ A typically. This automatic power-down feature (or sleep mode) allows for power savings in slow clock systems and asynchronous applications. Also, the pin-keeper circuits eliminate the need for internal pull-up resistors along with their attendant power consumption.



**High-
performance
EE PLD**

ATF16V8CZ

Figure 1-1. Block Diagram



2. Pin Configuration and Pinouts

Table 2-1. Pinouts - All Pinouts Top View

| Pin Name | Function |
|-----------------|------------------------|
| CLK | Clock |
| I | Logic Inputs |
| I/O | Bi-directional Buffers |
| \overline{OE} | Output Enable |
| VCC | +5V Supply |

Figure 2-1. TSSOP

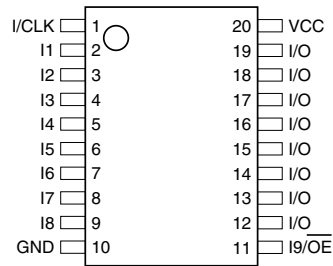


Figure 2-2. DIP/SOIC

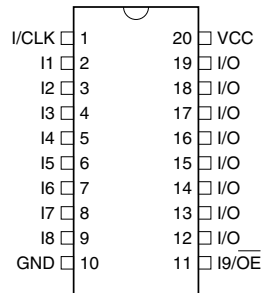
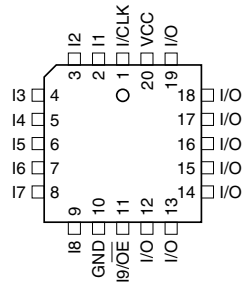


Figure 2-3. PLCC



3. Absolute Maximum Ratings*

| | |
|--|--------------------------------|
| Temperature Under Bias..... | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V ⁽¹⁾ |
| Voltage on Input Pins with Respect to Ground During Programming..... | -2.0V to +14.0V ⁽¹⁾ |
| Programming Voltage with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to 7.0V for pulses of less than 20 ns.

4. DC and AC Operating Conditions

| | Commercial | Industrial |
|---------------------------------|------------|--------------|
| Operating Temperature (Ambient) | 0°C - 70°C | -40°C - 85°C |
| V_{CC} Power Supply | 5V ±5% | 5V ±10% |

4.1 DC Characteristics

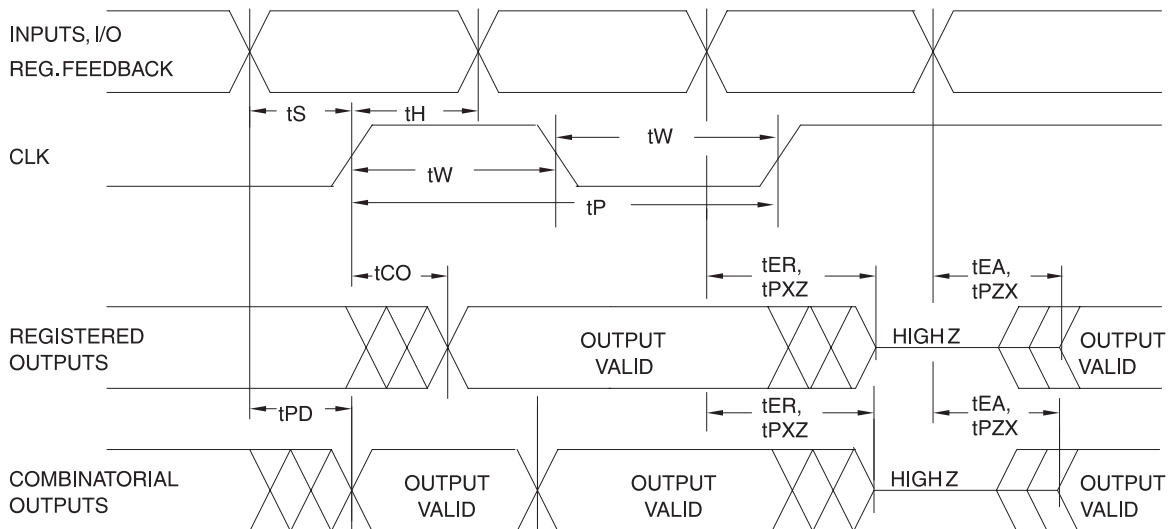
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|------------------------------------|---|------|-----|------------|---------|
| I_{IL} | Input or I/O Low Leakage Current | $0 \leq V_{IN} \leq V_{IL}(\text{Max})$ | | | -10 | μA |
| I_{IH} | Input or I/O High Leakage Current | $3.5 \leq V_{IN} \leq V_{CC}$ | | | 10 | μA |
| I_{CC1} | Power Supply Current | 15 MHz, $V_{CC} = \text{Max}$, $V_{IN} = 0$, V_{CC} , Outputs Open | Com | | 95 | mA |
| | | | Ind. | | 105 | mA |
| $I_{CC}^{(1)}$ | Power Supply Current, Standby Mode | 0 MHz, $V_{CC} = \text{Max}$, $V_{IN} = 0$, V_{CC} , Outputs Open | Com. | 5 | | μA |
| | | | Ind | 5 | | μA |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0.5V$; $V_{CC} = 5V$; $T_A = 25^\circ C$ | | | -150 | mA |
| V_{IL} | Input Low Voltage | $\text{Min} < V_{CC} < \text{Max}$ | -0.5 | | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | | $V_{CC}+1$ | V |
| V_{OL} | Output Low Voltage | $V_{CC} = \text{Min}$, All Outputs $I_{OL} = -16 \text{ mA}$ | | | 0.5 | V |

4.1 DC Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|---------------------|---|------------|-----|-----|-------|
| V_{OH} | Output High Voltage | $V_{CC} = \text{Min}$ $I_{OL} = -3.2 \text{ mA}$ | 2.4 | | | V |
| I_{OL} | Output Low Current | $V_{CC} = \text{Min}$ | Com. | 24 | | mA |
| | | | Ind. | 12 | | |
| I_{OH} | Output High Current | $V_{CC} = \text{Min}$ | Com., Ind. | 4 | | mA |

Note: 1. All I_{CC} parameters measured with outputs open. Data is based on Atmel test patterns. Reading may vary with pattern.

4.2 AC Waveforms⁽¹⁾



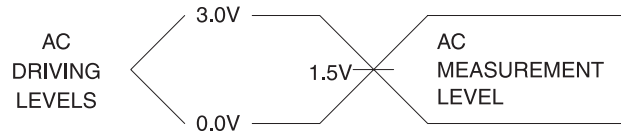
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

4.3 AC Characteristics

| Symbol | Parameter | -12 | | -15 | | Units |
|-----------|--|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | |
| t_{PD} | Input or Feedback to Non-registered Output | 3 | 12 | 3 | 15 | ns |
| t_{CF} | Clock to Feedback | | 6 | | 8 | ns |
| t_{CO} | Clock to Output | 2 | 8 | 2 | 10 | ns |
| t_S | Input or Feedback Setup Time | 10 | | 12 | | ns |
| t_H | Input Hold Time | 0 | | 0 | | ns |
| t_P | Clock Period | 12 | | 16 | | ns |
| t_W | Clock Width | 6 | | 8 | | ns |
| f_{MAX} | External Feedback $1/(t_S + t_{CO})$ | | 55 | | 45 | MHz |
| | Internal Feedback $1/(t_S + t_{CF})$ | | 62 | | 50 | MHz |
| | No Feedback $1/(t_P)$ | | 83 | | 62 | MHz |
| t_{EA} | Input to Output Enable – Product Term | 3 | 12 | 3 | 15 | ns |
| t_{ER} | Input to Output Disable – Product Term | 2 | 15 | 2 | 15 | ns |
| t_{PZX} | \overline{OE} pin to Output Enable | 2 | 12 | 2 | 15 | ns |
| t_{PZX} | \overline{OE} pin to Output Disable | 1.5 | 12 | 1.5 | 15 | ns |

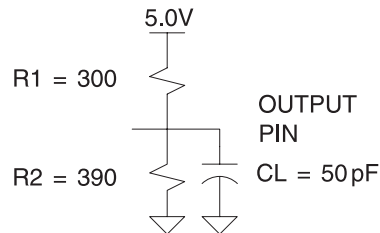
4.4 Input Test Waveforms

4.4.1 Input Test Waveforms and Measurement Levels



$$t_R, t_F < 1.5 \text{ ns (10% to 90%)}$$

4.4.2 Output Test Loads



Note: Similar devices are tested with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible devices.

4.4.3 Pin Capacitance

Table 4-1. Pin Capacitance (f = 1 MHz, T = 25°C⁽¹⁾)

| | Typ | Max | Units | Conditions |
|------------------|-----|-----|-------|-----------------------|
| C _{IN} | 5 | 8 | pF | V _{IN} = 0V |
| C _{OUT} | 6 | 8 | pF | V _{OUT} = 0V |

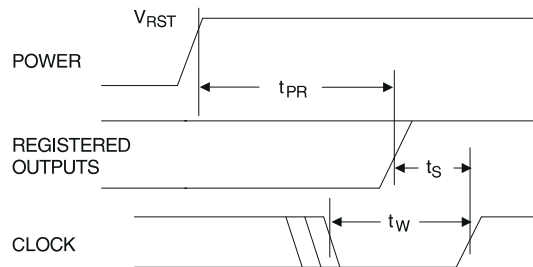
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

4.5 Power-up Reset

The ATF16V8CZ's registers are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic, from below 0.7V,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3. The signals from which the clock is derived must remain stable during t_{PR} .



| Parameter | Description | Typ | Max | Units |
|-----------|------------------------|-----|-------|-------|
| t_{PR} | Power-up Reset Time | 600 | 1,000 | ns |
| V_{RST} | Power-up Reset Voltage | 3.8 | 4.5 | V |

4.6 Preload of Registered Outputs

The ATF16V8CZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by approved programmers.

5. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8CZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

6. Input and I/O Pin-keeper Circuits

The ATF16V8CZ contains internal input and I/O pin-keeper circuits. These circuits allow each ATF16V8CZ pin to hold its previous value even when it is not being driven by an external source or by the device's output buffer. This helps insure that all logic array inputs are at known, valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin-keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin-keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40 μ A.

Figure 6-1. Input Diagram

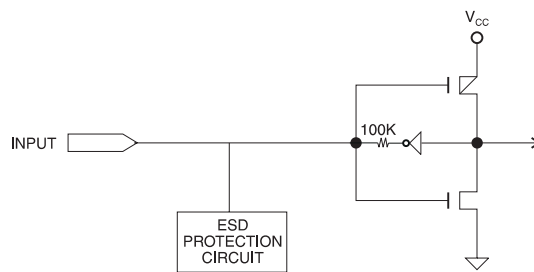
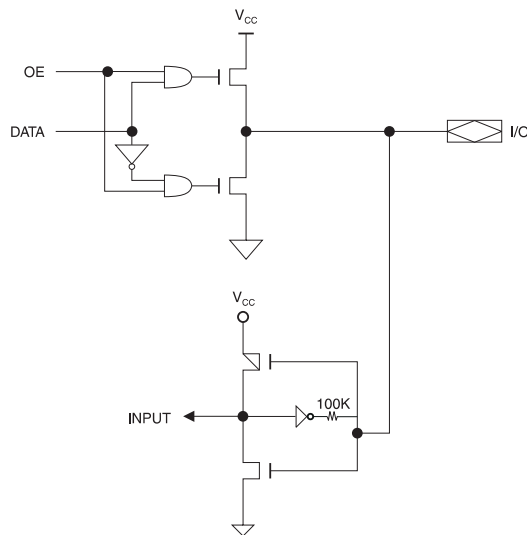


Figure 6-2. I/O Diagram



7. Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF16V8CZ architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8CZ can be configured in one of three different modes. Each mode makes the ATF16V8CZ look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8CZ universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8CZ can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the content of the ATF16V8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the security fuse.

Table 7-1. Compiler Mode Selection

| | Registered | Complex | Simple | Auto Select |
|-------------------------|--------------------------|---------------------------|---------------------------|-------------|
| ABEL, Atmel-ABEL | P16C8R | P16V8C | P16V8AS | P16V8 |
| CUPL | G16V8MS | G16V8MA | G16V8AS | G16V8A |
| LOG/iC | GAL16V8_R ⁽¹⁾ | GAL16V8_C7 ⁽¹⁾ | GAL16V8_C8 ⁽¹⁾ | GAL16V8 |
| OrCAD-PLD | “Registered” | “Complex” | “Simple” | GAL16V8A |
| PLDesigner | P16V8R | P16V8C | P16V8C | P16V8A |
| Tango-PLD | G16V8R | G16V8C | G16V8AS | G16V8 |

Notes: 1. Only applicable for version 3.4 or lower.

8. Macrocell Configuration

Software compilers support the three different OMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (\overline{OE}) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with \overline{OE} controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without \overline{OE} control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

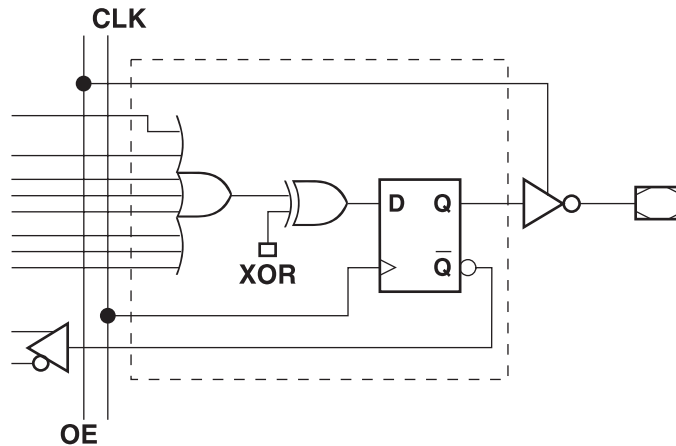
8.1 ATF16V8CZ Registered Mode

PAL Device Emulation/PAL Replacement. The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the \overline{OE} pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

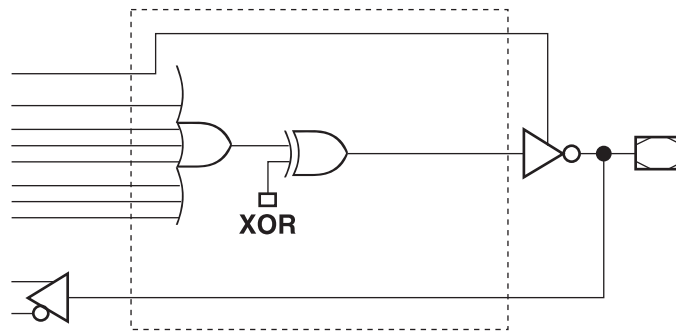
| | |
|------|-------|
| 16R8 | 16RP8 |
| 16R6 | 16RP6 |
| 16R4 | 16RP4 |

Figure 8-1. Registered Configuration for Registered Mode⁽¹⁾⁽²⁾



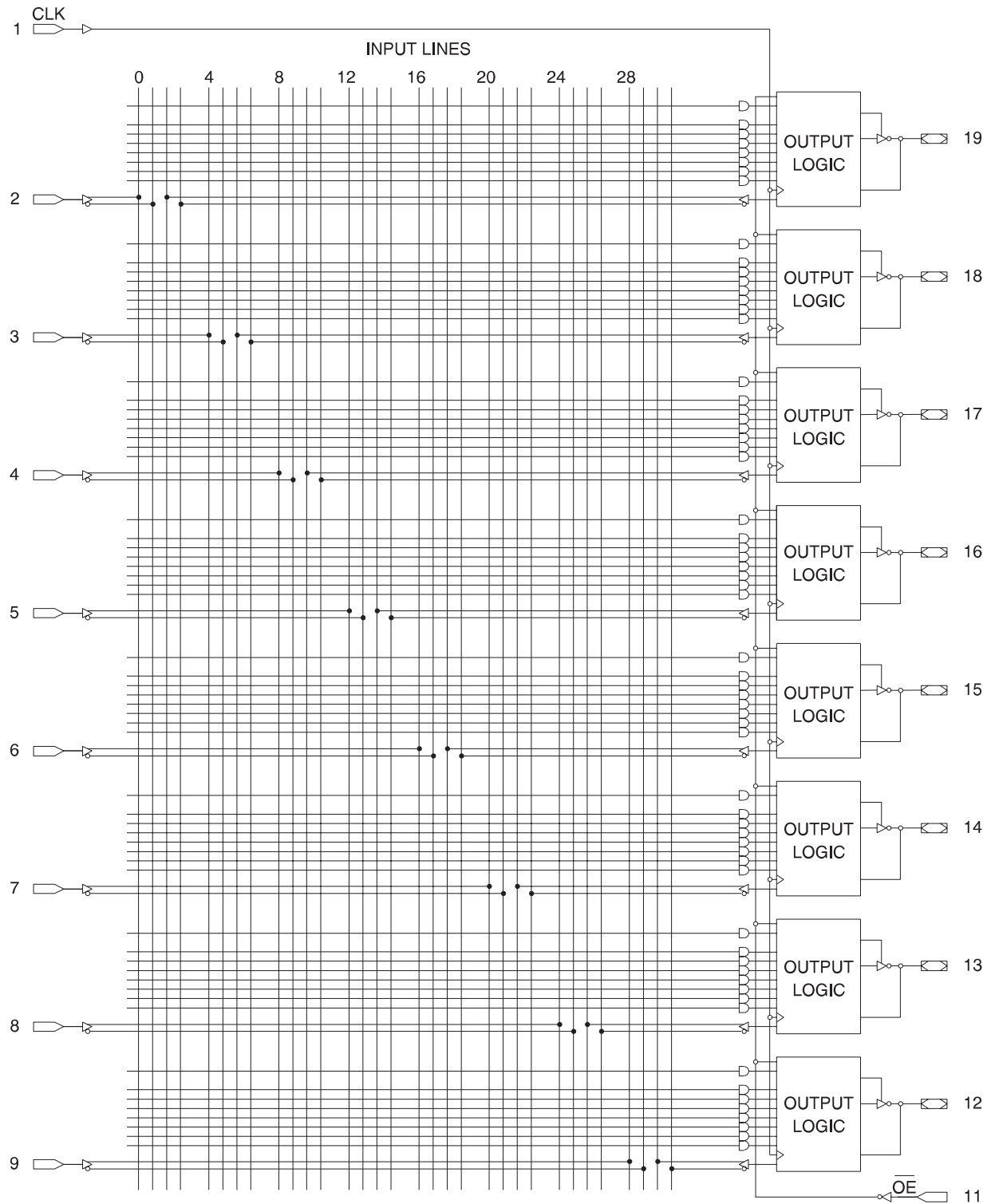
- Notes:
1. Pin 1 controls common CLK for the registered outputs.
Pin 11 controls common \overline{OE} for the registered outputs.
Pin 1 and Pin 11 are permanently configured as CLK and \overline{OE} .
 2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 8-2. Combinatorial Configuration for Registered Mode⁽¹⁾⁽²⁾



- Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and \overline{OE} .
 2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 8-3. Registered Mode Logic Diagram



8.2 ATF16V8CZ Complex Mode

PAL Device Emulation/PAL Replacement. In the complex mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

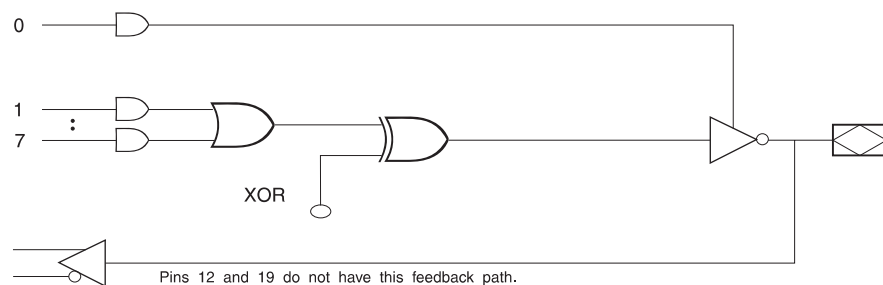
Combinatorial applications with an \overline{OE} requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8

16H8

16P8

Figure 8-4. Complex Mode Option



9. ATF16V8CZ Simple Mode

PAL Device Emulation/PAL Replacement. In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without \overline{OE} control. The following simple PALs can be emulated using this mode:

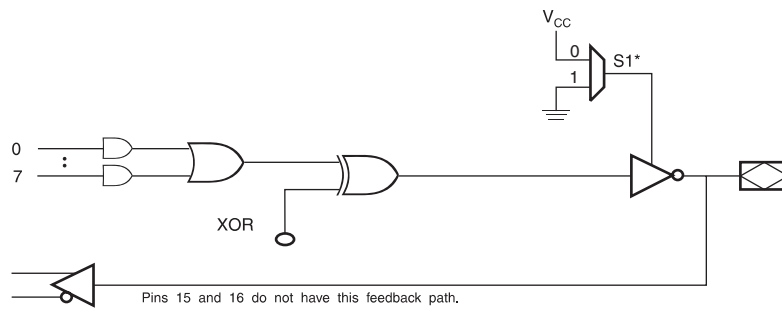
10L8 10H8 10P8

12L6 12H6 12P6

14L4 14H4 14P4

16L2 16H2 16P2

Figure 9-1. Simple Mode Option



* - Pins 15 and 16 are always enabled.

Figure 9-2. Complex Mode Logic Diagram

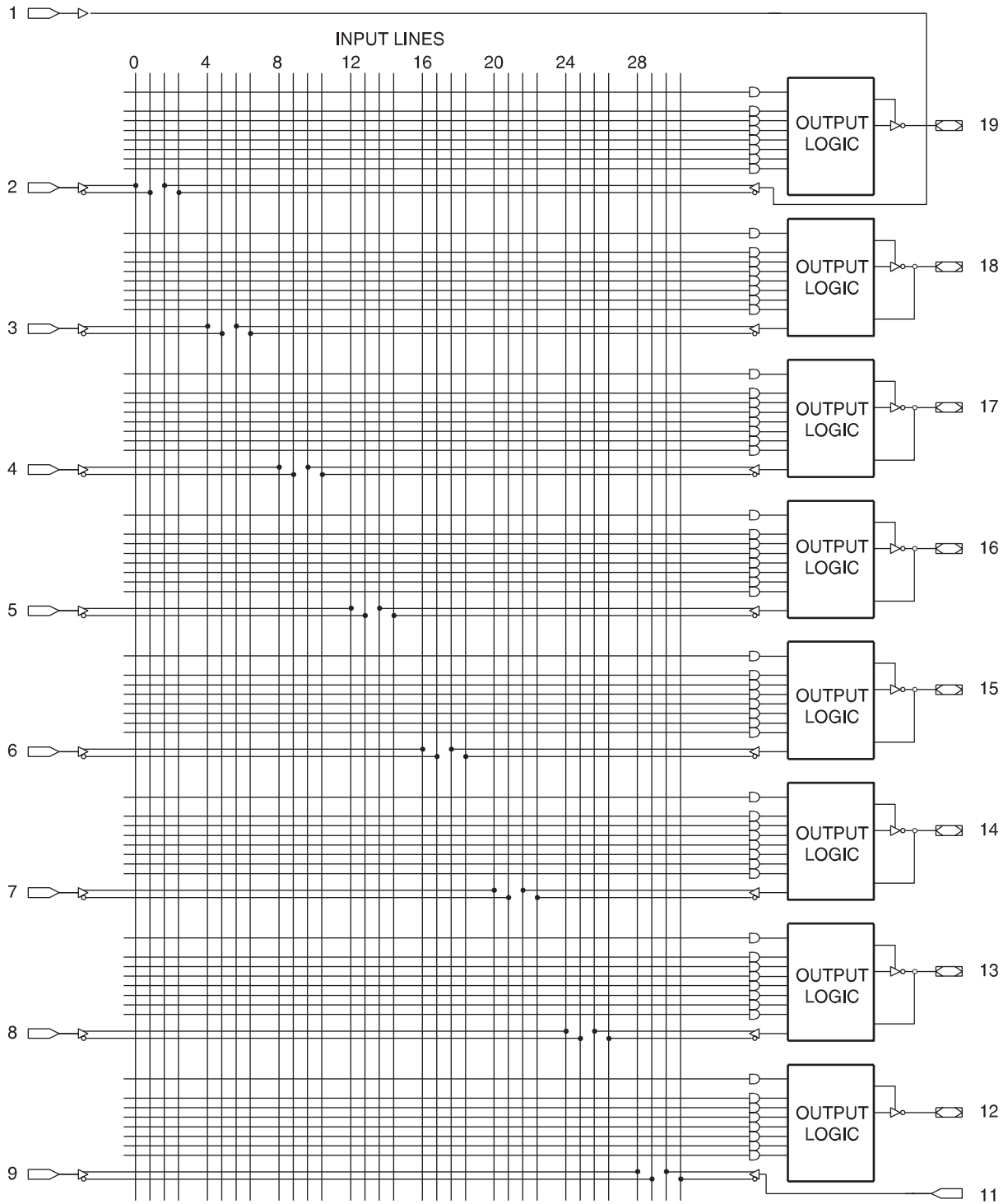
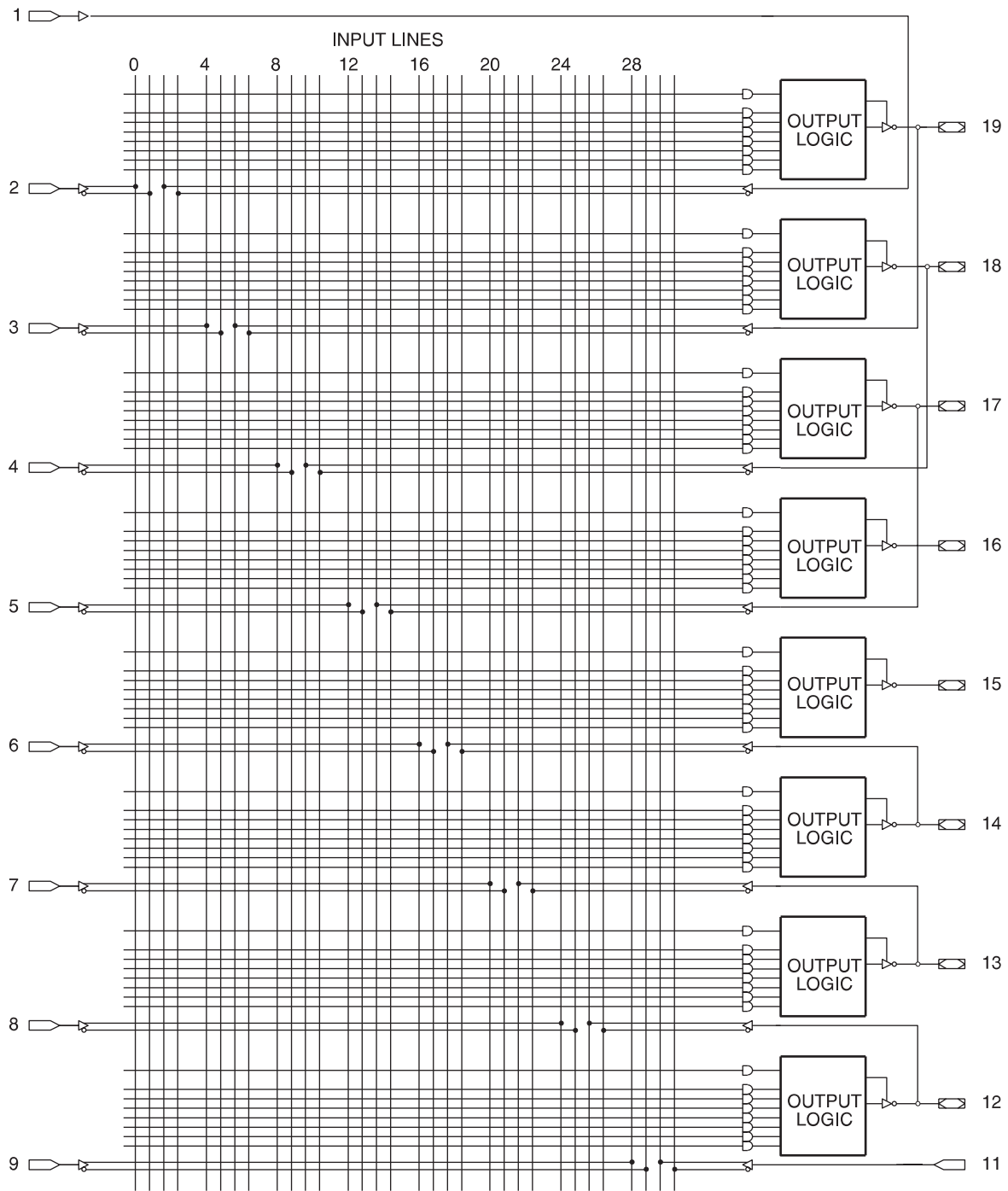
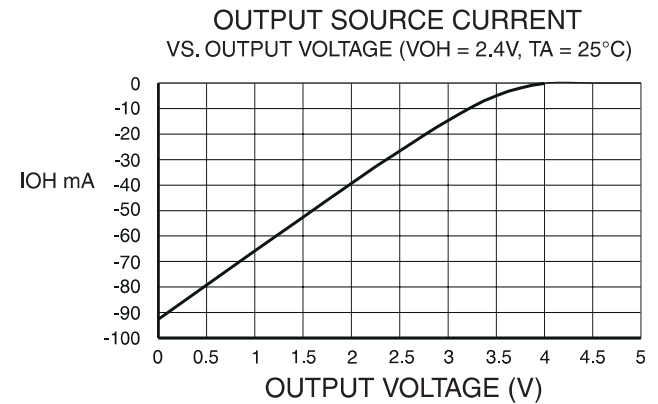
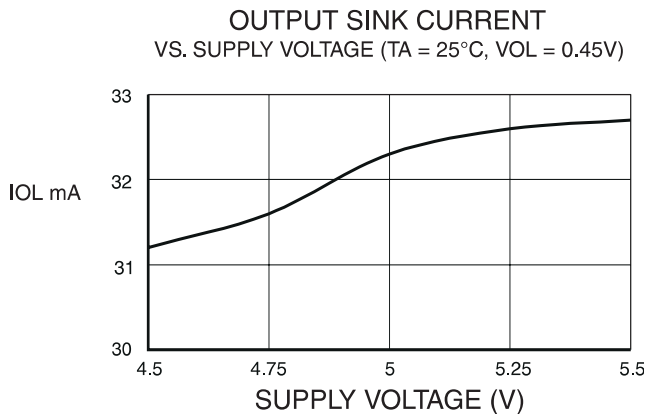
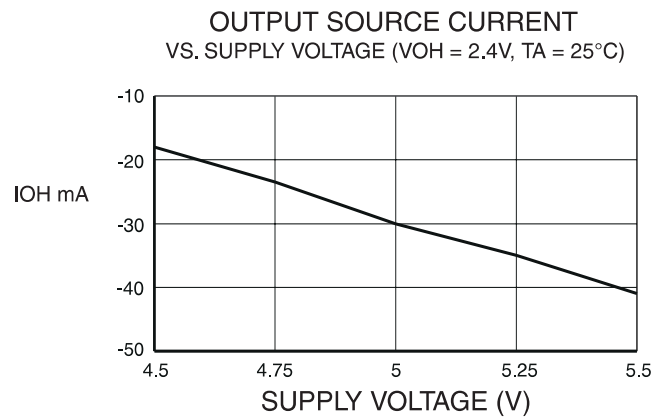
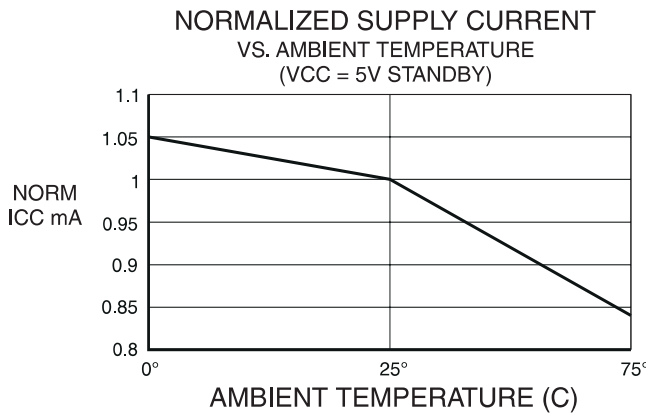
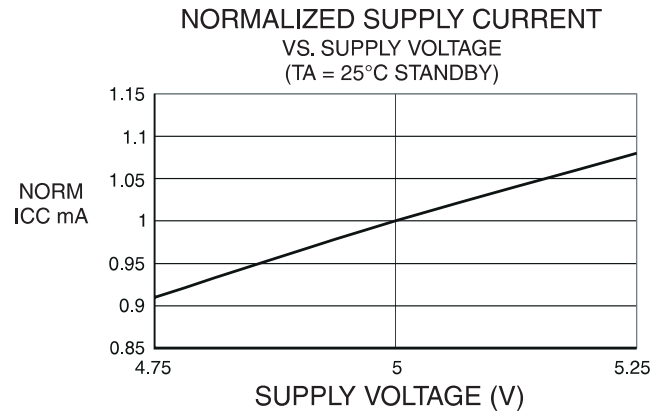
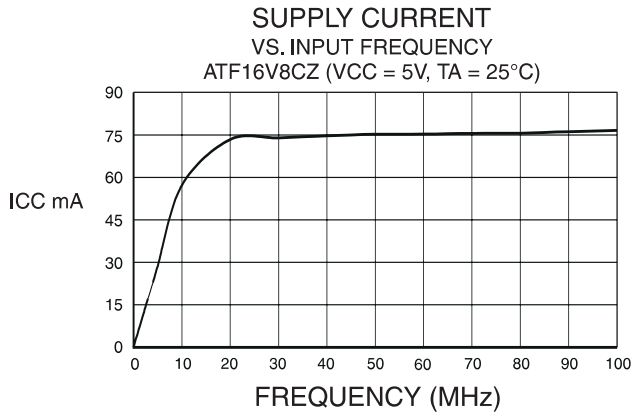


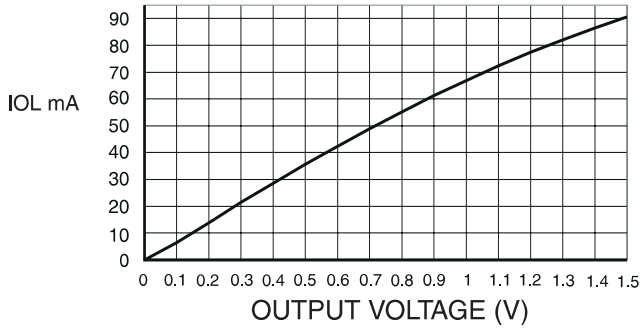
Figure 9-3. Simple Mode Logic Diagram



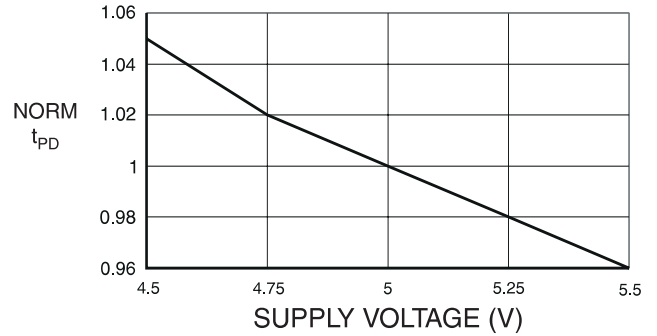
9.1 Test Characterization Data



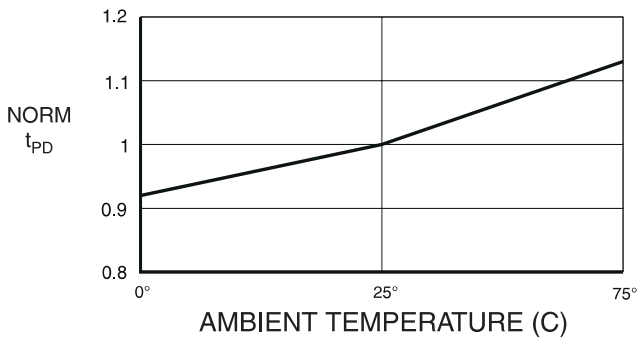
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)



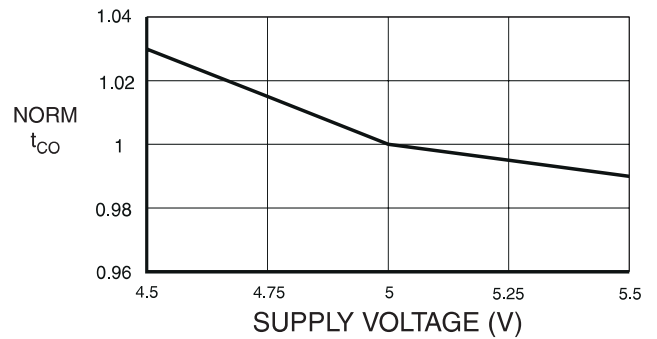
NORMALIZED t_{PD}
VS. SUPPLY VOLTAGE (TA = 25°C)



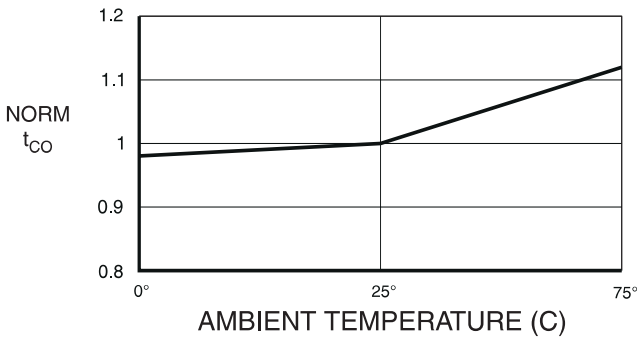
NORMALIZED t_{PD}
VS. AMBIENT TEMPERATURE (TA = 25°C)



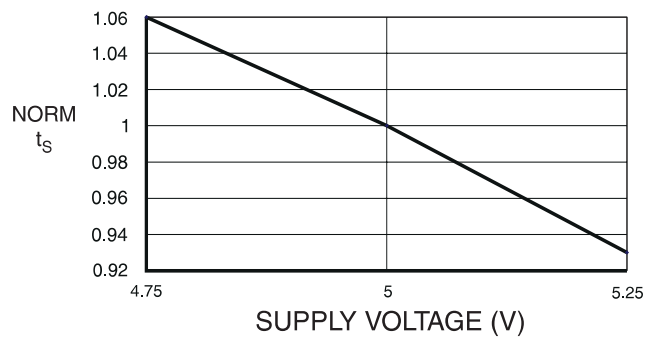
NORMALIZED t_{CO}
VS. SUPPLY VOLTAGE (TA = 25°C)

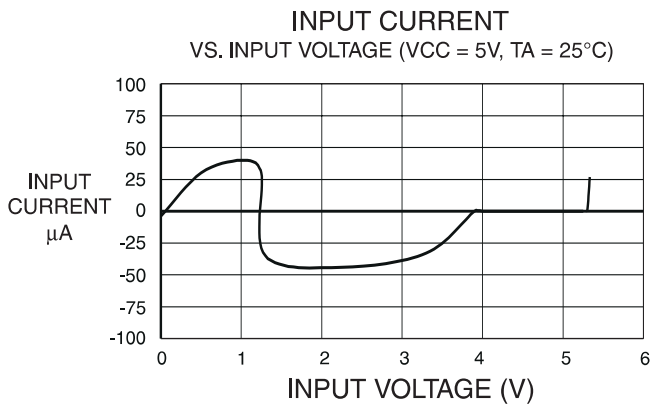
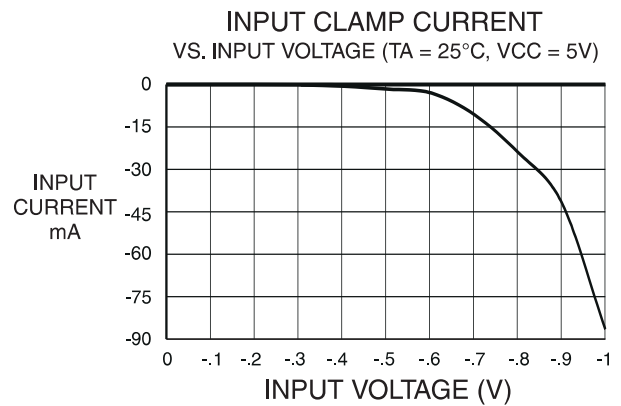
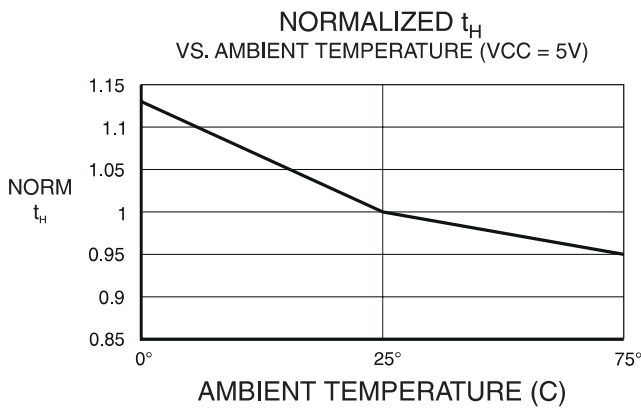
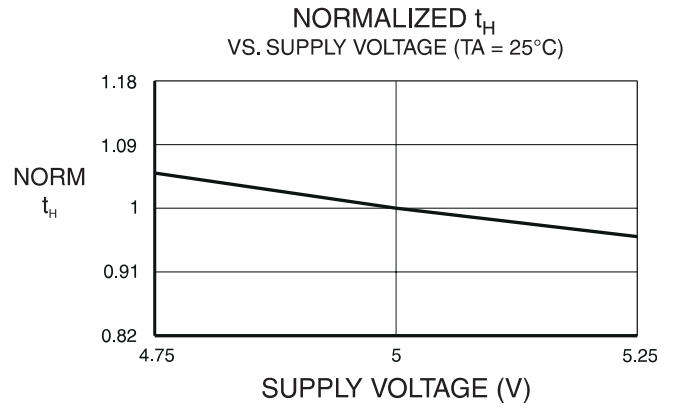
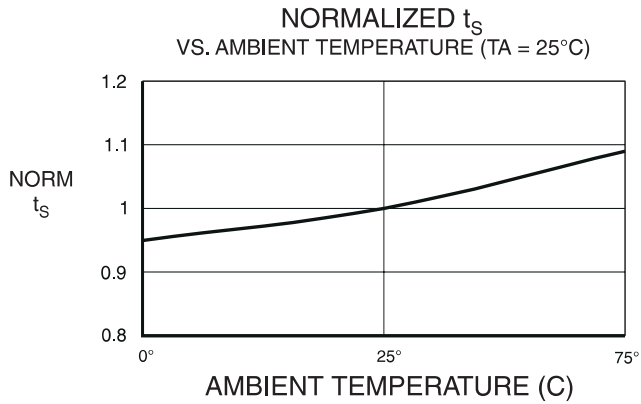


NORMALIZED t_{CO}
VS. AMBIENT TEMPERATURE (VCC = 5V)



NORMALIZED t_S
VS. SUPPLY VOLTAGE (TA = 25°C)





10. Ordering Information

10.1 Standard Package Options

| t_{PD} (ns) | t_s (ns) | t_{CO} (ns) | Ordering Code | Package | Operation Range |
|------------------|---------------|------------------|----------------|---------|-------------------------------|
| 12 | 10 | 8 | ATF16V8CZ-12JC | 20J | Commercial (0°C to 70°C) |
| | | | ATF16V8CZ-12PC | 20P3 | |
| | | | ATF16V8CZ-12SC | 20S | |
| | | | ATF16V8CZ-12XC | 20X | |
| 15 | 12 | 10 | ATF16V8CZ-15JC | 20J | Commercial (0°C to 70°C) |
| | | | ATF16V8CZ-15PC | 20P3 | |
| | | | ATF16V8CZ-15SC | 20S | |
| | | | ATF16V8CZ-15XC | 20X | |
| 15 | 12 | 10 | ATF16V8CZ-15JI | 20J | Industrial (-40°C to 85°C) |
| | | | ATF16V8CZ-15PI | 20P3 | |
| | | | ATF16V8CZ-15SI | 20S | |
| | | | ATF16V8CZ-15XI | 20X | |

Note: Shaded parts are being obsoleted in Q3-05 and being replaced by Green parts.

10.2 Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

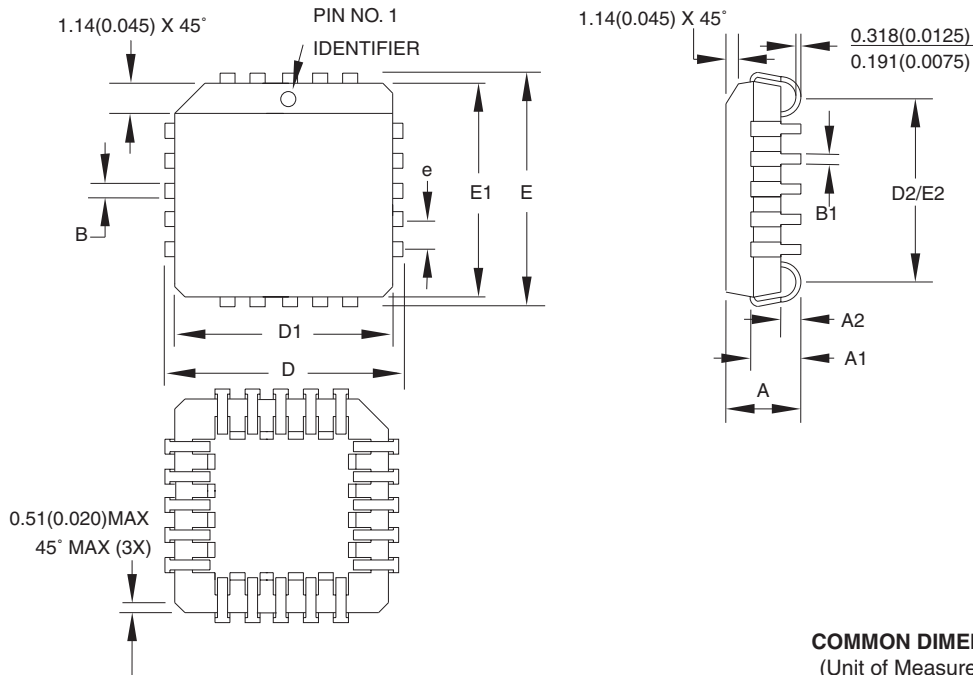
10.3 Green Package Options (Pb/Halide-free/RoHS Compliant)

| t_{PD} (ns) | t_s (ns) | t_{CO} (ns) | Ordering Code | Package | Operation Range |
|------------------|---------------|------------------|----------------|---------|-------------------------------|
| 15 | 12 | 10 | ATF16V8CZ-15JU | 20J | Industrial (-40°C to 85°C) |
| | | | ATF16V8CZ-15PU | 20P3 | |
| | | | ATF16V8CZ-15SU | 20S | |
| | | | ATF16V8CZ-15XU | 20X | |

| Package Type | |
|--------------|---|
| 20J | 20-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 20P3 | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20S | 20-lead, 0.300" Wide, Plastic Gull-wing Small Outline (SOIC) |
| 20X | 20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP) |

11. Package Information

11.1 20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | 4.191 | - | 4.572 | |
| A1 | 2.286 | - | 3.048 | |
| A2 | 0.508 | - | - | |
| D | 9.779 | - | 10.033 | |
| D1 | 8.890 | - | 9.042 | Note 2 |
| E | 9.779 | - | 10.033 | |
| E1 | 8.890 | - | 9.042 | Note 2 |
| D2/E2 | 7.366 | - | 8.382 | |
| B | 0.660 | - | 0.813 | |
| B1 | 0.330 | - | 0.533 | |
| e | 1.270 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

20J

REV.

B



11.2 20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | – | – | 5.334 | |
| A1 | 0.381 | – | – | |
| D | 24.892 | – | 26.924 | Note 2 |
| E | 7.620 | – | 8.255 | |
| E1 | 6.096 | – | 7.112 | Note 2 |
| B | 0.356 | – | 0.559 | |
| B1 | 1.270 | – | 1.551 | |
| L | 2.921 | – | 3.810 | |
| C | 0.203 | – | 0.356 | |
| eB | – | – | 10.922 | |
| eC | 0.000 | – | 1.524 | |
| e | 2.540 TYP | | | |

- Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

1/23/04



2325 Orchard Parkway
San Jose, CA 95131

TITLE

20P3, 20-lead (0.300"/7.62 mm Wide) Plastic Dual
Inline Package (PDIP)

DRAWING NO.

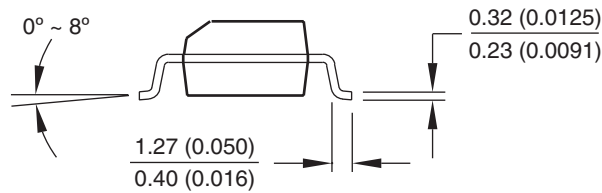
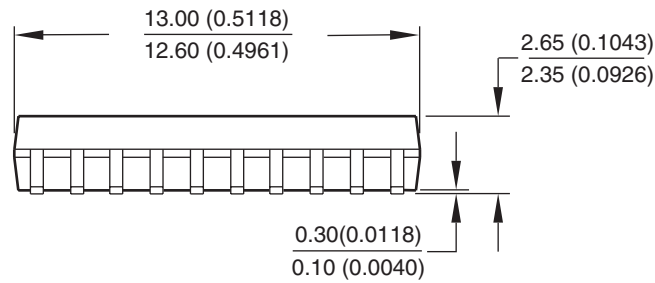
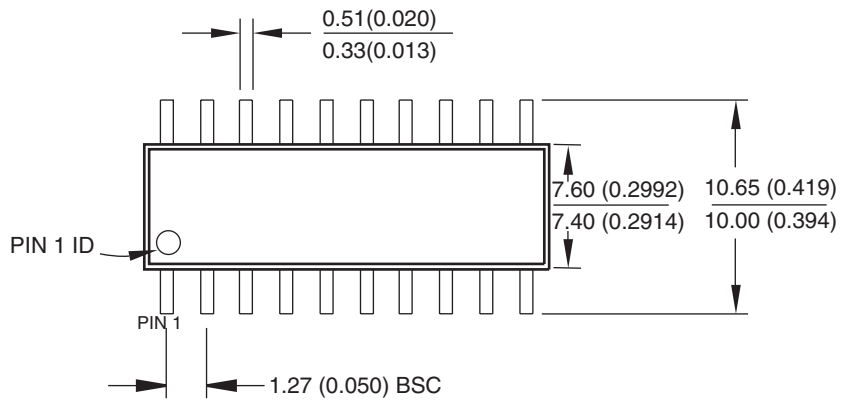
20P3

REV.

D

11.3 20S – SOIC

Dimensions in Millimeters and (Inches).
 Controlling dimension: Inches.
 JEDEC Standard MS-013



10/23/03



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

20S, 20-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC)

DRAWING NO.

20S

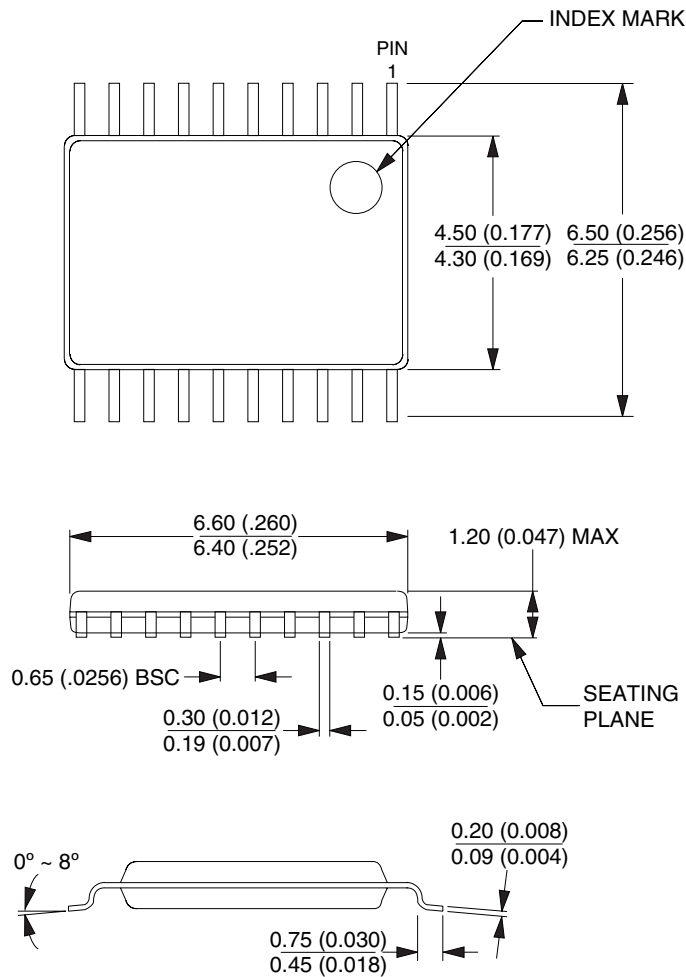
REV.

B



11.4 20X – TSSOP

Dimensions in Millimeters and (Inches).
 Controlling dimension: Millimeters.
 JEDEC Standard MO-153 AC



10/23/03



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

20X, (Formerly 20T), 20-lead, 4.4 mm Body Width,
 Plastic Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.

20X

REV.

C

12. Revision History

12.1 0453H

1. Green Package options added in 2005.



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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