XC95288XV High-Performance CPLD

DS050 (v3.0) June 25, 2007

Product Specification

Note: This product is being discontinued. You cannot order parts after May 14, 2008. Xilinx recommends replacing XC95288XV devices with equivalent XC95288XL devices in all designs as soon as possible. Recommended replacements are pin compatible, however require a V_{CC} change to 3.3V, and a recompile of the design file. In addition, there is no 1.8V I/O support, and only one output bank is supported. See **XCN07010** for details regarding this discontinuation, including device replacement recomendations for the XC95288XV CPLD.

Features

- 288 macrocells with 6,400 usable gates
- Available in small footprint packages
  - 144-pin TQFP (117 user I/O pins)
  - 208-pin PQFP (168 user I/O pins)
  - 280-pin CSP (192 user I/O pins)
  - 256-pin FBGA (192 user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Four separate output banks
  - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - 20 year data retention
  - ESD protection exceeding 2,000V

Description

The XC95288XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of 16 54V18 Function Blocks, providing 6,400 usable gates with propagation delays of 6 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

$$P_{TOTAL} = P_{INT} + P_{IO} = I_{CCINT} \times V_{CCINT} + P_{IO}$$

Separating internal and I/O power here is convenient because XC9500XV CPLDs also separate the corresponding power pins. P_{IO} is a strong function of the load capacitance driven, so it is handled by I = CVf. I_{CCINT} is another situation that reflects the actual design considered and the internal switching speeds. An estimation expression for I_{CCINT} (taken from simulation) is:

$$I_{CCINT}(mA) = MC_{HS}(0.122 \times PT_{HS} + 0.238) + MC_{LP}(0.042 \times PT_{LP} + 0.171) + 0.04(MC_{HS} + MC_{LP}) \times f_{MAX} \times MC_{TOG}$$

where:

MC_{HS} = # macrocells used in high speed mode

MC_{LP} = #macrocells used in low power mode

PT_{HS} = average p-terms used per high speed macrocell

PT_{LP} = average p-terms used over low power macrocell

f_{MAX} = max clocking frequency in the device

MC_{TOG} = % macrocells toggling on each clock (12% is frequently a good estimate

This calculation was derived from laboratory measurements of an XC9500XV part filled with 16-bit counters and allowing a single output (the LSB) to be enabled. The actual I_{CC} value varies with the design application and should be verified during normal system operation. Figure 1 shows the above estimation in a graphical form. For a more detailed discussion of power consumption in this device, see Xilinx

application note **XAPP361, "Planning for High Speed XC9500XV Designs."**

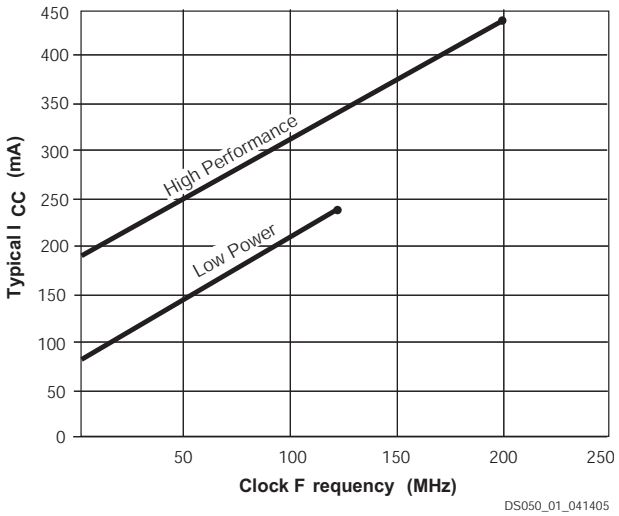


Figure 1: **Typical I_{CC} vs. Frequency for XC95288XV**

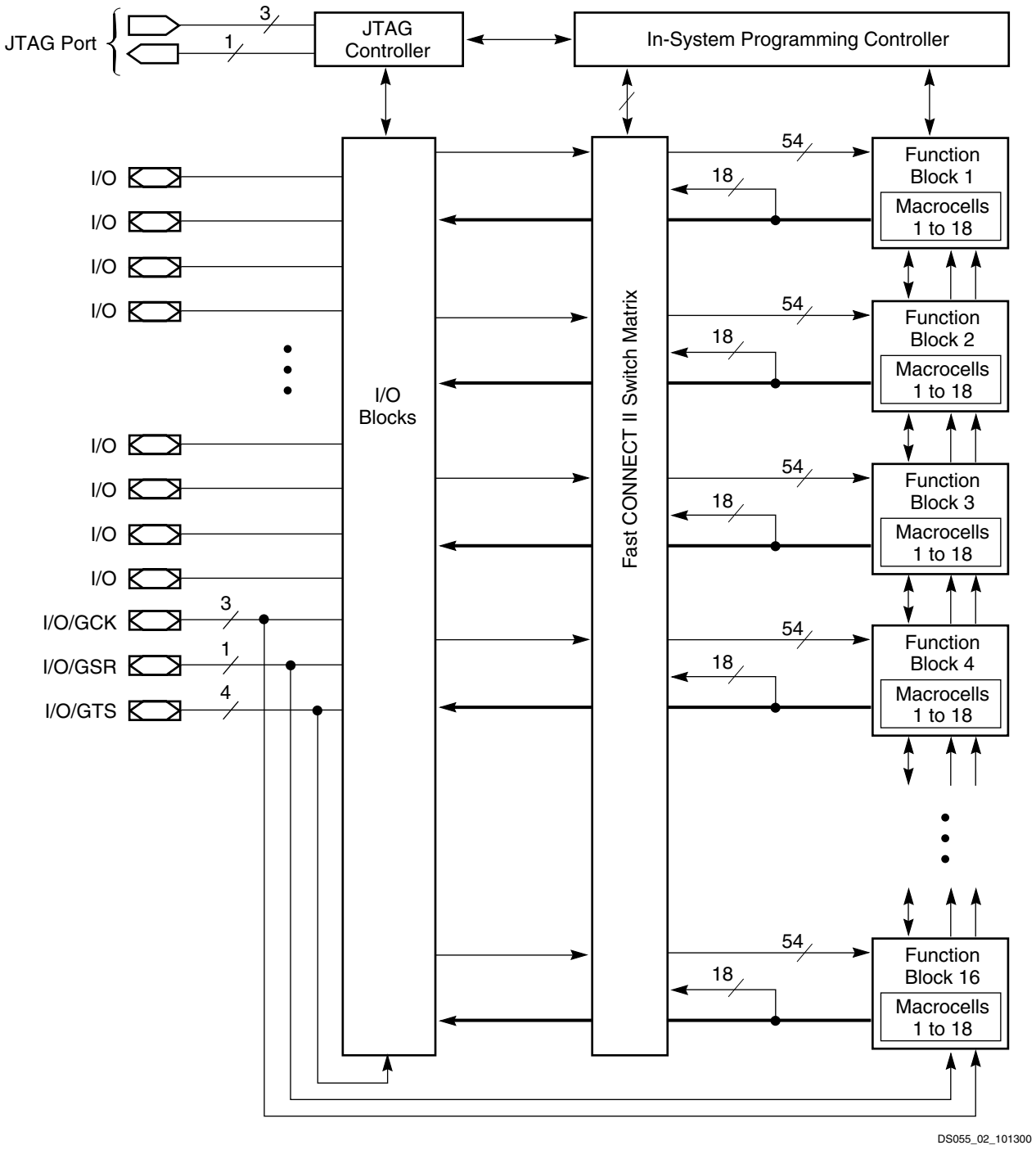


Figure 2: **XC95288XV Architecture**
(Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.)

Supported I/O Standards

Table 1: **IOSTANDARD Options**

IOSTANDARD	V_{CCIO}
LVTTL	3.3V
LVCMOS2	2.5V
X25TO18	1.8V

The XC95288XV CPLD features both LVCMOS and LVTTL I/O implementations. See Table 1 for I/O standard voltages.

The LVTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS2 standard is used in 2.5V applications.

XC9500XV CPLDs are also 1.8V I/O compatible. The X25TO18 setting is provided for generating 1.8V compatible outputs from a CPLD normally operating in a 2.5V environment. The ISE software automatically groups outputs with matching IOSTANDARD settings into the same V_{CCIO} bank when no location constraints are specified. The default I/O Standard for pads without IOSTANDARD attributes is LVTTL for XC9500XV devices.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 2.7	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 3.6	V
V_{IN}	Input voltage relative to GND(1)	–0.5 to 3.6	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 3.6	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to +3.6V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
3. For solder specifications, see **Xilinx Packaging**.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to +70°C	2.37	2.62	V
		Industrial T_A = –40°C to +85°C	2.37	2.62	
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.37	2.62	V
	Supply voltage for output drivers for 1.8V operation		1.71	1.89	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		1.7	3.6	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/Erase cycles (endurance)	1,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

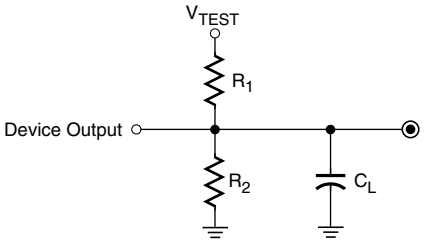
DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –1.0 mA	2.0	-	V
	Output high voltage for 1.8V outputs	I_{OH} = –100 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 1.0 mA	-	0.4	V
	Output low voltage for 1.8V outputs	I_{OL} = 100 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = 2.62V V_{CCIO} = 3.6V V_{IN} = GND or 3.6V	-	±10	µA
I_{IH}	Input high-Z leakage current	V_{CC} = 2.62V V_{CCIO} = 3.6V V_{IN} = GND or 3.6V	-	±10	µA
		V_{CC} min < V_{IN} < 3.6V	-	±150	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz	-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	59		mA

AC Characteristics

Symbol	Parameter	XC95288XV-6		XC95288XV-7		XC95288XV-10		Units
		Min	Max	Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	6.0	-	7.5	-	10	ns
T_{SU}	I/O setup time before GCK	4.0	-	4.8	-	6.5	-	ns
T_H	I/O hold time after GCK	0	-	0	-	0	-	ns
T_{CO}	GCK to output valid	-	3.8	-	4.5	-	5.8	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	208	-	125.0	-	100.0	MHz
T_{PSU}	I/O setup time before p-term clock input	1.0	-	1.6	-	2.1	-	ns
T_{PH}	I/O hold time after p-term clock input	2.6	-	3.2	-	4.4	-	ns
T_{PCO}	P-term clock output valid	-	6.8	-	7.7	-	10.2	ns
T_{OE}	GTS to output valid	-	4.5	-	5.0	-	7.0	ns
T_{OD}	GTS to output disable	-	4.5	-	5.0	-	7.0	ns
T_{POE}	Product term OE to output enabled	-	8.4	-	9.5	-	11.0	ns
T_{POD}	Product term OE to output disabled	-	8.4	-	9.5	-	11.0	ns

Symbol	Parameter	XC95288XV-6		XC95288XV-7		XC95288XV-10		Units
		Min	Max	Min	Max	Min	Max	
T_{AO}	GSR to output valid	-	10.8	-	12.0	-	14.5	ns
T_{PAO}	P-term S/R to output valid	-	11.8	-	12.6	-	15.3	ns
T_{WLH}	GCK pulse width (High or Low)	2.4	-	4.0	-	5.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	6.0	-	6.5	-	7.0	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	6.0	-	6.5	-	7.0	-	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3V	3.3V	320Ω	360Ω	35 pF
	2.5V	2.5V	250Ω	660Ω	35 pF
	1.8V	1.8V	10KΩ	14KΩ	35 pF

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Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XC95288XV-6		XC95288XV-7		XC95288XV-10		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
T_{IN}	Input buffer delay	-	2.2	-	2.3	-	3.5	ns
T_{GCK}	GCK buffer delay	-	1.2	-	1.5	-	1.8	ns
T_{GSR}	GSR buffer delay	-	2.2	-	3.1	-	4.5	ns
T_{GTS}	GTS buffer delay	-	4.5	-	5.0	-	7.0	ns
T_{OUT}	Output buffer delay	-	2.4	-	2.5	-	3.0	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	-	0	ns
Product Term Control Delays								
T_{PTCK}	Product term clock delay	-	2.0	-	2.4	-	2.7	ns
T_{PTSR}	Product term set/reset delay	-	1.0	-	1.4	-	1.8	ns
T_{PTTS}	Product term 3-state delay	-	6.2	-	7.2	-	7.5	ns
Internal Register and Combinatorial Delays								
T_{PDI}	Combinatorial logic propagation delay	-	0.4	-	1.3	-	1.7	ns
T_{SUI}	Register setup time	2.0	-	2.6	-	3.0	-	ns
T_{HI}	Register hold time	1.6	-	2.2	-	3.5	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.6	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	1.6	-	2.2	-	3.5	-	ns
T_{COI}	Register clock to output valid time	-	0.2	-	0.5	-	1.0	ns
T_{AOI}	Register async. S/R to output delay	-	6.2	-	6.4	-	7.0	ns
T_{RAI}	Register async. S/R recover before clock	6.0	-	7.5		10.0	-	ns
T_{LOGI}	Internal logic delay	-	1.0	-	1.4	-	1.8	ns
T_{LOGILP}	Internal low power logic delay	-	5.5	-	6.4	-	7.3	ns
Feedback Delays								
T_F	Fast CONNECT II feedback delay	-	1.6	-	3.5	-	4.2	ns
Time Adders								
T_{PTA}	Incremental product term allocator delay	-	0.8	-	0.8	-	1.0	ns
T_{PTA2}	Adjacent macrocell p-term allocator delay	-	0.3	-	0.3	-	0.4	ns
T_{SLEW}	Slew-rate limited delay	-	3.5	-	4.0	-	4.5	ns

XC95288XV I/O Pins

Function Block	Macro-cell	TQ144	PQ208	FG256	CS280	BScan Order	Bank	Function Block	Macro-cell	TQ144	PQ208	FG256	CS280	BScan Order	Bank
1	1	-	-	-	-	861	-	3	1	-	-	-	-	753	-
1	2	-	28	H1	K2	858	1	3	2	28	38	L2	N2	750	1
1	3	-	29	H5	K3	855	1	3	3	-	39	L5	P1	747	1
1	4	-	-	-	-	852	-	3	4	-	-	-	-	744	-
1	5	20	30	J1	K4	849	1	3	5	-	40	M1	P2	741	1
1	6	21	31	J5	L1	846	1	3	6	-	41	L4	P3	738	1
1	7	-	-	-	-	843	-	3	7	-	-	-	-	735	-
1	8	22	32	J2	L2	840	1	3	8	-	43	N1	P4	732	1
1	9	-	-	J3	L3	837	1	3	9	-	-	L3	R1	729	1
1	10	23	33	K1	L4	834	1	3	10	30(1)	44(1)	M2(1)	R3(1)	726	1
1	11	-	-	J4	M1	831	1	3	11	-	-	M4	R2	723	1
1	12	24	34	K2	M2	828	1	3	12	31	45	P1	R4	720	1
1	13	-	-	-	-	825	-	3	13	-	-	-	-	717	-
1	14	25	35	K5	M3	822	1	3	14	32(1)	46(1)	M3(1)	T1(1)	714	1
1	15	26	36	L1	M4	819	1	3	15	33	47	N2	T2	711	1
1	16	-	-	-	-	816	-	3	16	-	-	-	-	708	-
1	17	27	37	K3	N1	813	1	3	17	-	48	N4	T3	705	1
1	18	-	-	-	-	810	-	3	18	-	-	-	-	702	-
2	1	-	-	-	-	807	-	4	1	-	-	-	-	699	-
2	2	9	15	D1	G3	804	2	4	2	2(1)	3(1)	D3(1)	C2(1)	696	2
2	3	10	16	G4	G2	801	2	4	3	-	4	D2	B1	693	2
2	4	-	-	-	-	798	-	4	4	-	-	-	-	690	-
2	5	11	17	E1	G1	795	2	4	5	3(1)	5(1)	E3(1)	C1(1)	687	2
2	6	12	18	G3	G4	792	2	4	6	4	6	C2	D4	684	2
2	7	-	-	-	-	789	-	4	7	-	-	-	-	681	-
2	8	13	19	G2	H1	786	2	4	8	5(1)	7(1)	D4(1)	D3(1)	678	2
2	9	-	-	F5	H3	783	2	4	9	-	-	B1	D2	675	2
2	10	14	20	F1	H2	780	2	4	10	-	8	E4	D1	672	2
2	11	-	-	G5	H4	777	2	4	11	-	-	C1	E3	669	2
2	12	15	21	H2	J1	774	2	4	12	6(1)	9(1)	E5(1)	E2(1)	666	2
2	13	-	-	-	-	771	-	4	13	-	-	-	-	663	-
2	14	16	22	H4	J2	768	2	4	14	7	10	E2	E4	660	2
2	15	17	23	G1	J3	765	2	4	15	-	12	F2	F3	657	2
2	16	-	-	-	-	762	-	4	16	-	-	-	-	654	-
2	17	19	25	H3	J4	759	2	4	17	-	14	E6	F4	651	2
2	18	-	-	-	-	756	-	4	18	-	-	-	-	648	-

Notes:
1. Global control pin

XC95288XV I/O Pins (continued)

Function Block	Macro-cell	TQ144	PQ208	FG256	CS280	BScan Order	Bank	Function Block	Macro-cell	TQ144	PQ208	FG256	CS280	BScan Order	Bank
5	1	-	-	-	-	645	-	7	1	-	-	-	-	537	-
5	2	34	49	R1	U1	642	1	7	2	-	62	R3	W5	534	1
5	3	-	50	N3	V1	639	1	7	3	45	63	M6	U6	531	1
5	4	-	-	-	-	636	-	7	4	-	-	-	-	528	-
5	5	35	51	P2	U2	633	1	7	5	46	64	T3	V6	525	1
5	6	-	54	P4	V3	630	1	7	6	-	66	T4	W6	522	1
5	7	-	-	-	-	627	-	7	7	-	-	-	-	519	-
5	8	38(1)	55(1)	P5(1)	W2(1)	624	1	7	8	-	67	P7	U7	516	1
5	9	-	-	T2	W3	621	1	7	9	-	-	T5	V7	513	1
5	10	39	56	N5	T4	618	1	7	10	-	69	N7	W7	510	1
5	11	-	-	R4	U4	615	1	7	11	-	-	R7	T7	507	1
5	12	40	57	M5	V4	612	1	7	12	48	70	M7	W8	504	1
5	13	-	-	-	-	609	-	7	13	-	-	-	-	501	-
5	14	41	58	R5	W4	606	1	7	14	-	71	T6	U8	498	1
5	15	43	60	R6	V5	603	1	7	15	49	72	N8	V8	495	1
5	16	-	-	-	-	600	-	7	16	-	-	-	-	492	-
5	17	44	61	N6	T5	597	1	7	17	-	73	T7	T8	489	1
5	18	-	-	-	-	594	-	7	18	-	-	-	-	486	-
6	1	-	-	-	-	591	-	8	1	-	-	-	-	483	-
6	2	135	197	A5	D7	588	2	8	2	130	186	E11	B10	480	2
6	3	136	198	D6	A6	585	2	8	3	131	187	A8	C10	477	2
6	4	-	-	-	-	582	-	8	4	-	-	-	-	474	-
6	5	137	199	B5	B6	579	2	8	5	132	188	C8	D10	471	2
6	6	138	200	C6	C6	576	2	8	6	-	189	B8	A9	468	2
6	7	-	-	-	-	573	-	8	7	-	-	-	-	465	-
6	8	139	201	A4	D6	570	2	8	8	133	191	D8	B9	462	2
6	9	-	-	E7	A5	567	2	8	9	-	-	A7	C9	459	2
6	10	140	202	A3	C5	564	2	8	10	134	192	E9	D9	456	2
6	11	-	-	C5	B5	561	2	8	11	-	-	B7	A8	453	2
6	12	-	203	A2	D5	558	2	8	12	-	193	D7	B8	450	2
6	13	-	-	-	-	555	-	8	13	-	-	-	-	447	-
6	14	142	205	B4	B4	552	2	8	14	-	194	A6	C8	444	2
6	15	143(1)	206(1)	C4(1)	C4(1)	549	2	8	15	-	195	B6	B7	441	2
6	16	-	-	-	-	546	-	8	16	-	-	-	-	438	-
6	17	-	208	B3	A3	543	2	8	17	-	196	E8	C7	435	2
6	18	-	-	-	-	540	-	8	18	-	-	-	-	432	-

Notes:
1. Global control pin

XC95288XV I/O Pins (continued)

Function Block	Macro-cell	TQ144	PQ208	FG256	CS280	BScan Order	Bank	Function Block	Macro-cell	TQ144	PQ208	FG256	CS280	BScan Order	Bank
9	1	-	-	-	-	429	-	11	1	-	-	-	-	321	-
9	2	50	74	R8	U9	426	3	11	2	-	87	P10	W13	318	3
9	3	51	75	P8	T9	423	3	11	3	60	88	T12	V13	315	3
9	4	-	-	-	-	420	-	11	4	-	-	-	-	312	-
9	5	52	76	T8	W10	417	3	11	5	61	89	N10	U13	309	3
9	6	53	77	M8	V10	414	3	11	6	-	90	T13	T13	306	3
9	7	-	-	-	-	411	-	11	7	-	-	-	-	303	-
9	8	54	78	T9	U10	408	3	11	8	-	91	M11	W14	300	3
9	9	-	-	P9	W11	405	3	11	9	-	-	N11	T14	297	3
9	10	-	80	R9	V11	402	3	11	10	64	95	T14	W15	294	3
9	11	56	82	M9	U11	399	3	11	11	66	97	R12	V15	291	3
9	12	57	83	T10	T11	396	3	11	12	68	99	T15	W16	288	3
9	13	-	-	-	-	393	-	11	13	-	-	-	-	285	-
9	14	58	84	M10	W12	390	3	11	14	69	100	R14	U16	282	3
9	15	-	85	R10	V12	387	3	11	15	-	101	N13	W17	279	3
9	16	-	-	-	-	384	-	11	16	-	-	-	-	276	-
9	17	59	86	T11	T12	381	3	11	17	70	102	R13	W18	273	3
9	18	-	-	-	-	378	-	11	18	-	-	-	-	270	-
10	1	-	-	-	-	375	-	12	1	-	-	-	-	267	-
10	2	117	170	B11	C14	372	4	12	2	110	158	B13	B19	264	4
10	3	118	171	D11	B14	369	4	12	3	111	159	B14	B18	261	4
10	4	-	-	-	-	366	-	12	4	-	-	-	-	258	-
10	5	119	173	A11	A14	363	4	12	5	112	160	C13	B17	255	4
10	6	120	174	D10	C13	360	4	12	6	-	161	A15	A18	252	4
10	7	-	-	-	-	357	-	12	7	-	-	-	-	249	-
10	8	121	175	B10	B13	354	4	12	8	113	162	C12	A17	246	4
10	9	-	-	E12	A13	351	4	12	9	-	-	B12	D16	243	4
10	10	124	178	F12	A12	348	4	12	10	115	164	D13	C16	240	4
10	11	125	179	B9	C12	345	4	12	11	-	165	A14	B16	237	4
10	12	126	180	C9	B12	342	4	12	12	116	166	E13	A16	234	4
10	13	-	-	-	-	339	-	12	13	-	-	-	-	231	-
10	14	128	182	A9	B11	336	4	12	14	-	167	A13	C15	228	4
10	15	-	183	D9	C11	333	4	12	15	-	168	C11	B15	225	4
10	16	-	-	-	-	330	-	12	16	-	-	-	-	222	-
10	17	129	185	E10	A10	327	4	12	17	-	169	A12	D15	219	4
10	18	-	-	-	-	324	-	12	18	-	-	-	-	216	-

XC95288XV I/O Pins (continued)

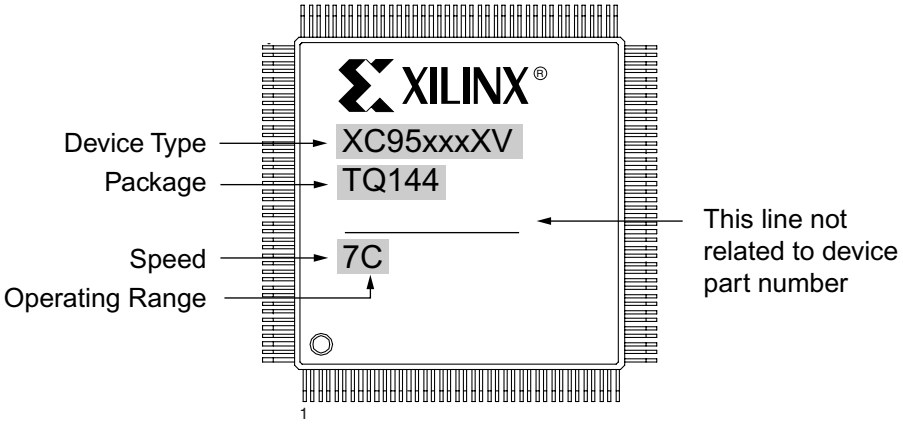
Function Block	Macro-cell	TQ144	PQ208	FG256	CS280	BScan Order	Bank	Function Block	Macro-cell	TQ144	PQ208	FG256	CS280	BScan Order	Bank
13	1	-	-	-	-	213	-	15	1	-	-	-	-	105	-
13	2	71	103	P13	V17	210	3	15	2	79	117	M12	P16	102	3
13	3	-	106	P15	U18	207	3	15	3	80	118	M16	P19	99	3
13	4	-	-	-	-	204	-	15	4	-	-	-	-	96	-
13	5	-	107	N14	V19	201	3	15	5	-	119	K14	N17	93	3
13	6	-	109	R16	U19	198	3	15	6	-	120	L16	N18	90	3
13	7	-	-	-	-	195	-	15	7	-	-	-	-	87	-
13	8	74	110	N15	T16	192	3	15	8	81	121	K13	N19	84	3
13	9	-	-	M15	T17	189	3	15	9	-	-	K15	N16	81	3
13	10	-	111	M13	T18	186	3	15	10	82	122	L12	M19	78	3
13	11	75	112	P16	T19	183	3	15	11	83	123	K16	M17	75	3
13	12	-	113	N16	R18	180	3	15	12	85	125	J14	M16	72	3
13	13	-	-	-	-	177	-	15	13	-	-	-	-	69	-
13	14	76	114	M14	R16	174	3	15	14	86	126	J15	L19	66	3
13	15	77	115	L15	R19	171	3	15	15	87	127	J13	L18	63	3
13	16	-	-	-	-	168	-	15	16	-	-	-	-	60	-
13	17	78	116	L13	P17	165	3	15	17	88	128	J16	L17	57	3
13	18	-	-	-	-	162	-	15	18	-	-	-	-	54	-
14	1	-	-	-	-	159	-	16	1	-	-	-	-	51	-
14	2	-	144	F15	G19	156	4	16	2	91	131	K12	L16	48	4
14	3	100	145	E15	G16	153	4	16	3	92	133	J12	K18	45	4
14	4	-	-	-	-	150	-	16	4	-	-	-	-	42	-
14	5	101	146	F13	F19	147	4	16	5	93	134	H15	K17	39	4
14	6	102	147	D16	F18	144	4	16	6	94	135	H14	K16	36	4
14	7	-	-	-	-	141	-	16	7	-	-	-	-	33	-
14	8	103	148	F14	F17	138	4	16	8	95	136	G16	J19	30	4
14	9	-	-	C16	F16	135	4	16	9	-	-	H13	J18	27	4
14	10	104	149	E14	E19	132	4	16	10	96	137	G15	J17	24	4
14	11	105	150	D15	E17	129	4	16	11	97	138	H16	J16	21	4
14	12	-	151	G12	E18	126	4	16	12	98	139	F16	H19	18	4
14	13	-	-	-	-	123	-	16	13	-	-	-	-	15	-
14	14	106	152	C15	E16	120	4	16	14	-	140	H12	H18	12	4
14	15	107	154	D14	D18	117	4	16	15	-	142	E16	H17	9	4
14	16	-	-	-	-	114	-	16	16	-	-	-	-	6	-
14	17	-	155	B16	D17	111	4	16	17	-	143	G14	H16	3	4
14	18	-	-	-	-	108	-	16	18	-	-	-	-	0	-

XC95288XV Global, JTAG and Power Pins

Pin Type	TQ144	PQ208	FG256	CS280
I/O/GCK1	30	44	M2	R3
I/O/GCK2	32	46	M3	T1
I/O/GCK3	38	55	P5	W2
I/O/GTS1	5	7	D4	D3
I/O/GTS2	6	9	E5	E2
I/O/GTS3	2	3	D3	C2
I/O/GTS4	3	5	E3	C1
I/O/GSR	143	206	C4	C4
TCK	67	98	P12	T15
TDI	63	94	R11	U14
TDO(1)	122	176	A10	D13
TMS	65	96	N12	U15
V_{CCINT} 2.5V	8, 42, 84, 141	11, 59, 124, 153, 204	F4, G6, H6, J6, K6, F7, L7, F8., L8, F9, L9, F10, L10, G11, H11, J11, K11	E1, F2, N3, U5, W9, V9, U12, V16, R17, M18, G18, D19, C18, A15, A11, D8, A4
V_{CCIO1}	37	53, 65	K4, L6, P6	N4, V2, T6
V_{CCIO2}	1	1, 26	C7, D5, F3, F6	A7, C3, F1, K1
V_{CCIO3}	55, 73	79, 92, 105	L11, L14, N9, P11	T10, V14, V18, P18
V_{CCIO4}	109, 127	132, 157, 172, 181, 184	C10, F11, D12, G13	K19, G17, C19, D14, D12, D11
GND	18, 29, 36, 47, 62, 72, 89, 90, 99, 108, 114, 123, 144	2, 13, 24, 27, 42, 52, 68, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207	A1, T1, B2, R2, C3, P3, G7, H7, J7, K7, G8, H8, J8, K8, G9, H9, J9, K9, G10, H10, J10, K10, C14, P14, B15, R15, A16, T16	E5, F5, G5, H5, J5, K5, L5, M5, N5, P5, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, P15, N15, M15, L15, K15, J15, H15, G15, F15, E15, E14, E13, E12, E11, E10, E9, E8, E7, E6
No Connects	-	-	-	A1, W1, U3, W19, U17, A19, C17, A2, B3, B2

Notes:
1. TDO voltage is controlled by V_{CCIO4}.

Device Part Marking and Ordering Combination Information



Sample package with part marking.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC95288XV-6TQ144C	6 ns	TQ144	144-pin	Thin Quad Flat Pack	C
XC95288XV-6PQ208C	6 ns	PQ208	208-pin	Plastic Quad Flat Package	C
XC95288XV-6FG256C	6 ns	FG256	256-ball	Plastic Fineline Ball Grid Array	C
XC95288XV-6CS280C	6 ns	CS280	280-ball	Chipscale Package	C
XC95288XV-7TQ144C	7.5 ns	TQ144	144-pin	Thin Quad Flat Pack	C
XC95288XV-7PQ208C	7.5 ns	PQ208	208-pin	Plastic Quad Flat Package	C
XC95288XV-7FG256C	7.5 ns	FG256	256-ball	Plastic Fineline Ball Grid Array	C
XC95288XV-7CS280C	7.5 ns	CS280	280-pin	Chipscale Package	C
XC95288XV-7TQ144I	7.5 ns	TQ144	144-pin	Thin Quad Flat Pack	I
XC95288XV-7PQ208I	7.5 ns	PQ208	208-pin	Plastic Quad Flat Package	I
XC95288XV-7FG256I	7.5 ns	FG256	256-ball	Plastic Fineline Ball Grid Array	I
XC95288XV-7CS280I	7.5 ns	CS280	280-pin	Chipscale Package	I
XC95288XV-10TQ144C	10 ns	TQ144	144-pin	Thin Quad Flat Pack	C
XC95288XV-10PQ208C	10 ns	PQ208	208-pin	Plastic Quad Flat Package	C
XC95288XV-10FG256C	10 ns	FG256	256-ball	Plastic Fineline Ball Grid Array	C
XC95288XV-10CS280C	10 ns	CS280	280-ball	Chipscale Package	C
XC95288XV-10TQ144I	10 ns	TQ144	144-pin	Thin Quad Flat Pack	I
XC95288XV-10PQ208I	10 ns	PQ208	208-pin	Plastic Quad Flat Package	I
XC95288XV-10FG256I	10 ns	FG256	256-ball	Plastic Fineline Ball Grid Array	I
XC95288XV-10CS280I	10 ns	CS280	280-ball	Chipscale Package	I

Notes:
1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C
2. Some packages available in Pb-free option. See **Xilinx Packaging** for more information.

Revision History

Date	Version	Revision
09/28/98	1.0	Original creation of data sheet.
12/10/98	1.1	Revision of tables.
2/5/99	1.2	Updated pinouts to reflect BG256 (replaces BG352).
6/7/99	1.3	Add -7 speed and CS280 package.
4/11/00	1.4	Updated AC specifications, added bank information to pinout tables.
01/29/01	2.0	Added -5 performance specification, deleted -6; changed BG256 package to FG256 package. Updated I_{CC} vs. Frequency Figure 1.
05/15/01	2.1	Updated I_{CC} formula, Recommended Operation Conditions, -5 AC Characteristics and Internal Timing Parameters
08/27/01	2.2	Changed V_{CCIO} 3.3V from 3.13 to 3.0 (min), 3.46 to 3.60 (max); DC characteristics: I_{IL} - added "low" current, I_{IH} - changed to "Input leakage high current"; Internal Timing: -5 T_{AOI} from 6.5 to 5.9.
06/24/02	2.3	Updated I_{CC} equation on page 1. Updated Figure 3: AC Load Circuit 1.8V parameters. Added second test condition and max measurement to I_{IH} DC Characteristics. Added Part Marking Information to Ordering Information. Changed to Preliminary. Changed -5 speed to -6 speed; added -7 Industrial.
05/27/03	2.4	Updated T_{SOL} from 260 to 220°C. Updated Device Part Marking.
08/21/03	2.5	Updated Package Device Marking Pin 1 orientation.
04/15/05	2.6	Added T_{APRPW} specification to AC Characteristics. Added IOSTANDARD information.
06/25/07	3.0	Notice of discontinuance.