

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

**TIBPAL20L10-25M, TIBPAL20X4-25M, TIBPAL20X8-25M, TIBPAL20X10-25M
TIBPAL20L10-20C, TIBPAL20X4-20C, TIBPAL20X8-20C, TIBPAL20X10-20C
HIGH-PERFORMANCE EXCLUSIVE-OR IMPACT™ PAL® CIRCUITS**

D2920, OCTOBER 1985—REVISED DECEMBER 1987

- High Performance . . . 35 MHz Min
- Preload Capability on Output Registers Simplifies Testing
- Power-Up Clear on Registered Devices
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
*PAL20L10	12	2	0	8
*PAL20X4	10	0	4 (3-state buffers)	6
*PAL20X8	10	0	8 (3-state buffers)	2
*PAL20X10	10	0	10 (3-state buffers)	0

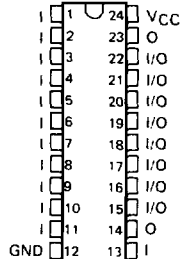
description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

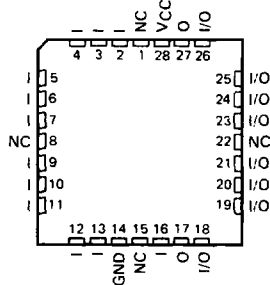
All of the registered outputs are set to a low level during power-up. In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The PAL20' M series is characterized for operation over the full military temperature range of -55°C to 125°C. The PAL20' C series is characterized for operation from 0°C to 75°C.

TIBPAL20L10'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L10'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

2

Data Sheets

IMPACT is a trademark of Texas Instruments Incorporated.

PAL is a registered trademark of Monolithic Memories Inc.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

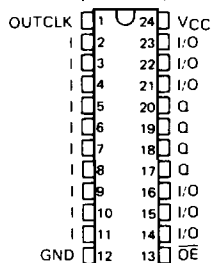


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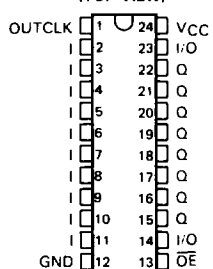
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**TIBPAL20X4-25M, TIBPAL20X8-25M, TIBPAL20X10-25M
TIBPAL20X4-20C, TIBPAL20X8-20C, TIBPAL20X10-20C
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT*™ *PAL*® CIRCUITS**

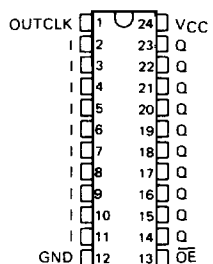
TIBPAL20X4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20X8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



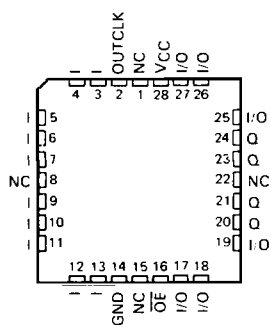
TIBPAL20X10'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



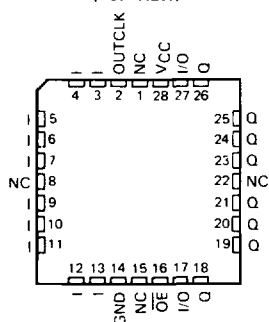
NC—No internal connection

Pin assignments in operating mode

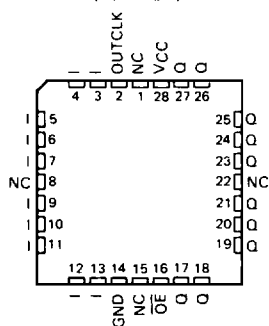
TIBPAL20X4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20X8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



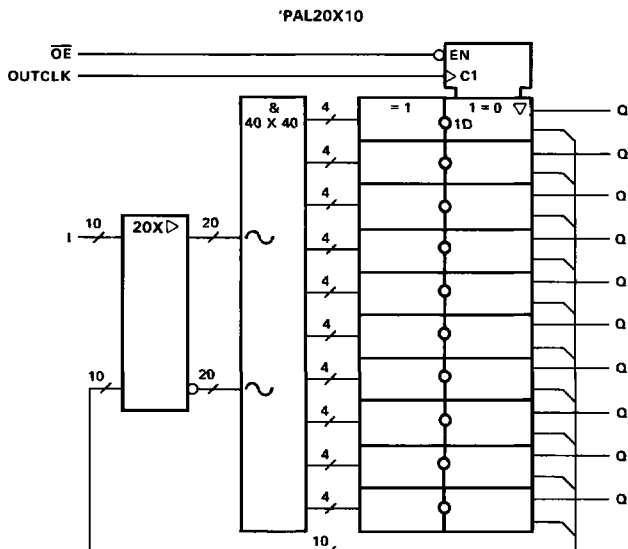
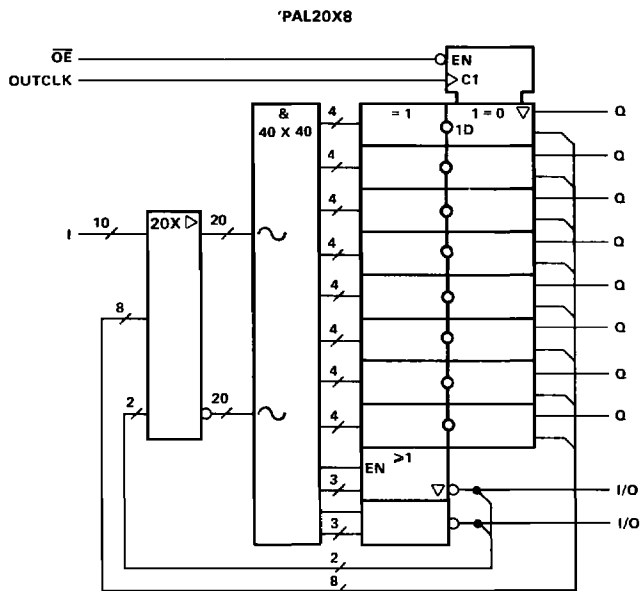
TIBPAL20X10'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



**TIBPAL20X8-25M, TIBPAL20X10-25M
TIBPAL20X8-20C, TIBPAL20X10-20C
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT*™ *PAL*® CIRCUITS**

functional block diagrams (positive logic)

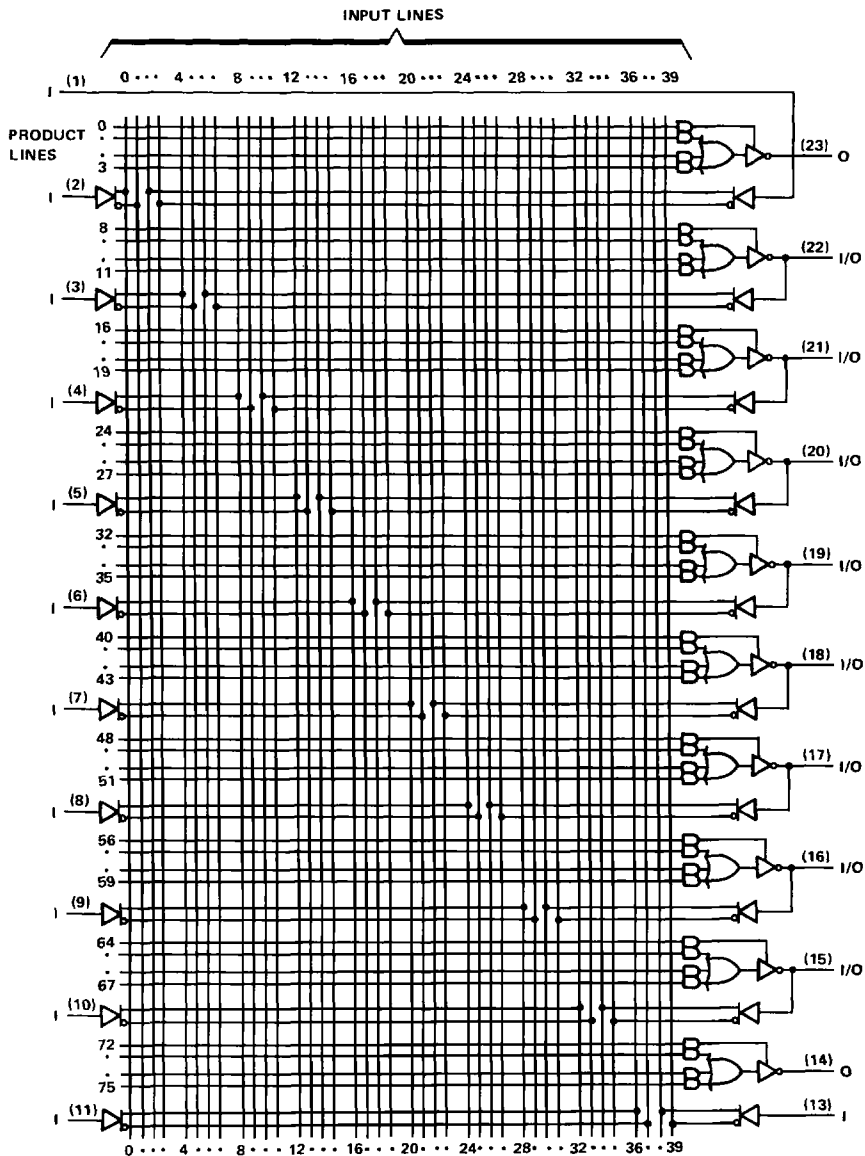
2
Data Sheets



~ denotes fused inputs

TIBPAL20L10-25M
TIBPAL20L10-20C
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT*™ PAL® CIRCUITS

logic diagram (positive logic)



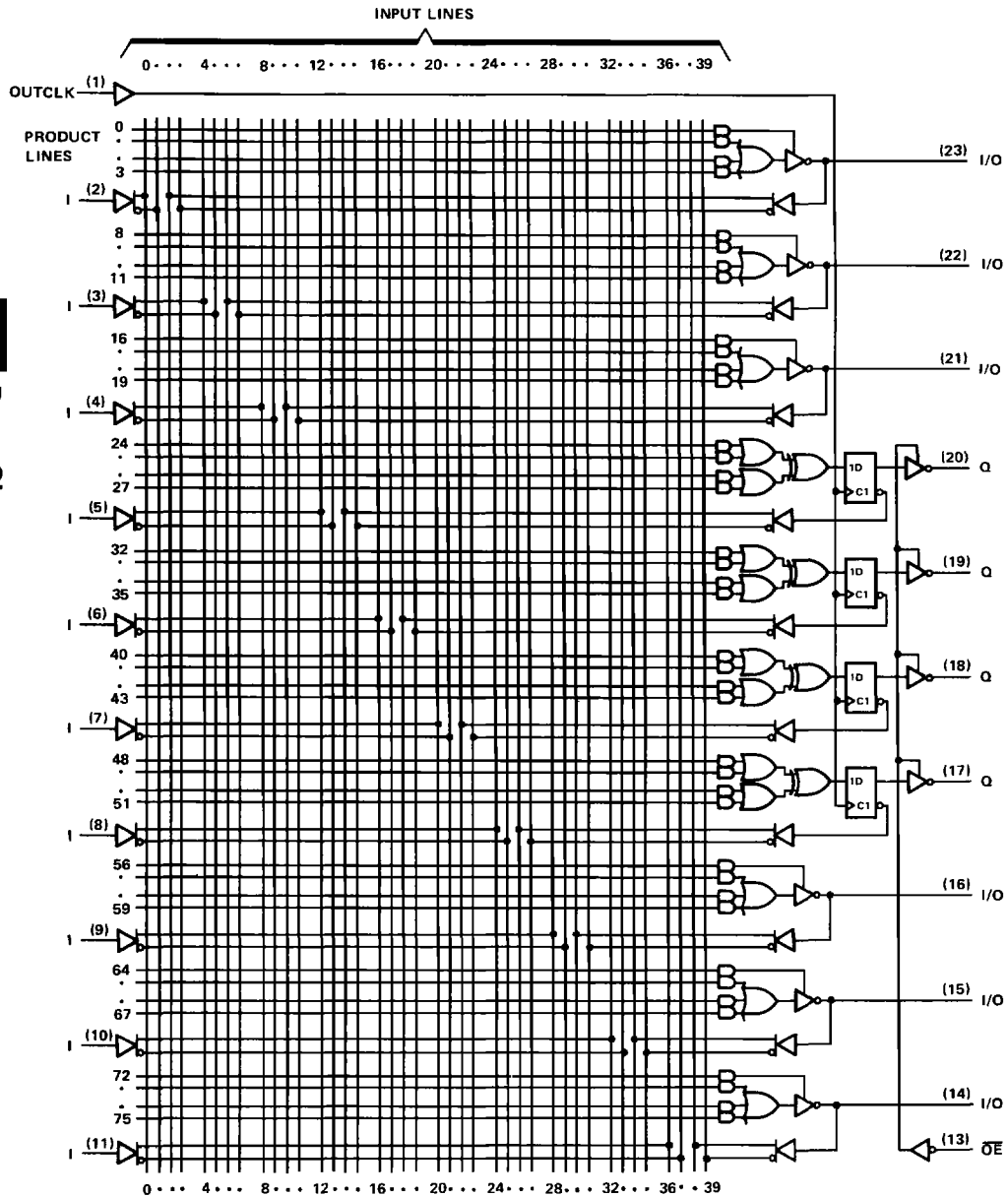
Pin numbers shown are for JT and NT packages.

2
Data Sheets



TIBPAL20X4-25M
TIBPAL20X4-20C
HIGH-PERFORMANCE EXCLUSIVE-OR IMPACT™ PAL® CIRCUITS

logic diagram (positive logic)

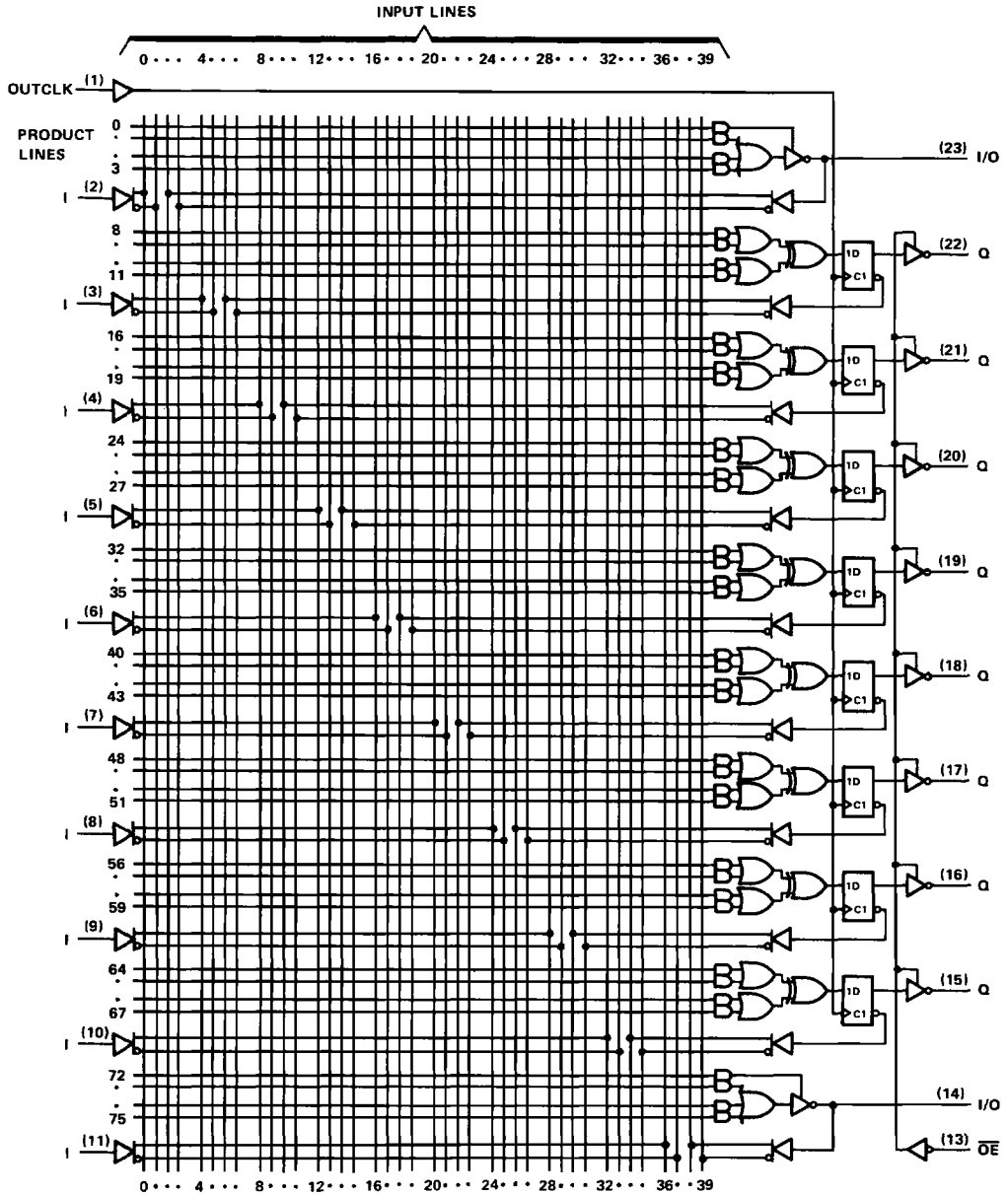


Pin numbers shown are for JT and NT packages.

2
Data Sheets

TIBPAL20X8-25M
TIBPAL20X8-20C
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT*™ PAL® CIRCUITS

logic diagram (positive logic)

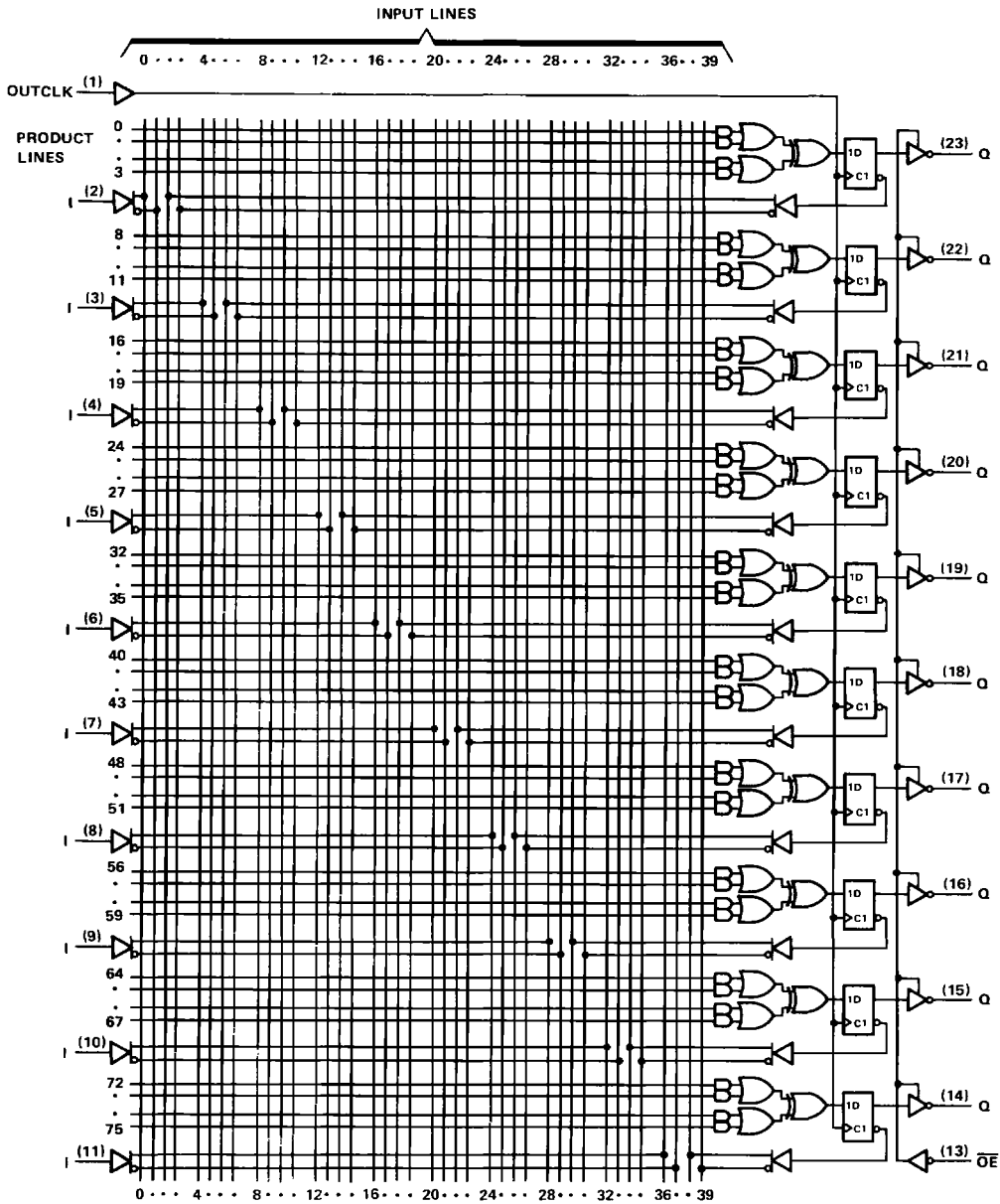


Pin numbers shown are for JT and NT packages.

2
Data Sheets

TIBPAL20X10-25M
TIBPAL20X10-20C
HIGH-PERFORMANCE EXCLUSIVE-OR IMPACT™ PAL® CIRCUITS

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

2
Data Sheets

**TIBPAL20L10-25M, TIBPAL20X4-25M, TIBPAL20X8-25M, TIBPAL20X10-25M
TIBPAL20L10-20C, TIBPAL20X4-20C, TIBPAL20X8-20C, TIBPAL20X10-20C
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* *PAL®* CIRCUITS**

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-25M			-20C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			R1 = 200 Ω , R2 = 390 Ω , C _L = 50 pF	25			36			MHz
t_{pd}	I, I/O	O, I/O		12	25		12	20	ns	
t_{pd}	OUTCLK†	Q		10	20		10	15	ns	
t_{en}	\overline{OE}	Q		7	20		7	15	ns	
t_{dis}	$\overline{OE}\dagger$	Q		7	20		7	15	ns	
t_{en}	I, I/O	O, I/O		15	25		15	20	ns	
t_{dis}	I, I/O	O, I/O		15	25		15	20	ns	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

2

Data Sheets

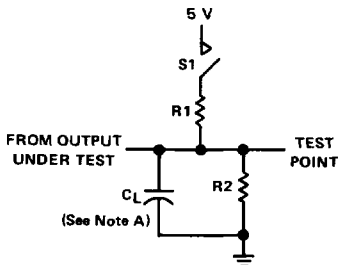
programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

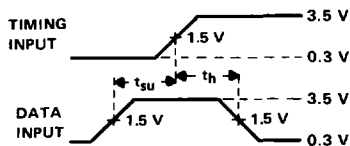
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5762.

**TIBPAL20L10-25M, TIBPAL20X4-25M, TIBPAL20X8-25M, TIBPAL20X10-25M
TIBPAL20L10-20C, TIBPAL20X4-20C, TIBPAL20X8-20C, TIBPAL20X10-20C
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* PAL® CIRCUITS**

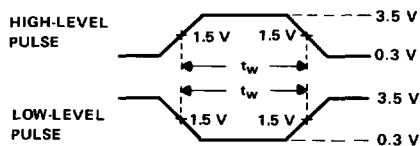
PARAMETER MEASUREMENT INFORMATION



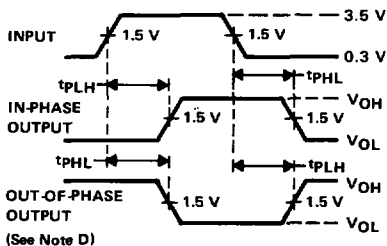
**LOAD CIRCUIT FOR
THREE-STATE OUTPUTS**



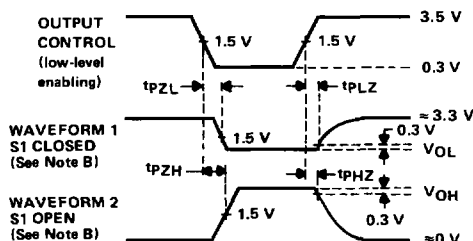
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

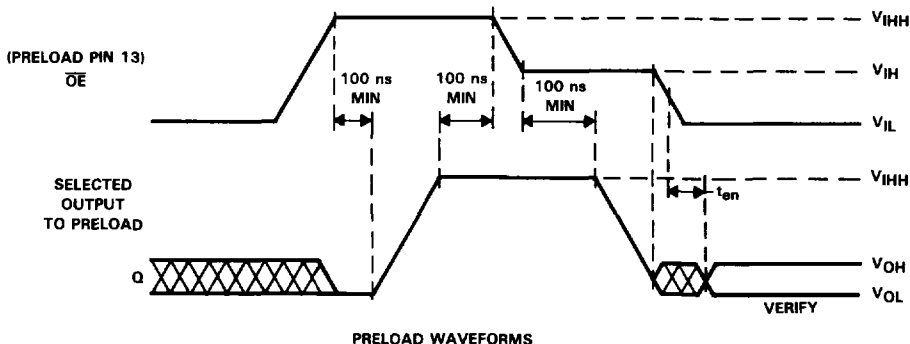
2
Data Sheets

**TIBPAL20L10-25M, TIBPAL20X4-25M, TIBPAL20X8-25M, TIBPAL20X10-25M
TIBPAL20L10-20C, TIBPAL20X4-20C, TIBPAL20X8-20C, TIBPAL20X10-20C
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* PAL® CIRCUITS**

preload procedures

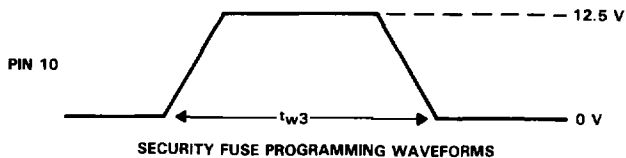
preload procedure for registered outputs

- Step 1 With V_{CC} at 5 volts, raise Pin 13 (\overline{OE}) to V_{IH} to disable the outputs and clear the registers (output goes low). Since the outputs are low, only high levels need be preloaded.
- Step 2 Raise the selected output to be preloaded high to V_{IH} .
- Step 3 Lower Pin 13 to V_{IH} .
- Step 4 Remove the voltages applied to the outputs. (At least a 100-ns wait is required between step 3 and step 4)
- Step 5 Lower Pin 13 to V_{iL} to verify preload.



PRELOAD WAVEFORMS

security fuse programming



SECURITY FUSE PROGRAMMING WAVEFORMS

NOTE: Pin numbers shown apply only for the DIP package. If a chip carrier socket adaptor is not used, pin numbers must be changed accordingly.