# USE GAL DEVICES FOR NEW DESIGNS

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**Lattice Semiconductor**

# PALCE26V12 Family

## 28-Pin EE CMOS Versatile PAL Device

### DISTINCTIVE CHARACTERISTICS

- **28-pin versatile PAL programmable logic device architecture**
- **Electrically erasable CMOS technology provides half power (only 115 mA) at high speed (7.5 ns propagation delay)**
- **14 dedicated inputs and 12 input/output macrocells for architectural flexibility**
- **Macrocells can be registered or combinatorial, and active high or active low**
- **Varied product term distribution allows up to 16 product terms per output**
- **Two clock inputs for independent functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Register preload for testability and built-in register reset on power-up**
- **Space-efficient 28-pin SKINNYDIP and PLCC packages**
- **Center $V_{CC}$ and GND pins to improve signal characteristics**
- **Extensive third-party software and programmer support through FusionPLD partners**

### GENERAL DESCRIPTION

The PALCE26V12 is a 28-pin version of the popular PAL22V10 architecture. Built with low-power, high-speed, electrically-erasable CMOS technology, the PALCE26V12 offers many unique advantages.

Device logic is automatically configured according to the user's design specification. Design is simplified by design software, allowing automatic creation of a programming file based on Boolean or state equations. The software can also be used to verify the design and can provide test vectors for the programmed device.

The PALCE26V12 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The functions are programmed into the device through electrically-erasable floating-gate cells in the AND logic array and the macrocells. In the unprogrammed state, all AND product terms float HIGH. If both true and complement of any input are connected, the term will be permanently LOW.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, active high or active low, with registered I/O possible. The flip-flop can be clocked by one of two clock inputs. The output configuration is determined by four bits controlling three multiplexers in each macrocell.



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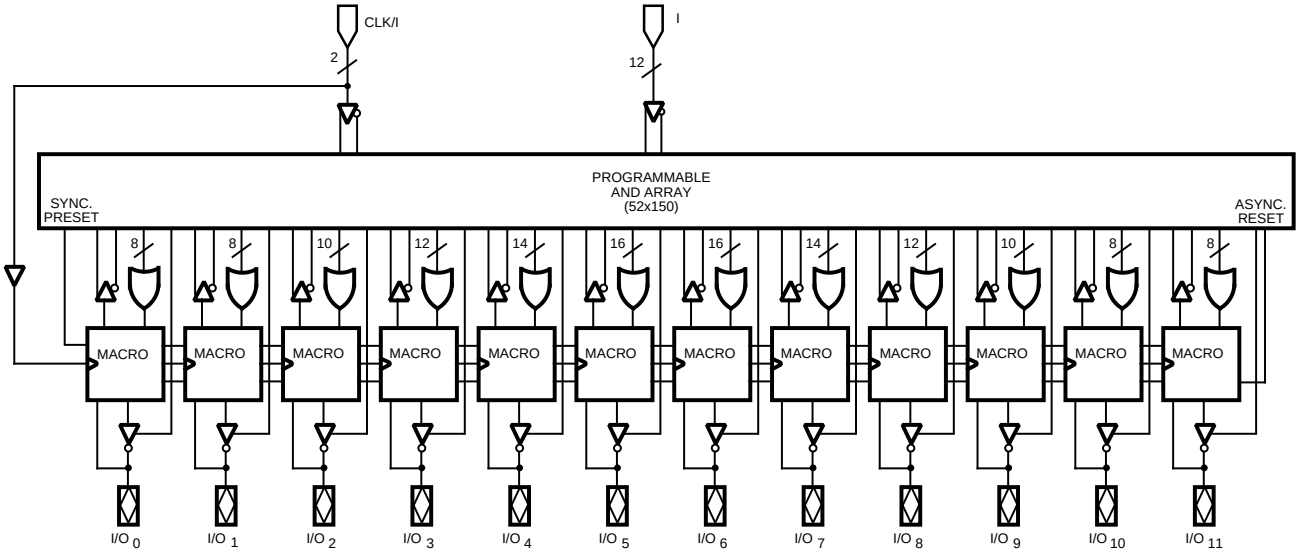
## BLOCK DIAGRAM

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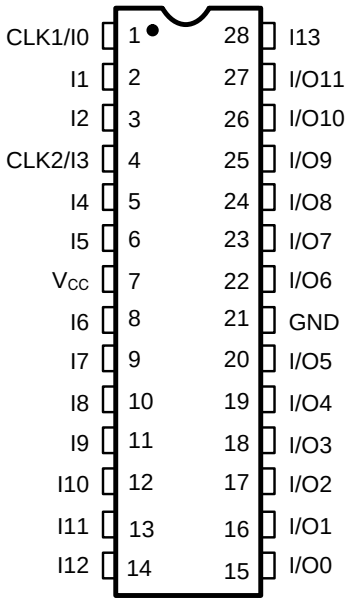
## CONNECTION DIAGRAMS

### Top View

**DIP**

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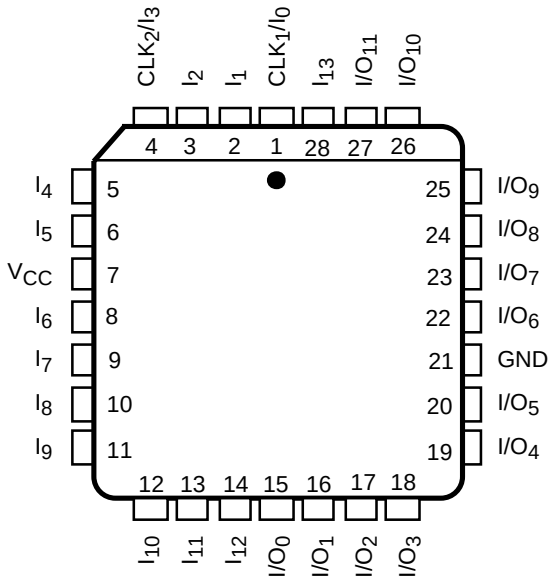
***Note:***

*Pin 1 is marked for orientation.*

**PLCC**

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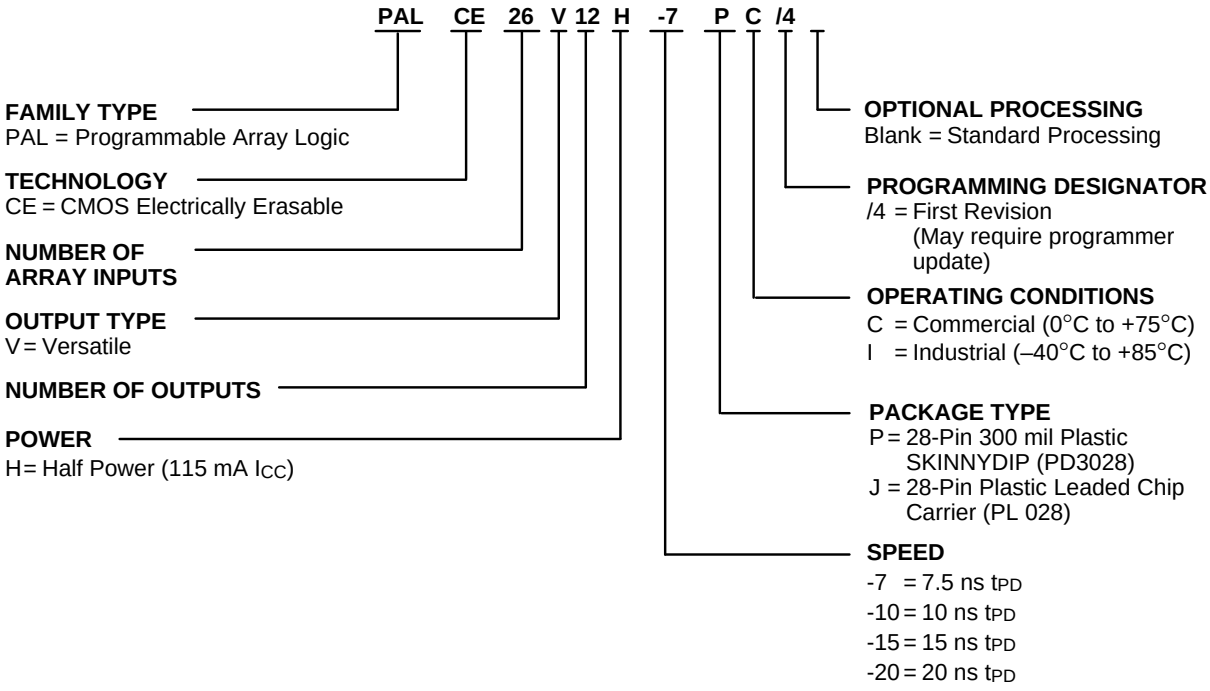
## PIN DESCRIPTION

| | | |
|---|---|---|
| CLK | = | Clock |
| GND | = | Ground |
| I | = | Input |
| I/O | = | Input/Output |
| $V_{CC}$ | = | Supply Voltage |

## ORDERING INFORMATION

### Commercial and Industrial Products

Commercial and industrial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | | |
|---|---|---|
| PALCE26V12H-7 | JC | /4 |
| PALCE26V12H-10 | PC, JC, PI, JI | |
| PALCE26V12H-15 | | |
| PALCE26V12H-20 | | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## FUNCTIONAL DESCRIPTION

The PALCE26V12 has fourteen dedicated input lines, two of which can be used as clock inputs. Unused inputs should be tied directly to ground or $V_{CC}$. Buffers for device inputs and feedbacks have both true and complementary outputs to provide user-selectable signal polarity. The inputs drive a programmable AND logic array, which feeds a fixed OR logic array.

The OR gates feed the twelve I/O macrocells (see Figure 1). The macrocell allows one of eight potential output configurations; registered or combinatorial, active high or active low, with register or I/O pin feedback (see Figure 2). In addition, registered configurations can be clocked by either of the two clock inputs.

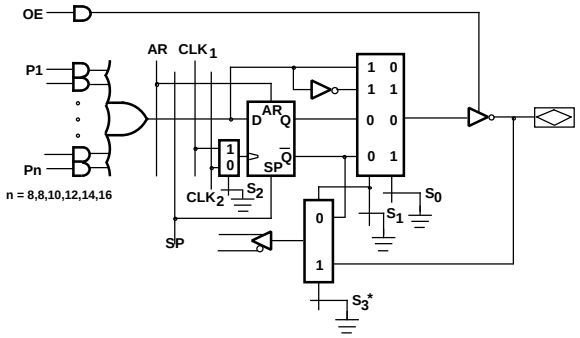
The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S0–S3 (see Table 1). Multiplexer controls initially float to $V_{CC}$ (1) through a programmable cell, selecting the "1" path through the multiplexer. Programming the cell connects the control line to GND (0), selecting the "0" path.

**Table 1. Macrocell Configuration Table**

| S3 | S1 | S0 | Output Configuration |
|---|---|---|---|
| 1 | 0 | 0 | Registered Output and Feedback, Active Low |
| 1 | 0 | 1 | Registered Output and Feedback, Active High |
| 1 | 1 | 0 | Combinatorial I/O, Active Low |
| 1 | 1 | 1 | Combinatorial I/O, Active High |
| 0 | 0 | 0 | Registered I/O, Active Low |
| 0 | 0 | 1 | Registered I/O, Active High |
| 0 | 1 | 0 | Combinatorial Output, Registered Feedback, Active Low |
| 0 | 1 | 1 | Combinatorial Output, Registered Feedback, Active High |

*1 = Unprogrammed EE bit*
*0 = Programmed EE bit*

| S2 | Clock Input |
|---|---|
| 1 | $CLK_1/I_0$ |
| 0 | $CLK_2/I_3$ |




**When $S_3$ = 1 (unprogrammed) the feedback is selected by $S_1$. When $S_3$ = 0 (programmed), the feedback is the opposite of that selected by $S_1$.*

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**Figure 1. PALCE26V12 Macrocell**

### Registered or Combinatorial

Each macrocell of the PALCE26V12 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH edge of the selected clock input. Any macrocell can be configured as combinatorial by selecting a multiplexer path that bypasses the flip-flop. Bypass is controlled by bit S1.

### Programmable Clock

The clock input for any flip-flop can be selected to be from either pin 1 or pin 4. A 2:1 multiplexer controlled by bit S2 determines the clock input.

### Programmable Feedback

A 2:1 multiplexer allows the user to determine whether the macrocell feedback comes from the flip-flop or from the I/O pin, independent of whether the output is registered or combinatorial. Thus, registered outputs may have internal register feedback for higher speed ($f_{MAX}$ internal), or I/O feedback for use of the pin as a direct input ($f_{MAX}$ external). Combinatorial outputs may have I/O feedback, either for use of the signal in other equations or for use as another direct input, or register feedback.

The feedback multiplexer is controlled by the same bit (S1) that controls whether the output is registered or combinatorial, as on the 22V10, with an additional control bit (S3) that allows the alternative feedback path to be selected. When S3 = 1, S1 selects register feedback for registered outputs (S1 = 0) and I/O feedback for combinatorial outputs (S1 = 1). When S3 = 0, the opposite is selected: I/O feedback for registered outputs and register feedback for combinatorial outputs.

## Programmable Enable and I/O

Each macrocell has a three-state output buffer controlled by an individual product term. Enable and disable can be a function of any combination of device inputs or feedback. The macrocell provides a bidirectional I/O pin if I/O feedback is selected, and may be configured as a dedicated input if the buffer is always disabled. This is accomplished by connecting all inputs to the enable term, forcing the AND of the complemented inputs to be always LOW. To permanently enable the outputs, all inputs are left disconnected from the term (the unprogrammed state).

## Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save “DeMorganizing” efforts.

Selection is controlled by programmable bit S0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high.

## Preset/Reset

For initialization, the PALCE26V12 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH or the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

## Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE26V12 will be HIGH or LOW depending on whether the output is active low or active high, respectively. The $V_{CC}$ rise must be monotonic, and the reset delay time is 1000 ns maximum.

## Register Preload

The register on the PALCE26V12 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

## Security Bit

After programming and verification, a PALCE26V12 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. Programming the security bit disables preload, and the array will read as if every bit is disconnected. The security bit can only be erased in conjunction with erasure of the entire pattern.

## Programming and Erasing

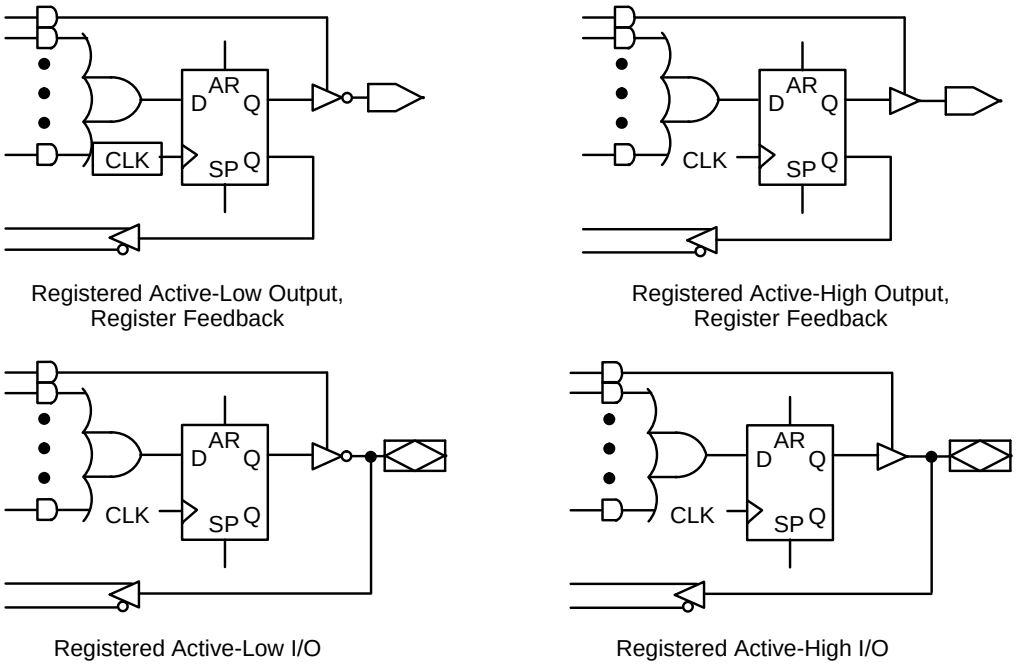
The PALCE26V12 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

## Quality and Testability

The PALCE26V12 offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

## Technology

The high-speed PALCE26V12 is fabricated with our advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.



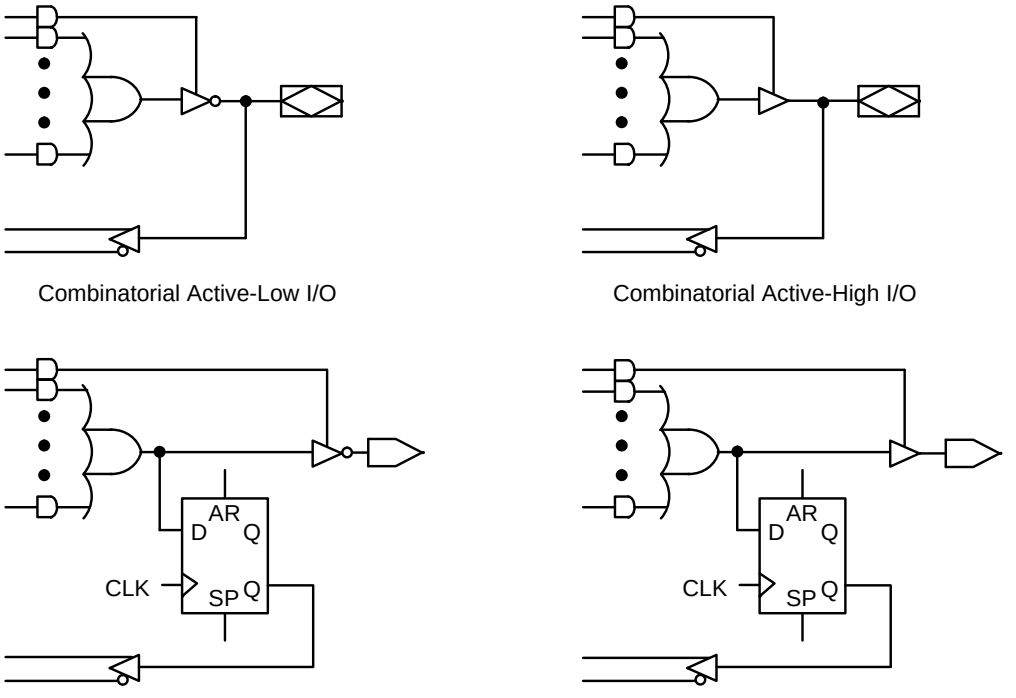

Registered Active-Low Output, Register Feedback

Registered Active-High Output, Register Feedback

Registered Active-Low I/O

Registered Active-High I/O

**Registered Outputs**




Combinatorial Active-Low I/O

Combinatorial Active-High I/O

Combinatorial Active-Low Output, Register Feedback

Combinatorial Active-High Output, Register Feedback

**Combinatorial Outputs**

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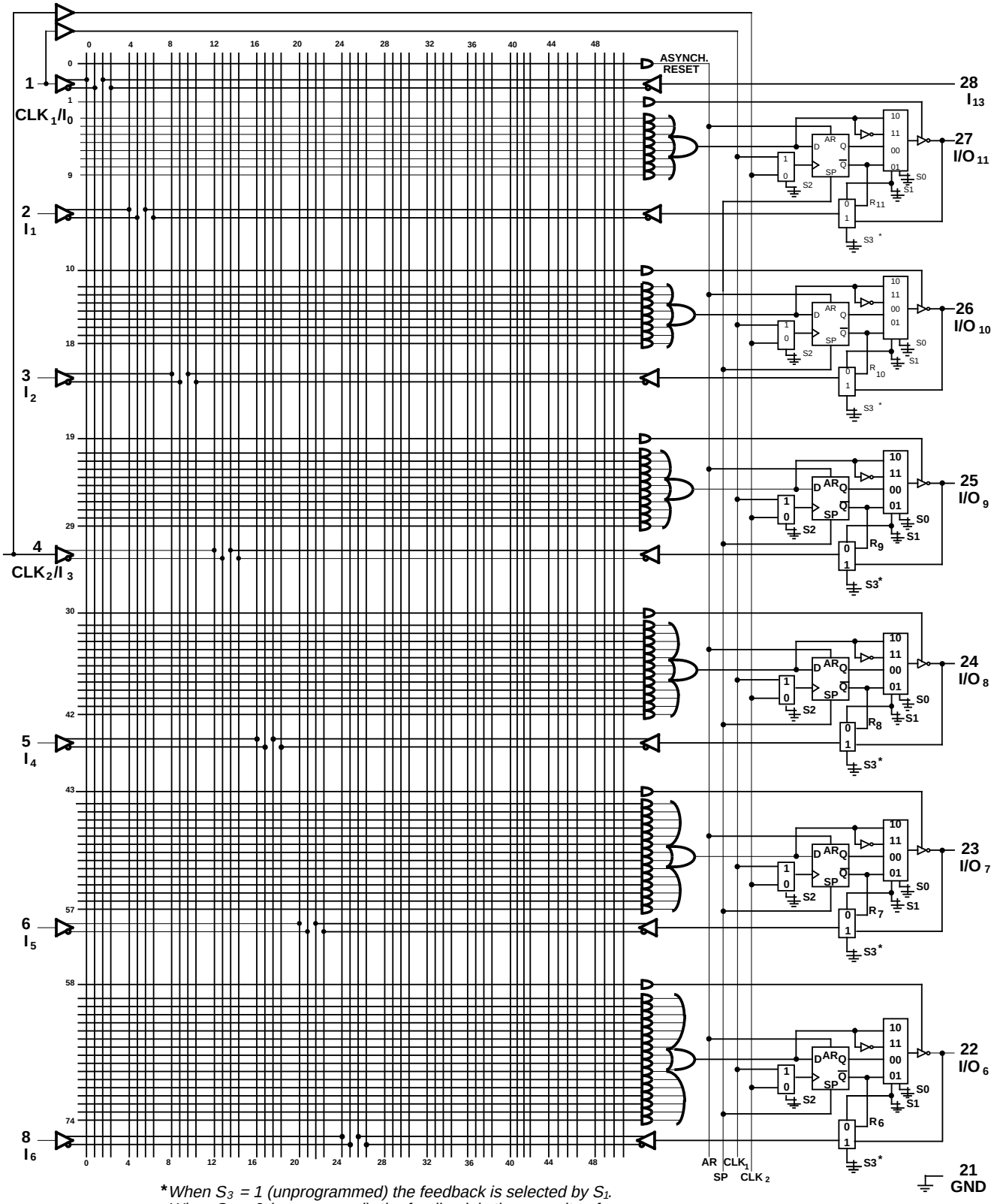
**Figure 2. PALCE26V12 Macrocell Configuration Options**

## LOGIC DIAGRAM

### PALCE26V12




***** *When $S_3$ = 1 (unprogrammed) the feedback is selected by $S_1$. When $S_3$ = 0 (programmed), the feedback is the opposite of that selected by $S_1$.*

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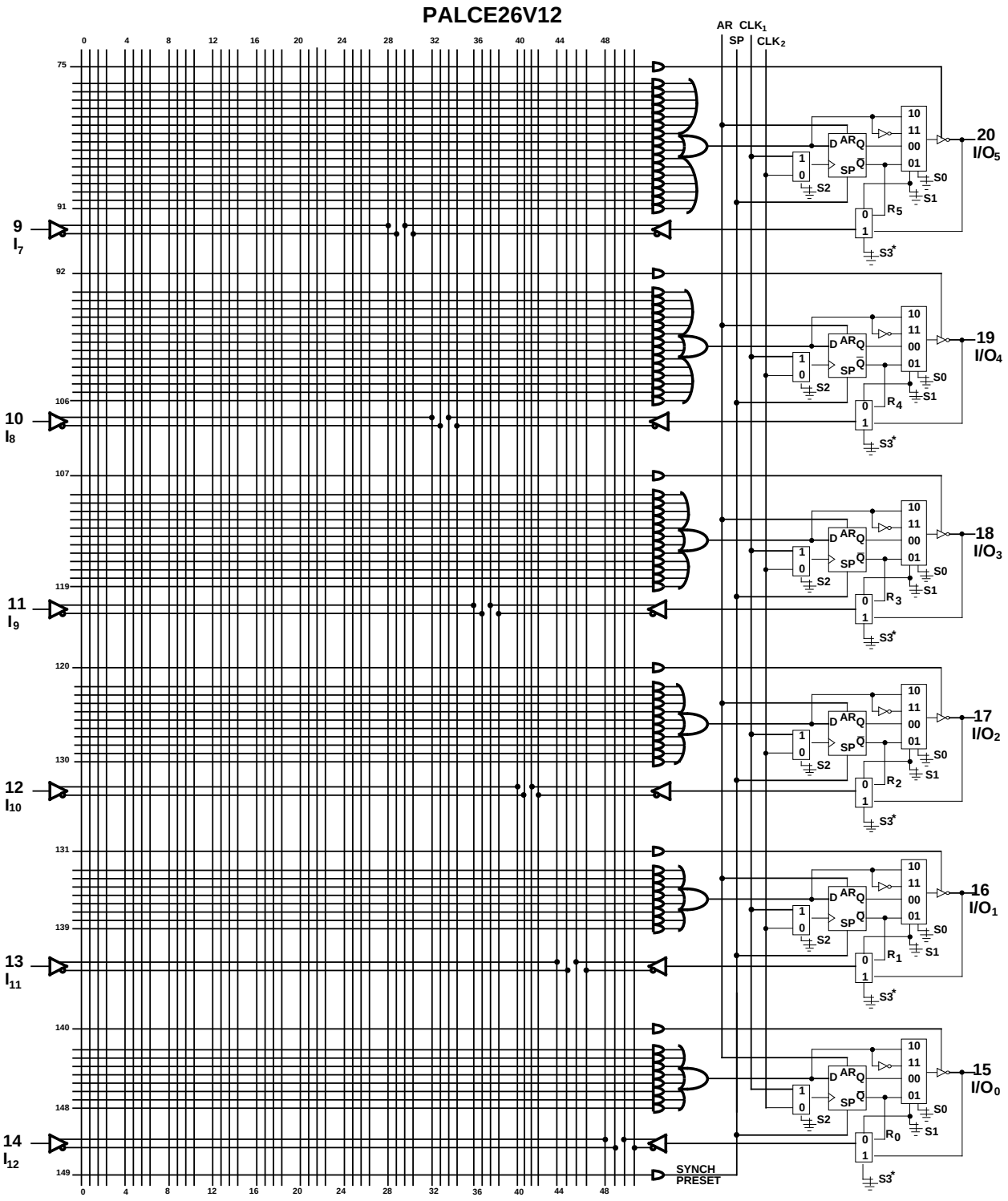
## LOGIC DIAGRAM (continued)




*When $S_3$ = 1 (unprogrammed) the feedback is selected by $S_1$. When $S_3$ = 0 (programmed), the feedback is the opposite of that selected by $S_1$.*

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(concluded)

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.6 V to +7.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage . . . . . 2001 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground . . . . . +4.75 V to +5.25 V

**Industrial (I) Devices**

Ambient Temperature ($T_A$) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage ($V_{CC}$) with Respect to Ground . . . . . +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 16 mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.25 V, $V_{CC}$ = Max (Note 2) | | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max (Note 2) | | | –10 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.25 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | –10 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | | –30 | –170 | mA |
| $I_{CC}$ (Static) | Commercial Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max, f = 0 MHz | H-7/10 | | 115 | mA |
| $I_{CC}$ (Dynamic) | Commercial Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max, f = 15 MHz | H-7/10 | | 140 | mA |
| $I_{CC}$ (Dynamic) | Industrial Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max, f = 15 MHz | H-10 | | 150 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 V | $V_{CC}$ = 5.0 V<br>$T_A$ = +25°C<br>f = 1 MHz | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 V | | 8 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | -7 | | -10 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | | 7.5 | | 10 | ns |
| $t_{S1}$ | Setup Time from Input or Feedback | | | 3.5 | | 5 | | ns |
| $t_{S2}$ | Setup Time from SP to Clock | | | 4.5 | | 5 | | ns |
| $t_H$ | Hold Time | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 6 | | 9 | ns |
| $t_{AR}$ | Asynchronous Reset to Registered Output | | | | 11 | | 13 | ns |
| $t_{ARW}$ | Asynchronous Reset Width | | | 6 | | 8 | | ns |
| $t_{ARR}$ | Asynchronous Reset Recovery Time | | | 5 | | 8 | | ns |
| $t_{SPR}$ | Synchronous Preset Recovery Time | | | 5 | | 8 | | ns |
| $t_{WL}$ | Clock Width | LOW | | 3.5 | | 4 | | ns |
| $t_{WH}$ | | HIGH | | 3.5 | | 4 | | ns |
| $f_{MAX}$ | Maximum Frequency (Notes 3 and 4) | External Feedback | $1/(t_S + t_{CO})$ | 105.3 | | 71.4 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | $1/(t_S + t_{CF})$ | 125 | | 105 | | MHz |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | | 8 | | 10 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | 7.5 | | 10 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *$t_{CF}$ is a calculated value and is not guaranteed. $t_{CF}$ can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – $t_S$.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.6 V to +7.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage . . . . . 2001 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground . . . . . +4.75 V to +5.25 V

**Industrial (I) Devices**

Ambient Temperature ($T_A$) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage ($V_{CC}$) with Respect to Ground . . . . . +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 16 mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.25 V, $V_{CC}$ = Max (Note 2) | | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max (Note 2) | | | –10 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.25 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | –10 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | | –30 | –160 | mA |
| $I_{CC}$ (Static) | Commerical Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max, f = 0 MHz | H-15/20 | | 105 | mA |
| $I_{CC}$ (Dynamic) | Industrial Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max, f = 15 MHz | H-15 | | 150 | mA |
| $I_{CC}$ (Static) | | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max | H-20 | | 130 | mA |
| $I_{CC}$ (Dynamic) | | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max, f = 15 MHz | H-20 | | 150 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 V | $V_{CC}$ = 5.0 V<br>$T_A$ = +25°C<br>f = 1 MHz | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 V | | 8 | |

***Note:***

*1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | | 15 | | 20 | ns |
| $t_S$ | Setup Time from Input, Feedback, or SP to Clock | | | 10 | | 13 | | ns |
| $t_H$ | Hold Time | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 10 | | 12 | ns |
| $t_{AR}$ | Asynchronous Reset to Registered Output | | | | 20 | | 25 | ns |
| $t_{ARW}$ | Asynchronous Reset Width | | | 15 | | 20 | | ns |
| $t_{ARR}$ | Asynchronous Reset Recovery Time | | | 15 | | 20 | | ns |
| $t_{SPR}$ | Synchronous Preset Recovery Time | | | 10 | | 13 | | ns |
| $t_{WL}$ | Clock Width | LOW | | 8 | | 10 | | ns |
| $t_{WH}$ | | HIGH | | 8 | | 10 | | ns |
| $f_{MAX}$ | Maximum Frequency (Notes 3 and 4) | External Feedback | $1/(t_S + t_{CO})$ | 50 | | 40 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | $1/(t_S + t_{CF})$ | 58.8 | | 43 | | MHz |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | | 15 | | 20 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | 15 | | 20 | ns |

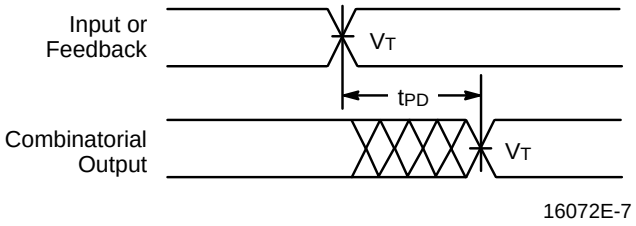
***Notes:***

*2. See Switching Test Circuit for test conditions.*

*3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

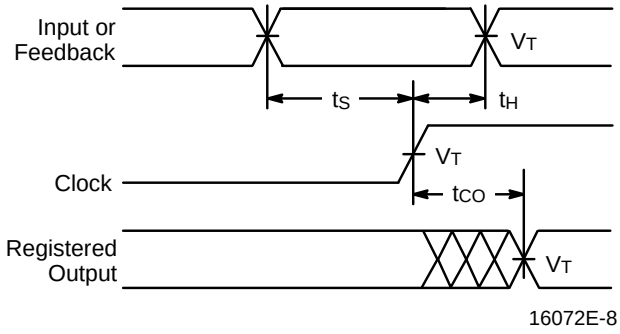
*6. $t_{CF}$ is a calculated value and is not guaranteed. $t_{CF}$ can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – $t_S$.*

## SWITCHING WAVEFORMS



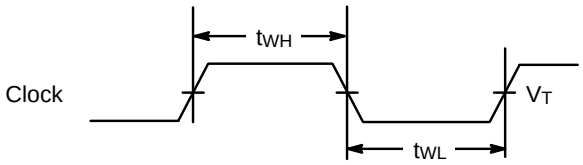

16072E-7

**Combinatorial Output**



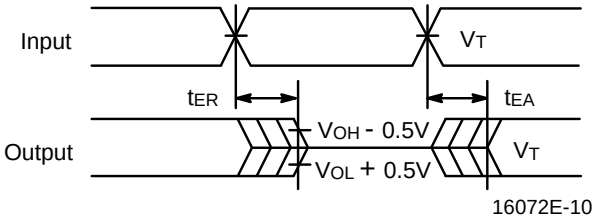

16072E-8

**Registered Output**



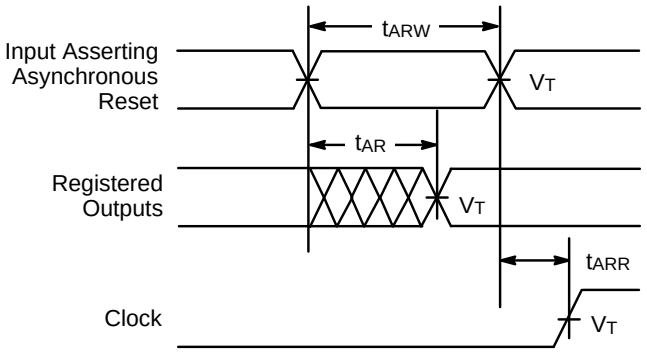

16072E-9

**Clock Width**



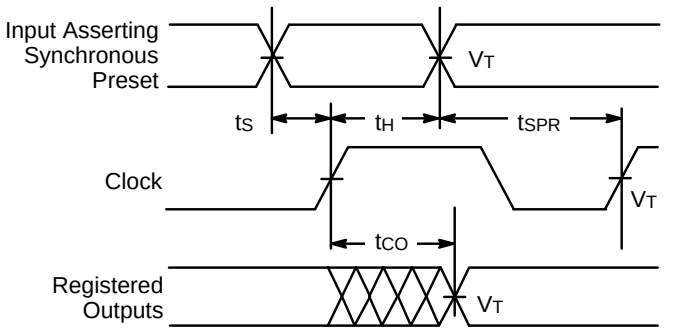

16072E-10

**Input to Output Disable/Enable**




16072E-11

**Asynchronous Reset**



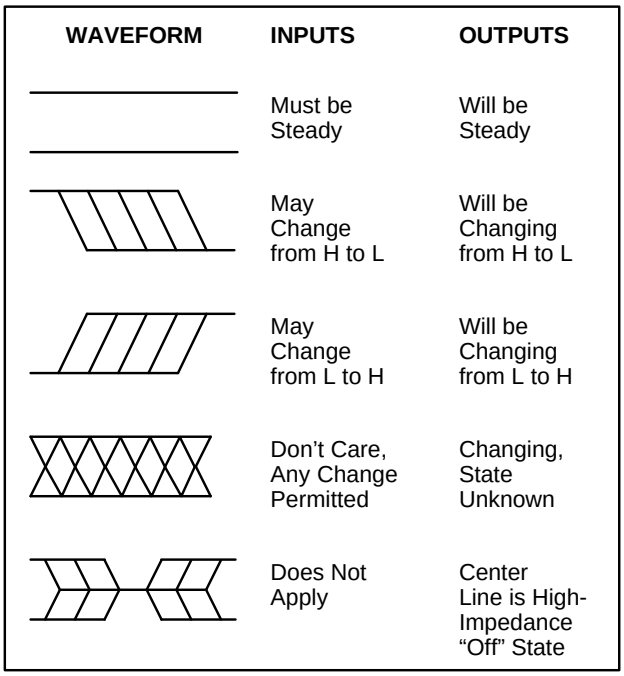

16072E-12

**Synchronous Preset**

***Notes:***

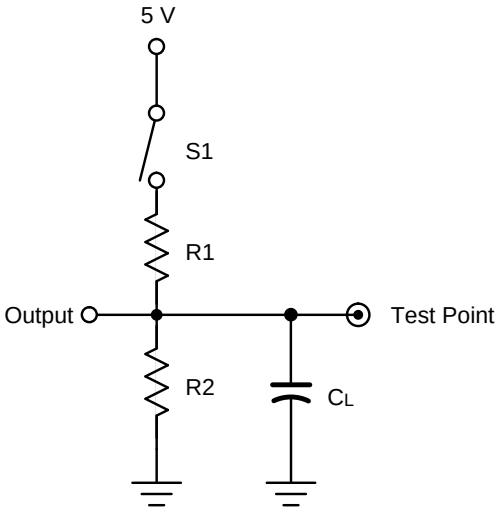
1. *$V_T$ = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–5 ns typical.*

## KEY TO SWITCHING WAVEFORMS




KS000010-PAL

## SWITCHING TEST CIRCUIT

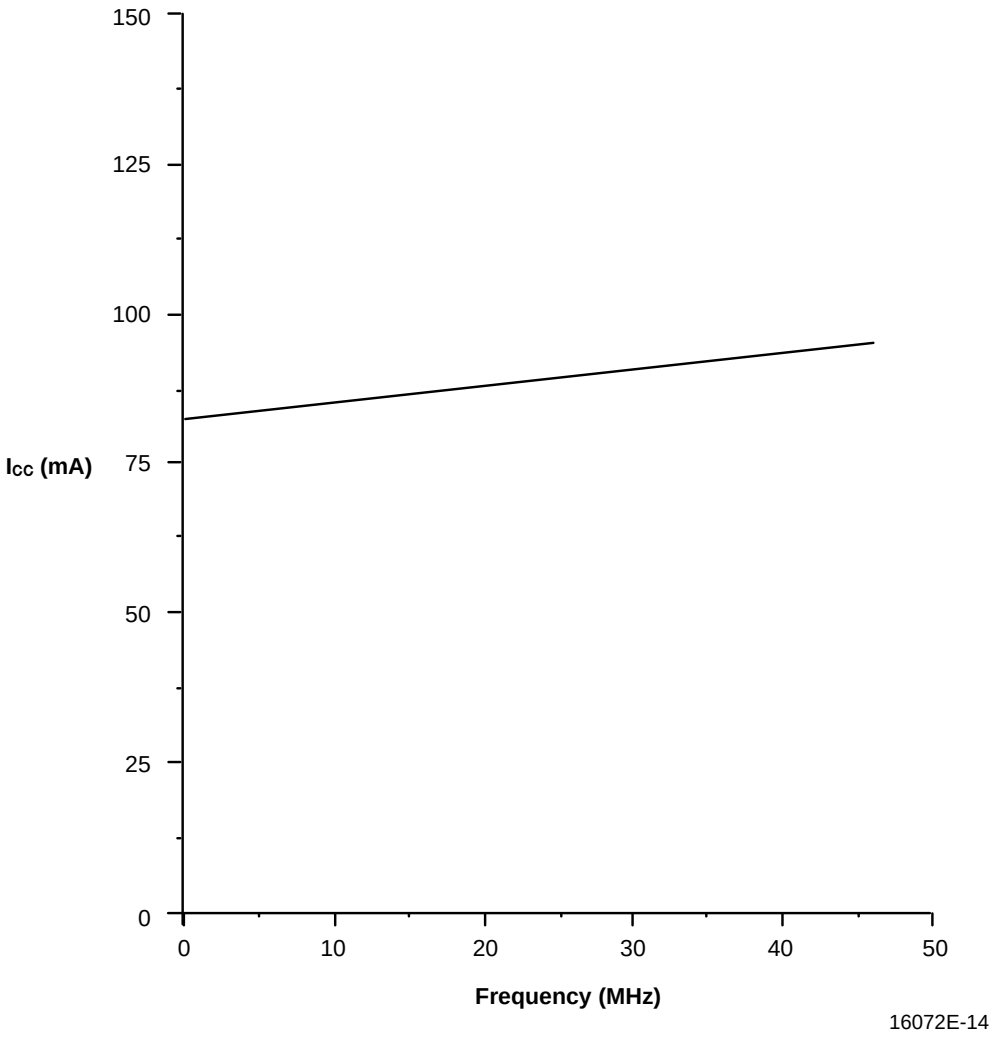



16072E-13

| Specification | S1 | $C_L$ | R1 | R2 | Measured Output Value |
|---|---|---|---|---|---|
| $t_{PD}$, $t_{CO}$ | Closed | 50 pF | 300 Ω | Com'l: H-15/20<br>Ind: H-20<br>390 Ω | 1.5 V |
| $t_{EA}$ | Z → H: Open<br>Z → L: Closed | | | | 1.5 V |
| $t_{ER}$ | H → Z: Open<br>L → Z: Closed | 5 pF | | Com'l: H-7/10<br>Ind: H-10/15<br>300 Ω | H → Z: $V_{OH}$ – 0.5 V<br>L → Z: $V_{OL}$ + 0.5 V |

## TYPICAL $I_{CC}$ CHARACTERISTICS FOR THE PALCE26V12H-7/10

$V_{CC}$ = 5.0 V, $T_A$ = 25°C




*The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.*

*By utilizing 50% of the device, a midpoint is defined for $I_{CC}$. From this midpoint, a designer may scale the $I_{CC}$ graphs up or down to estimate the $I_{CC}$ requirements for a particular design.*

## ENDURANCE CHARACTERISTICS

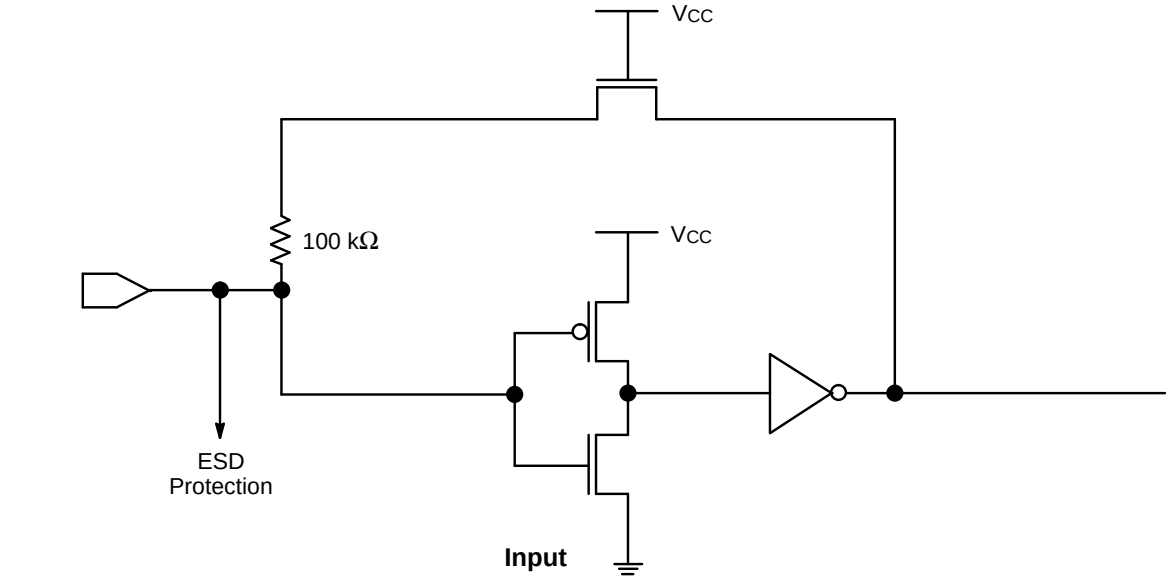
The PALCE26V12 is manufactured using our advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

| Symbol | Parameter | Test Conditions | Min | Unit |
|---|---|---|---|---|
| $t_{DR}$ | Min Pattern Data Retention Time | Max Storage Temperature | 10 | Years |
| | | Max Operating Temperature | 20 | Years |
| N | Min Reprogramming Cycles | Normal Programming Conditions | 100 | Cycles |

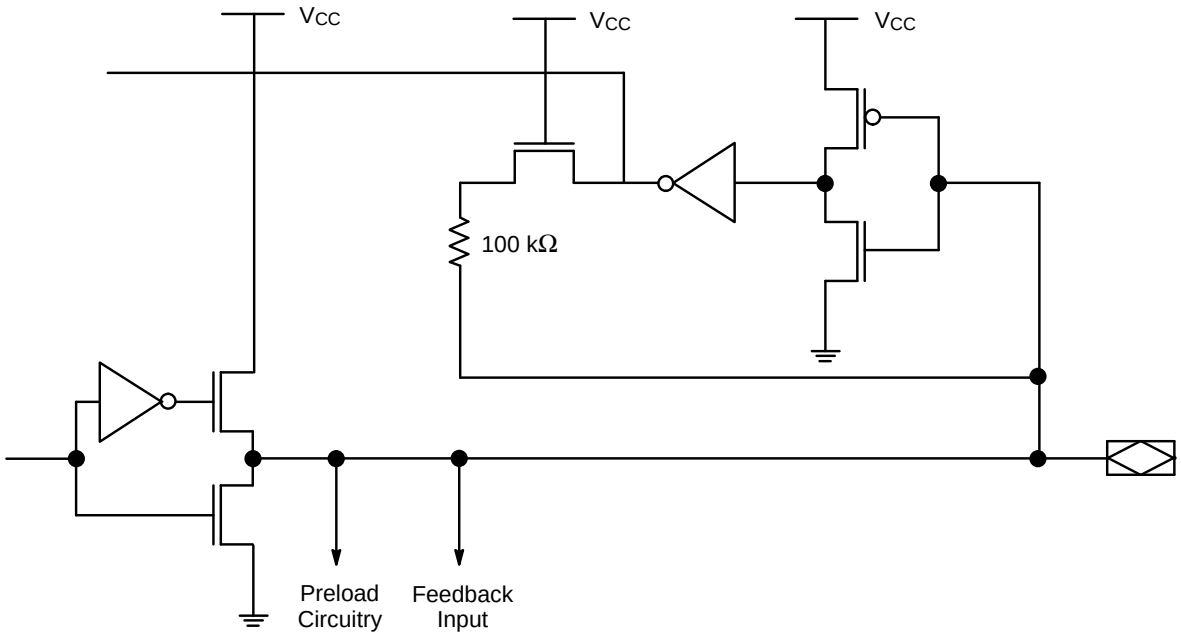
## Bus-Friendly Inputs

The PALCE26V12H-7/10 (Com'l) and H-10/15 (Ind) inputs and I/O loop back to the input after the second stage of the input buffer. This configuration reinforces the state of the input and pulls the voltage away from the input threshold voltage where noise can cause oscillations. For an illustration of this configuration, see below.

## INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR REV. C VERSION*




**Input**




16072E-15

**Output**

*

| Device | Rev. Letter |
|---|---|
| PALCE26V12H-7 | C |
| PALCE26V12H-10 | |
| PALCE26V12H-15 | |

***Topside Marking:***

*CMOS PLDs are marked on top of the package in the following manner:*

*PALCE xxxx*

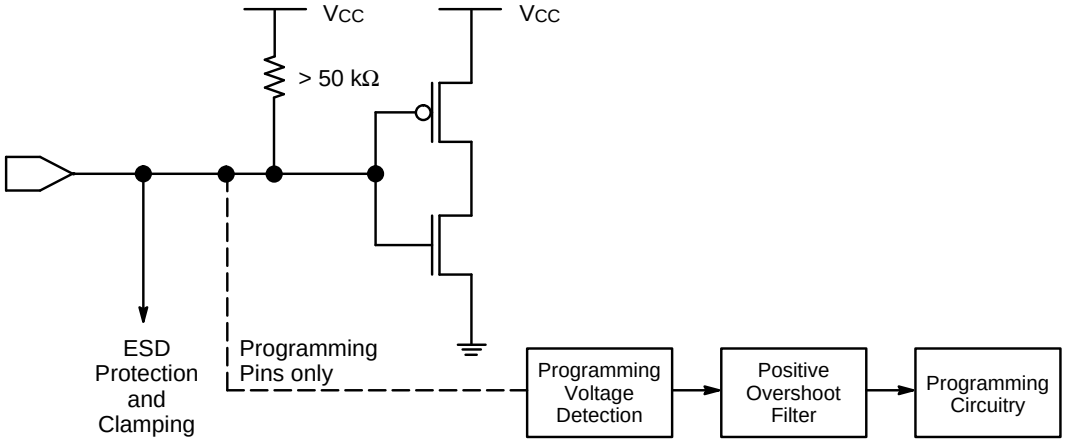
*Datecode (4 numbers) LOT ID (3 characters) – – (Rev. Letter)*

*The Lot ID and Rev. letter are separated by two spaces.*

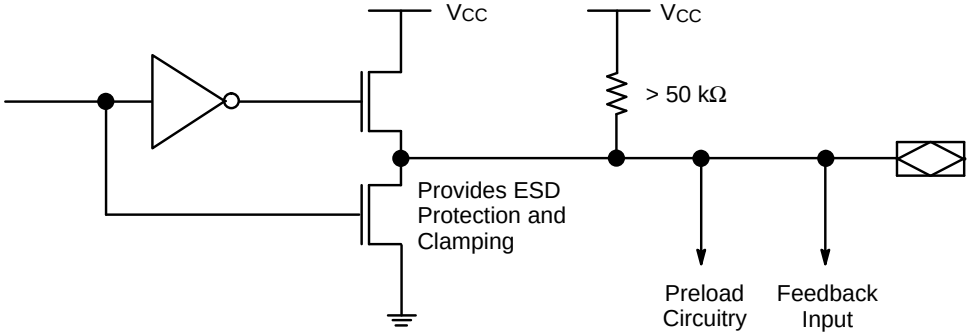
## ROBUSTNESS FEATURES

The PALCE26V12 has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

## INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR REV. B VERSION*




**Typical Input**




**Typical Output**

16072E-16

*

| Device | Rev. Letter |
|---|---|
| PALCE26V12-15 | B |
| PALCE26V12-20 | |

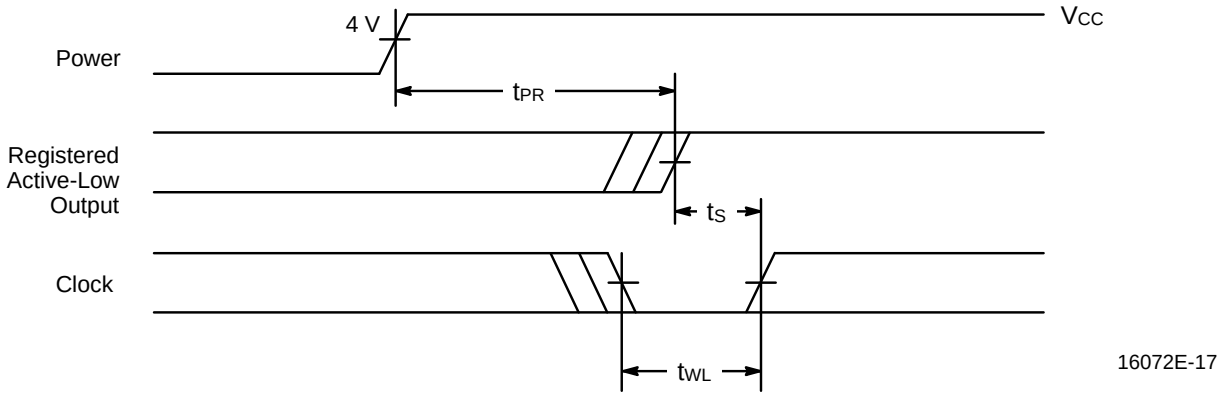
***Topside Marking:***
*CMOS PLDs are marked on top of the package in the following manner:*
*PALCE xxxx*
*Datecode (4 numbers) LOT ID (3 characters) – – (Rev. Letter)*
*The Lot ID and Rev. letter are separated by two spaces.*

## POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways $V_{CC}$ can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The $V_{CC}$ rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

| Parameter Symbol | Parameter Description | Max | Unit |
|---|---|---|---|
| $t_{PR}$ | Power-Up Reset Time | 1000 | ns |
| $t_S$ | Input or Feedback Setup Time | See Switching Characteristics | |
| $t_{WL}$ | Clock Width LOW | | |




**Power-Up Reset Waveform**

## TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

### PALCE26V12

| Parameter Symbol | Parameter Description | | Typ | | Unit |
|---|---|---|---|---|---|
| | | | SKINNYDIP | PLCC | |
| $\theta_{jc}$ | Thermal impedance, junction to case | | 19 | 18 | °C/W |
| $\theta_{ja}$ | Thermal impedance, junction to ambient | | 65 | 55 | °C/W |
| $\theta_{jma}$ | Thermal impedance, junction to ambient with air flow | 200 lfpm air | 59 | 48 | °C/W |
| | | 400 lfpm air | 54 | 44 | °C/W |
| | | 600 lfpm air | 50 | 39 | °C/W |
| | | 800 lfpm air | 50 | 37 | °C/W |

***Plastic θjc Considerations***

*The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.*