This is an abbreviated datasheet. Contact a Cypress representative for complete specifications. For new designs, please refer to the PALCE22V10.

CYPRESS

PALC22V10

Reprogrammable CMOS PAL® Device

Features

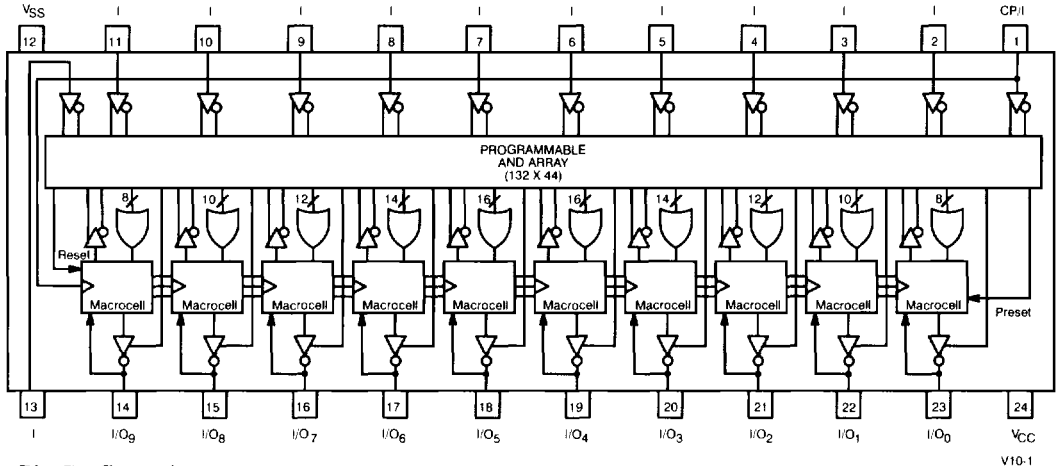
- **Advanced second-generation PAL architecture**
- **Low power**
  - **— 55 mA max. "L"**
  - **— 90 mA max. standard**
  - **— 120 mA max. military**
- **CMOS EPROM technology for reprogrammability**
- **Variable product terms**
  - **— 2 x (8 through 16) product terms**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **20, 25, 35 ns commercial and industrial**
- **25, 30, 40 ns military**
- **Up to 22 input terms and 10 outputs**
- **High reliability**
  - **— Proven EPROM technology**
  - **— 100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, and PLCC available**

Functional Description

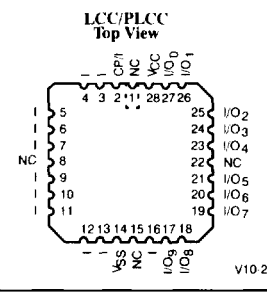
The Cypress PALC22V10 is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "programmable macrocell."

The PALC22V10 is available in 24-pin 300-mil molded DIPs, 300-mil windowed cerDIPs, 28-lead square ceramic leadless chip carriers, 28-lead square plastic leaded chip carriers, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10 is erased and can then be reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as registered or combinatorial. Polarity of each output may also be individually selected, allowing complete flexibility of output configuration. Further configurability is provided through array-configurable output enable for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

Logic Block Diagram (PDIP/CDIP)



Pin Configuration



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