

# Critical Conduction Mode PFC Control IC SSC2016S

## Data Sheet

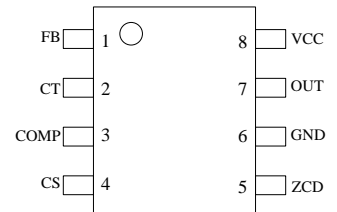
### Description

SSC2016S is a Critical Conduction Mode (CRM) control IC for power factor correction (PFC).

Since no input voltage sensing is required, the IC allows the realization of low standby power and the low number of external components. The product achieves high cost-performance and high efficiency PFC converter system.

### Package

SOIC8



Not to Scale

### Features

- Low Standby Power  
(No input voltage sensing required)
- Maximum Switching Frequency Limitation Function
- Minimum On-time Limitation Function
- Restart Function
- Protection Functions
  - Overcurrent Protection 1 (OCP1): Pulse-by-pulse
  - Overcurrent Protection 2 (OCP2): Latched shutdown
  - Overvoltage Protection (OVP): Auto-restart
  - FB Pin Undervoltage Protection (FB\_UVP): Auto-restart
  - Thermal Shutdown Protection with hysteresis (TSD): Auto-restart

### Electrical Characteristics

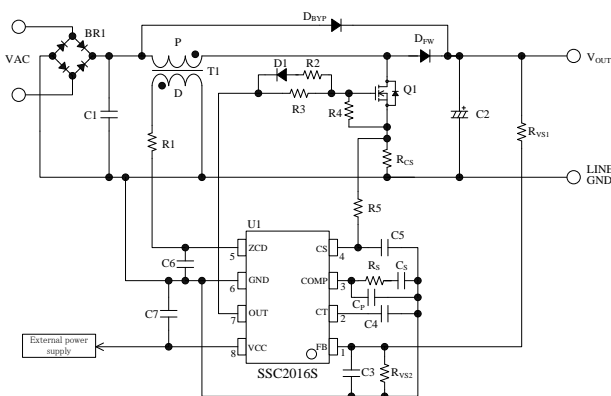
- VCC Pin Absolute Maximum Ratings,  $V_{CC} = 28\text{ V}$
- OUT Pin Source Current,  $I_{OUT(SRC)} = -500\text{ mA}$
- OUT Pin Sink Current,  $I_{OUT(SNK)} = 1000\text{ mA}$

### Application

PFC circuit up to 200 W of output power such as:

- AC/DC Power Supply
- Digital Appliances (large size LCD television and so forth).
- OA Equipment (Computer, Server, Monitor, and so forth).
- Communication Facilities
- Other Switching Mode Power Supply, SMPS

### Typical Application



TC\_SSC2016S\_1\_R2

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**1. Absolute Maximum Ratings**

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (-).

Unless specifically noted  $T_A = 25\text{ }^\circ\text{C}$ .

Parameter	Symbol	Conditions	Pins	Rating	Unit	Remarks
FB Pin Voltage	$V_{FB}$		1 – 6	- 0.3 to 5	V	
CT Pin Voltage	$V_{CT}$		2 – 6	- 0.3 to 5	V	
COMP Pin Voltage	$V_{COMP}$		3 – 6	- 0.3 to 5	V	
COMP Pin Current	$I_{COMP}$		3 – 6	- 100 to 100	$\mu\text{A}$	
CS Pin Voltage (DC)	$V_{CS(DC)}$		4 – 6	- 0.3 to 5	V	
CS Pin Voltage (Pulse)	$V_{CS(PULSE)}$	Pulse with $\tau = 1\mu\text{s}$	4 – 6	- 2 to 5	V	
ZCD Pin Voltage	$V_{ZCD}$		5 – 6	- 10 to 10	V	
ZCD Pin Current	$I_{ZCD}$		5 – 6	- 10 to 10	mA	
OUT Pin Voltage	$V_{OUT}$		7 – 6	- 0.3 to $V_{CC} + 0.3$	V	
OUT Pin Source Current	$I_{OUT(SRC)}$		7 – 6	- 500	mA	
OUT Pin Sink Current	$I_{OUT(SNK)}$		7 – 6	1000	mA	
VCC Pin Voltage	$V_{CC}$		8 – 6	28	V	
Allowable Power Dissipation	$P_D$		-	0.5	W	
Operating Ambient Temperature	$T_{OP}$		-	-40 to 110	$^\circ\text{C}$	
Storage Temperature	$T_{stg}$		-	-40 to 150	$^\circ\text{C}$	
Junction Temperature	$T_j$		-	150	$^\circ\text{C}$	

2. Electrical Characteristics

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (-).

Unless specifically noted,  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 14\text{ V}$ .

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
<b>Power Supply Operation</b>							
Operation Start Voltage	$V_{CC(ON)}$		8 – 6	7.5	8.5	9.5	V
Operation Stop Voltage	$V_{CC(OFF)}$		8 – 6	6.5	7.5	8.5	V
Operation Voltage Hysteresis	$V_{CC(HYS)}$		8 – 6	0.5	1.0	1.5	V
Circuit Current in Operation	$I_{CC(ON)}$		8 – 6	1.2	2.1	3.2	mA
Circuit Current in Non-Operation	$I_{CC(OFF)}$	$V_{CC} = 7\text{ V}$	8 – 6	–	50	100	$\mu\text{A}$
<b>Frequency Control</b>							
FB Pin Sink Current	$I_{FB}$		1 – 6	0.3	0.7	1.1	$\mu\text{A}$
Feedback Voltage Reference	$V_{REF}$		1 – 6	2.475	2.500	2.525	V
$V_{REF}$ Line Regulation	$V_{REF(LR)}$	$V_{CC} = 11.5\text{ V}$ $\sim 28\text{ V}$	1 – 6	– 8.0	1.0	12.0	mV
COMP Pin Source Current 1	$I_{COMP(SRC)1}$	$V_{FB} = 2.4\text{ V}$	3 – 6	– 22	– 11	– 1	$\mu\text{A}$
COMP Pin Sink Current 1	$I_{COMP(SNK)1}$	$V_{FB} = 2.6\text{ V}$	3 – 6	1	11	22	$\mu\text{A}$
COMP Pin Sink Current 2	$I_{COMP(SNK)2}$	$V_{FB} = 2.7\text{ V}$	3 – 6	15	35	55	$\mu\text{A}$
Error Amplifier Transconductance Gain	gm		1 – 6 3 – 6	60	100	140	$\mu\text{S}$
Zero Duty COMP Voltage	$V_{COMP(ZD)}$		3 – 6	0.50	0.65	0.90	V
Restart Time	$t_{RS}$		7 – 6	140	220	300	$\mu\text{s}$
ON Time in Restart Operation	$t_{ON(RS)}$		7 – 6	0.5	1.7	2.9	$\mu\text{s}$
CT Pin Source Current	$I_{CT}$		2 – 6	– 165	– 150	– 135	$\mu\text{A}$
CT Pin Threshold Voltage	$V_{CT(OFF)}$	$V_{COMP} = 4.5\text{ V}$	2 – 6	2.60	2.75	2.90	V
CT Pin Delay Time of Control	$t_{DLY(PWM)}$	$V_{COMP} = 2.2\text{ V}$	2 – 6	–	120	220	ns
Maximum Switching Frequency <sup>(1)</sup>	$f_{MAX}$		7 – 6	–	300	400	kHz
<b>Drive Output</b>							
Output Voltage (High)	$V_{OH}$	$I_{OUT} = -100\text{ mA}$	7 – 6	10.0	12.0	13.5	V
Output Voltage (low)	$V_{OL}$	$I_{OUT} = 200\text{ mA}$	7 – 6	0.40	0.75	1.25	V
Output Rise Time <sup>(2)</sup>	$t_r$	$C_{OUT} = 1000\text{ pF}$	7 – 6	–	60	120	ns
Output Fall Time <sup>(2)</sup>	$t_f$	$C_{OUT} = 1000\text{ pF}$	7 – 6	–	20	70	ns
<b>Zero Current Detection</b>							

<sup>(1)</sup> Design assurance item

<sup>(2)</sup> Shown in Figure 3-1

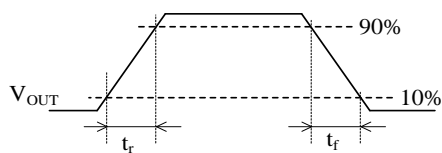


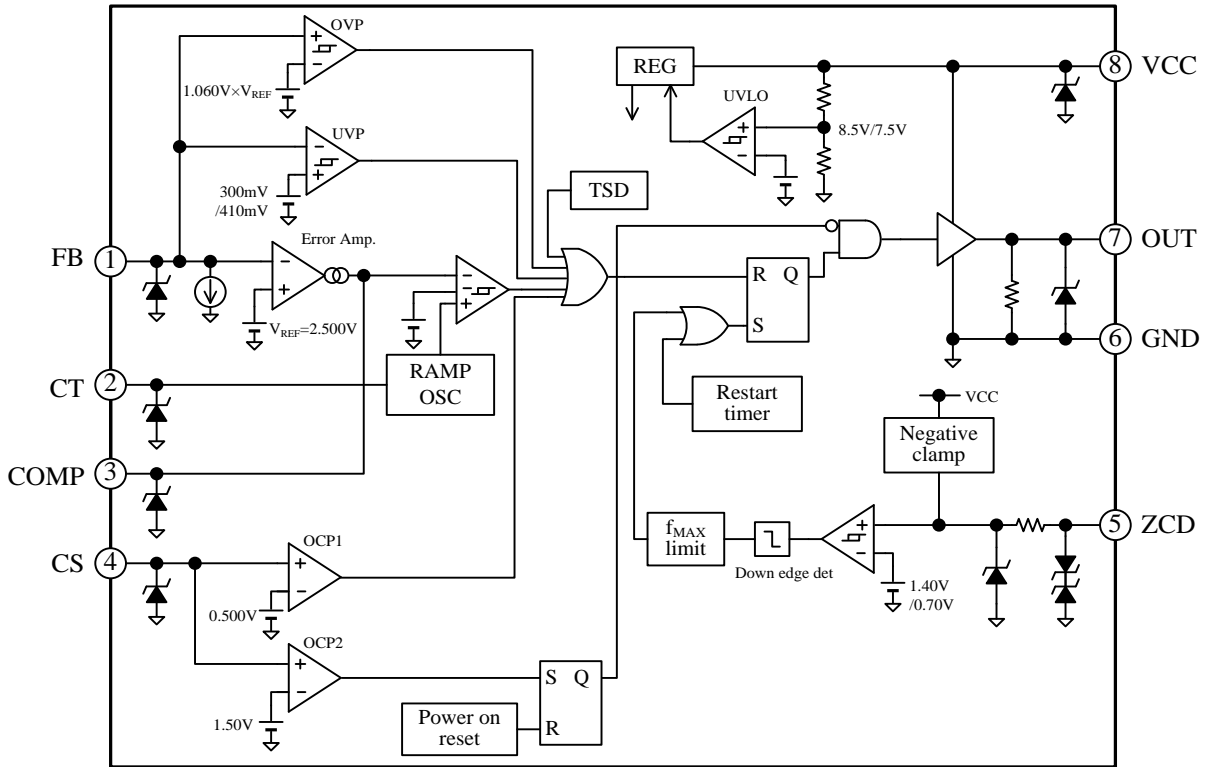
Figure 3-1 Switching time

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Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Zero Current Detection Threshold Voltage (High)	$V_{ZCD(H)}$		5 – 6	1.25	1.40	1.55	V
Zero Current Detection Threshold Voltage (Low)	$V_{ZCD(L)}$		5 – 6	0.60	0.70	0.80	V
Zero Current Detection Delay Time <sup>(1)</sup>	$t_{DLY(ZCD)}$		5 – 6	–	70	160	ns
ZCD Pin Clamp Voltage	$V_{ZCD(CL)}$	$I_{ZCD}=3mA$	5 – 6	6.5	7.7	9.0	V
<b>Overcurrent Protection Function</b>							
Overcurrent Protection Threshold Voltage 1	$V_{CS(OC1)}$		4 – 6	0.475	0.500	0.525	V
Overcurrent Protection Threshold Voltage 2	$V_{CS(OC2)}$		4 – 6	1.35	1.50	1.65	V
Overcurrent Protection Delay Time	$t_{DLY(OC)}$		4 – 6	90	215	340	ns
CS Pin Source Current	$I_{CS}$		4 – 6	– 40	– 20	– 10	$\mu A$
<b>FB Pin Protection Function</b>							
Overvoltage Protection Threshold Voltage	$V_{OVP}$		1 – 6	$1.040 \times V_{REF}$	$1.060 \times V_{REF}$	$1.080 \times V_{REF}$	V
Overvoltage Protection Hysteresis	$V_{OVP(HYS)}$		1 – 6	40	60	80	mV
Undervoltage Protection Threshold Voltage	$V_{UVP}$		1 – 6	200	300	400	mV
Undervoltage Protection Hysteresis	$V_{UVP(HYS)}$		1 – 6	70	110	150	mV
<b>Thermal Shutdown Protection</b>							
Thermal Shutdown Threshold <sup>(1)</sup>	$T_{j(TSD)}$		–	135	150	–	°C
Thermal Shutdown Hysteresis <sup>(1)</sup>	$T_{j(TSDHYS)}$		–	–	10	–	°C
<b>Thermal Resistance</b>							
Junction to Ambient Resistance <sup>(1)</sup>	$\theta_{j-A}$		–	–	–	180	°C/W

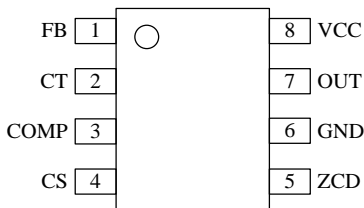
<sup>(1)</sup> Design assurance item

3. Block Diagram



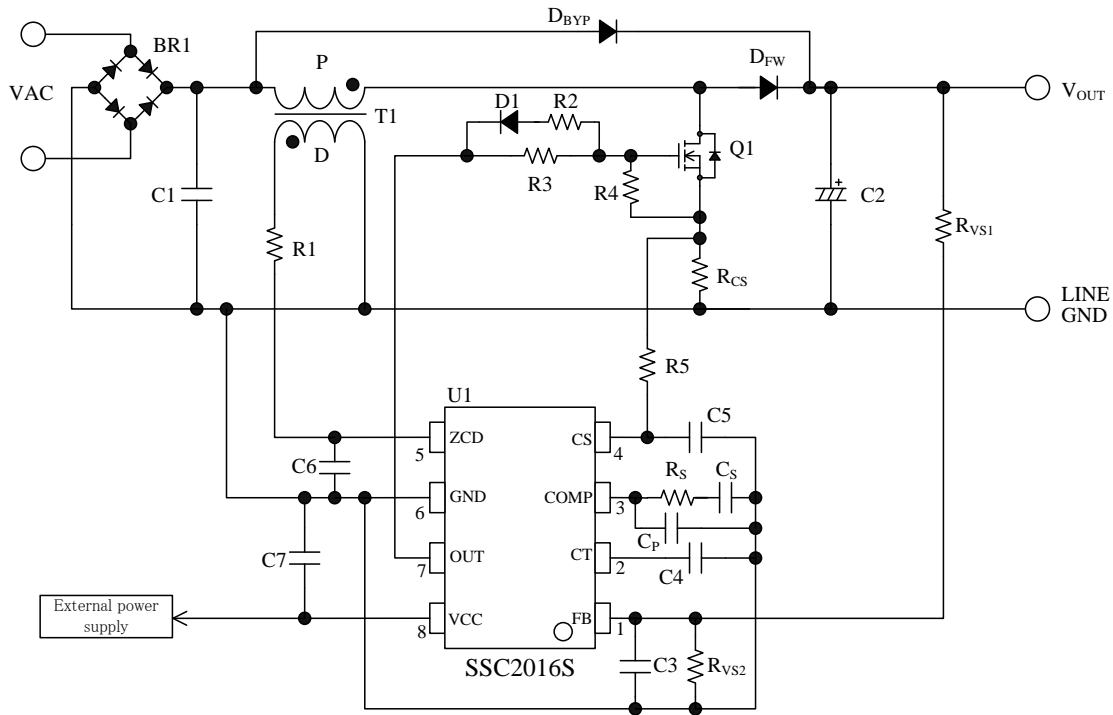
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4. Pin Configuration Definitions



Number	Name	Function
1	FB	Feedback signal input, Overvoltage Protection signal input and FB pin Undervoltage Protection signal input
2	CT	Timing capacitor connection
3	COMP	Phase compensation
4	CS	Overcurrent Protection signal input
5	ZCD	Zero current detection signal input and bottom-on-timing adjustment
6	GND	Ground
7	OUT	Gate drive output
8	VCC	Power supply input for control circuit

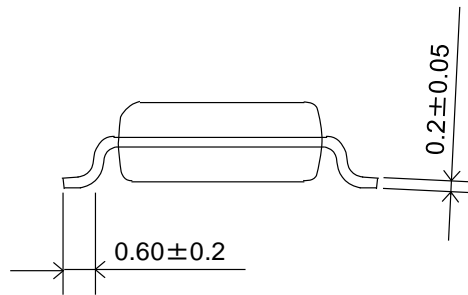
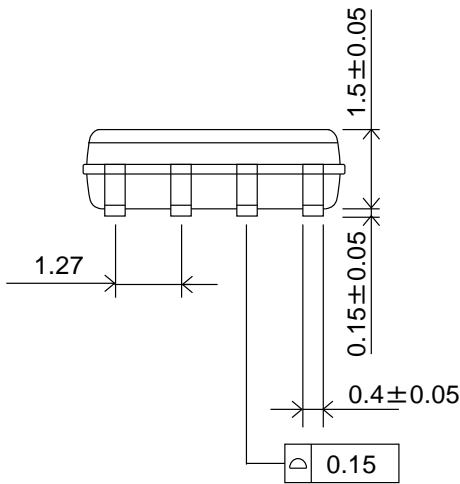
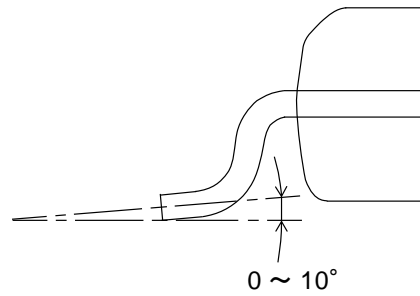
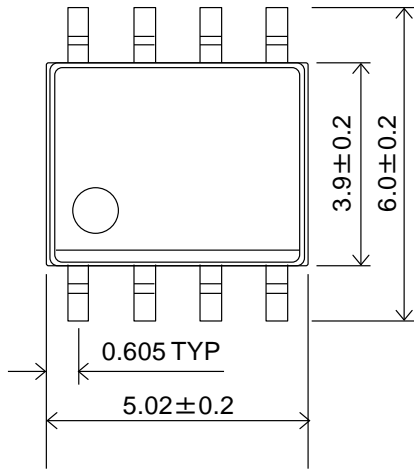
5. Typical Application



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6. External Dimensions

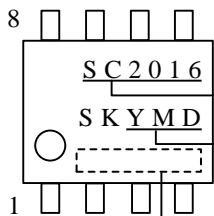
SOIC8



NOTES:

- All linear dimensions are in millimeters
- Pb-free. Device composition compliant with the RoHS directive.

7. Marking Diagram



Part Number

Lot Number:

Y is the last digit of the year of manufacture (0 to 9)

M is the month of the year (1 to 9, O, N, or D)

D is a period of days:

1: the first 10 days of the month (1st to 10th)

2: the second 10 days of the month (11th to 20th)

3: the last 10-11 days of the month (21st to 31st)

Control Number



### 8. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (-).

#### 8.1 Critical Conduction Mode: CRM

Figure 8-1 and Figure 8-2 show the PFC circuit and CRM operation waveform. The IC performs the on/off operation of switching device Q1 in critical mode (the inductor current is zero). Thus, the low drain current variation di/dt of power MOSFET is accomplished. Also, adjusting the turn-on timing at the bottom point of  $V_{DS}$  free oscillation waveform (quasi-resonant operation), low noise and high efficiency PFC circuit is realized.

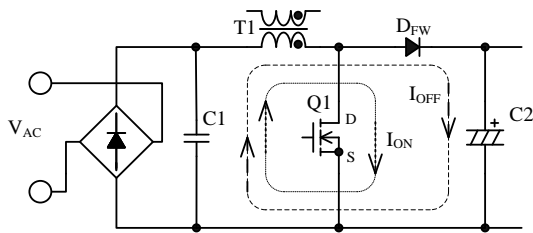


Figure 8-1. PFC Circuit

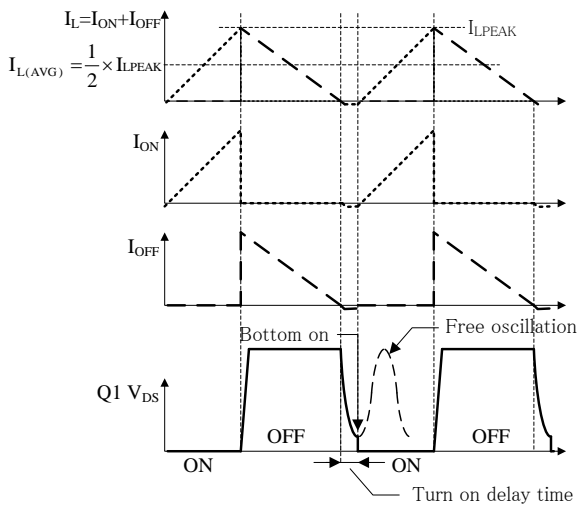


Figure 8-2. CRM Operation and Bottom On Operation

Figure 8-3 shows the internal CRM control circuit.

The power MOSFET Q1 starts switching operation by self-oscillation.

The on-time control is as follows: the detection

voltage  $R_{VS2}$  is compared with the Feedback Voltage Reference  $V_{REF} = 2.500 \text{ V}$  by using error amplifier (Error AMP) connected to FB pin. The output of the Error AMP is averaged and the phase is compensated. This signal  $V_{COMP}$  is compared with the ramp signal  $V_{OSC}$  to achieve the on-time control. The on-time becomes almost constant in commercial cycle by setting  $V_{COMP}$  to respond below 20 Hz (Figure 8-4). This is achieved by tuning the capacitor connected to COMP pin.

The off-time is set by detecting the zero current signal of boost winding P. The zero current is detected by auxiliary winding D and ZCD pin.

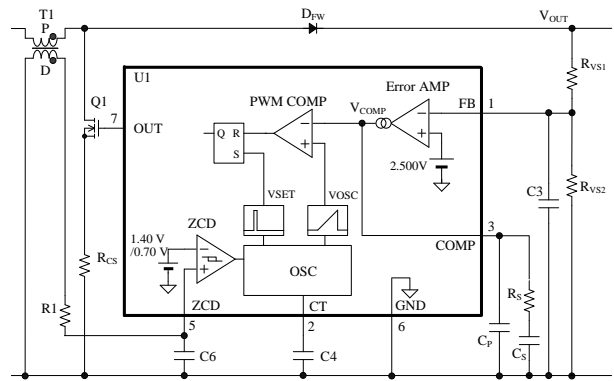


Figure 8-3. CRM Control Circuit

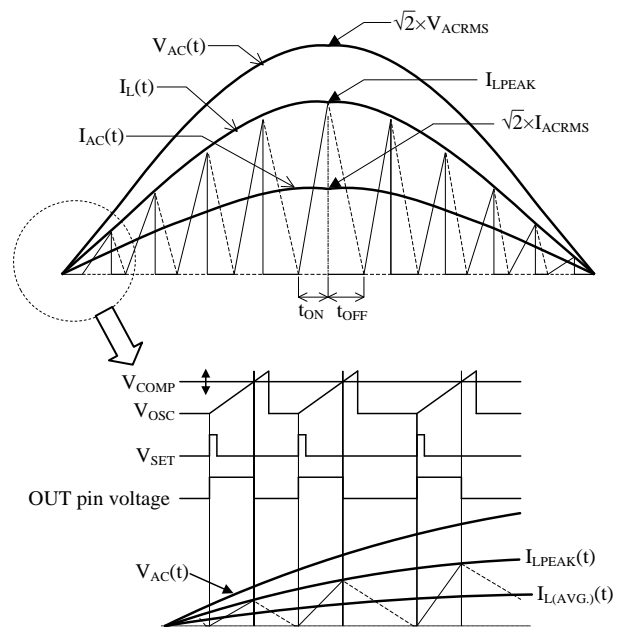


Figure 8-4 CRM Operation Waveforms

The off duty  $D_{OFF}$  of boost converter in CRM mode have the relation of  $D_{OFF}(t) = V_{AC}(t)/V_{OUT}$  and is proportional to input voltage, where  $V_{AC}(t)$  is the input

voltage of AC line as a function of time.

As a result of aforementioned control shown in Figure 8-4, the peak current  $I_{LPEAK}$  of the inductance current  $I_L$  becomes sinusoidal. Since the averaged input current become similar to AC input voltage waveform by Low Pass Filter at input stage, high power factor is achieved.

## 8.2 Startup Operation

Figure 8-5 and Figure 8-7 show the VCC pin peripheral circuit. Figure 8-5 shows how to use an external power supply. Figure 8-7 shows how to use an auxiliary winding.

### 8.2.1 To Use an External Power Supply

When an external power supply shown in Figure 8-5 is used, the startup operation is as follows.

As shown in Figure 8-6, when VCC pin voltage rises to the Operation Start Voltage  $V_{CC(ON)} = 8.5\text{ V}$ , the control circuit starts operation and the COMP pin voltage increases. The COMP pin voltage increases to the Zero Duty COMP Voltage  $V_{COMP(ZD)} = 0.65\text{ V}$ , switching operation starts.

When the VCC pin voltage decreases to  $V_{CC(OFF)} = 7.5\text{ V}$ , the control circuit stops operation by Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

Since the COMP pin voltage rises from zero during startup period, the  $V_{COMP}$  signal shown in Figure 8-3 gradually rises from low voltage. The on-width gradually increased to restrict the rise of output power by the Softstart Function. Thus, the stress of the peripheral component is reduced.

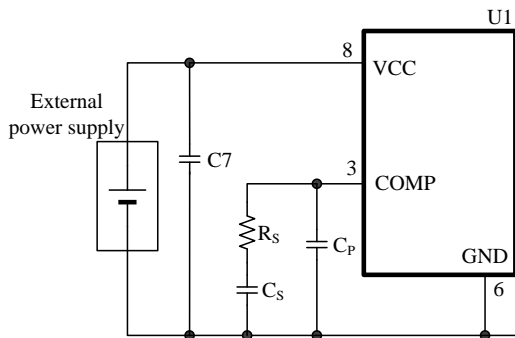


Figure 8-5. VCC Pin Peripheral Circuit (Power supply from external power supply)

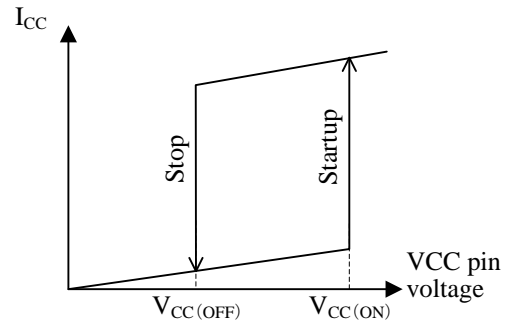


Figure 8-6. Relationship between VCC Pin Voltage and  $I_{CC}$

### 8.2.2 To Use an Auxiliary Winding

When an auxiliary winding is used as shown in Figure 8-7,  $C_{VCC}$  is charged through  $R_{ST}$  at startup. When VCC pin voltage rises to  $V_{CC(ON)} = 8.5\text{ V}$ , the control circuit starts operation.

Figure 8-8 shows the VCC pin voltage behavior during startup period.

When the VCC pin voltage reaches  $V_{CC(ON)}$ , the control circuit starts operation. Then the circuit current increases and the VCC pin voltage decreases. At the same time, the auxiliary winding voltage  $V_D$  increases in proportion to the output voltage. These are all balanced to produce VCC pin voltage.

The value of  $C_{VCC}$ , the turns ratio of boost winding P and auxiliary winding D should be set so that VCC pin voltage is maintained higher than  $V_{CC(OFF)}$  (See Section 9.1.2).

If the values of  $R_{ST}$  and  $C_{VCC}$  are large, the startup time becomes longer. Adjustment is necessary in actual operation.

When the COMP pin voltage increases to the Zero Duty COMP Voltage  $V_{COMP(ZD)} = 0.65\text{ V}$  after the control circuit starts operation, switching operation starts and the circuit current is supplied from auxiliary winding D as follows.

$V_B$  and  $V_D$  are the voltage of auxiliary winding during Q1 on and off, respectively.

When Q1 is on,  $C_{CP}$  is charged by  $V_B$ . When Q1 is off, the capacitor connected to VCC pin,  $C_{VCC}$ , is charged by  $V_D + V_B (=V_{CCP})$ .

$V_B$  is calculated using Equation (1).

$$V_B = V_{IN} \times \frac{N_D}{N_P} \quad (V) \quad (1)$$

Where

$V_{IN}$ : C1 voltage (V)

$N_P$ : Number of turns of boost winding P (turns)

$N_D$ : Number of turns of auxiliary winding D (turns)

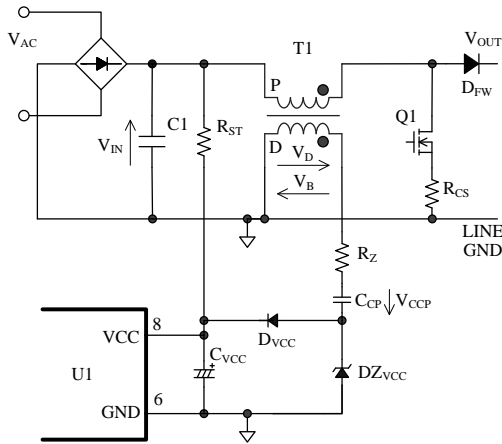


Figure 8-7. VCC Pin Peripheral Circuit (Power supply from auxiliary winding)

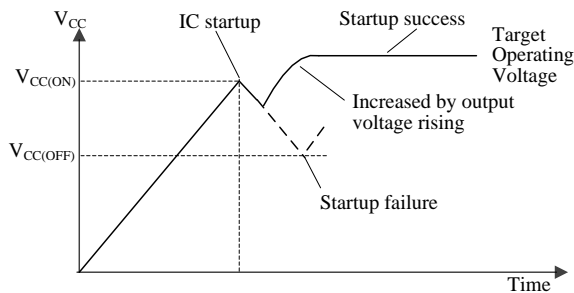


Figure 8-8. VCC During Startup Period

### 8.3 Restart Circuit

The IC is self-oscillation type. The off-time of OUT pin is set by the detecting zero current signal at ZCD pin.

When the off-time of OUT pin is maintained for  $t_{RS} = 220 \mu s$  or more, the restart circuit is activated and OUT pin turns on. The ON time of the OUT pin is  $t_{ON(RS)} = 1.7 \mu s$  in the restart operation.

At intermittent oscillation period in startup and light load, the restart circuit is activated and the switching operation is stabilized.

Since  $t_{RS} = 220 \mu s$  corresponds to the operational frequency of 6.25 kHz, the minimum frequency should be set to higher than 20 kHz (above audible frequency) at the inductance value design.

### 8.4 Maximum On-time Setting

In order to reduce audible noise of transformer at transient state, the Maximum on-time,  $t_{ON(MAX)}$ , should be set. The  $t_{ON(MAX)}$  depends on the value of C4 connected to CT pin. Section 9.1 shows about  $t_{ON(MAX)}$  setting.

### 8.5 Zero Current Detection and Bottom-on Timing Setting

Figure 8-9 shows the peripheral circuit of ZCD pin, Figure 8-10 shows the zero current detection waveform.

The off-time is determined by detecting the zero current of the boost winding P via the auxiliary winding D and ZCD pin

The polarity of winding P and winding D of transformer T1 are shown in Figure 8-9.

When the OUT pin voltage becomes low and the power MOSFET turns off, the ZCD pin voltage becomes the voltage of auxiliary winding D as shown in Figure 8-10. After the turning off of the power MOSFET, when ZCD pin voltage is above  $V_{ZCD(H)} = 1.40 V$ , OUT pin voltage is kept to be Low. When ZCD pin voltage becomes below  $V_{ZCD(L)} = 0.70 V$ , OUT pin voltage becomes High and power MOSFET turns on.

After the turning off of the power MOSFET, when the current in boost winding become zero,  $V_{DS}$  waveform starts free oscillation based on the inductance  $L_P$ , the output capacitance of power MOSFET  $C_{OSS}$  and the parasitic capacitance. The bottom point of  $V_{DS}$  is calculated as follows:

$$t_{HFP} \approx \pi \sqrt{L_P \times C_V} \quad (2)$$

where

$t_{HFP}$ : Half cycle of free oscillation (s)

$L_P$ : Inductance of boost winding (H)

$C_V$ : Combined output capacitance of power MOSFET  $C_{OSS}$  and parasitic capacitance (F)

In order to set the timing of turn on to the bottom point of  $V_{DS}$  as shown in Figure 8-11, adjust the turn on delay time  $t_{HFP}$  by using C6 and R1 in actual operation condition as shown in Figure 8-9. Since R1 have a role as the current limiting resistor of ZCD pin, adjust the C6 value if R1 value exceeds the range of limiting.

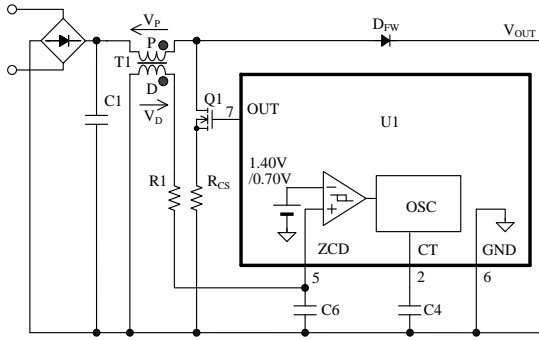


Figure 8-9. ZCD Pin Peripheral Circuit

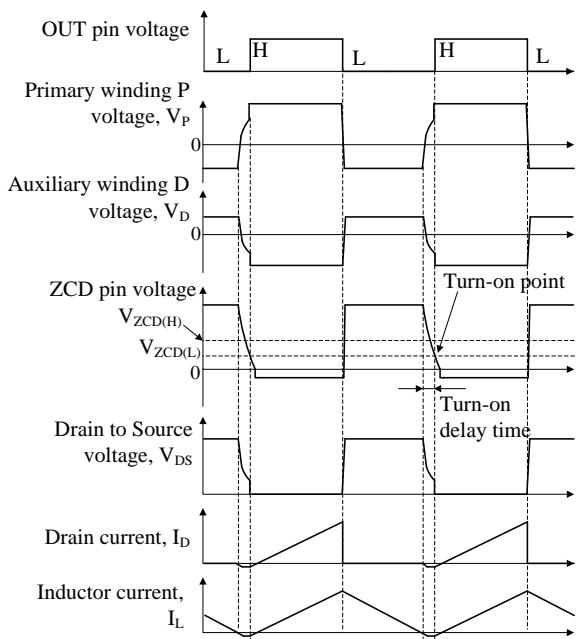


Figure 8-10. Zero Current Detection Waveform

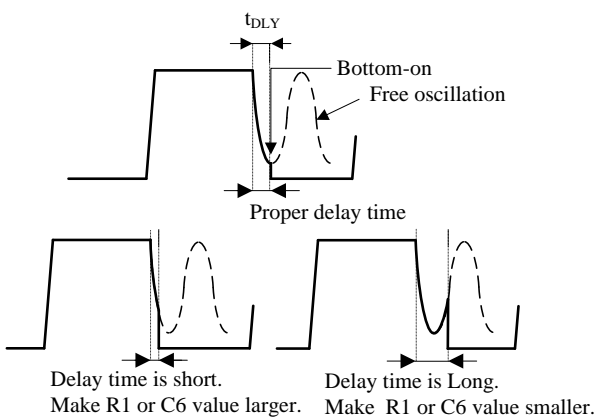


Figure 8-11.  $V_{DS}$  Turn On Timing

### 8.6 Maximum Switching Frequency Limitation Function

In the CRM operation, the switching frequency of a power MOSFET is varied in a period of sinusoidal AC input voltage. The switching frequency is lowest in the peak of AC input voltage and is high as getting close to the bottom of it. In addition, when output load decreases, the switching frequency increases entirely. In order to reduce the switching loss, the IC has the Maximum Switching Frequency Limitation Function that limits the switching frequency to  $f_{MAX}$  of 300 kHz.

### 8.7 Overcurrent Protection (OCP)

Figure 8-12 shows the CS pin peripheral circuit and internal circuit. The inductor current,  $I_L$  is detected by the detection resistor,  $R_{CS}$ . The detection voltage,  $V_{RCS}$ , is fed into CS pin. As shown in Figure 8-12, the CS pin is connected to capacitor-resistor filter ( $R5$  and  $C5$ ).

The IC has two Overcurrent Protection (OCP) threshold voltages.

- OCP1**  
 When  $V_{RCS}$  increases  $V_{CS(OCP1)} = 0.500\text{ V}$  or more, the output of the OUT pin becomes Low by pulse-by-pulse.
- OCP2**  
 OCP2 is activated by malfunctions such as the short of a boost diode,  $D_{FW}$ . If the instantaneous large current flows to a power MOSFET and the CS pin voltage increases to  $V_{CS(OSP2)} = 1.50\text{ V}$  or more and this operation continues seven times, the output of OUT pin is latched to low level. Releasing the latched state is done by turning off the input voltage and by dropping VCC pin voltage below  $V_{CC(OFF)}$ .

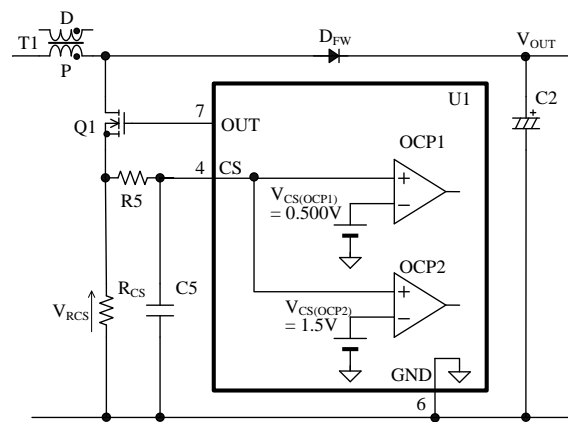


Figure 8-12. The CS Pin Peripheral Circuit and Internal Circuit.

### 8.8 Overvoltage Protection (OVP)

Figure 8-13 shows the waveforms of Overvoltage Protection (OVP) operation. When the FB pin voltage increase to Overvoltage Protection Threshold Voltage,  $V_{OVP}$ , OUT pin voltage become Low immediately and the switching operation stops. As a result, the rise of output voltage is prevented.  $V_{OVP}$  is 1.060 times the Feedback Voltage Reference,  $V_{REF} = 2.500\text{ V}$ . When the cause of the overvoltage is removed and FB pin voltage decreases to  $V_{OVP} - V_{OVP(HYS)}$  the switching operation restarts.

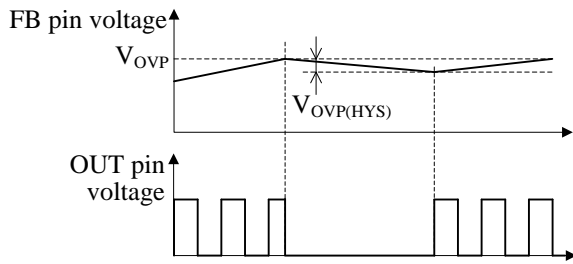


Figure 8-13. OVP Waveforms

### 8.9 FB Pin Under Voltage Protection (FB\_UVP)

FB pin Under Voltage Protection (FB\_UVP) is activated when the FB pin voltage is decreased by the malfunctions in feedback loop such as the open of  $R_{VS1}$ , the short of  $R_{VS2}$ , or the open of FB pin.

Figure 8-14 shows the FB pin peripheral circuit and internal circuit. When the FB pin voltage is decreased to  $V_{UVP} = 300\text{ mV}$  or less, the OUT pin output is turned-off immediately and switching operation stops. This prevents the rise of output voltage. When the cause of malfunction is removed and the FB pin voltage rises to  $V_{UVP} + V_{UVP(HYS)}$ , the switching operation restarts.

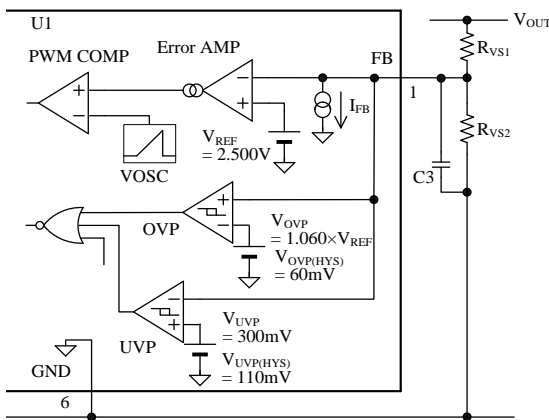


Figure 8-14. The FB Pin Peripheral Circuit and Internal Circuit.

### 8.10 Thermal Shutdown (TSD)

#### < Using External Power Supply >

When the temperature of control circuit increases to  $T_{j(TSD)} = 150\text{ }^\circ\text{C}$  or more, Thermal Shutdown (TSD) is activated and the IC stops switching operation.

When the fault condition is removed and the temperature decreases to less than  $T_{j(TSD)} - T_{j(TSDHYS)}$ , the IC returns to normal operation automatically.

#### < Using Auxiliary Winding D for VCC supply >

When TSD is activated and the IC stops switching operation, VCC pin voltage decreases to  $V_{CC(OFF)}$  and the control circuit stops operation. After that, the IC reverts to the initial state by UVLO circuit, and the IC starts operation when VCC pin voltage increases to  $V_{CC(ON)}$  by startup current. Thus the intermittent operation by UVLO is repeated in TSD state.

When the fault condition is removed and the temperature decreases to less than  $T_{j(TSD)} - T_{j(TSDHYS)}$ , the IC returns to normal operation automatically.

## 9. Design Notes

### 9.1 Inductor Design

Inductor T1 consists of a boost winding P and auxiliary winding D. The winding P is used for boosting the voltage and winding D is used for off-timing detection.

The calculation methods of winding P and winding D are as shown below. Since the following calculating formulas are approximated, the peak current and the frequency of operational waveforms may be different from the setting value at calculating. Eventually, the inductance value should be adjusted in actual operation.

Apply proper design margin to temperature rise by core loss and copper loss.

#### 9.1.1 Boost winding, P

Inductance  $L_P$  of PFC in CRM mode is calculated as follows:

##### 1) Output Voltage, $V_{OUT}$

The output voltage  $V_{OUT}$  of boost-converter should be set higher than peak value of input voltage as following equation:

$$V_{OUT} \geq \sqrt{2} \times V_{ACRMS(MAX)} \times V_{DIF} \quad (3)$$

where

$V_{ACRMS(MAX)}$ : Maximum AC input voltage rms value (V)

$V_{DIF}$ : Boost voltage (about 10V) (V)

**2) Operational Frequency,  $f_{SW(SET)}$**

Determine  $f_{SW(SET)}$  that is minimum operational frequency at the peak of the AC line waveform. The frequency becomes higher with lowering the input voltage. The frequency at the peak of the AC line waveform,  $f_{SW(SET)}$  should be set more than the audible frequency (20 kHz).

**3) Inductance,  $L_P$**

Substituting both minimum and maximum of AC input voltage to  $V_{ACRMS}$ , choose a smaller one as  $L_P$  value.  $L_P$  is calculated as follows:

$$L_P = \frac{\eta \times V_{ACRMS}^2 \times (V_{OUT} - \sqrt{2} \times V_{ACRMS})}{2 \times P_{OUT} \times f_{SW(SET)} \times V_{OUT}} \quad (H) \quad (4)$$

where

$V_{ACRMS}$ : Maximum or minimum AC input voltage rms value (V)

$P_{OUT}$ : Output Power (W)

$f_{SW(SET)}$ : Minimum operational frequency at the peak of the AC line waveform (kHz)

(The operational frequency becomes lowest at the peak of the AC line waveform.  $f_{SW(SET)}$  should be set above frequency of 20 kHz.)

$\eta$ : Efficiency of PFC

(In general, the range of  $\eta$  is 0.90 to 0.97, depending on on-resistance of power MOSFET  $R_{DS(ON)}$  and forward voltage drop of rectifier diode  $V_F$ .)

**4) Inductor peak current,  $I_{LP}$**

$I_{LP}$  is peak current at the minimum of AC input voltage waveform.  $I_{LP}$  calculated as follows:

$$I_{LP} = \frac{2\sqrt{2} \times P_{OUT}}{\eta \times V_{ACRMS(MIN)}} \quad (A) \quad (5)$$

where,

$P_{OUT}$ : Output power (W)

$V_{ACRMS(MIN)}$ : Minimum AC input voltage rms value (V)

$\eta$ : Efficiency of PFC (About 0.90 to 0.97)

**5) Maximum On-time,  $t_{ON(SET)MAX}$**

$t_{ON(MAX)_OP}$  is calculated by Equation (6) with results of Equation (4) and Equation (5).  $t_{ON(MAX)_OP}$  is the maximum on time of the peak voltage of the minimum AC input voltage.

$$t_{ON(MAX)_OP} = \frac{L_P \times I_P}{\sqrt{2} \times V_{ACRMS(MIN)}} \quad (s) \quad (6)$$

where,

$L_P$ : Inductance value of the result of Equation (4)

$V_{ACRMS(MIN)}$ : Minimum AC input voltage rms value (V)

Equation (7) shows the relationship between maximum on time,  $t_{ON(MAX)}$ , and CT pin capacitor, C4

(see Section 8.4). C4 should be set so as  $t_{ON(MAX)}$  is larger than  $t_{ON(MAX)_OP}$  that is calculated by Equation (6). The value of C4 is about 330 pF to 1500 pF

$$t_{ON(MAX)} = \frac{C4 \times V_{CT(OFF)}}{|I_{CT}|} \quad (s) \quad (7)$$

where

C4: Capacitance of capacitor connected to CT pin ( $\mu F$ )

$V_{CT(OFF)}$ : CT Pin Threshold Voltage (V)

$I_{CT}$ : CT Pin Source Current ( $\mu A$ )

**9.1.2 Auxiliary Winding, D**

Figure 9-1 shows the polarity of boost winding P and auxiliary winding D.

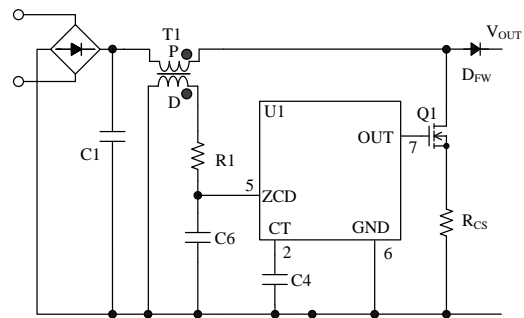


Figure 9-1. ZCD Peripheral Circuit

Given the number of windings of each winding as  $N_P$  and  $N_D$ , the turn ratio  $N_D/N_P$  is set satisfying following conditions.

The condition of  $N_D/N_P$  making ZCD pin voltage above  $V_{ZCD(H)} = 1.40 V$  after power MOSFET turns off is expressed as follows:

$$\frac{N_D}{N_P} > \frac{V_{ZCD(H)}}{V_{OUT} - \sqrt{2} \times V_{ACRMS(MAX)}} \quad (8)$$

where

$N_P$ : The number of turns of boost winding P (turns)

$N_D$ : The number of turns of auxiliary winding D (turns)

$V_{OUT}$ : Output voltage (V)

$V_{ACRMS(MAX)}$ : Maximum AC input voltage rms value (turns)

When power supply of VCC pin is supplied from auxiliary winding as shown in Figure 9-2, the condition of  $N_D/N_P$  is set to larger rate of Equation (8) or Equation (9).

The maximum VCC pin input voltage is limited by the zener voltage of  $DZ_{VCC}$ . The minimum VCC pin input voltage must be set higher than the maximum

value of  $V_{CC(ON)}$ , 9.5 V.

$$\frac{N_D}{N_P} > \frac{2(V_{CC(ON)max.} + V_{FVCC})}{V_{OUT}} \quad (9)$$

where

$N_P$ : The number of turns of boost winding P (turns)

$N_D$ : The number of turns of auxiliary winding D (turns)

$V_{OUT}$ : Output voltage (V)

$V_{CC(ON)max.}$ : the maximum value of Operation Start Voltage,  $V_{CC(ON)}$ , (V)

$V_{FVCC}$ : Forward voltage of  $D_{VCC}$  (V)

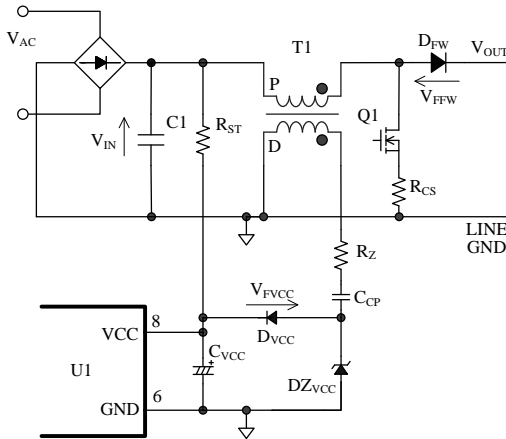


Figure 9-2. VCC Pin Peripheral Circuit (Power supply from auxiliary winding)

## 9.2 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

Figure 9-3 shows the IC peripheral circuit.

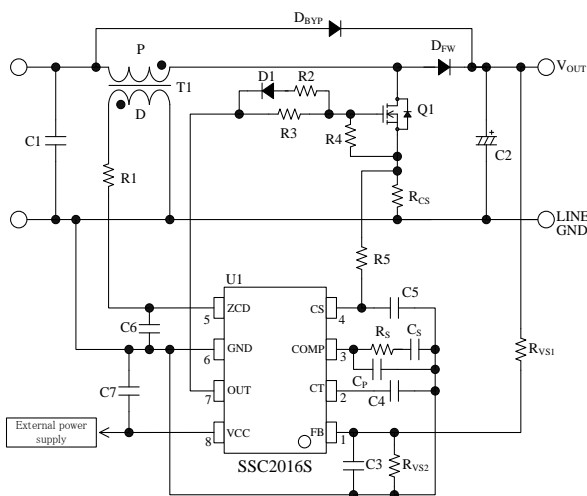


Figure 9-3. The IC Peripheral Circuit.

### 9.2.1 FB Pin Peripheral Circuit (Output Voltage Detection)

The output voltage  $V_{OUT}$  is set using  $R_{VS1}$  and  $R_{VS2}$ . It is expressed by the following formula:

$$V_{OUT} = \left( \frac{V_{REF}}{R_{VS2}} + I_{FB} \right) \times R_{VS1} + V_{REF} \quad (10)$$

where

$V_{REF}$ : Feedback Voltage Reference = 2.500 V

$I_{FB}$ : FB sink current = 0.7  $\mu$ A

$R_{VS1}$ ,  $R_{VS2}$ : Combined resistance to set  $V_{OUT}$  ( $\Omega$ )

Since  $R_{VS1}$  have applied high voltage and have high resistance value,  $R_{VS1}$  should be selected from resistors designed against electromigration or use a combination of resistors for that.

The value of capacitor C3 between FB pin and GND pin is set approximately 100 pF to 0.01  $\mu$ F, in order to reduce the switching noise.

### 9.2.2 COMP Pin Peripheral Circuit, $R_S$ , $C_S$ and $C_P$

The FB pin voltage is induced into internal Error AMP. The output voltage of the Error AMP is averaged by the COMP pin. The on-time control is achieved by comparing the signal  $V_{COMP}$  and the ramp signal  $V_{OSC}$ .  $C_S$  and  $R_S$  adjust the response speed of changing on-time according to output power.

The typical value of  $C_S$  and  $R_S$  are 1  $\mu$ F and 68 k $\Omega$ , respectively. When  $C_S$  value is too large, the response becomes slow at dynamic variation of output and the output voltage decreases.

Since  $C_S$  and  $R_S$  affect on the soft-start period at startup, adjustment is necessary in actual operation.

The ripple of output detection signal is averaged by  $C_P$ . When the  $C_P$  value is too small, the IC operation may become unstable due to the output ripple. The value of capacitor  $C_P$  is approximately 1  $\mu$ F.

### 9.2.3 CT Pin Peripheral Circuit, $C_4$

$C_4$  in Figure 9-3 is a capacitor for the maximum on time setting. See Section 9.1.1 for  $C_4$  setting.

### 9.2.4 CS Pin Peripheral Circuit, $R_{CS}$ , $R_5$ and $C_5$

$R_{CS}$  shown in Figure 9-3 is current sensing resistor.  $R_{CS}$  is the resistor for the current detection. A high frequency switching current flows to  $R_{CS}$ , and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

$R_{CS}$  is calculated using the following Equation (11), where Overcurrent Protection Threshold Voltage  $V_{CS(OCp)}$  is 0.500 V and  $I_{LP}$  is calculated using Equation (5).

$$R_{CS} \leq \frac{|V_{CS(OCp)}|}{I_{LP}} (\Omega) \quad (11)$$

The loss  $P_{RCS}$  at  $R_{CS}$  is calculated by Equation (13) using Equation (12).

$$I_{DRMS} = \frac{2\sqrt{2} \times P_{OUT}}{\eta \times V_{ACRMS(MIN)}} \times \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times V_{ACRMS(MIN)}}{9 \times \pi \times V_{OUT}}} (A) \quad (12)$$

$$P_{RCS} = I_{DRMS}^2 \times R_{CS} (W) \quad (13)$$

Where

- $I_{DRMS}$ : RMS Drain current (A)
- $V_{ACRMS(MIN)}$ : Minimum AC input voltage rms value (V)
- $V_{OUT}$ : Output voltage (V)
- $P_{OUT}$ : Output power (W)
- $\eta$ : Efficiency of PFC

The CR filter (R5 and C5) is connected to CS pin.

CR filter (R5 and C5) prevents IC from responding to the drain current surge at MOSFET turn-on and avoids the unstable operation of the IC.

R5 value of approximately 47  $\Omega$  is recommended, since the CS Pin Source Current affects the accuracy of OCP detection.

C5 value is recommended to be calculated by using following formula in which cut-off frequency of CR filter (C5 and R5) is approximately 0.5 MHz to 3.0MHz.

$$C5 = \frac{1}{2\pi \times 1 \times 10^6 \times R5} (F) \quad (14)$$

If R5 value is 47  $\Omega$ , C5 value is approximately 1000 pF to 6800 pF. C5 value should adjust based on actual operation in application.

### 9.2.5 ZCD Pin Peripheral Circuit, R1 and C6

R1 is for the limiting of the input and output current to ZCD pin. The value of resistor R1 is determined so that the ZCD pin current is smaller than the absolute maximum rating. The recommended value of ZCD pin current is less than 3 mA.

The R1 value is chosen to satisfy both Equation (15) and Equation (16). In addition, the bottom-on timing is set by C6 and R1 (See Section 8.5).

#### 1) Limiting of ZCD pin source current (at Q1 ON state)

$$R1 > \frac{\sqrt{2} \times V_{ACRMS(MAX)} \times \frac{N_D}{N_P}}{3 \times 10^{-3}(A)} (\Omega) \quad (15)$$

Where

$V_{ACRMS(MAX)}$ : Maximum AC input voltage rms value (V)

$N_P$ : The number of turns of boost winding P (turns)

$N_D$ : The number of turns of auxiliary winding D (turns)

#### 2) Limiting of ZCD pin sink current (at Q1 OFF state)

$$R1 > \frac{V_{OUT} \times \frac{N_D}{N_P}}{3 \times 10^{-3}(A)} (\Omega) \quad (16)$$

Where

$V_{OUT}$ : Output voltage (V)

$N_P$ : The number of turns of boost winding P (turns)

$N_D$ : The number of turns of auxiliary winding D (turns)

### 9.2.6 OUT Pin Peripheral Circuit (Gate Drive Circuit)

The OUT pin is the gate drive output that can drive the external power MOSFET directly.

The maximum output voltage of OUT pin is the VCC pin voltage. The maximum current is -500 mA for source and 1000 mA for sink, respectively.

R3 is for source current limiting. Both R2 and D1 are for sink current limiting. The values of these components are adjusted to decrease the ringing of Gate pin voltage and the EMI noise. The reference value is several ohms to several dozen ohms.

R4 is used to prevent malfunctions due to steep dv/dt at turn-off of the power MOSFET, and the resistor is connected near the MOSFET, between the gate and source. The reference value of R4 is from 10 k $\Omega$  to 100 k $\Omega$ . R2, R3, D1 and R4 are affected by the printed circuit board trace layout and the power MOSFET capacitance. Thus, the optimal values should be adjusted under actual operation of the application.



### 9.2.7 VCC Pin Peripheral Circuit

< Using External Power Supply >

Figure 9-4 shows the VCC pin peripheral circuit. The value of capacitor C7 is set approximately 1000 pF, in order to reduce the switching noise.

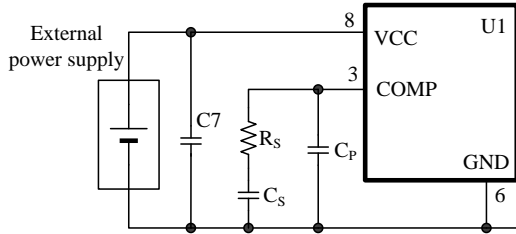


Figure 9-4. VCC Pin Peripheral Circuit (Power supply from external power supply)

< Using Auxiliary Winding D for VCC supply >

Figure 9-5 shows the VCC pin peripheral circuit when VCC pin is supplied from auxiliary winding.

• R<sub>ST</sub>

The value of startup resistor, R<sub>ST</sub> is selected so that the current more than I<sub>CC(OFF)</sub> = 100 μA (max.) can be supplied to VCC pin at startup. R<sub>ST</sub> is expressed as follows:

$$R_{ST} < \frac{\sqrt{2} \times V_{ACRMS(MIN)} - V_{CC(ON)max.}}{I_{CC(OFF)max.}} (\Omega) \quad (17)$$

Where, V<sub>ACRMS(MIN)</sub> is Minimum AC input voltage rms value (V)

When the specification of AC input voltage is 100 V or Universal, the value of R<sub>ST</sub> is approximately 100 kΩ to 220 kΩ. When the specification of AC input voltage is 230 V, the value of R<sub>ST</sub> is approximately 180 kΩ to 330 kΩ.

The rating of R<sub>ST</sub> is chosen taking into account the loss of R<sub>ST</sub> at maximum input voltage. Since the high voltage is applied to resistor, choose a resistor designed against electromigration or use a series combination of resistors.

• C<sub>VCC</sub>

The approximate startup time is determined by the value of C<sub>VCC</sub>. It is calculated as follows where the initial voltage of VCC pin is zero.

$$t_{START} \approx \frac{C7 \times V_{CC(ON)}}{\frac{\sqrt{2} \times V_{ACRMS} - V_{CC(ON)}}{R_{ST}} - I_{CC(OFF)}} (s) \quad (18)$$

In general, power supply applications, C<sub>VCC</sub>, is approximately 22 μF to 47 μF.

• R<sub>Z</sub>, C<sub>CP</sub> and DZ<sub>VCC</sub>

The circuit consists of R<sub>Z</sub>, C<sub>CP</sub> and DZ<sub>VCC</sub> is the boost circuit of VCC pin.

R<sub>Z</sub> is the limiting resistor for the breakdown current of DZ<sub>VCC</sub>. The R<sub>Z</sub> value is approximately 150 Ω.

C<sub>CP</sub> is charged when Q1 is in ON state. The C<sub>CP</sub> value is approximately 22 nF.

Since the absolute maximum rating value of VCC pin is 28 V, the zener voltage of DZ<sub>VCC</sub> is chosen to be less than it.

• C7

If CVCC and the VCC pin are distant from each other, a capacitor C7 should be placed as close as possible to the VCC pin. C7 is approximately 1000 pF, in order to reduce the switching noise.

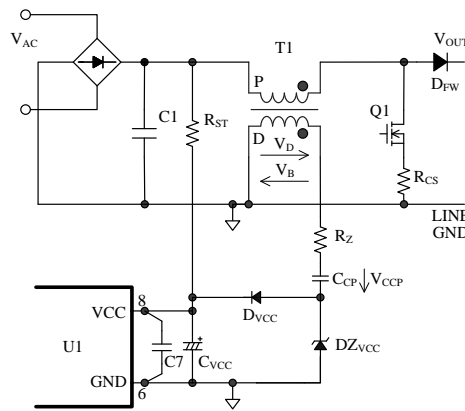


Figure 9-5. VCC Pin Peripheral Circuit (Power supply from auxiliary winding)

### 9.2.8 Power MOSFET, Q1

Choose a power MOSFET having proper margin of V<sub>DSS</sub> against output voltage, V<sub>OUT</sub>. The size of heat sink is chosen taking into account some loss by switching and ON resistance of MOSFET.

The loss P<sub>RDS(ON)</sub> by on-resistance, R<sub>DS(ON)</sub> of power MOSFET is calculated using I<sub>DRMS</sub> of the result of Equation (12) as follows:

$$P_{RDS(ON)} = I_{DRMS}^2 \times R_{DS(ON)125^\circ C} (W) \quad (19)$$

Where

R<sub>DS(ON)125°C</sub>: ON resistance of MOSFET at T<sub>ch</sub> = 125 °C (Ω)

### 9.2.9 Boost Diode, $D_{FW}$

Choose a boost diode having proper margin of a peak reverse voltage  $V_{RSM}$  against output voltage  $V_{OUT}$ .

A fast recovery diode is recommended to reduce the switching noise and loss. Please ask our staff about our lineup. The size of heat sink is chosen taking into account some loss by  $V_F$  and recovery current of boost diode.

The loss of  $V_F$ ,  $P_{DFW}$  is expressed as follows:

$$P_{DFW} = V_F \times I_{OUT} \quad (W) \quad (20)$$

Where

$V_F$ : Forward voltage of boost diode (V)

$I_{OUT}$ : Out put current (A)

### 9.2.10 Bypass Diode, $D_{BYP}$

Bypass diode protects the boost diode from a large current such as an inrush current. A high surge current tolerance diode is recommended. Please ask our staff about our lineup.

### 9.2.11 Output Capacitor, $C_2$

Apply proper design margin to accommodate the ripple current, the ripple voltage and the temperature rise. Use of high ripple current and low impedance types, designed for switch-mode power supplies, is recommended, depending on their purposes.

In order to obtain  $C_2$  value  $C_O$ , calculate both Equation (21) and (23) described in following and select a larger value.

#### 1) Ripple voltage considered

$$C_2 = \frac{I_{OUT}}{2\pi \times f_{LINE} \times V_{OUT(RI)}} \quad (F) \quad (21)$$

Where

$V_{OUT(RIPPLE)}$ :  $C_2$  ripple voltage (10  $V_{PP}$  for example)

$f_{LINE}$ : Line frequency (Hz)

$I_{OUT}$ : Output current (A)

The  $C_2$  voltage is expressed Equation (22).

When the output ripple is high, the  $V_{C_2}$  voltage may reach to Overvoltage Protection voltage,  $V_{OVP}$  in near the maximum value of  $V_{C_2}$ , or input current waveform may be distorted due to the stop of the boost operation in near the minimum value of  $V_{C_2}$ . It is necessary to select large  $C_O$  value or change the setting of output voltage (boost voltage).

$$V_{C_2} = V_{OUT} \pm \frac{V_{OUT(RI)}}{2} \quad (V) \quad (22)$$

#### 2) Output hold time considered

$$C_2 > \frac{2 \times P_{OUT} \times t_{HOLD}}{V_{OUT}^2 - V_{OUT(MIN)}^2} \quad (F) \quad (23)$$

Where

$t_{HOLD}$ : Output hold time (s)

$V_{OUT(MIN)}$ : Minmum output voltage of  $C_2$  during output hold (V)

If  $t_{HOLD} = 20$  ms,  $P_O = 200$  W,  $\eta = 90$  % and the output voltage = 330 V to 390 V,  $C_2$  value is derived as 205  $\mu F$ . Thus,  $C_2$  value of approximately 220  $\mu F$  is connected.

## 9.3 PCB Trace Layout and Component Placement

Since the PCB traces design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 9-6 shows the circuit design example.

#### 1) Main Circuit Trace

This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

#### 2) Control Ground Trace Layout

Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 9-6 as close to the  $R_{CS}$  pin as possible.

#### 3) $R_{CS}$ Trace Layout

$R_{CS}$  should be placed as close as possible to the Source pin and the CS pin. The peripheral components of CS pin should be connected by dedicated pattern from root of  $R_{CS}$ .

The connection between the power ground of the main trace and the IC ground should be at a single point ground which is close to the base of  $R_{CS}$ .

#### 4) Peripheral Component of IC

The components for control connected to the IC should be placed as close as possible to the IC, and should be connected as short as possible to the each pin.

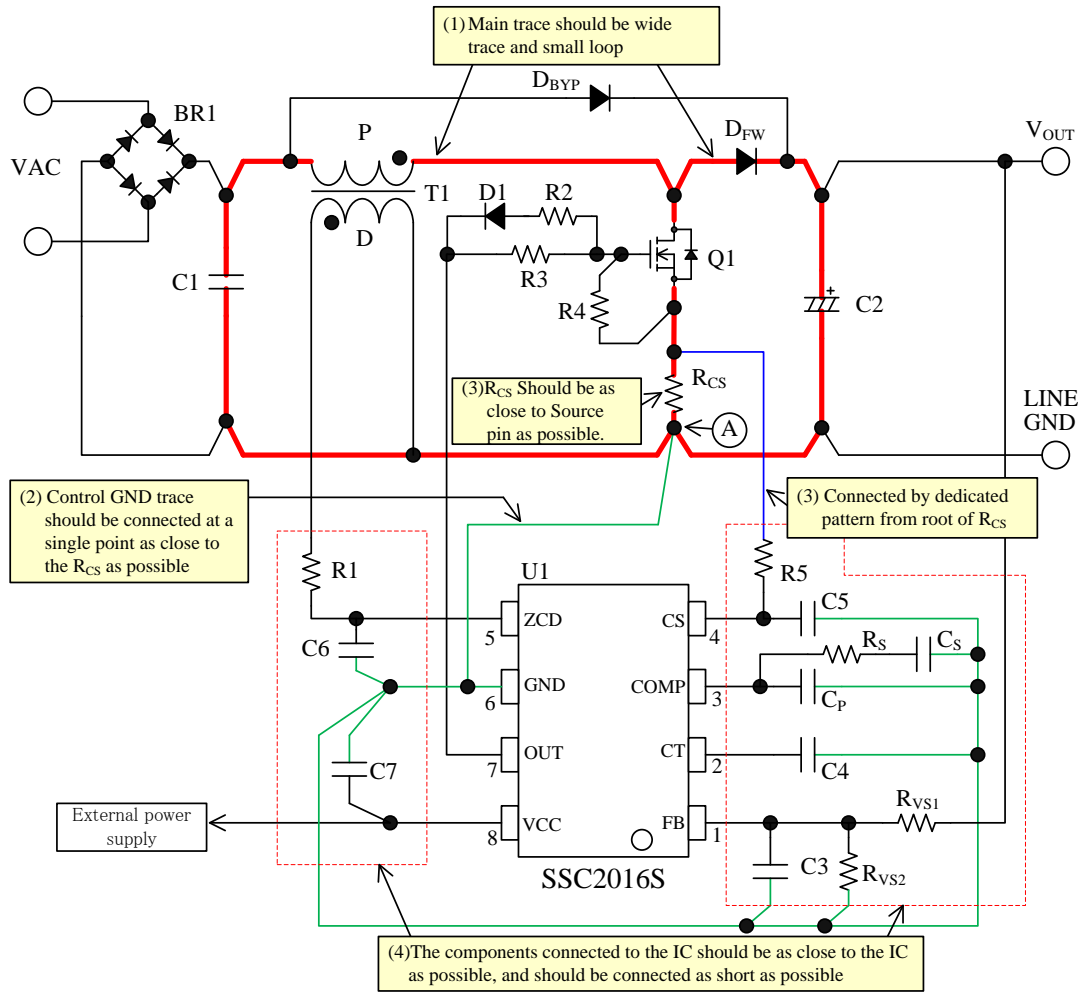


Figure 9-6. Example of Connection of Peripheral Component

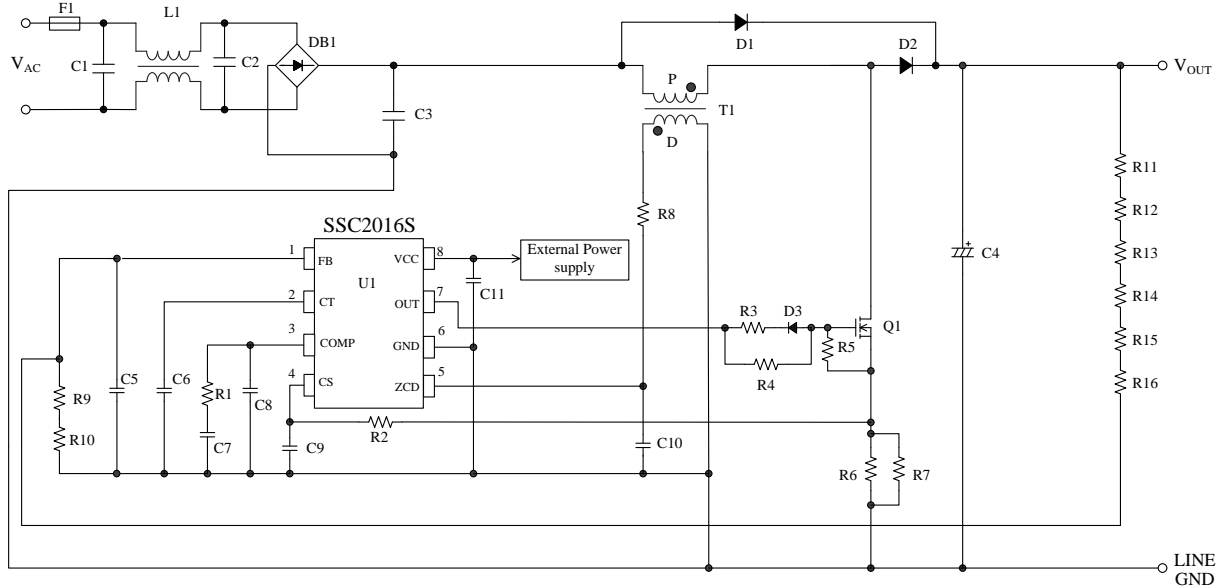
### 10. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

● Power Supply Specifications

IC	SSC2016S
Input Voltage	85V AC to 265VAC
Output Power	100 W (390V, 0.256 A)
Minimum Frequency	45 kHz

● Circuit Schematic



● Bill of Materials

Symbol	Ratings <sup>(1)</sup>	Recommended Sanken Parts	Symbol	Ratings <sup>(1)</sup>	Recommended Sanken Parts
F1	Fuse, AC250 V, 4 A		R1	68 kΩ	
L1	CM inductor, 12 mH		R2	47 Ω	
DB1	Bridge diode, 600 V, 4 A		R3	10 Ω	
D1	600 V, 3 A	RM 4A	R4	100 Ω	
D2	Fast recovery, 600 V, 5 A	FMX-G16S	R5	10 kΩ	
D3	Schottky, 40 V, 1 A	AK 04	R6	0.24 Ω, 1 W	
C1	Film, 0.22 μF, 310 V		R7	0.24 Ω, 1 W	
C2	Film, 0.22 μF, 310 V		R8	47 kΩ	
C3	Ceramic, 0.82 μF, 450V		R9	22 kΩ, ± 1 %	
C4	Electrolytic, 120 μF, 450 V		R10	2 kΩ, ± 1 %	
C5	Ceramic, 0.01 μF		R11	750 kΩ, ± 1 %	
C6	Ceramic, 1000 pF		R12	750 kΩ, ± 1 %	
C7	Ceramic, 0.47 μF		R13	750 kΩ, ± 1 %	
C8	Ceramic, 1 μF		R14	750 kΩ, ± 1 %	
C9	Ceramic, 3300 pF		R15	750 kΩ, ± 1 %	
C10	Ceramic, Open		R16	30 kΩ, ± 1 %	
C11	Ceramic, Open		T1	See the specification	
Q1	Power MOSFET, 600 V, 10A, < 0.75 Ω		U1	IC	SSC2016S

<sup>(1)</sup> Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.

<sup>(2)</sup> It is necessary to be adjusted based on actual operation in the application.

<sup>(3)</sup> Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

## SSC2016S

- Transformer Specification

Primary Inductance : 290  $\mu$ H

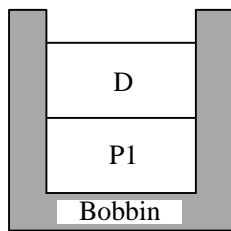
Core Size : EER28

AL-Value : 92.5 nH/N<sup>2</sup>

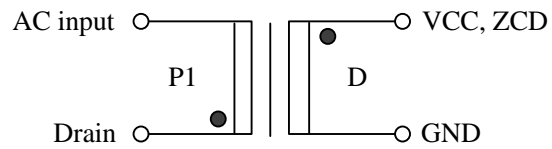
Gap Length : 1.2 mm (center gap)

Winding Specification

Location	Symbol	Number of Turns (turns)	Wire (mm)	Configuration	Note
Primary Winding	P1	56	$\phi$ 0.20 $\times$ 10	Solenoid winding	Litz wire
Auxiliary Winding	D	8	$\phi$ 0.32	Solenoid winding	



Cross-section view



● mark shows the start point of winding

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