

8-IN 4-OUT STEREO AUDIO SELECTOR

■ GENERAL DESCRIPTION

The **NJW1112** is an 8-input 4-output stereo audio selector. It includes four independent 8-input-1output stereo audio selectors and 0dB fixed gain buffers.

The **NJW1112** performs superior audio characteristics such as low distortion, low output noise and low crosstalk.

In addition, the **NJW1112** is available to expand to 16-input 4-output stereo audio selector without sound quality deterioration, because it is able to connect in parallel by Output switch function.

All of internal status and variables are controlled by three-wired serial bus. Selectable two Chip address is available for using two chips on same serial bus line. It is suitable for AV amplifiers, AV receivers, Analog audio switchers, Video conferencing, Security systems and others.

■ PACKAGE OUTLINE

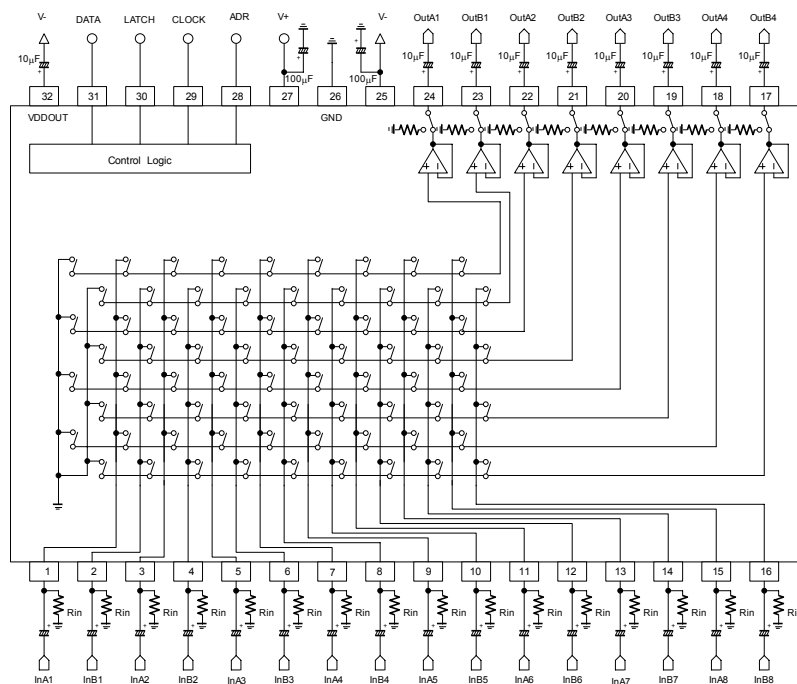


NJW1112V

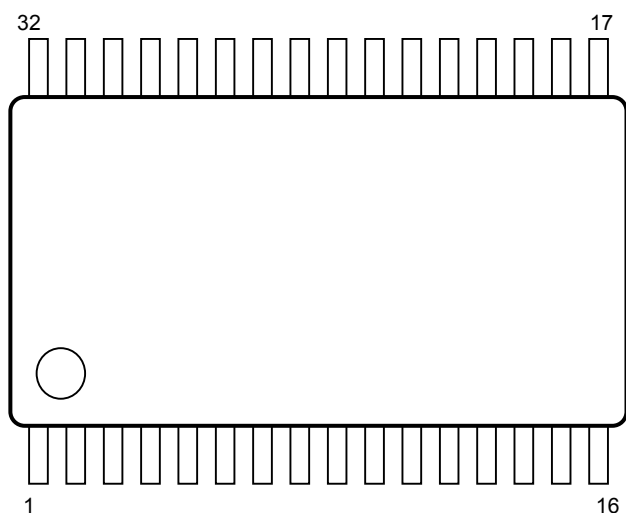
■ FEATURES

- Operating Voltage ± 4.5 to $\pm 7.5V$
- 8-Input, 4-Output Stereo Audio Selector
- Operating Current 14mA typ.
- Low On Resistance Output Switch On Resistance : 15Ω typ.
- Low Distortion 0.0007% typ.
- Low Output Noise -119dBV typ.
- Low Crosstalk 120dB typ.
- Channel Separation 116dB typ.
- 3-Wired Serial Control
- Bi-CMOS Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



■PIN CONFIGURATION



| No. | Symbol | Function | No. | Symbol | Function |
|-----|--------|-------------|-----|--------|--------------------------------------|
| 1 | InA1 | Ach Input 1 | 17 | OutB4 | Bch Output 4 |
| 2 | InB1 | Bch Input 1 | 18 | OutA4 | Ach Output 4 |
| 3 | InA2 | Ach Input 2 | 19 | OutB3 | Bch Output 3 |
| 4 | InB2 | Bch Input 2 | 20 | OutA3 | Ach Output 3 |
| 5 | InA3 | Ach Input 3 | 21 | OutB2 | Bch Output 2 |
| 6 | InB3 | Bch Input 3 | 22 | OutA2 | Ach Output 2 |
| 7 | InA4 | Ach Input 4 | 23 | OutB1 | Bch Output 1 |
| 8 | InB4 | Bch Input 4 | 24 | OutA1 | Ach Output 1 |
| 9 | InA5 | Ach Input 5 | 25 | V- | V- Power Supply Terminal |
| 10 | InB5 | Bch Input 5 | 26 | GND | Ground Terminal |
| 11 | InA6 | Ach Input 6 | 27 | V+ | V+ Power Supply Terminal |
| 12 | InB6 | Bch Input 6 | 28 | ADR | Chip address setting terminal |
| 13 | InA7 | Ach Input 7 | 29 | CLOCK | CLOCK |
| 14 | InB7 | Bch Input 7 | 30 | LATCH | LATCH |
| 15 | InA8 | Ach Input 8 | 31 | DATA | DATA |
| 16 | InB8 | Bch Input 8 | 32 | VDDOUT | Internal Digital Power Supply Output |

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

| PARAMETER | SYMBOL | RATING | UNIT |
|-----------------------------|-----------------|---|------|
| Power Supply Voltage | V ⁺ | +8/-8 | V |
| Maximum Input Voltage | V _{IM} | V ⁺ /V ⁻ | V |
| Power Dissipation | P _D | 800 <small>NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting</small> | mW |
| Operating Temperature Range | Topr | -40 to +85 | °C |
| Storage Temperature Range | Tstg | -40 to +125 | °C |

■ RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------|--------------------------------|----------------|------|------|------|------|
| Operating Voltage | V ⁺ /V ⁻ | - | ±4.5 | ±7.0 | ±7.5 | V |

■ ELECTRICAL CHARACTERISTICS

◆ Power Supply (Ta=25°C, V⁺/V⁻=±7V)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|-----------------|----------------------------|------|------|------|------|
| Supply Current 1 | I _{CC} | V ⁺ , No Signal | 7.0 | 14.0 | 21.0 | mA |
| Supply Current 2 | I _{EE} | V ⁻ , No Signal | 7.0 | 14.0 | 21.0 | mA |

◆ AC CHARACTERISTICS (Ta=25°C, V⁺/V⁻=±7V, V_{IN}=2Vrms, f=1kHz, R_L=47kΩ)

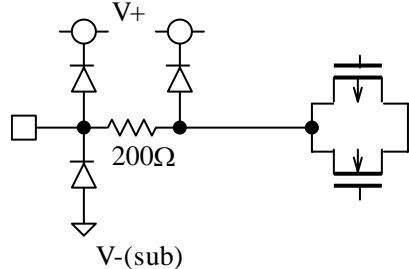
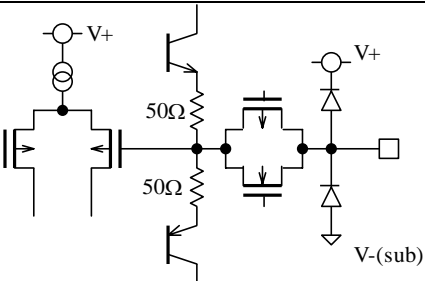
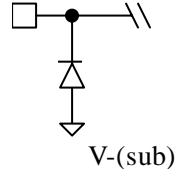
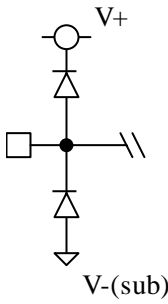
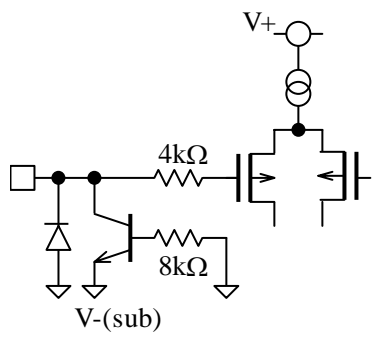
| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------------------------|------------------|---|---------------|---------------|---------------|----------------|
| Maximum Output Voltage | V _{OM} | THD=1% | 11.1 (3.6) | 12.9 (4.4) | - | dBV (Vrms) |
| Voltage Gain | G _V | - | -1.0 | 0 | 1.0 | dB |
| Total Harmonic Distortion 1 | THD1 | BW=400Hz-30kHz | - | 0.001 | 0.02 | % |
| Total Harmonic Distortion 2 | THD2 | V _{in} =1Vrms, BW=400Hz-30kHz | - | 0.0007 | - | |
| Total Harmonic Distortion 3 | THD3 | f=10kHz, BW=400Hz-30kHz | - | 0.002 | - | |
| Mute Level | A _{TT} | Selector=Mute, A-weighted | - | -120 | - | dB |
| Output Noise | V _{NO} | Rg=0Ω, A-Weighted | - | -119 (1.1) | -110 (3.2) | dBV (μVrms) |
| Cross Talk 1 | CT1 | Rg=0Ω, A-Weighted | - | -120 | - | dB |
| Cross Talk 2 | CT2 | Rg=0Ω, f=20kHz | - | -100 | - | |
| Channel Separation 1 | CS1 | Rg=0Ω, A-Weighted | - | -116 | -90 | dB |
| Channel Separation 2 | CS2 | Rg=0Ω, f=20kHz | - | -96 | - | |
| Output impedance | R _{OUT} | Output Switch = ON | - | 15 | 30 | Ω |

BW: Band Width

◆ Logic Control Characteristics (Ta=25°C, V⁺/V⁻=±7V)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------------------------|----------------|----------------------------------|------|------|----------------|------|
| High Level Input Voltage | V _H | ADR, LATCH, DATA, CLOCK Terminal | 2.5 | - | V ⁺ | V |
| Low Level Input Voltage | V _L | ADR, LATCH, DATA, CLOCK Terminal | 0 | - | 1.5 | |

■ TERMINAL DESCRIPTION

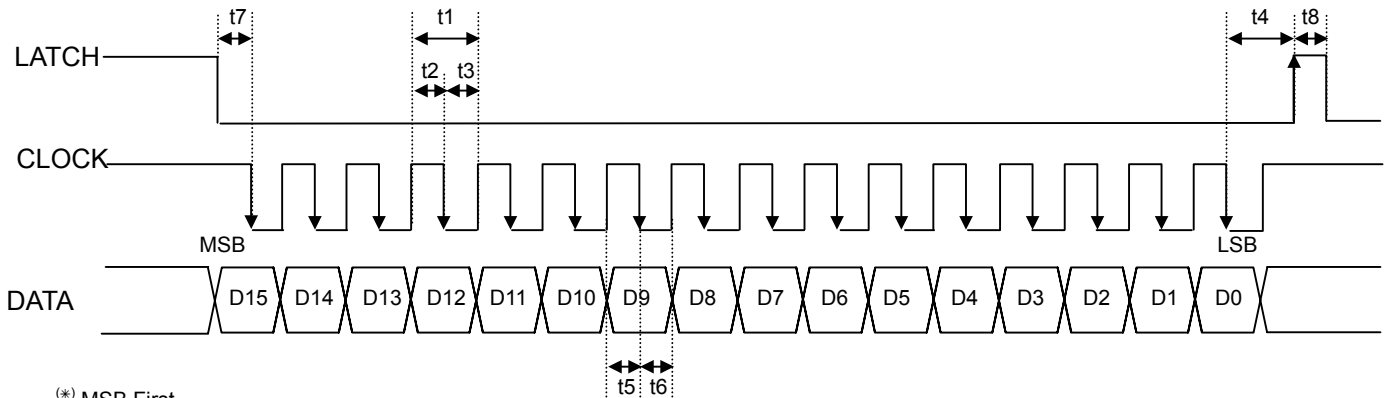
| PIN NO. | SYMBOL | FUNCTION | EQUIVALENT CIRCUIT | TERMINAL DC VOLTAGE |
|----------------------|-------------------------------|---|--|---------------------|
| 1 to 16 | InA1 to 8 InB1 to 8 | Ach Input 1 to 8 Bch Input 1 to 8 |  | 0V |
| 17 to 24 | OutA1 to 4 OutB1 to 4 | Ach Output 1 to 4 Bch Output 1 to 4 |  | 0V |
| 27 | V ⁺ | V+ Power Supply Terminal |  | V+ |
| 26 | GND | Ground Terminal |  | 0V |
| 28 29 30 31 | ADR CLOCK LATCH DATA | Chip address setting terminal CLOCK LATCH DATA |  | 0V |

■ TERMINAL DESCRIPTION

| PIN NO. | SYMBOL | FUNCTION | EQUIVALENT CIRCUIT | TERMINAL DC VOLTAGE |
|---------|--------|--------------------------------------|--------------------|---------------------|
| 32 | VDDOUT | Internal Digital Power Supply Output | | V-(sub)+5V |

NJW1112

CONTROL DATA FORMAT



(*) MSB First

Note.) Set CLOCK in High to prevent incorrect operation during a standby period.

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|--------|--------------------------|-----|-----|-----|------|
| t1 | CLOCK Clock Width | 4 | - | - | μsec |
| t2 | CLOCK Pulse Width (High) | 2 | - | - | μsec |
| t3 | CLOCK Pulse Width (Low) | 2 | - | - | μsec |
| t4 | LATCH Rise Hold Time | 4 | - | - | μsec |
| t5 | DATA Setup Time | 1.6 | - | - | μsec |
| t6 | DATA Hold Time | 1.6 | - | - | μsec |
| t7 | CLOCK Setup Time | 1.6 | - | - | μsec |
| t8 | LATCH High Pulse Width | 1.6 | - | - | μsec |

CONTROL DATA

NJW1112 control data is constructed with 16bits.

| MSB | | | | | | | | | | | | | | | LSB |
|--------------|-----|-----|--------|-----------|-----|----|----------------|----|----|----|--------------|----|----|----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Setting DATA | | | | | | | Select Address | | | | Chip Address | | | | |
| MSB | | | | | | | | | | | | | | | LSB |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Don't Care | | | OutSW1 | Selector1 | | | | 0 | 0 | 0 | 0 | * | * | * | * |
| Don't Care | | | OutSW2 | Selector2 | | | | 0 | 0 | 0 | 1 | * | * | * | * |
| Don't Care | | | OutSW3 | Selector3 | | | | 0 | 0 | 1 | 0 | * | * | * | * |
| Don't Care | | | OutSW4 | Selector4 | | | | 0 | 0 | 1 | 1 | * | * | * | * |

* Chip address is set by chip address select terminal (ADR) status.

| Chip address | | | | |
|--------------|----|----|----|----|
| ADR | D3 | D2 | D1 | D0 |
| Low | 1 | 0 | 1 | 0 |
| High | 1 | 0 | 1 | 1 |

■ INITIAL CONDITION

MSB

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | * | * | * |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | * | * | * | * |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | * | * | * | * |

LSB

Note.) This product starts up by MUTE setting in power "ON". Use it after removing MUTE of each setting.

If any audio signal is inputted in input signal terminal before power "ON", it may cause initial condition abnormality. In conditions of use such as the above, it prevents that abnormality by setting MUTE before power "OFF"

■ CONTROL DATA

◆ **Selector** : Selector for the stereo inputs from InA1/B1 to InA8/B8
OutSW : Output ON/OFF setting

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|--------|-----------|-----|----|----|----|----|----|----|----|----|----|----|
| Don't Care | | | OutSW1 | Selector1 | | | | 0 | 0 | 0 | 0 | * | * | * | * |
| Don't Care | | | OutSW2 | Selector2 | | | | 0 | 0 | 0 | 1 | * | * | * | * |
| Don't Care | | | OutSW3 | Selector3 | | | | 0 | 0 | 1 | 0 | * | * | * | * |
| Don't Care | | | OutSW4 | Selector4 | | | | 0 | 0 | 1 | 1 | * | * | * | * |

a) Selector

| Data | | | | Setting |
|------|-----|----|----|---------------------|
| D11 | D10 | D9 | D8 | |
| 0 | 0 | 0 | 0 | Mute ^(*) |
| 0 | 0 | 0 | 1 | InA1/B1 |
| 0 | 0 | 1 | 0 | InA2/B2 |
| 0 | 0 | 1 | 1 | InA3/B3 |
| 0 | 1 | 0 | 0 | InA4/B4 |
| 0 | 1 | 0 | 1 | InA5/B5 |
| 0 | 1 | 1 | 0 | InA6/B6 |
| 0 | 1 | 1 | 1 | InA7/B7 |
| 1 | 0 | 0 | 0 | InA8/B8 |

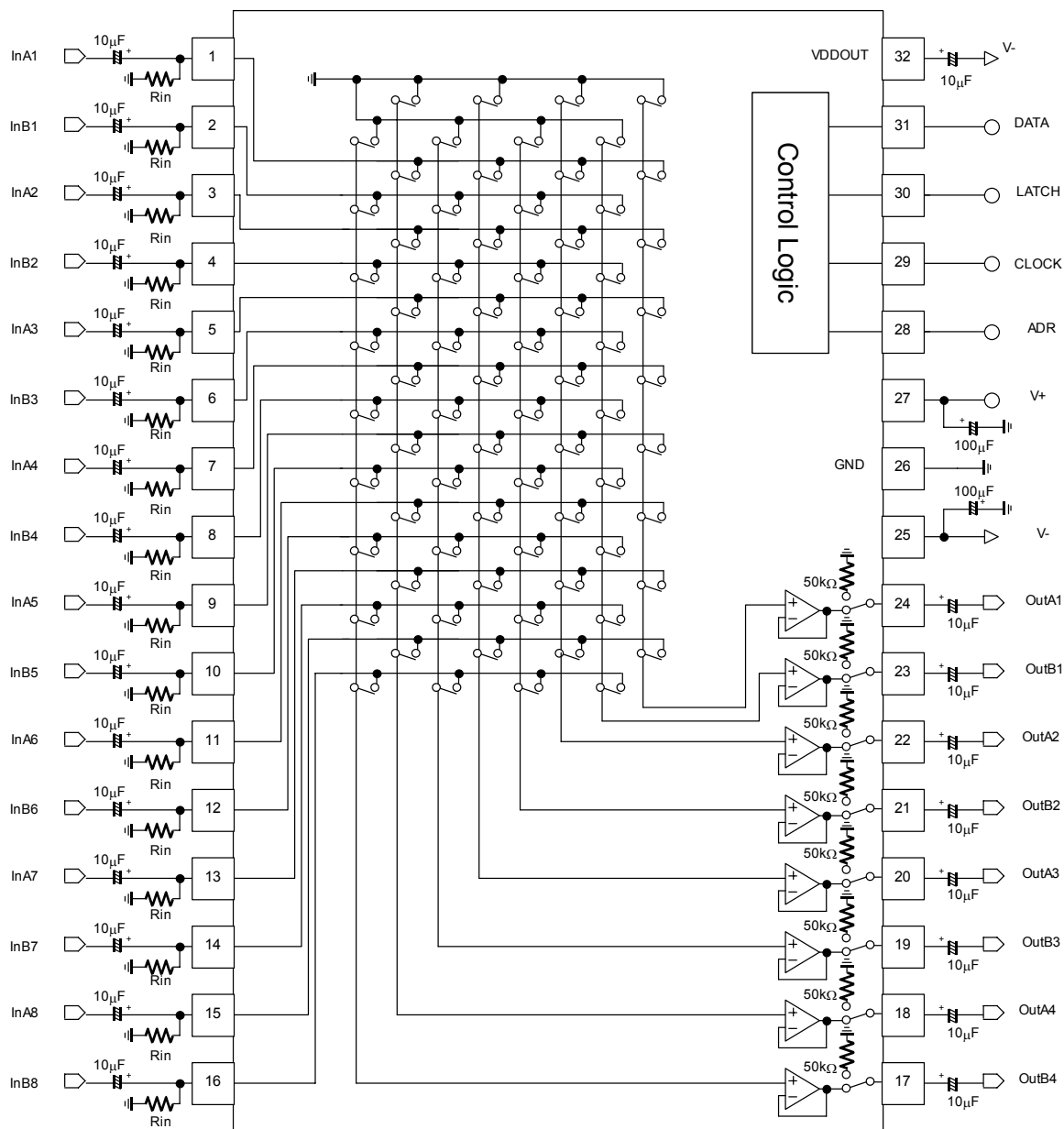
^(*)Initial Setting

b) OutSW

| Data | Setting |
|------|--------------------------|
| D12 | |
| 0 | Output ON ^(*) |
| 1 | Output OFF |

^(*)Initial Setting

APPLICATION CIRCUIT 1

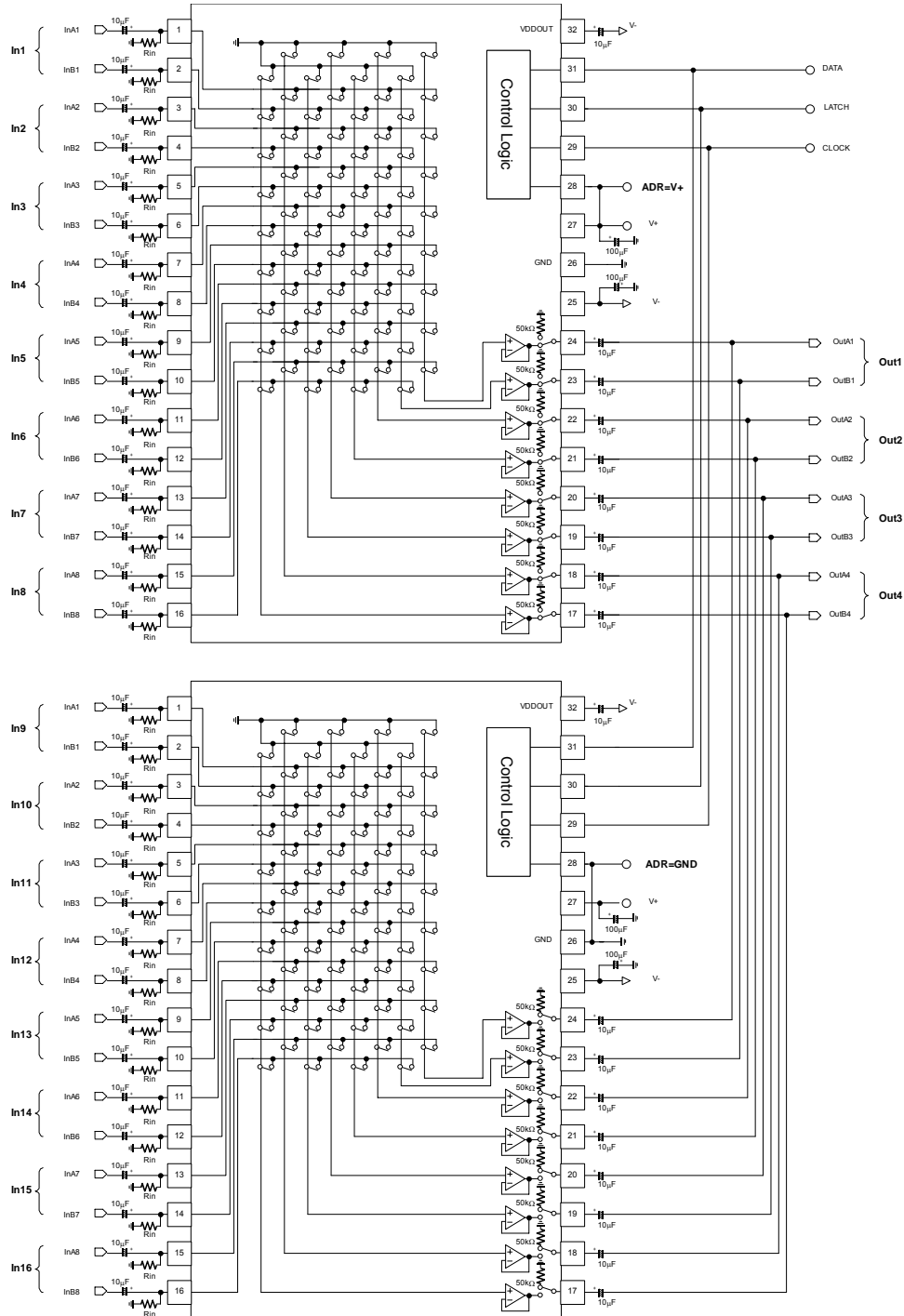


NOTES

- (*) Separate the 3-wired serial control bus line from the input terminals (1pin to 16pin) for avoiding digital noise problem and cross talk.
- (*) Cross talk performance may be effected by PCB patterning and Input resistor "Rin" in relation to input impedance. Widen intervals of input lines (1pin to 16pin) and put guard patterns (ground patterns) among input lines for avoiding cross talk problem. Further, cross talk performance may be effected by input resistor "Rin". In consideration of an actual operating condition, please decide Rin values after evaluating.
- (*) The output terminals of this device are designed as a line driver. Use them by load resistances more than 2kΩ because output waveforms may be in an unstable condition.

APPLICATION CIRCUIT 2

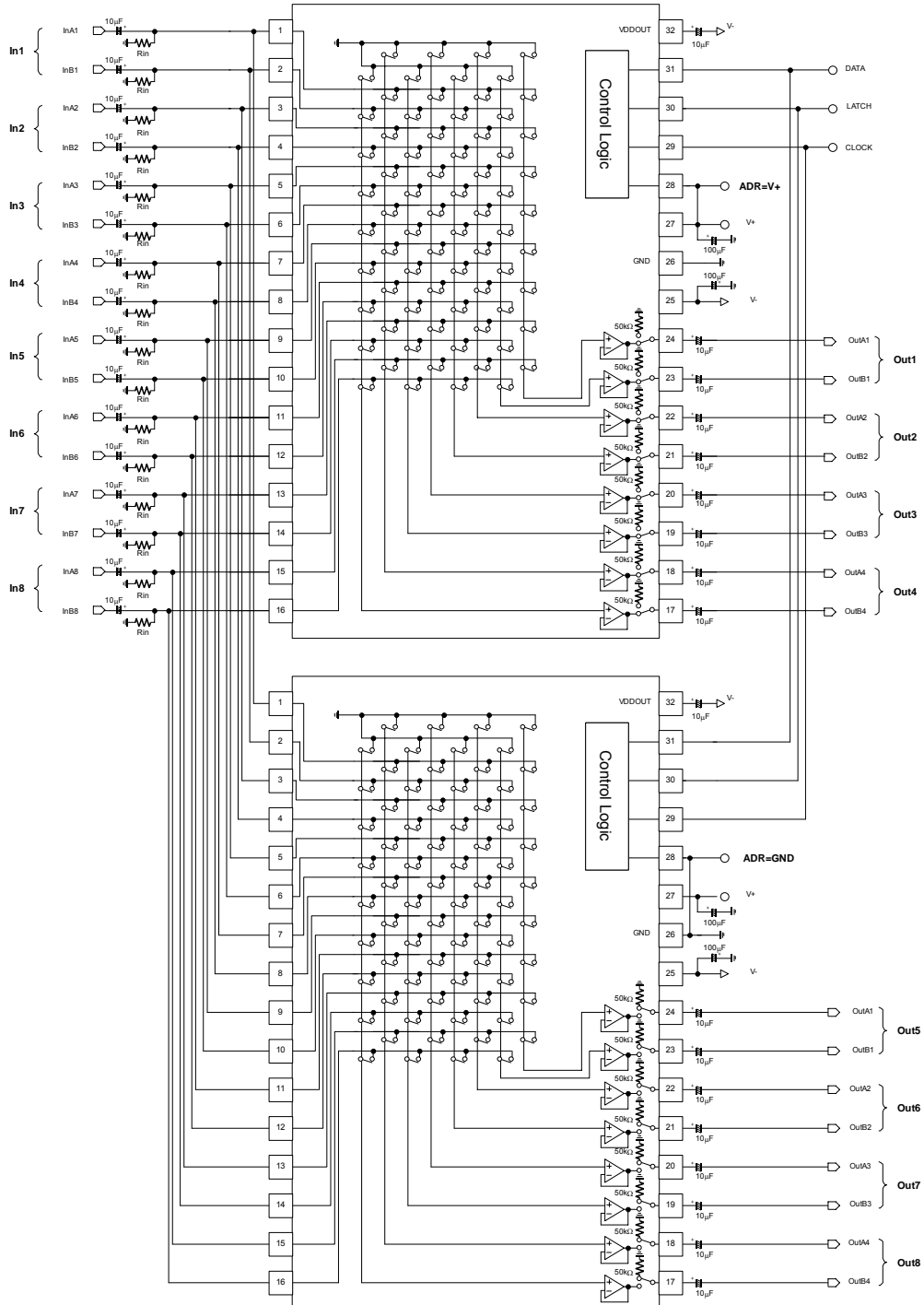
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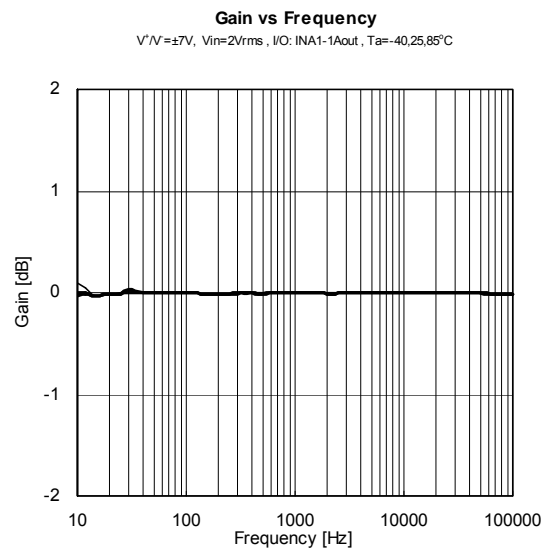
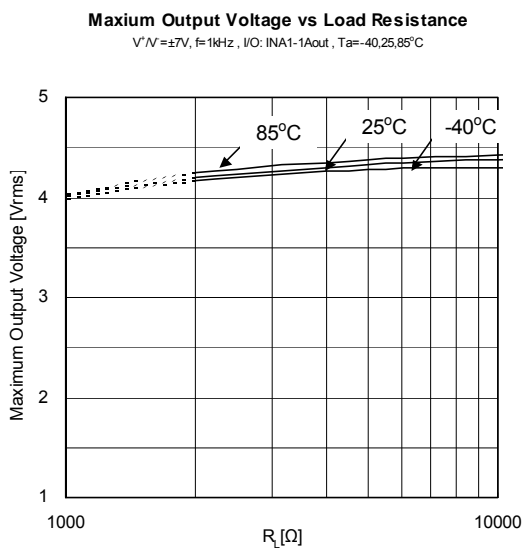
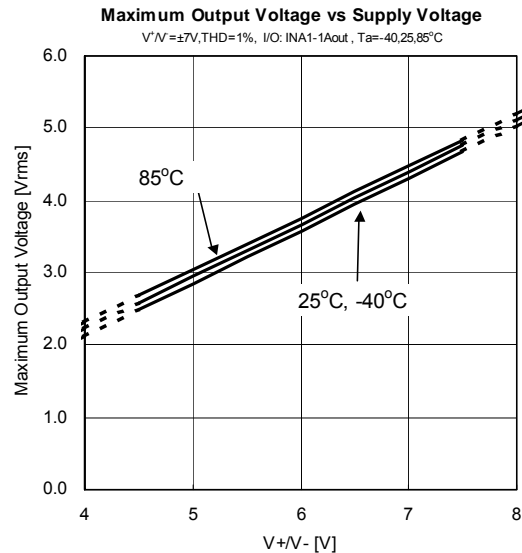
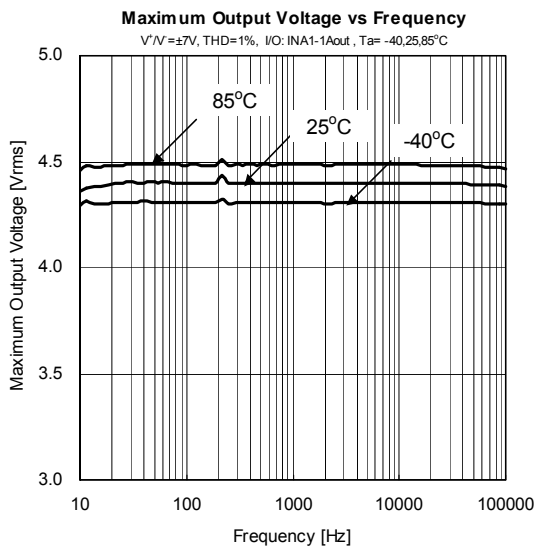
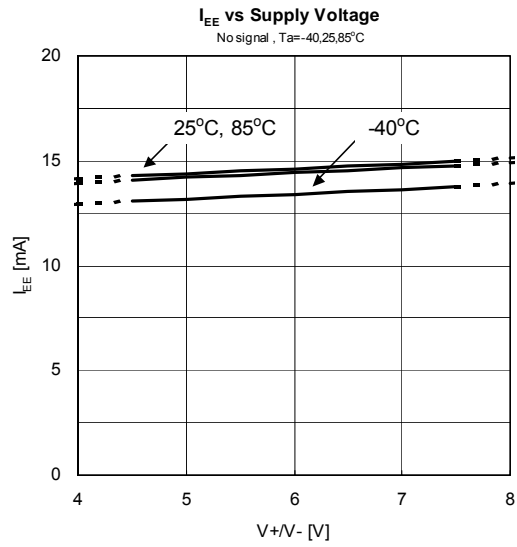
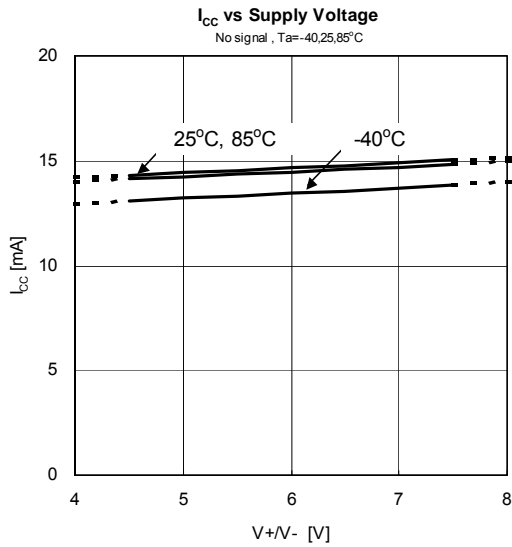
NJW1112

APPLICATION CIRCUIT 3

The NJW1112 is available to expand to 8-input 8-output stereo audio selector.



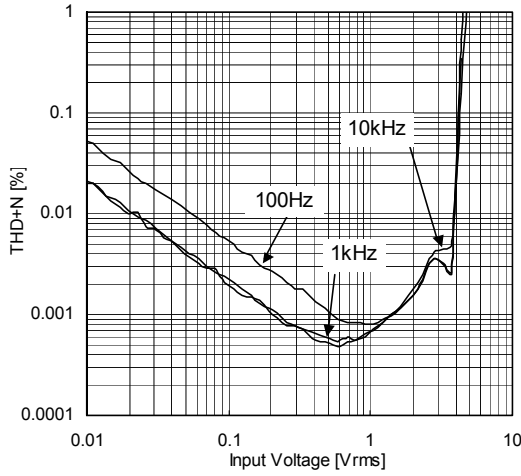
■ TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

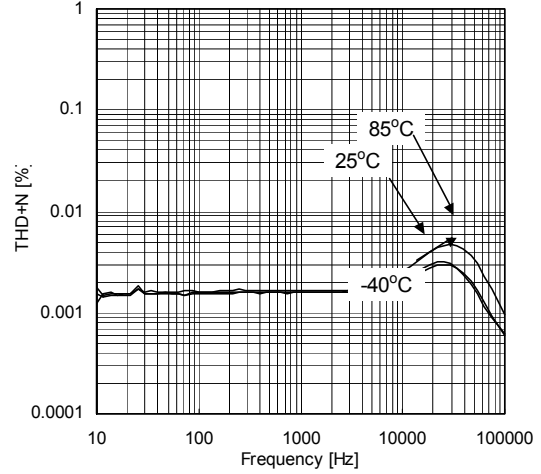
THD+N vs Input Voltage

V/V = ±7V, I/O: INA1-1Aout, BW: 10-22kHz (f = 100Hz)
400-30kHz (f = 1,10kHz), Ta = 25°C



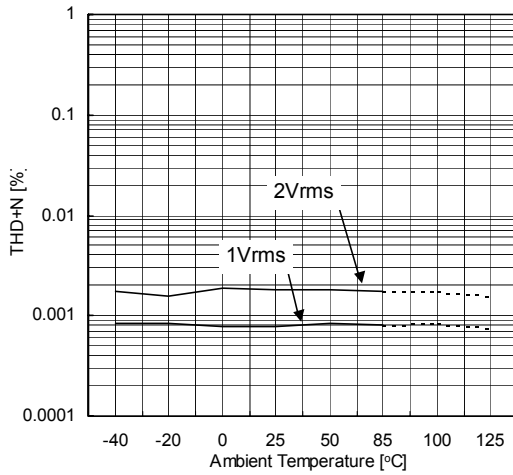
THD+N vs Frequency

V/V = ±7V, I/O: INA1-1Aout,
BW: 10-80kHz, Vin = 2Vrms, Ta = -40, 25, 85°C



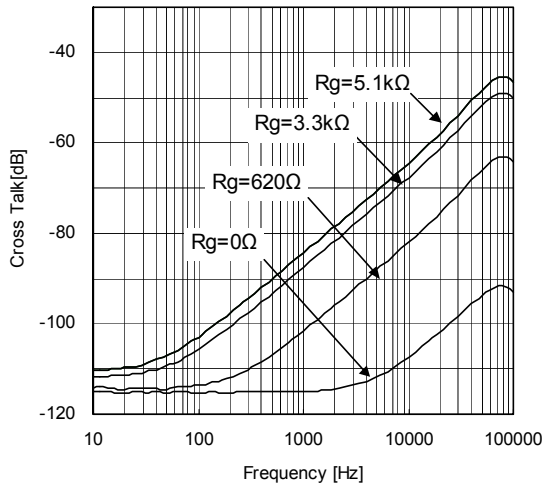
THD+N vs Ambient Temperature

V/V = ±7V, I/O: INA1-1Aout,
BW: 400-30kHz (f = 1 kHz)



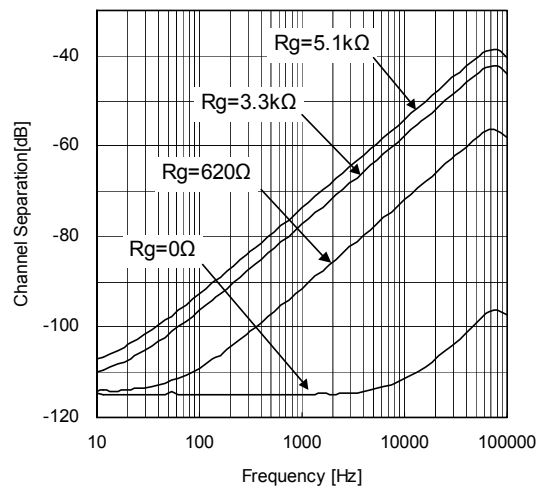
Cross Talk vs Frequency

V/V = ±7V, Vin = 2Vrms, BW: 10Hz-80kHz,
I/O: INA1,3,4,5,6,7,8 / OutA1, Select channel: INA2, Ta = 25°C



Channel Separation vs Frequency

V/V = ±7V, Vin = 2Vrms, BW: 10Hz-80kHz,
I/O: INB1,2,3,4,5,6,7,8 / OutA1, Select channel: INA2, Ta = 25°C



[CAUTION]

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