



AK4121

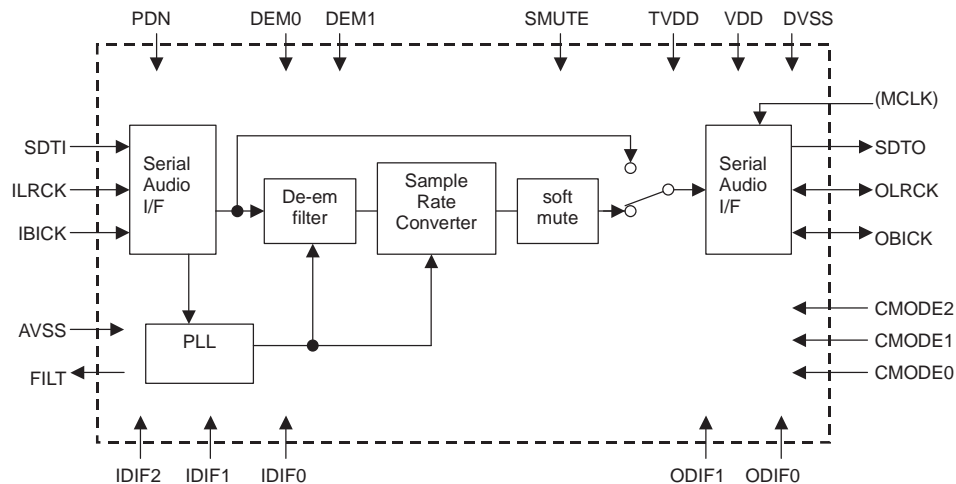
Asynchronous Sample Rate Converter

GENERAL DESCRIPTION

AK4121 is a stereo asynchronous sample rate converter. The input sample rate ranges from 8kHz to 96kHz. The output sample rate is 32kHz, 44.1kHz, 48kHz or 96kHz. Using the AK4121 simplifies system design, since the AK4121's internal PLL eliminates the need for a master clock in slave mode. Then the AK4121 is suitable for applications requiring multiple sample rates, such as Car Audio, DVD recorders, and digital audio recording.

FEATURES

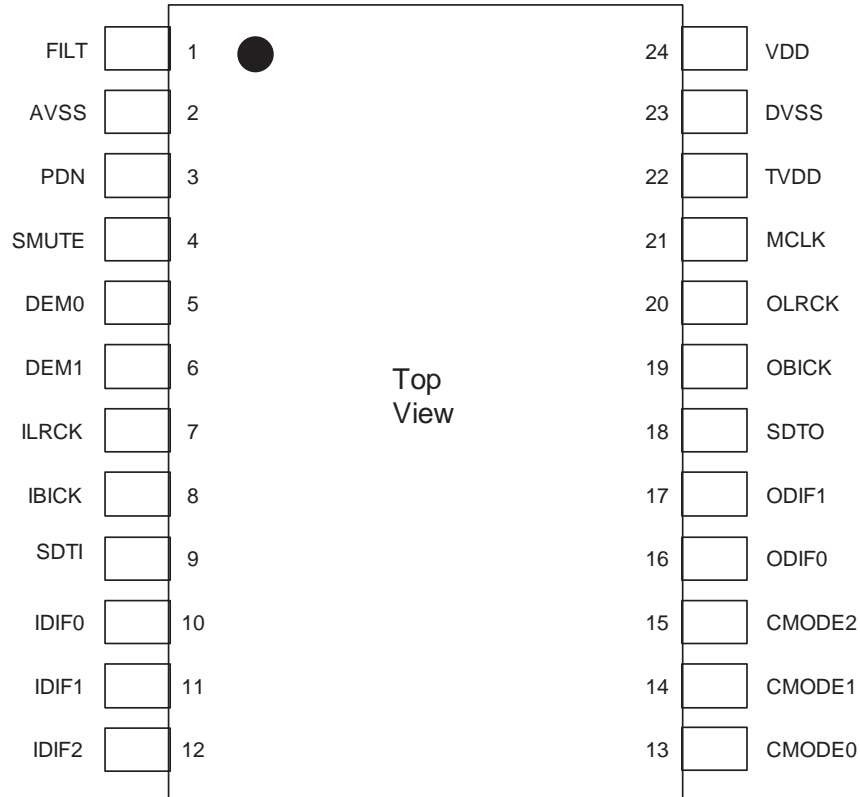
- Stereo asynchronous sample rate converter
- Input sample rate range (FSI): 8kHz to 96kHz
- Output sample rate (FSO): 32kHz/44.1kHz/48kHz/96kHz
- Input to output Sample rate ratio: FSO/FSI = 0.33 to 6
- THD+N: -113dB
- I/F format: MSB justified, LSB justified (24/20/16bit) and I²S
- Clock for Master mode: 256/384/512/768fso
- De-emphasis filter: 32kHz/44.1kHz/48kHz
- SRC Bypass mode
- Soft Mute function
- Power Supply: VDD: 3.0 to 3.6V, TVDD: 3.0 to 5.5V (for input tolerant)
- Ta: -40 to +85°C



■ Ordering Guide

AK4121VF -40 ~ +85°C 24pin VSOP (0.65mm pitch)
 AKD4121 Evaluation Board for AK4121

■ Pin Layout



■ Major Difference between AK4120 and AK4121

Items	AK4120	AK4121
MCLK Input	Needed (supports 256/512fs)	NOT Needed (Slave mode) / Needed (Master Mode: supports 256/384/512/768fs)
Input sample rate (max)	48kHz	96kHz
Vdd	2.7V ~ 3.6V	3.0V ~ 3.6V
Input 5V Tolerant	X	O
De-emphasis Filter	X	O
Soft Mute	X	O
Digital Volume	O	X
Digital Mixer	O	X

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	FILT	O	Loop-Filter Pin for PLL
2	AVSS	I	Analog Ground Pin
3	PDN	I	Power-Down pin When "L", the AK4121 is powered-down and reset.
4	SMUTE	I	Soft Mute Pin
5	DEM0	I	De-emphasis Filter Control Pin #0
6	DEM1	I	De-emphasis Filter Control Pin #1
7	ILRCK	I	L/R Clock Pin for Input
8	IBICK	I	Audio Serial Data Clock Pin for Input
9	SDTI	I	Audio Serial Data Input Pin
10	IDIF0	I	Input Data Format pin #0
11	IDIF1	I	Input Data Format pin #1
12	IDIF2	I	Input Data Format pin #2
13	CMODE0	I	Clock Mode Select Pin #0
14	CMODE1	I	Clock Mode Select Pin #1
15	CMODE2	I	Clock Mode Select Pin #2
16	ODIF0	I	Output Data Format pin #0
17	ODIF1	I	Output Data Format pin #1
18	SDTO	O	Audio Serial Data Output Pin
19	OBICK	I/O	Audio Serial Data Clock Pin for Output
20	OLRCK	I/O	L/R Clock Pin for Output
21	MCLK	I	Master Clock Pin for Output
22	TVDD	I	Input Buffer Power Supply Pin, 3.3V or 5V
23	DVSS	I	Digital Ground Pin
24	VDD	I	Power Supply Pin, 3.3V

ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies:				
Core	VDD	-0.3	4.6	V
Input Buffer	TVDD	-0.3	6.0	V
AVSS-DVSS (Note 1)	Δ GND		0.3	V
Input Current, Any Pin Except Supplies	IIN	-	\pm 10	mA
Input Voltage	VIN	-0.3	TVDD+0.3	V
Ambient Temperature (Power applied)	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS=0V; Note 2)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Core	VDD	3.0	3.3	3.6	V
Input Buffer	TVDD	VDD	5	5.5	V

Note 2. All voltages with respect to ground.

SRC PERFORMANCE

(Ta=-40~85°C; VDD=3.0~3.6V; TVDD=3.0~5.5V; data=20bit; measurement bandwidth=20Hz~FSO/2; unless otherwise specified.)

Parameter	Symbol	min	typ	max	Units
Resolution				20	Bits
Input Sample Rate	FSI	8		96	kHz
Output Sample Rate	FSO	32		96	kHz
Dynamic Range (Input= 1kHz, -60dBFS, Note 3)					
FSO/FSI=44.1kHz/48kHz		-	114	-	dB
FSO/FSI=48kHz/44.1kHz		-	114	-	dB
FSO/FSI=32kHz/48kHz		-	114	-	dB
FSO/FSI=96kHz/32kHz		-	115	-	dB
Worst Case (FSO/FSI=32kHz/44.1kHz)		112	-	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted, Note 3)					
FSO/FSI=44.1kHz/48kHz		-	117	-	dB
THD+N (Input= 1kHz, 0dBFS, Note 3)					
FSO/FSI=44.1kHz/48kHz		-	-113	-	dB
FSO/FSI=48kHz/44.1kHz		-	-112	-	dB
FSO/FSI=32kHz/48kHz		-	-113	-	dB
FSO/FSI=96kHz/32kHz		-	-111	-	dB
Worst Case (FSO/FSI=48kHz/8kHz)		-	-	-103	dB
Ratio between Input and Output Sample Rate (FSO/FSI, Note 4, Note 5)	FSO/FSI	0.33		6	-

Note 3. Measured by Rohde & Schwarz UPD04, Rejection Filter= wide, 8192point FFT.

Note 4. The "0.33" is the ratio of FSO/FSI when FSI is 96kHz and FSO is 32kHz

Note 5. The "6" is the ratio when FSI is 8kHz and FSO is 48kHz.

DIGITAL FILTER						
(Ta=-40~85°C; VDD=3.0~3.6V; TVDD=3.0~5.5V)						
Parameter	Symbol	min	typ	max	Units	
Digital Filter						
Passband -0.001dB	$0.985 \leq \text{FSO/FSI} \leq 6.000$	PB	0		0.4583FSI	kHz
	$0.905 \leq \text{FSO/FSI} < 0.985$	PB	0		0.4167FSI	kHz
	$0.714 \leq \text{FSO/FSI} < 0.905$	PB	0		0.3195FSI	kHz
	$0.656 \leq \text{FSO/FSI} < 0.714$	PB	0		0.2852FSI	kHz
	$0.536 \leq \text{FSO/FSI} < 0.656$	PB	0		0.2245FSI	kHz
	$0.492 \leq \text{FSO/FSI} < 0.536$	PB	0		0.2003FSI	kHz
	$0.452 \leq \text{FSO/FSI} < 0.492$	PB	0		0.1781FSI	kHz
	$0.333 \leq \text{FSO/FSI} < 0.452$	PB	0		0.1092FSI	kHz
Stopband	$0.985 \leq \text{FSO/FSI} \leq 6.000$	SB	0.5417FSI			kHz
	$0.905 \leq \text{FSO/FSI} < 0.985$	SB	0.5021FSI			kHz
	$0.714 \leq \text{FSO/FSI} < 0.905$	SB	0.3965FSI			kHz
	$0.656 \leq \text{FSO/FSI} < 0.714$	SB	0.3643FSI			kHz
	$0.536 \leq \text{FSO/FSI} < 0.656$	SB	0.2974FSI			kHz
	$0.492 \leq \text{FSO/FSI} < 0.536$	SB	0.2732FSI			kHz
	$0.452 \leq \text{FSO/FSI} < 0.492$	SB	0.2510FSI			kHz
	$0.333 \leq \text{FSO/FSI} < 0.452$	SB	0.1822FSI			kHz
Passband Ripple	PR			±0.01		dB
Stopband Attenuation	SA	96				dB
Group Delay (Note 6)	GD	-	57.5	-		1/fs

Note 6. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.(at 20bit MSB justified, 16bit and 20bit LSB justified)

DC CHARACTERISTICS					
(Ta=-40~85°C; VDD=3.0~3.6V; TVDD=3.0~5.5V)					
Parameter	Symbol	min	typ	max	Units
Power Supply Current					
Normal operation:					
FSI=FSO=48kHz at Slave Mode: VDD=3.3V			10	-	mA
FSI=FSO=96kHz at Master Mode: VDD=3.3V			20	-	mA
: VDD=3.6V				40	mA
Power down: PDN = "L" (Note 7)			10	100	μA
High-Level Input Voltage	VIH	0.7xVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	0.3xVDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	VDD-0.4	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

Note 7. All digital inputs including clock pins are held VSS.

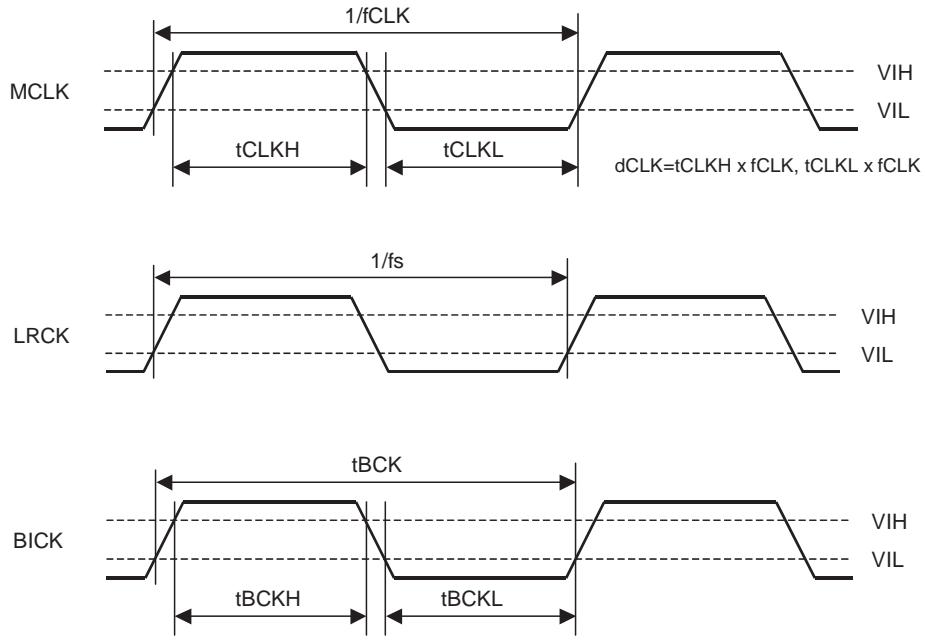
SWITCHING CHARACTERISTICS					
(Ta=-40~85°C; VDD=3.0~3.6V; TVDD=3.0~5.5V; CL=20pF)					
Parameter	Symbol	min	typ	max	Units
Master Clock Input (MCLK)					
Frequency	fCLK	8.192	-	36.864	MHz
Duty Cycle	dCLK	40	-	60	%
L/R clock for Input data (ILRCK)					
Frequency	fs	8		96	kHz
Duty Cycle	Duty	48	50	52	%
L/R clock for Output data (OLRCK)					
Frequency (Note 9)	fs	32		96	kHz
Duty Cycle Slave Mode	Duty	48	50	52	%
Duty Cycle Master Mode	Duty		50		%
Audio Interface Timing					
Input					
IBICK Period	tBCK	1/64fs			ns
IBICK Pulse Width Low	tBCKL	65			ns
IBICK Pulse Width High	tBCKH	65			ns
ILRCK Edge to IBICK “↑” (Note 9)	tBLR	30			ns
BICK “↑” to ILRCK Edge (Note 9)	tLRB	30			ns
SDTI Hold Time from IBICK “↑”	tSDH	30			ns
SDTI Setup Time to IBICK “↑”	tSDS	30			ns
Output (Slave Mode)					
OBICK Period	tBCK	1/64fs			ns
OBICK Pulse Width Low	tBCKL	65			ns
OBICK Pulse Width High	tBCKH	65			ns
OLRCK Edge to OBICK “↑” (Note 9)	tBLR	30			ns
OBICK “↑” to OLRCK Edge (Note 9)	tLRB	30			ns
OLRCK to SDTO (MSB)	tLRS			30	ns
OBICK “↓” to SDTO	tBSD			30	ns
Output (Master Mode)					
BICK Frequency	fBCK		64fs		Hz
BICK Duty	dBCK		50		%
BICK “↓” to LRCK	tMBLR	-20		20	ns
BICK “↓” to SDTO	tBSD	-20		30	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 10)	tPD	150			ns

Note 8. Min is 8kHz when BYPASS=“H”.

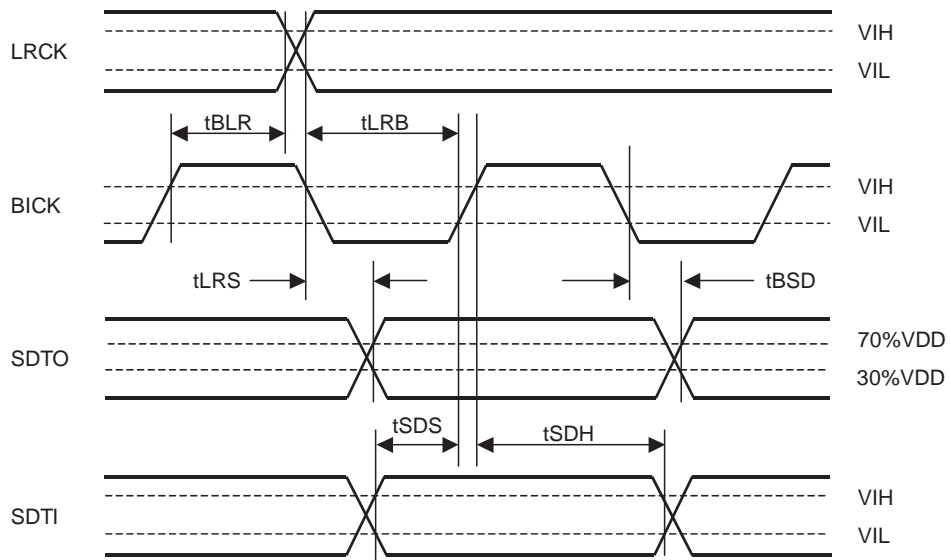
Note 9. BICK rising edge must not occur at the same time as LRCK edge.

Note 10. The AK4121 must be reset by bringing PDN “L” to “H” upon power-up.

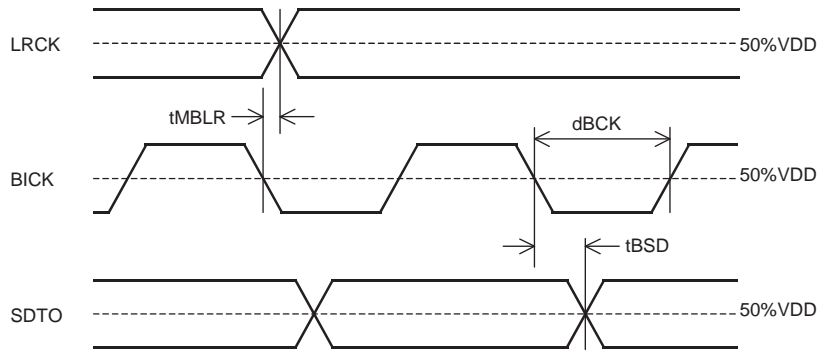
■ Timing Diagram



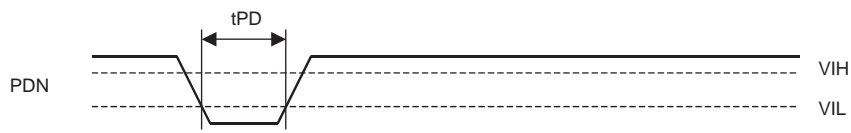
Clock Timing



Audio Interface Timing at Slave Mode



Audio Interface Timing at Master Mode



Power-down & Reset Timing

Note: BICK means IBICK and OBICK.
 LRCK means ILRCK and OLRCK.

OPERATION OVERVIEW

■ System Clock

The input port works in slave mode only. The output port works in slave or master mode. An internal system clock is created by the internal PLL using ILRCK. The MCLK is not needed when the output port is in slave mode, and in slave mode set the MCLK pin to DVSS. The CMODE2-0 pins select the master/slave and bypass mode. The CMODE2-0 pins should be controlled when pin PDN="L".

Mode	CMODE2	CMODE1	CMODE0	MCLK	Master/Slave (Output Port)
0	L	L	L	256fso (fso~96kHz)	Master
1	L	L	H	384fso (fso~96kHz)	Master
2	L	H	L	512fso (fso~48kHz)	Master
3	L	H	H	768fso (fso~48kHz)	Master
4	H	L	L	Not used. Set to DVSS	Slave
5	H	L	H	-	(Reserved)
6	H	H	L	-	(Reserved)
7	H	H	H	Not used. Set to DVSS	Master (BYPASS mode)

Table 1. Master/Slave control

■ Audio Interface Format

The IDIF2-0 pins select the data mode for the input port. The ODIF1-0 pins select the data mode for the output port. In all modes the audio data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of OBICK. Select these modes when PDN="L". When in BYPASS mode, both IBICK and OBICK are fixed to 64fs.

Mode	IDIF2	IDIF1	IDIF0	SDTI Format	IBICK (Slave)
0	L	L	L	16bit LSB Justified	≥32fs
1	L	L	H	20bit LSB Justified	≥40fs
2	L	H	L	20bit MSB Justified	≥40fs
3	L	H	H	20/16bit I ² S Compatible	≥40fs or 32fs
4	H	L	L	24bit LSB Justified	≥48fs

Table 2. Input Audio Data Formats

Mode	ODIF1	ODIF0	SDTO Format	OBICK (Slave)	OBICK (Master)
0	L	L	16bit LSB Justified	64fs	64fs
1	L	H	20bit LSB Justified	64fs	64fs
2	H	L	20/16bit MSB Justified	≥40fs or 32fs	64fs
3	H	H	20/16bit I ² S Compatible	≥40fs or 32fs	64fs

Table 3. Output Audio Data Formats

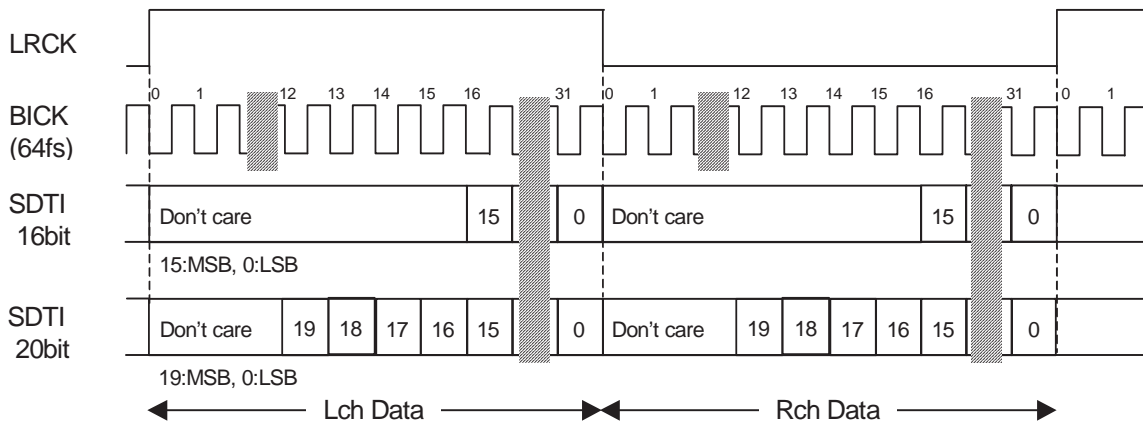


Figure 1. LSB justified Timing

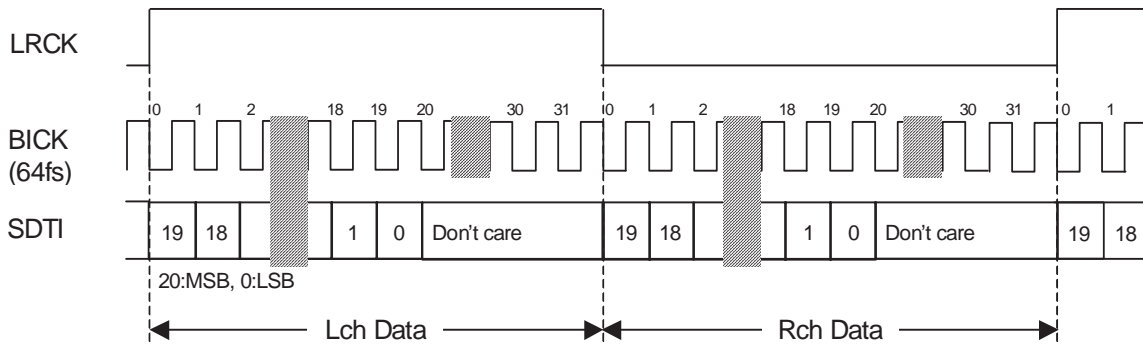


Figure 2. MSB justified Timing

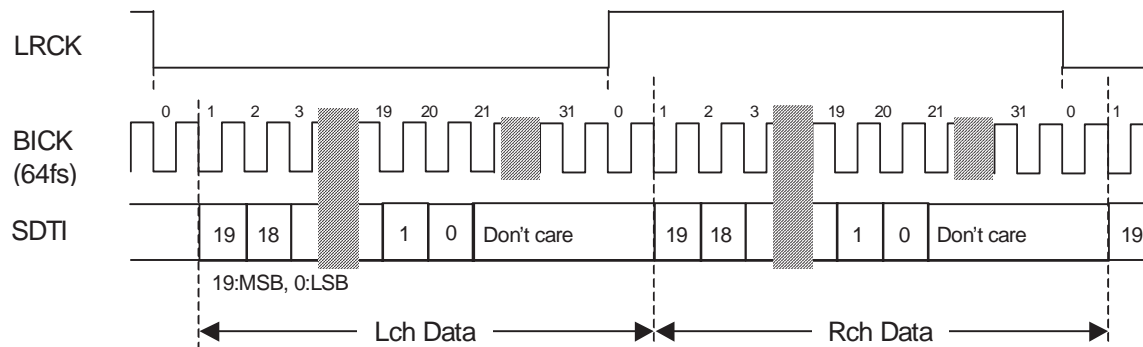
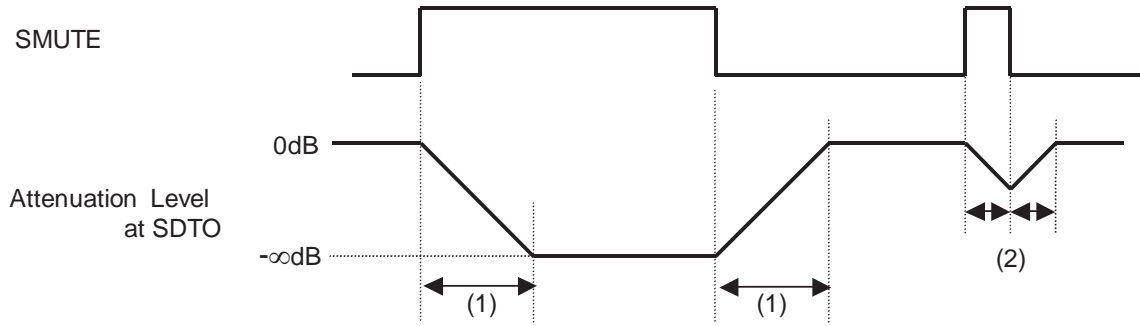


Figure 3. I²S Timing

■ Soft Mute Operation

When the SMUTE pin goes to “H”, the output signal is attenuated from 0dB to $-\infty$ dB during 1024 OLRCK cycles. When the SMUTE pin returns to “0”, the mute is cancelled and the attenuation gradually changes to 0dB during 1024 OLRCK cycles. If the soft mute is cancelled before attenuating to $-\infty$, the attenuation is discontinued and returns to 0dB. This return takes the same number of clock cycles as the point at which the soft mute cancel was initiated, i.e. if 500 clock cycles passed and then a soft mute cancel was issued, it will take 500 clock cycles to return to 0dB. The soft mute is used primarily when changing the signal source.



Notes:

- (1) Transition time. 1024 OLRCK cycles (1024/fso).
- (2) If the soft mute is cancelled before attenuating to $-\infty$ after starting the operation, the attenuation is discontinued and returned to 0dB by the same number of clock cycles.

Figure 4. Soft Mute

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates ($t_c=50/15\mu s$) and is enabled or disabled with DEM0 and DEM1.

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

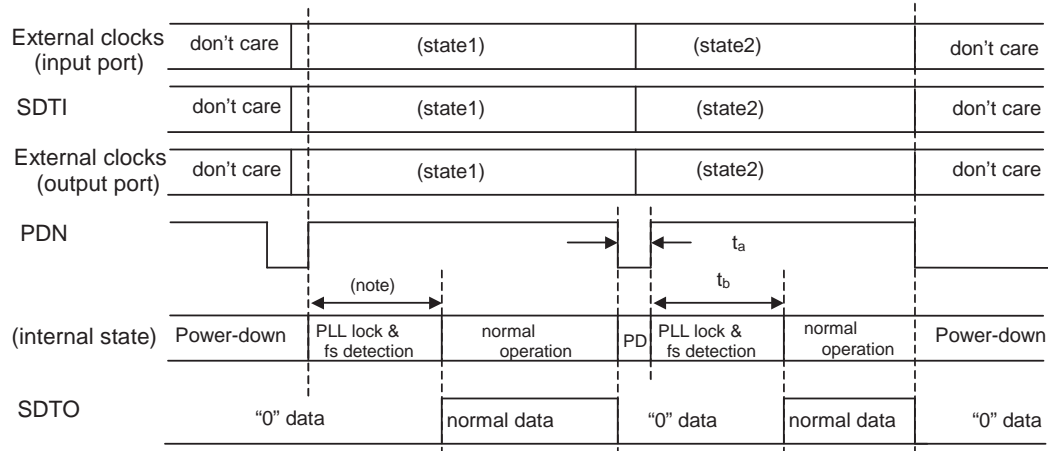
Default

Table 4. De-emphasis Filter Control

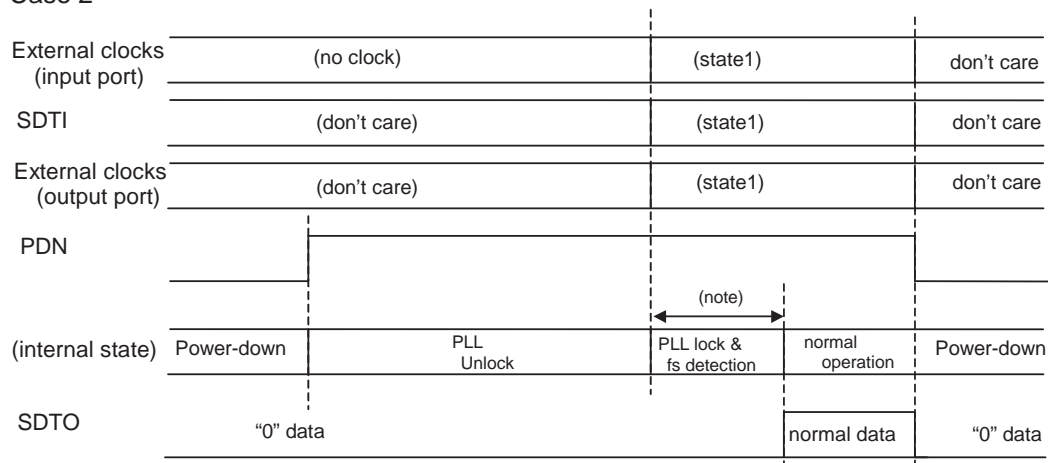
■ System Reset

Bringing the PDN="L" places the AK4121 in power-down mode and initializes the digital filter. The AK4121 should be reset once by bringing PDN="L" upon power-up. Regarding the SDTO valid time, please refer following table. Until then, the SDTO outputs "L".

Case 1



Case 2



Note: <100ms for recommended value 2, <200ms for recommended value 1. (ref. Figure 7)

Figure 5. System Reset

Reset time t_a	Data valid time t_b
$\leq 10\text{ms}$	<100ms
$10\text{ms} <$	<200ms

Table 5. Reset time t_a and Data valid time t_b .

■ Internal Reset Function for Clock Change

The internal reset is executed when the input or the output clock are changed. The SDTO is placed “0” during reset. Within 100ms, the SDTO outputs normal data. When the frequency transition occurs gradually without phase change or the clock of output port is changed keeping $f_{so}/f_{si} > 4$, the internal reset is not executed and the SDTO takes time over 100ms to output normal data. To output normal data within 100ms, please reset by $PDN=L$ (refer following section).

■ Sequence of changing clocks

The recommended sequence for changing clocks is shown in Figure 6.

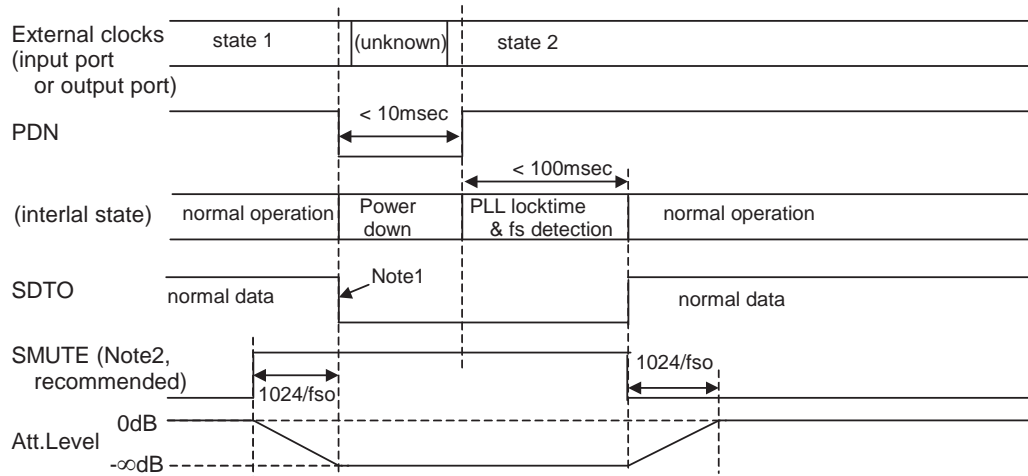


Figure 6. Sequence of changing clocks

Note:

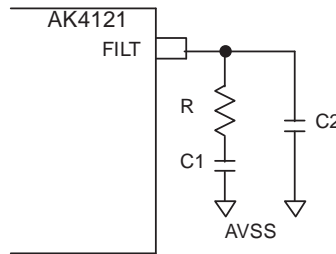
1. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to “0” from GD before PDN goes “L”, which will cause the data on SDTO to remain “0”.
2. SMUTE can also be used to remove the unknown data.

■ **Grounding and Power Supply Decoupling**

The AK4121 requires careful attention to power supply and grounding arrangements. VDD are usually supplied from the system's analog supply. **AVSS and DVSS of the AK4121 must be connected to the analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors especially a 0.1μF ceramic capacitor for high frequency noise should be placed as near to VDD as possible.

■ **PLL Loop-Filter**

The C1 (4.7μF) and R (560ohms) should be connected in series and attached between FILT pin and AVSS in parallel with C2 (1.0nF). Care should be taken to ensure that noise on the FILT pin is minimized.



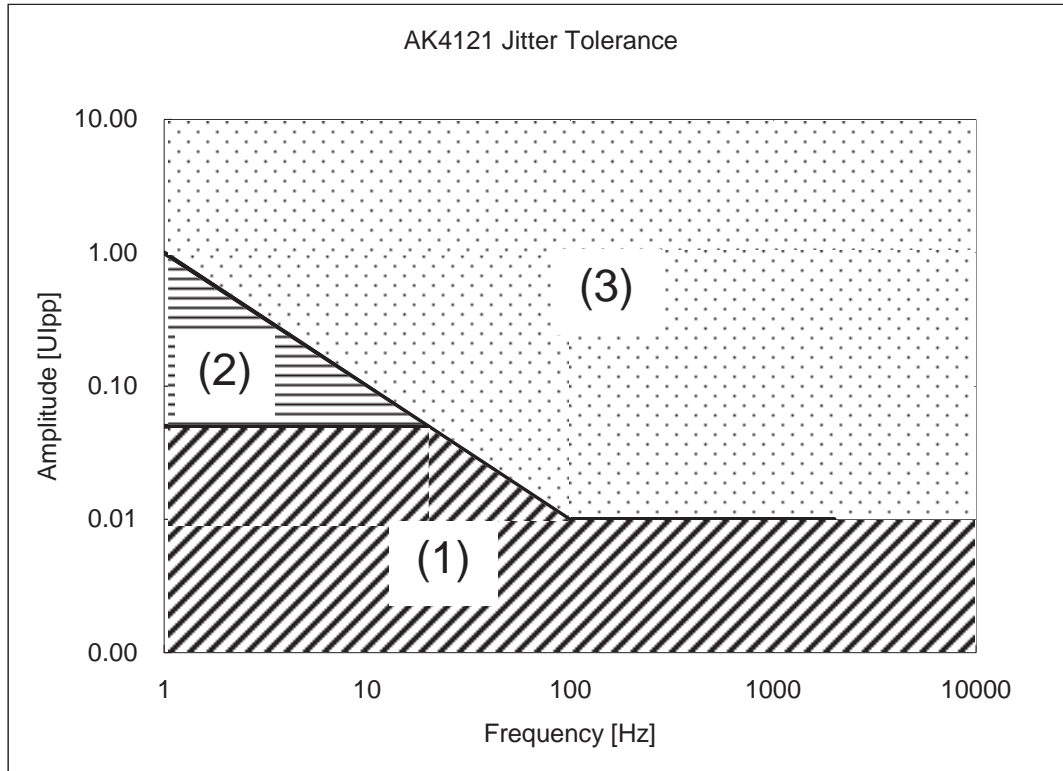
Parameter	Recommended value 1	Recommended value 2
R	560ohm +/-8%	1.2kohm +/-8%
C1	4.7μF +/-40%	2.2μF +/-40%
C2	1.0nF +/-40%	2.2nF +/-40%
fsi range	8k ~ 96kHz	16k ~ 96kHz

Note: Those recommended values include temperature dependence.

Figure 7. PLL Loop-Filter

■ Jitter Tolerance

Figure 8 shows the jitter tolerance to ILRCK for AK4121. The jitter frequency and the jitter amplitude shown in Figure 8 define the jitter quantity. When the jitter amplitude is 0.01UIpp or less, the AK4121 operate normally regardless of the jitter frequency.



- (1) Normal operation
- (2) There is a possibility that the distortion degrades. (It may degrade up to about -50dB.)
- (3) There is a possibility that the output data is lost.

Note:

- The jitter amplitude is for ILRCK and 1UI (Unit Interval) is one cycle of ILRCK. When FSI = 48kHz, 1UI is 1/48kHz = 20.8μs.

Figure 8. Jitter Tolerance

SYSTEM DESIGN

Figure 9 and Figure 10 illustrate typical system connection diagrams. An evaluation board is available which demonstrates this application circuit, the optimum layout, and power supply arrangement and performance measurement results.

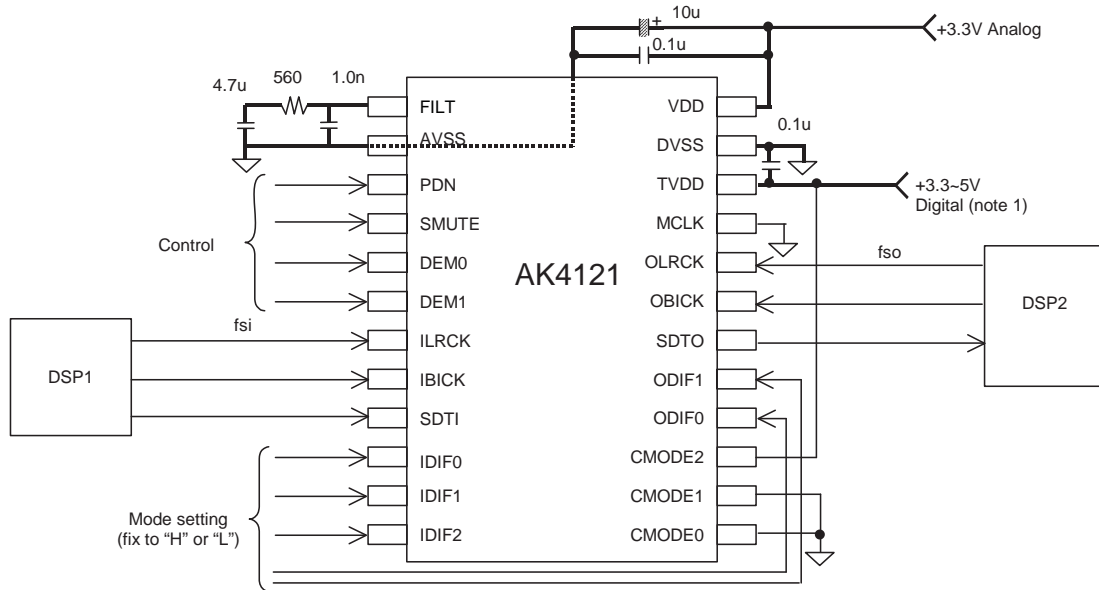


Figure 9. Example of a typical design (Slave Mode)

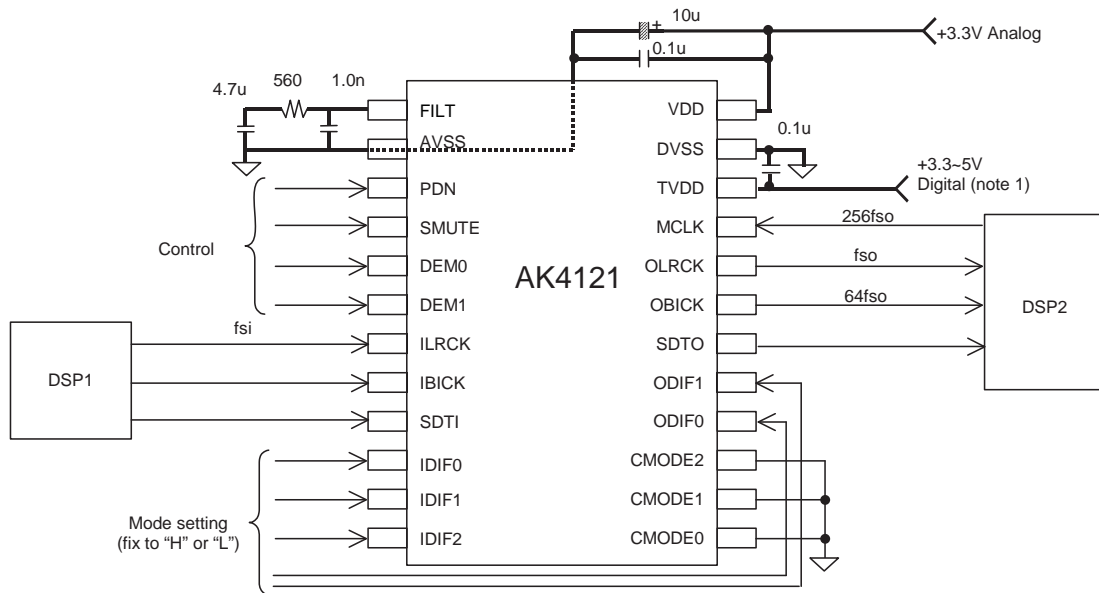
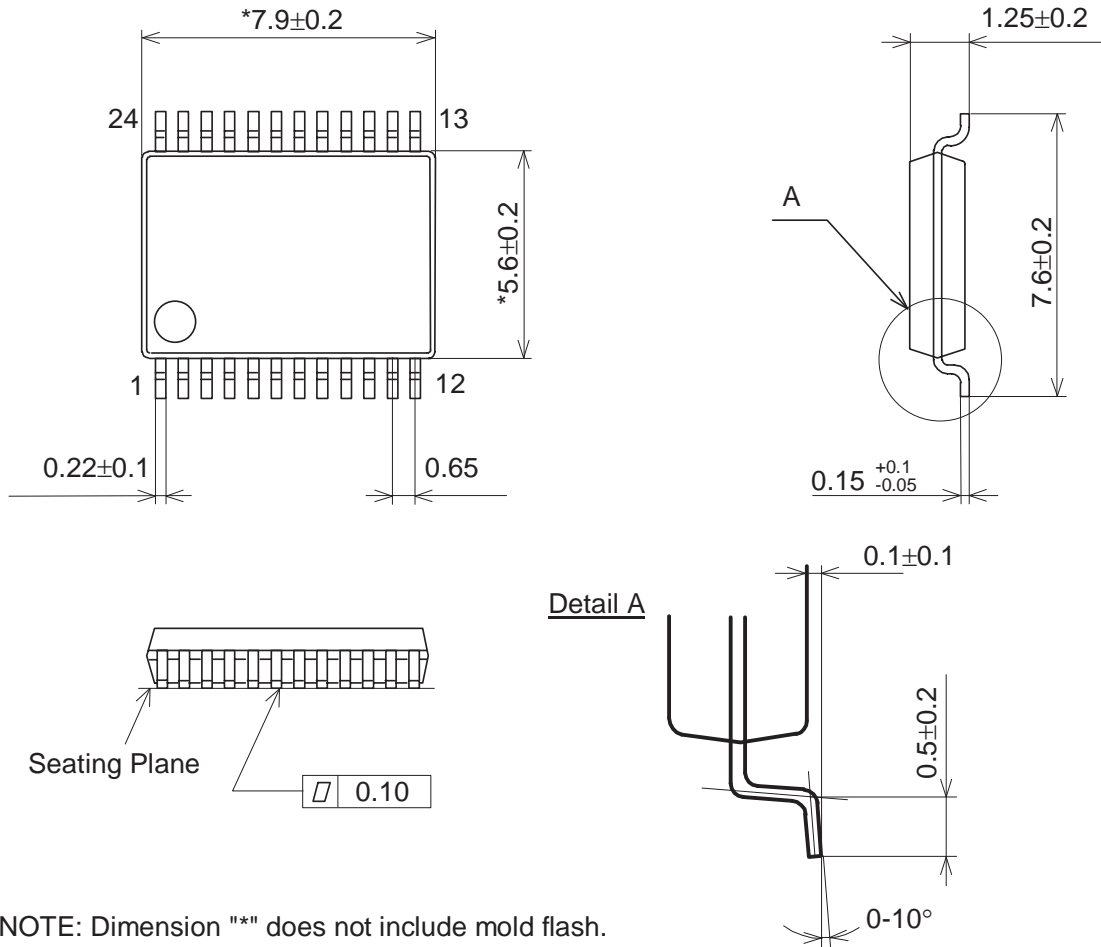


Figure 10. Example of a typical design (Master Mode; MCLK=256fso)

Note 1. TVDD should be the same as the maximum input voltage.

PACKAGE

24pin VSOP (Unit: mm)

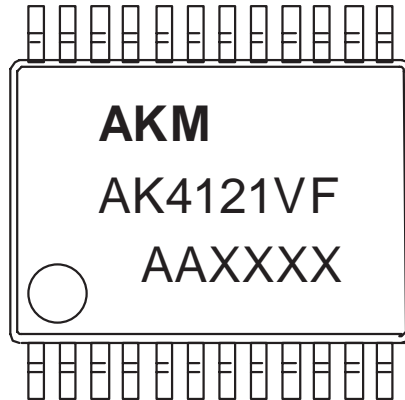


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate (Pb free)

MARKING



Contents of AAXXXX
 AA: Lot#
 XXXX: Date Code

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
02/11/28	00	First Edition		
02/12/26	01	Error Correct	4	Polarity of THD+N is corrected.
		Error Correct	8	Figure for Power-down & Reset Timing is corrected.
		Spec Change	12 ~ 15	Values of external elements are changed. Condition for data valid time is changed.
04/01/27	02	Add Spec	6	SWITCHING CHARACTERISTICS Audio Interface Timing IBICK Period : min 160ns → 1/64fs OBICK Period : min 160ns → 1/64fs
04/08/16	03	Add Spec	5	Add FILTER CHARACTERISTICS
		Add Spec	15	Add Jitter Tolerance

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