LC78615E

CMOS LSI

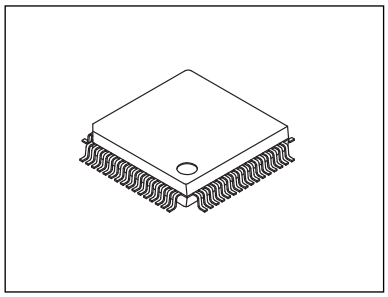
Compact Disc Player IC

ON Semiconductor®

www.onsemi.com

Overview

The LC78615E integrates RF signal processor for CD-DA/R/RW, servo control, EFM signal processing and playback controller (Sequencer : 8-bit CPU). It is possible to make CD player system using with micro controller and driver IC's with less components.



PQFP64 14x14 / QIP64E

Function

- RF signal processing for CD-DA/R/RW, servo control and EFM signal processing.
- Outputs CDDA, CDROM data
- Outputs CD-TEXT decoded data using the serial interface or Serial communication line with external main controller.
- CD playback system is realized with simple macro commands by the external controller because of the internal Sequencer (8-bit CPU).
- Operating Voltage : 3.3V Typical
- Operating Temperature : –40°C to +85°C
- Package : QIP64E(14×14)

ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

Detail of Functions

[CD-DSP functions]

< Playback functions>

- Playback mode : CLV playback / Jitter free playback (VCEC)
- Playback speed : Normal speed, double speed, quadruple speed (CLV playback / Jitter free playback)

<RF processing block>

- RF system : AGC, CD-R and CD-R/W playback support, peak hold, bottom hold
- Error system : TE signal generation, FE signal generation
- Detection : Track count signal, Jitter, Defect (black, mirror)
- LASER power controller (APC)
- DC offset voltage cancellation

<Servo control block>

- All servo systems as tracking, focus, sled and spindle are implemented with digital processing.
- Automatic adjustment functions : focus gain, focus bias, focus offset, tracking gain, tracking offset and tracking balance
- Shock detection / Interruption detection

<CD signal processing block>

- EFM signal synchronization detection, protection and interpolation
- Error detection, correction (C1=double, C2=quadruple/double)
- Jitter margin ±19 frames

<CD-TEXT processing block>

- Buffers CD-TEXT decoded data to the buffer memory.
- Starts buffering of CD-TEXT decoded data from desired ID3/ID4.

[CD data processing functions]

<CDDA data processing block>

- Interpolation
- Mute function(−12dB, −∞)
- Digital attenuator
- De-emphasis filter

<CDROM data processing block >

- CLV playback : Fixed normal speed or double speed
- Jitter free playback (VCEC) : Free speed within quadruple speed

<Outputs format >

- Digital 3 lines output (LRCK, BCK, DATA)
- Supports various external audio data output format
  IIS (48fs), MSB First, Right-Justified, Left-Justified (32fs/48fs), 16 bit data length
- Slave mode
  Output DATA synchronized to external Clock input (LRCK/BCK)
- Digital output (S/PDIF, only CLV playback mode)

[Internal Microcontroller functions]

<Sequencer control>

- CD playback control
  Servo control, CD-TEXT processing, Digital data output control, etc.

<Communication control between main controller>

- The SIO interface using CE,CL,DI,DO and BUSYB pins is available as communication format.
- External main controller can control this IC directly such as “stop oscillation” or “restart oscillation” or so on at the internal register open mode (REG_READY high condition).
- Even while the clock is stopped, some of general port can be controlled by host controller.

<Peripheral interface block>

- GPIO port 15 ports maximum(Shared with other functionslerate.)

<Program memory block>

- Mask-ROM type
- ROM Collect function is built in for the partial change of the program and Host controller can use this.

<Others>

- Watch Dog Timer
  Notifies to outside from a pin or resets internally.
- Power management (Two kinds of sleep mode)
  (1) Only the clock for CPU core is operating and clocks for other blocks are stopping.
  (2) All clocks are stopping.

[Others]

<Internal power supply>

- 1.5V regulator for internal blocks

Specifications

Absolute Maximum Ratings at Ta=25°C, DV_{SS}=AV_{SS}=XV_{SS}=VV_{SS}1=0V

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	V_{DD} max	DVDD, AVDD, XVDD, VVDD1	−0.3 to +3.95	V
Input voltage 1	V_{IN}1		−0.3 to DV_{DD}+0.3	V
Output voltage	V_{OUT}		−0.3 to DV_{DD} +0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C Mounted reference PCB (*)	300	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−40 to +125	°C

(*) Reference PCB : 114.3mm×76.1mm×1.6mm, glass epoxy resin

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta=−40 to 85°C, DV_{SS}=AV_{SS}=XV_{SS}=VV_{SS}1=0V

Parameter	Symbol	Pin Name	Type	Conditions	Ratings			unit
					min	typ	max	
Supply voltage	V_{DD}	DVDD, AVDD, XVDD, VVDD1			3.00		3.60	V
High-level input voltage	V_{IH}	XIN, RESB, MODE,CE, CL, DI, DO CONT00, CONT01, CONT02, CONT03, CONT04, CONT05, CONT06, CONT07, CONT08, CONT09, CONT10, CONT11, CONT12, CONT13, CONT14,	Schmitt		2.00		VDD	V
Low-level input voltage	V_{IL}	XIN, RESB, TEST,CE, CL, DI, DO CONT00, CONT01, CONT02, CONT03, CONT04, CONT05, CONT06, CONT07, CONT08, CONT09, CONT10, CONT11, CONT12, CONT13, CONT14,	Schmitt		0.00		0.80	V
Crystal Oscillator Frequency	FX	XIN, XOUT	Oscillator circuit			16.9344		MHz
External clock Input	EXCK	XIN	Schmitt			16.9344	18.0	MHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta=–40 to 85°C, V_{DD}=3.0 to 3.6V, DV_{SS}=AV_{SS}=XV_{SS}=VV_{SS}1=0V

Parameter	Symbol	Pin Name	Type	Conditions	Ratings			unit
					min	typ	max	
Current drain	$I_{DD}1$	DVDD, AVDD, XVDD, VVDD1				40	60	mA
High-level input current	I_{IH}	RESB, MODE,CE, CL, DI, DO CONT00, CONT01, CONT02, CONT03, CONT04, CONT05, CONT06, CONT07, CONT08, CONT09, CONT10, CONT11, CONT12, CONT13, CONT14,	Schmitt	V_{IN}=V_{DD} Built-in Pull-down /Pull-up resistor OFF			10.00	µA
Low-level input current	I_{IL}	RESB, TEST,CE, CL, DI, DO CONT00, CONT01, CONT02, CONT03, CONT04, CONT05, CONT06, CONT07, CONT08, CONT09, CONT10, CONT11, CONT12, CONT13, CONT14	Schmitt	VIN=0.0V Built-in Pull-down /Pull-up resistor OFF	–10.00			
High-level output voltage	V_{OH}(1)	DO, BUSYB, CONT00,CONT01, CONT02, CONT03,CONT04, CONT05, CONT06,CONT07, CONT09,CONT10, CONT11, CONT12,CONT13, CONT14	CMOS	I_{OH}=–2mA	V_{DD}–0.6			V
	V_{OH}(2)	CONT08	CMOS	I_{OH}=–4mA				
Low-level output voltage	V_{OL}(1)	DO, BUSYB, CONT00,CONT01, CONT02, CONT03,CONT04, CONT05, CONT06,CONT07, CONT09,CONT10, CONT11, CONT12,CONT13, CONT14	CMOS	I_{OL}=2mA			0.40	
	V_{OL}(2)	CONT08	CMOS	I_{OL}=4mA				
Output off-leakage current	IOFF(1)	PDOUT0,PDOUT1		Hi-Z Out	–10.00		10.00	µA
	IOFF(2)	DO		Hi-Z Out	–10.00		10.00	
Built-in Pull-down resistor	RPD	CONT01,CONT02, CONT03, CONT04,CONT05, CONT06, CONT07,CONT08, CONT09, CONT10,CONT11, CONT12, CONT13,CONT14			50	100	200	kΩ
Built-in Pull-up resistor	RPU	CONT00			50	100	200	kΩ
Charge pump output current	IPDOH	PDOUT1,PDOUT0		PCKIST=100kΩ Current value setting:1x	35	50	65	µA
	IPDOL	PDOUT1,PDOUT0			–65	–50	–35	

(Notes)

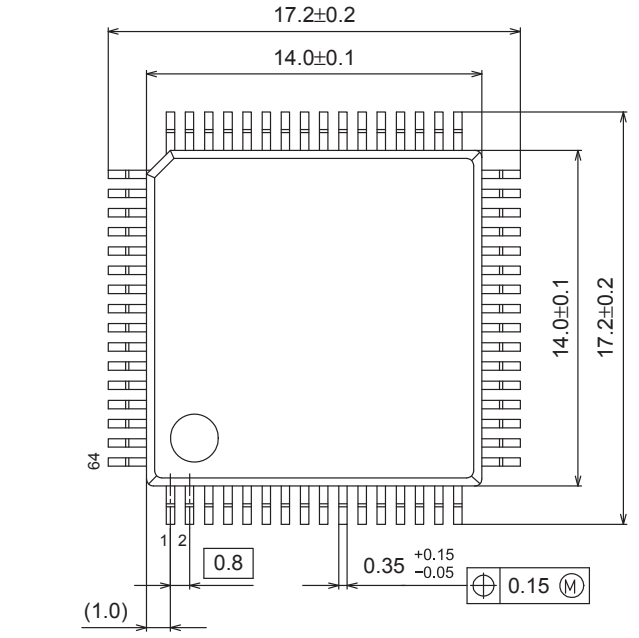
- Connect and use the pull-up or the pull-down resister with the outside when you use serial communications because the terminal DO is 3- State output (initial state).

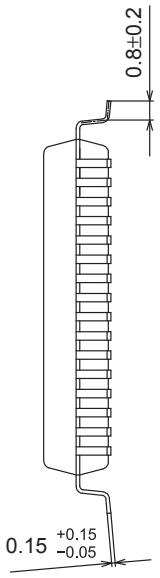
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

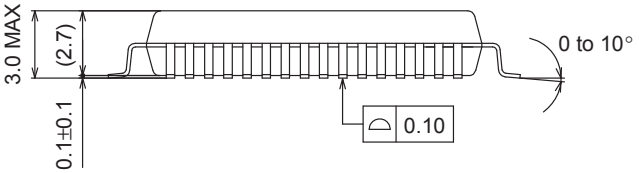
Package Dimensions

unit : mm

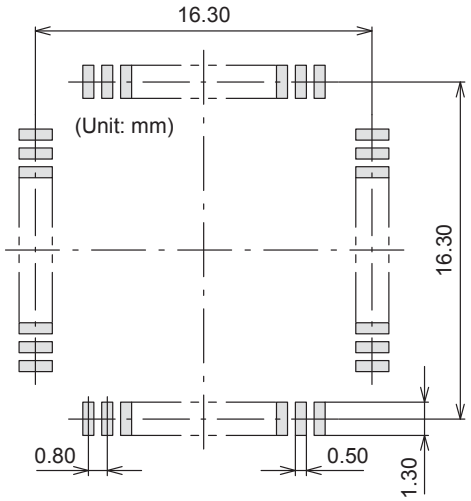
PQFP64 14x14 / QIP64E
CASE 122BP
ISSUE A



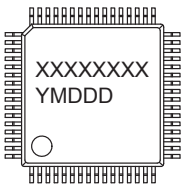




SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



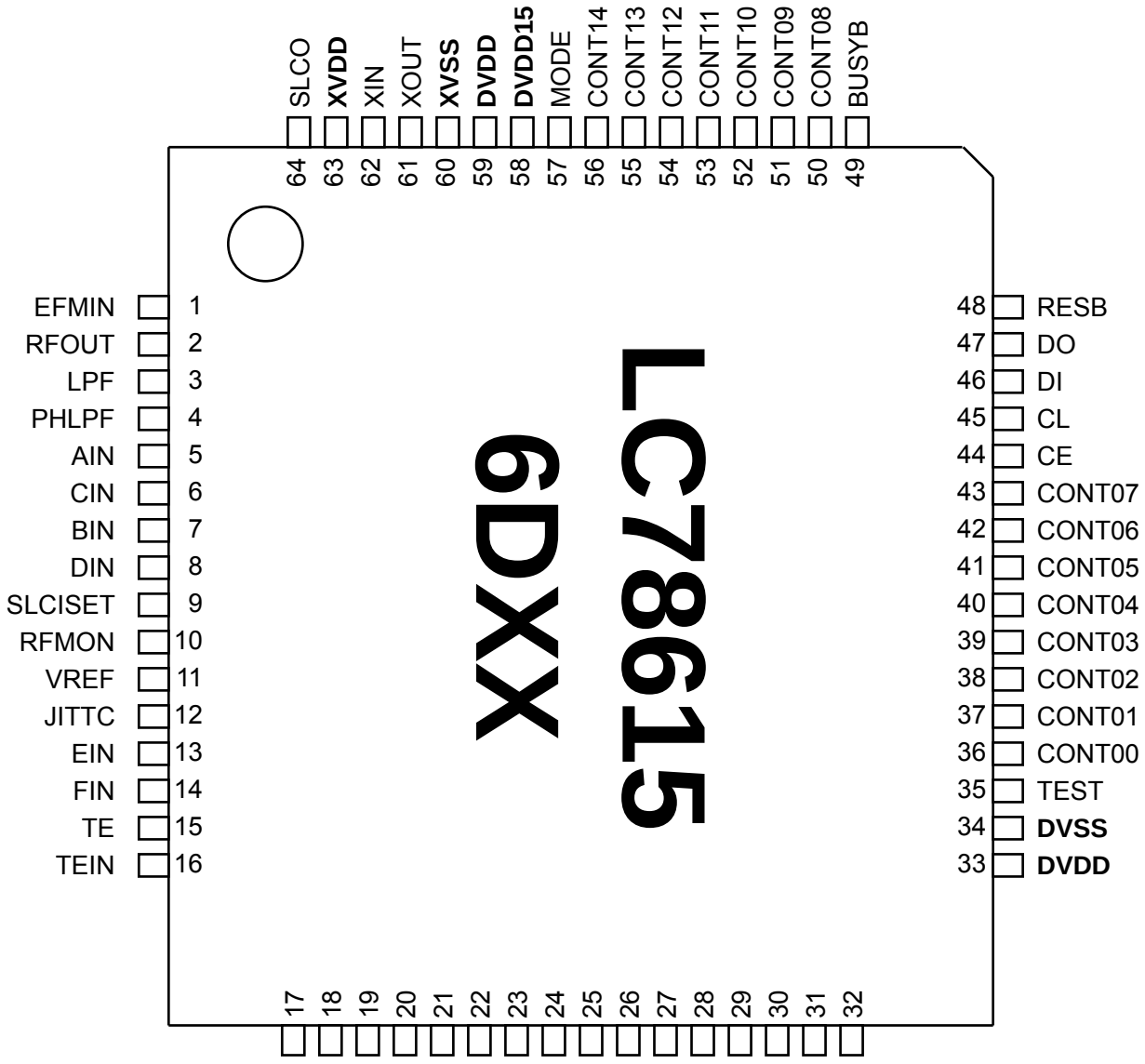
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment



Pin Description

Pin No.	Pin name	I/O	State when "Reset"	Function
1	EFMIN	AI	Input	RF signal input
2	RFOUT	AO	Undefined	RF signal output
3	LPF	AO	Undefined	RF signal DC level detection low-pass filter capacitor connection
4	PHLPF	AO	Undefined	Defect detection low-pass filter capacitor connection
5	AIN	AI	Input	A signal input
6	CIN	AI	Input	C signal input
7	BIN	AI	Input	B signal input
8	DIN	AI	Input	D signal input
9	SLCISET	AI	Input	SLCO output current setting resistor connection
10	RFMON	AO	Undefined	IC internal analog signal monitor
11	VREF	AO	AVDD/2	Reference voltage output for RF
12	JITTC	AO	Undefined	Jitter detection capacitor connection
13	EIN	AI	Input	E signal input
14	FIN	AI	Input	F signal input
15	TE	AO	Undefined	TE signal output
16	TEIN	AI	Input	TE signal input used for TES signal generation
17	AVSS	–	–	Analog system ground. This pin must be connected to the 0V level.
18	AVDD	–	–	Analog system power supply
19	LDD	AO	Undefined	Laser power control signal output
20	LDS	AI	Input	Laser power detection signal input
21	FDO	AO	AVDD/2	Focus control signal output
22	TDO	AO	AVDD/2	Tracking control signal output
23	SLDO	AO	AVDD/2	Sled control signal output
24	SPDO	AO	AVDD/2	Spindle control signal output
25	VVSS1	–	–	EFMPLL ground. This pin must be connected to the 0V level.
26	PDOUT1	AO	Undefined	EFMPLL charge pump output 1
27	PDOUT0	AO	Undefined	EFMPLL charge pump output 0
28	PCKIST	AI	Input	EFMPLL charge pump current setting resistor connection pin
29	VVDD1	–	–	EFMPLL power supply
30	NC	–	–	NC Pin (Open)
31	NC	–	–	NC Pin (Open)
32	DVDD15	AO	High	Capacitor connection pin for internal regulator
33	DVDD	–	–	Digital system power supply
34	DVSS	–	–	Digital system ground. This pin must be connected to the 0V level.
35	TEST	I	Input	Test input. This pin must be connected to the 0V level.
36	CONT00	I/O	Input(High)	General purpose I/O port with pull up resistor SBCK clock input for CD subcode data (exclusive with CONT07 and CONT11)
37	CONT01	I/O	Input(Low)	General purpose I/O port with pull down resistor Block synchronization signal (SBSY) output for CD subcode
38	CONT02	I/O	Input(Low)	General purpose I/O port with pull down resistor Frame synchronization signal (SFSY) output for CD subcode
39	CONT03	I/O	Input(Low)	General purpose I/O port with pull down resistor PW data output in CD subcode Watch Dog Timer state monitor output
40	CONT04	I/O	Input(Low)	General purpose I/O port with pull down resistor LR clock output for CD data LR clock input for CD data (exclusive with CONT09 and CONT12) Block synchronization signal (SBSY) output for CD subcode Data request signal input for CD-TEXT interface (exclusive with CONT08, CONT09 and CONT12)

Pin No.	Pin name	I/O	State when "Reset"	Function
41	CONT05	I/O	Input(Low)	General purpose I/O port with pull down resistor Bit clock output for CD data Bit clock input for CD data (exclusive with CONT10 and CONT13) Frame synchronization signal (SFSY) output for CD subcode Clock input/output for CD-TEXT interface (exclusive with CONT10 and CONT13)
42	CONT06	I/O	Input(Low)	General purpose I/O port with pull down resistor Serial data output for CD data PW data output in CD subcode Serial data output for CD-TEXT interface
43	CONT07	I/O	Input(Low)	General purpose I/O port with pull down resistor C2 error flag output for CD data Digital audio output<S/PDIF> SBCK clock input for CD subcode data (exclusive with CONT00 and CONT11) Watch Dog Timer state monitor output
44	CE	I	Input	Host I/F Enable signal input for serial communication
45	CL	I	Input	Host I/F Data transfer clock input for serial communication
46	DI	I	Input	Host I/F Data input for serial communication
47	DO	O	Low	Host I/F Data output for serial communication
48	RESB	I	Input	IC reset input.(Low active) This pin must be set low once after power is first applied.
49	BUSYB	O	Low	Host I/F BUSYB output(High : Communication available)
50	CONT08	I/O	Input(Low)	General purpose I/O port with pull down resistor LR clock output for CD data Digital audio output<S/PDIF> FS384 clock input/output for Audio DAC Data request signal input for CD-TEXT interface (exclusive with CONT04, CONT09 and CONT12)
51	CONT09	I/O	Input(Low)	General purpose I/O port with pull down resistor LR clock output for CD data LR clock input for CD data (exclusive with CONT04 and CONT12) Frame synchronization signal (SFSY) output for CD subcode Data request signal input for CD-TEXT interface (exclusive with CONT04, CONT08 and CONT12)
52	CONT10	I/O	Input(Low)	General purpose I/O port with pull down resistor Bit clock output for CD data Bit clock input for CD data(exclusive with CONT05 and CONT13) PW data output in CD subcode Clock input/output for CD-TEXT interface (exclusive with CONT05 and CONT13)
53	CONT11	I/O	Input(Low)	General purpose I/O port with pull down resistor Serial data output for CD data Digital audio output<S/PDIF> SBCK clock input for CD subcode data (exclusive with CONT00 and CONT07) Serial data output for CD-TEXT interface

Pin No.	Pin name	I/O	State when "Reset"	Function
54	CONT12	I/O	Input(Low)	General purpose I/O port with pull down resistor LR clock input for CD data (exclusive with CONT04 and CONT09) C2 error flag output for CD data Block synchronization signal (SBSY) output for CD subcode Data request signal input for CD-TEXT interface (exclusive with CONT04, CONT08 and CONT09)
55	CONT13	I/O	Input(Low)	General purpose I/O port with pull down resistor Bit clock output for CD data Bit clock input for CD data(exclusive with CONT05 and CONT10) Frame synchronization signal (SFSY) output for CD subcode Clock input/output for CD-TEXT interface (exclusive with CONT05 and CONT10)
56	CONT14	I/O	Input(Low)	General purpose I/O port with pull down resistor Serial data output for CD data PW data output in CD subcode Serial data output for CD-TEXT interface Watch Dog Timer state monitor output
57	MODE	I	Input	LSI mode set input. This pin must be connected to the DV_{DD} level.
58	DVDD15	AO	High	Capacitor connection pin for internal regulator
59	DVDD	–	–	Digital system power supply
60	XVSS	–	–	Oscillator ground. This pin must be connected to the 0V level.
61	XOUT	O	Oscillation	16.9344MHz oscillator connection
62	XIN	I	Oscillation	16.9344MHz oscillator connection
63	XVDD	–	–	Oscillator power supply
64	SLCO	AO	Undefined	Slice Level Control output

<Notes>

(1) For Unused pins :

- The unused input pins must be connected to the GND(0V) level if there is no individual note in the above table.
- The unused output pins must be left open(No connection) if there is no individual note in the above table.
- The unused input/output pins must be connected to the GND(0V) or power supply pin for I/O block with internal pull down/up resistor OFF or be left open with internal pull down/up resistor ON when input pin mode or must be left open(No connection) when output pin mode if there is no individual note in the above table.
  When you connect an I/O pin which is an input pin without internal pull-down/up resistor at reset mode to the GND or power supply level, we recommend you to use pull-down resistor or pull-up resistor individually as fail-safe.

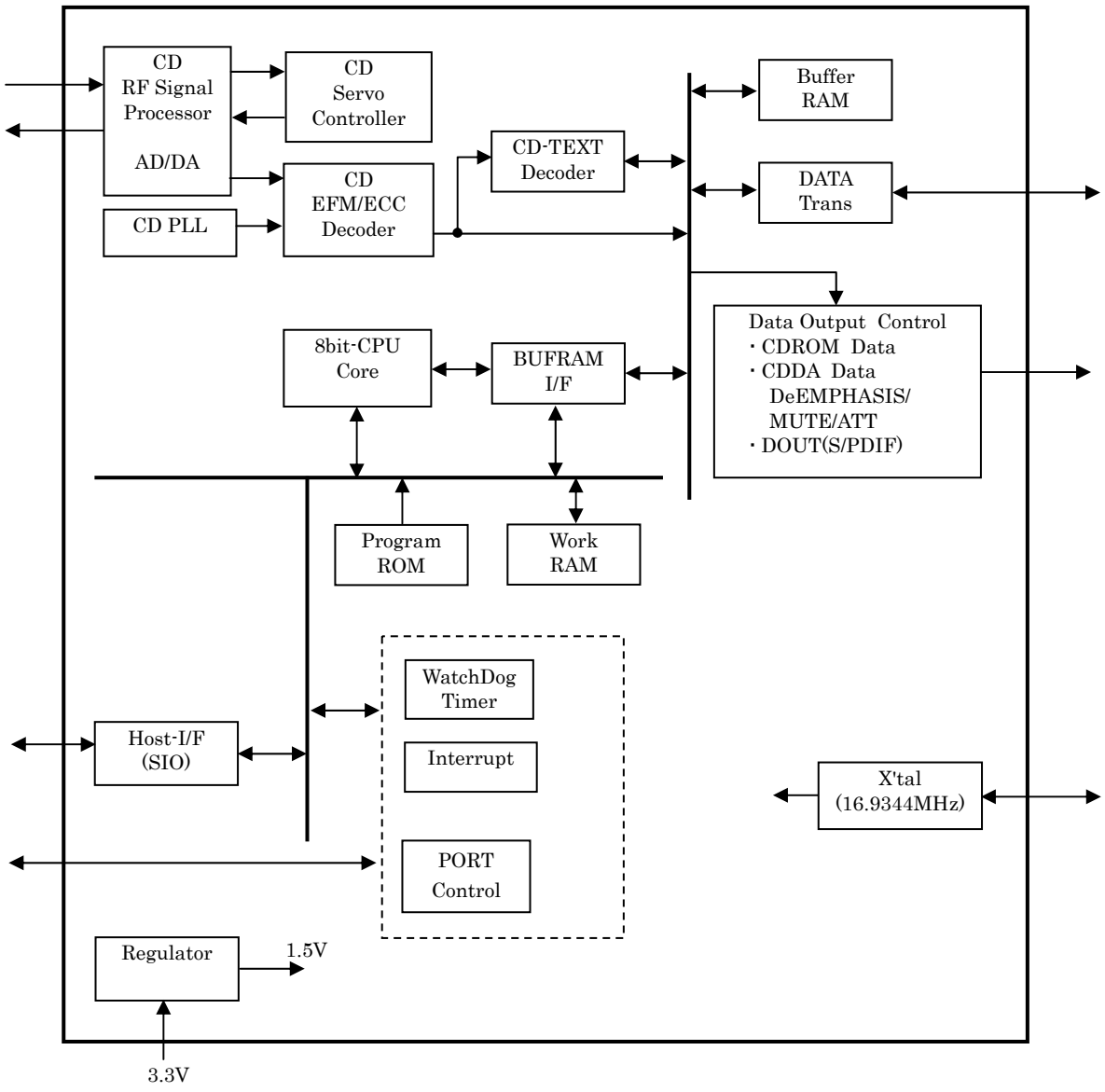
(2) For Power supply pins :

- Same voltage level must be supplied to DV_{DD}, AV_{DD}, XV_{DD} and $VV_{DD}1$ power supply pins.

(3) For "Reset" condition :

- This IC is not reset only by making the RESB pin "Low".
  Refer to "4. Power on and Reset control" for detail of "Reset" condition.

Block Diagram

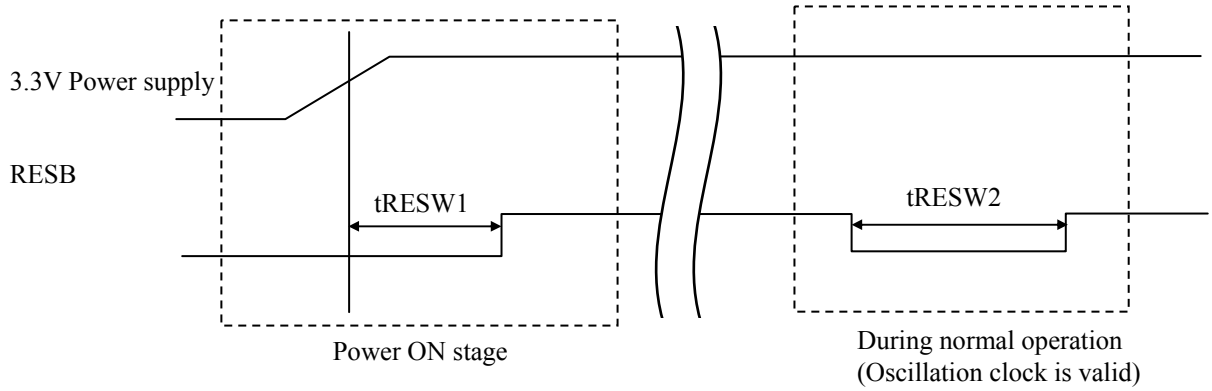


Power on and Reset control

・Attention when power on

The RESB pin must be set to “Low” level when power is first supplied. At that time, it is necessary to input a stable clock to the XIN pin.

You may input the voltage of V_{DD} or less to each input terminal when the power supply is off.



Parameter	Symbol	Min	Typ	Max	unit
Reset time(Power on)	tRESW1	20			ms
Reset time(Normal) (*1)	tRESW2	1			ms

*1 : The oscillation must be stable during tRESW2.

When the XIN clock has been stopped by the command etc. , the specification of tRESW2 could be larger than the value shown above, because it takes time that the XIN oscillator becomes stable.

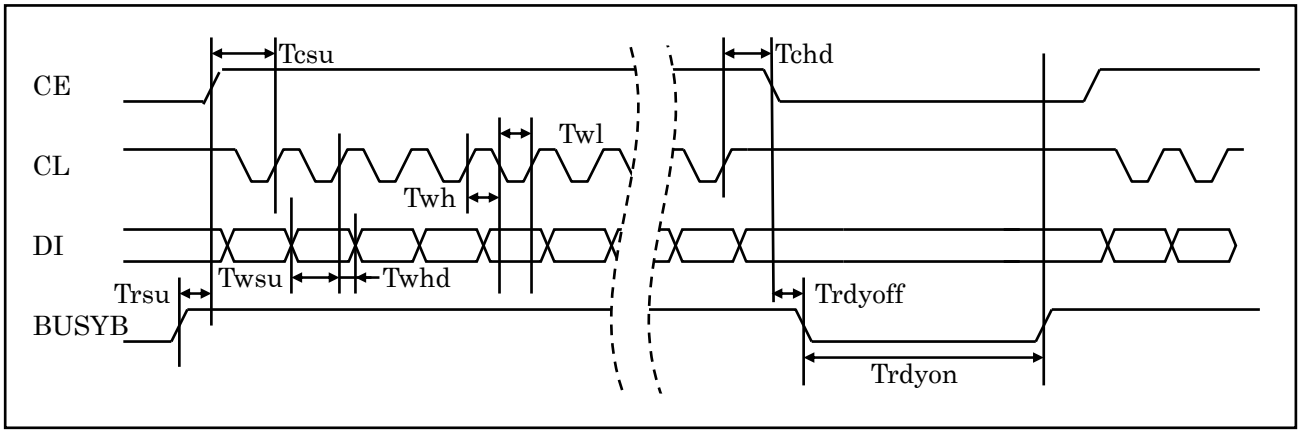
Host interface

The four wires serial interface is available as the data transmission protocol between this LSI and Host controller. It is able to know whether the internal sequencer could receive the command or not by the BUSYB pin.

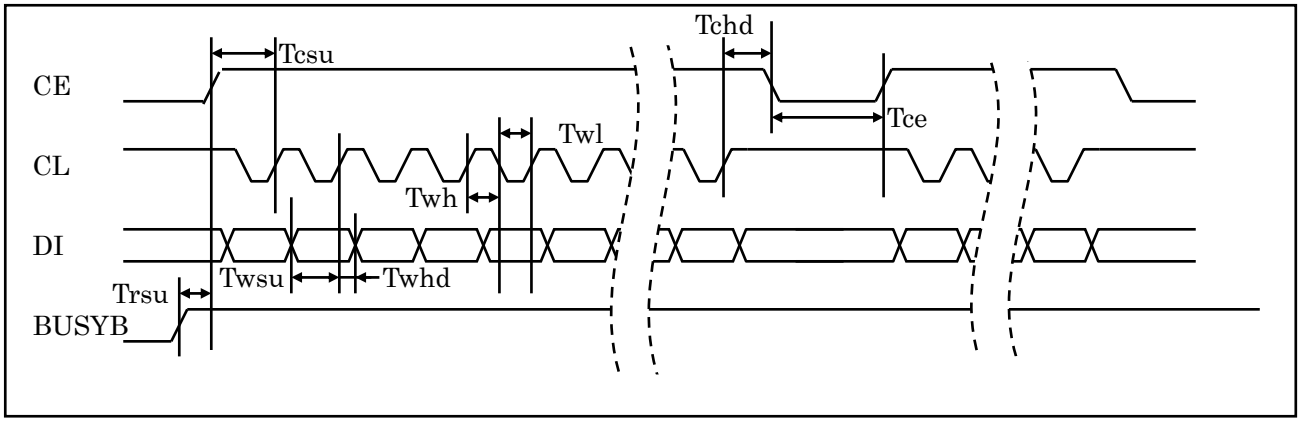
BUSYB	Command Acceptance situation
Low	All address command access disable
High	All address command access disable except A0h to A7h addresses BUSYB becomes Low if the A5h address command is transmitted. All address command except A0h to A7h addresses will be ignored.

By setting REG_READY command to High, internal register open mode is available. In this mode, Host controller can access to the all address command (internal sequencer can't control the CDDSP block). When the A5h address command is transmitted, REG_READY command and BUSYB pin is set to Low, and internal register open mode become finish.

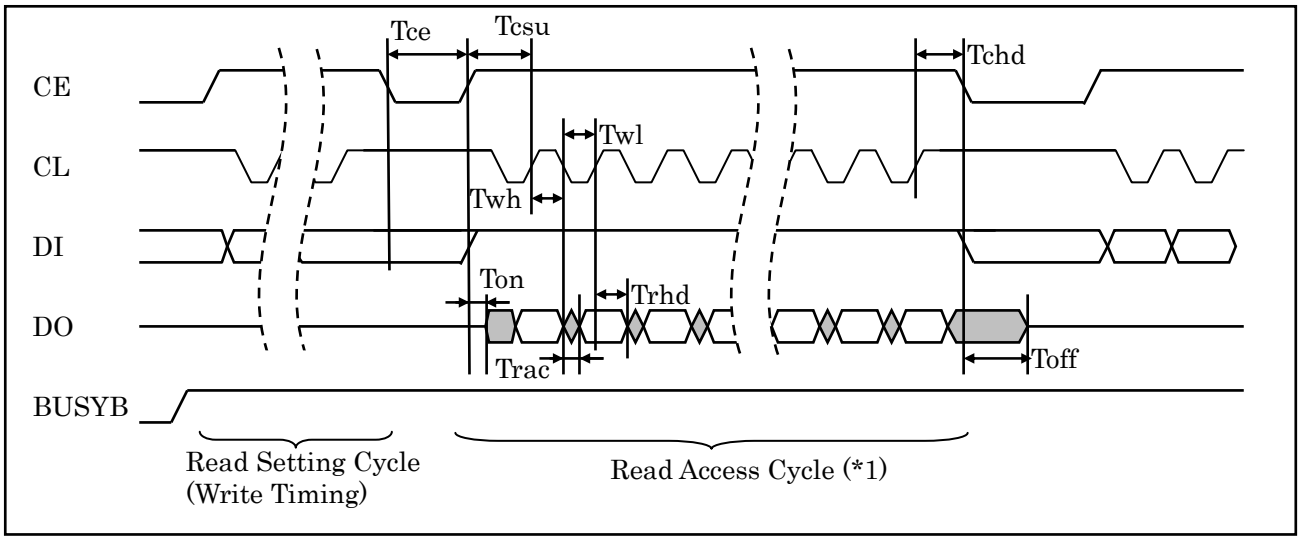
・Command Transfer Timing 1 : (Normal mode: BUSYB = "H" → "L")



・Command Transfer Timing 2 : (Internal register open mode: BUSYB = "H")

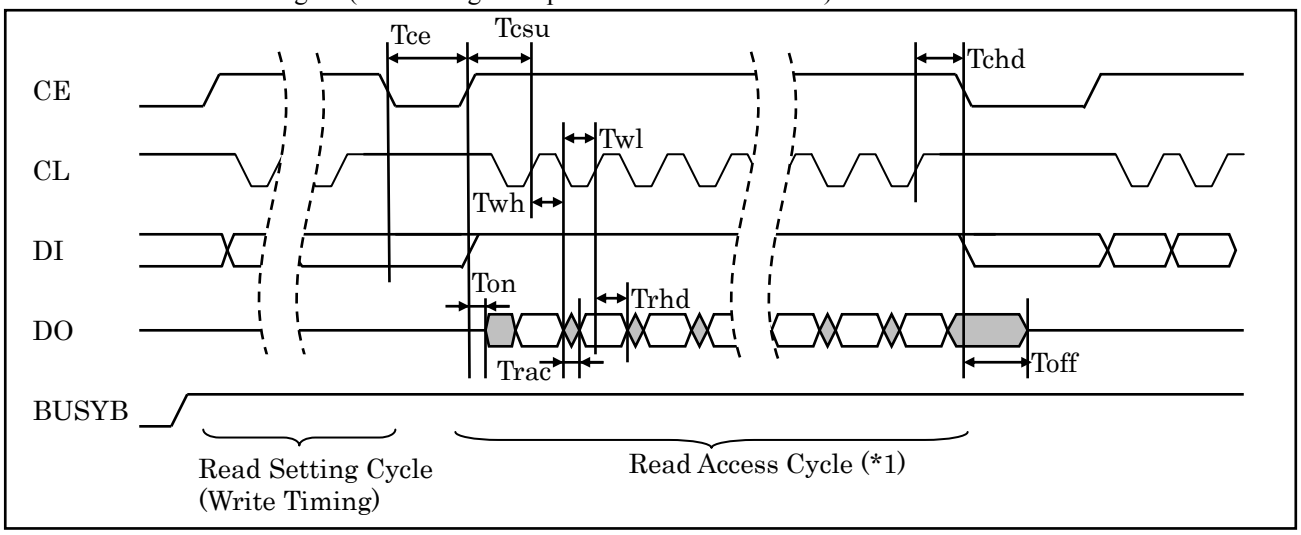


・Command Receive Timing 1 : (Normal mode : BUSYB = "H")



*1. High level must be supplied to the DI pin during Read Access Cycle.

・Command Receive Timing 2 : (Internal register open mode: BUSYB = "H")



*1. High level must be supplied to the DI pin during Read Access Cycle.

Parameter	Symbol	Pin Names	Min	Typ	Max	unit
Setup time for READY	Trsu	CE, BUSYB	60			ns
Setup time for CE	Tcsu	CE, CL	400			
Hold time for CE	Tchd	CE, CL	200			
Setup time for DI	Twsu	DI, CL	100			
Hold time for DI	Twhd	DI, CL	100			
High level clock pulse width	Twh	CL	200			
Low level clock pulse width	Twl	CL	200			
Access time for read data	Trac	CL, DO	0		100	
Hold time for read data	Trhd	CL, DO	120			
Turn On Time for DO	Ton	CE, DO	150			
Turn Off Time for DO	Toff	CE, DO	0		300	
Command transfer time	Tce	CE	1			µs
Turn Off Time for READY	Trdyoff	CE, BUSYB	0		200	ns
Turn On Time for READY(*1)	Trdyon	CE, BUSYB	0.175		50000	µs

*1. Never communicate in this period.

CD data output function

Two modes can be available for CD data output.

(1) Normal mode

In this mode, output signals are LRCK, BCK and DATA. CLV or Jitter-Free(VCEC) playback is supported.
When CDDA playback, depending on the specification of Audio DAC, FS384 clock output is also available .

(2) Slave mode

In ths mode, output signal is DATA, and input signals are LRCK, BCK. The DATA output is synchronized to input clocks (LRCK,BCK).
It is enable to output CD data synchronized to Audio DAC without connecting FS384clock.
This mode is only available for CD normal playback, and LRCK frequency must be 44.1kHz.

1. Normal mode

・Available format

Mode : IIS, MSB First Right-Justified, MSB First Left-Justified
Slot Length : 32fs, 48fs
Data Length : 16-bit

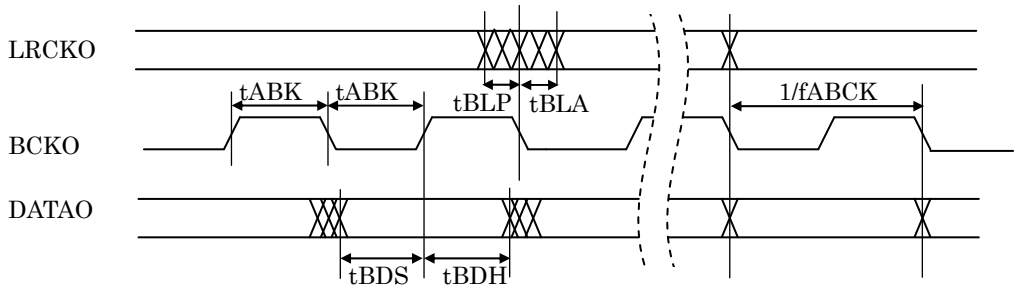
・Used Pin

LRCKO : CONT04, CONT08, CONT09
BCKO : CONT05, CONT10, CONT13
DATAO : CONT06, CONT11, CONT14

・Note

When CDDA Playback, FS384 can be optionally output from CONT08. The signal input from XIN pin is output as FS384 signal.

・CD Data output timing



Parameter	Symbol	Pin Names	Min	Typ	Max	unit
Bit clock Frequency	fABCKO	BCKO			10.5	MHz
Bit clock "H" level width	tABKOH	BCKO	47.5			ns
Bit clock "L" level width	tABKOL	BCKO	47.5			ns
Setup time for LRCK (based on BCK negedge)	tBLP	BCKO,LRCKO	0		15	ns
Hold time for LRCK (based on BCK negedge)	tBLA	BCKO,LRCKO	0		15	ns
Setup time for DATA output	tBDS	BCKO,DATAO	30			ns
Hold time for DATA output	tBDH	BCKO,DATAO	30			ns

* In case of quadruple speed playback, and setting the output format as 48fs slot length.

2. Slave mode

In this mode, LRCK (Fs=44.1kHz) and BCK are input from external device, and output data is synchronized with input clocks. So, it is possible to play CDDA without FS384 or SRC (Sampling Rate Converter).

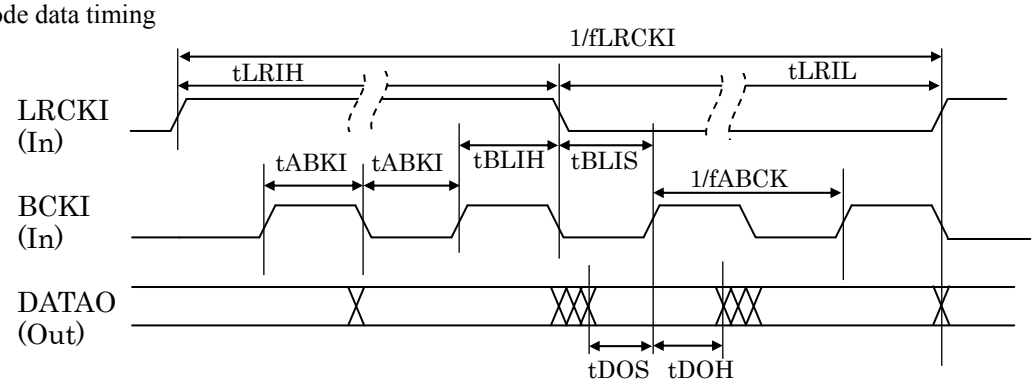
・Available format

Mode : IIS, MSB First Right-Justified, MSB First Left-Justified
Slot Length : 32fs, 48fs, 64fs
Data Length : 16-bit

・Used Pin

LRCKI : CONT04, CONT09, CONT12
BCKI : CONT05, CONT10, CONT13
DATAO : CONT06, CONT11, CONT14

・Slave mode data timing



Parameter	Symbol	Pin Names	Min	Typ	Max	unit
LRCK frequency	fLRCKI	LRCKI		44.1	48.5	kHz
LRCK "H" level width	tLRIH	LRCKI	10.3	11.34		μs
LRCK "L" level width	tLRIL	LRCKI	10.3	11.34		μs
Bit clock frequency	fABCKI	BCKI		2.1168 *1	3.10	MHz
Bit clock "H" level width	tABKIH	BCKI	160	236.2 *1		ns
Bit clock "L" level width	tABKIL	BCKI	160	236.2 *1		ns
Setup time for LRCK input	tBRIS	LRCKI,BCKI	50			ns
Hold time for LRCK input	tBLIH	LRCKI,BCKI	50			ns
Setup time for DATA output	tDOS	DATAO,BCKI	50			ns
Hold time for DATA output	tDOH	DATAO,BCKI	50			ns

*1: In case of setting the output format as 48fs slot length.

CD Subcode Data Output function

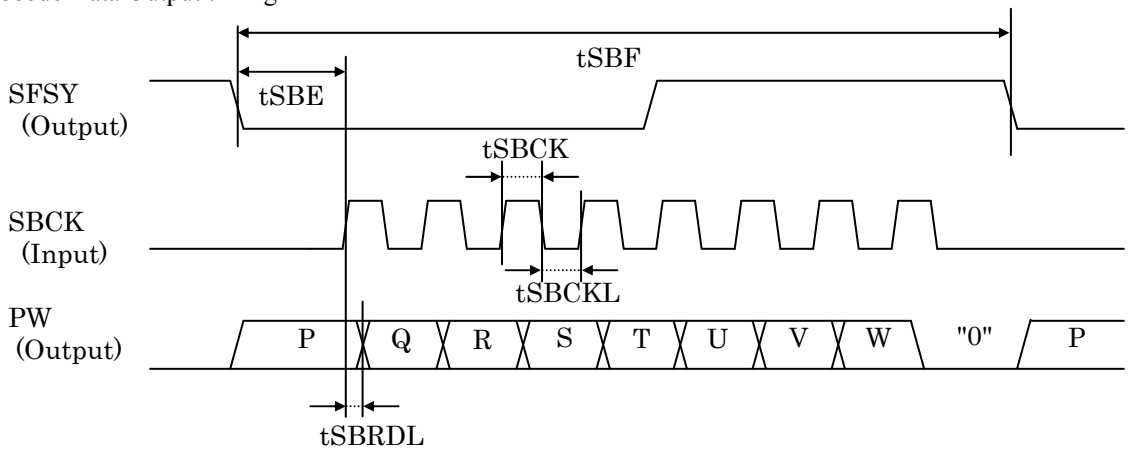
It is possible to output the subcode data (PW data) according to the terminal setting when CD playback mode.
The PW data are output at the rising edge of SBCK signal when the SBCK clock signal is input.

<Note>
The CD-TEXT function and the CD Subcode data output function are exclusive functions. It is impossible to use those two functions simultaneously.

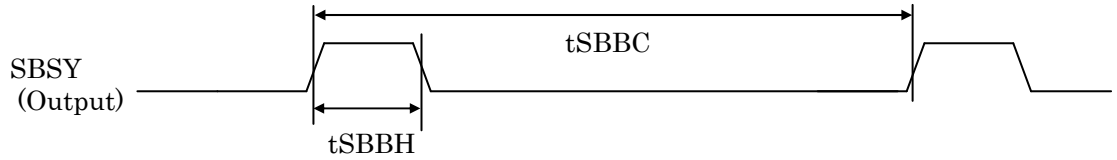
・Used pins

SBSY (Subcode Block Synchronous signal) : CONT01, CONT04, CONT12
SFSY (Subcode Frame Synchronous signal) : CONT02, CONT05, CONT09, CONT13
PW (Subcode PW data) : CONT03, CONT06, CONT10, CONT14
SBCK (Subcode data read clock) : CONT00, CONT07, CONT11

・Subcode Data Output timing



・Subcode Block Synchronous Signal Output timing



Parameter	Symbol	Pin Names	Min	Typ	Max	unit
Subcode Read Cycle time	tSBFC	SFSY		136 *1		μs
Subcode Read Enable time	tSBE	SFSY, SBCK	400			ns
SBCK clock "H" level width	tSBCKH	SBCK	250			ns
SBCK clock "L" level width	tSBCKL	SBCK	250			ns
PW data output Delay time	tSBRDL	SBCK, PW	0		100	ns
SBSY output Cycle time	tSBBC	SBSY		13.3 *2		ms
SBSY "H" level width	tSBBH	SBSY		272 *2		μs

<Notes>
1. When playback the CD at the normal speed (CLV playback).
   This value changes depending on the playback speed.
2. When playback the CD at the normal speed (CLV playback).
   The SBSY signal becomes high level during the first two subcoding symbols (S0 and S1) are asserted.

CD-TEXT data output function

There are two methods to output CD-TEXT data from the Buffer RAM in this IC.

(1) Command Communication output mode

Outputs the CD-TEXT data using the command communication protocol between this IC and external host controller.

(2) Hand shake output mode using with hardware interface function

A. Inputs data request signal and transfer clock then outputs CD-TEXT data

The CD-TEXT data(CTDATO) will be output synchronizing with the CTCKI clock when the CTCKI clock is input after the CD-TEXT data request signal is input(CTREQI="H").

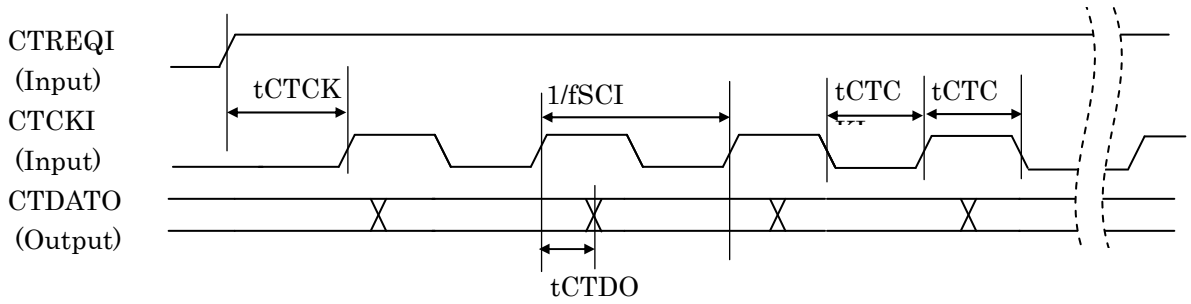
B. Inputs data request signal then outputs transfer clock and CD-TEXT data

The CTCKO and CTDATO synchronized with CTCKO will be output after the CD-TEXT data request signal is input (CTREQI= "H").

In both operation modes (1) and (2), the data transfer unit bit length is 2 Bytes (16 bits).

* The CD-TEXT function and CD subcode data output function are exclusive each other, and then those functions can not be used simultaneously.

・CD-TEXT data output Timing 1 : CTCK input mode



<Supplement>

Both modes below are available.

A. CTCKI="L" start mode

The CTDATO is output synchronized with the rising edge of the CTCKI clock.
The host controller should latch the CTDATO data at the falling edge of the CTCKI clock.

B. CTCKI="H" start mode

The CTDATO is output synchronized with the falling edge of the CTCKI clock.
The host controller should latch the CTDATO data at the rising edge of the CTCKI clock.

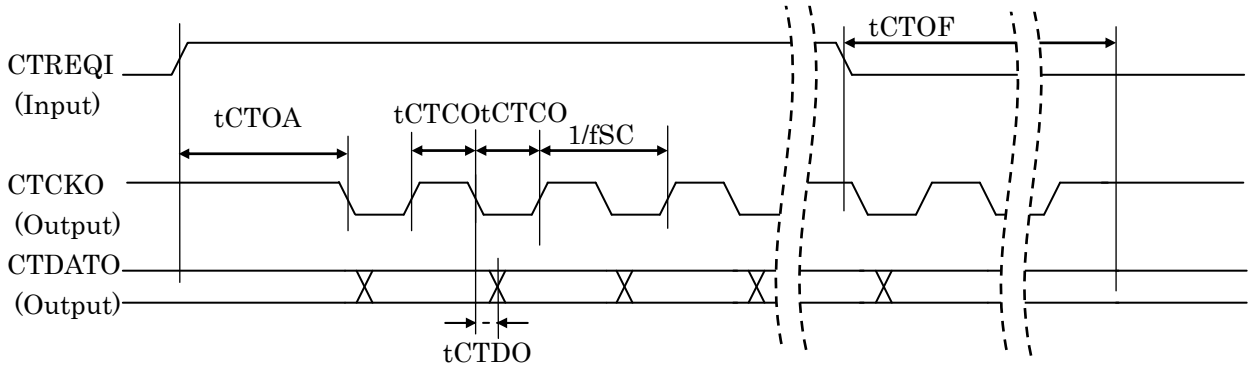
* The relationship between the signals in figure 8-1 and the pins is shown below.

CTREQI : CONT04, CONT08, CONT09, CONT12
CTCKI : CONT05, CONT10, CONT13
CTDATO : CONT06, CONT11, CONT14

Parameter	Symbol	Pin Names	Min	Typ	Max	unit
CTCKI clock Frequency	fSCI	CTCKI			1.25	MHz
CTCKI clock input start time	tCTCKIN	CTREQI, CTCKI	1000			ns
CTCKI clock "H" level width	tCTCKH	CTCKI	400			ns
CTCKI clock "L" level width	tCTCKL	CTCKI	400			ns
CTDATO output Delay time	tCTDODL1	CTCKI, CTDATO			250	ns

Note : The above figure shows the case of mode A that the clock starts low level (CTCKI="L").
The timings are same when the clock starts high level (CTCKI="H").

・CD-TEXT data output Timing 2 : CTCK output mode



<Supplement>

The CTCKO will be output starting with the high level then the CTDATO will be output synchronized with the falling edge of the CTCKO clock.
The host controller should latch the CTDATO data at the rising edge of the CTCKO clock.

* The relationship between the signals in figure 8-2 and the pins is shown below.

CTREQI : CONT04, CONT08, CONT09, CONT12
CTCKO : CONT05, CONT10, CONT13
CTDATO : CONT06, CONT11, CONT14

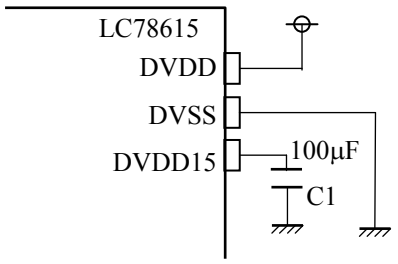
Parameter	Symbol	Pin Names	Min	Typ	Max	unit
CTCKO clock Frequency	fSCO	CTCKO	1.05		4.2	MHz
CD-TEXT data output start time	tCTOAT	CTREQI, CTCKO			(1/fSCO) ×32	ns
CD-TEXT data output stop time	tCTOFF	CTREQI, CTCKO			(1/fSCO) ×32	ns
CTCKO clock "H" level width	tCTCOH	CTCKO	400		100	ns
CTCKO clock "L" level width	tCTCOL	CTCKO	400		100	ns
CTDATO output Delay time	tCTDODL2	CTDATO, CTCKO	0		50	ns

Internal Voltage Regulator

at Ta=−40°C to 85°C, DV_{SS}=AV_{SS}=XV_{SS}=$VV_{SS}1$=0V

Parameter	Symbol	Condition	Min	Typ	Max	unit
Output Voltage	DVDD15	VDD=3.0 to 3.6V	1.35	1.50	1.65	V
Load current	Iope	VDD=3.3V			50	mA

・Example circuit for Regulator



* Same circuit need to be mounted both for two regulator pins.
(No.32 and No.58)

* C1 is the capacitor to avoid oscillation. This capacitor value must be low ESR and greater than 30µF in the range of the operating temperature. Because there is a possibility of the oscillation when the capacity value changes by the temperature change etc.
(The recommended value is 100µF.)

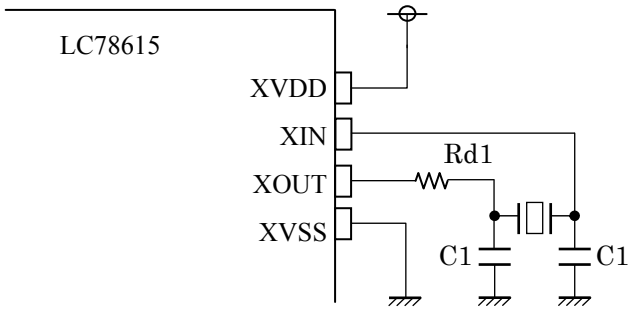
A/D, D/A converter Characteristics for servo

at Ta=−40°C to 85°C, V_{DD}=3.3V, DV_{SS}=AV_{SS}=XV_{SS}=$VV_{SS}1$=0V

Parameter	Symbol	Min	Typ	Max	unit
Resolution	Res		8		bit
Maximum input/output range	Vaio1		4/5×V_{DD}		V
Minimum input/output range	Vaio2		1/5×V_{DD}		V

Oscillator

・Example circuit for Oscillator

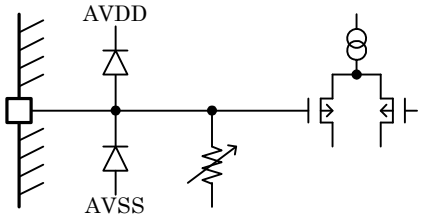
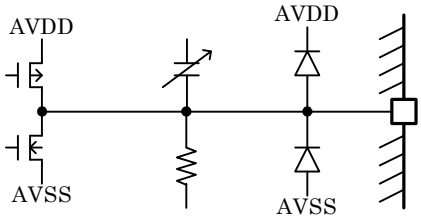
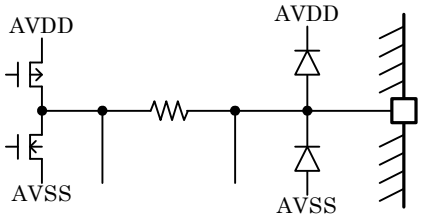
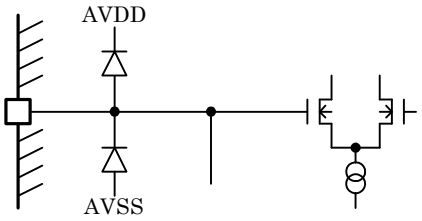
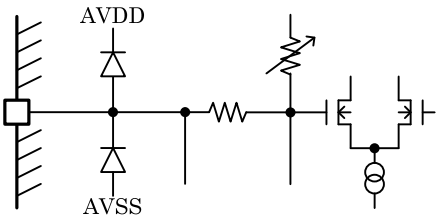
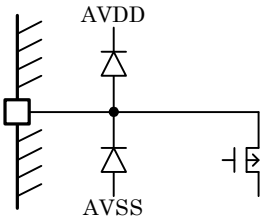
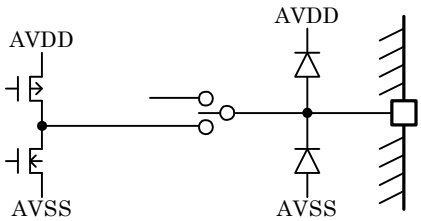


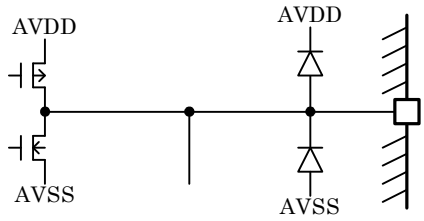
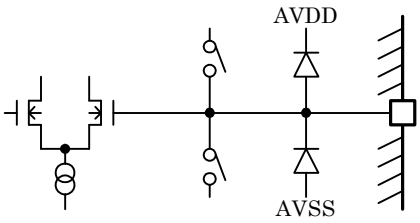
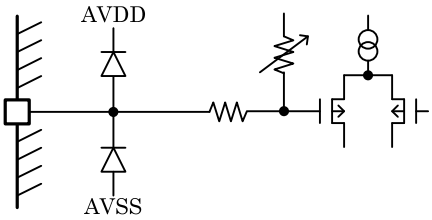
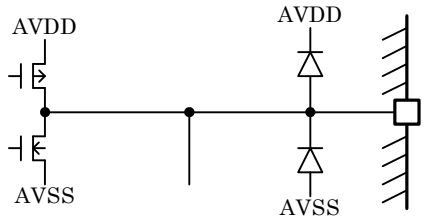
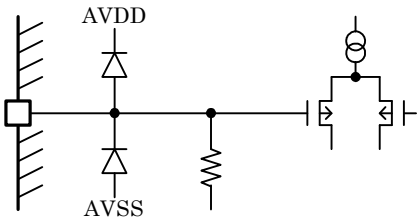
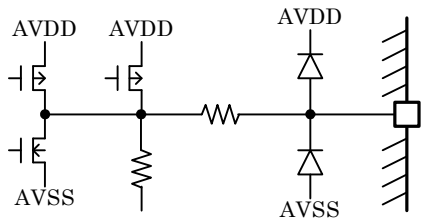
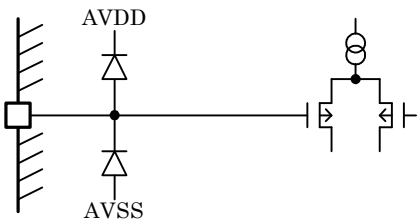
XIN/XOUT : 16.9344MHz
・For System clock of internal micro controller, CD control and Audio control
・Recommended Oscillators
Murata Manufacturing Co., Ltd.
SMD : CSTCE16M9V53-R0 <Built-in C>
: CSTCW16M9X51008-R0 <Built-in C>
Lead : CSTLS16M9X53-B0 <Built-in C>

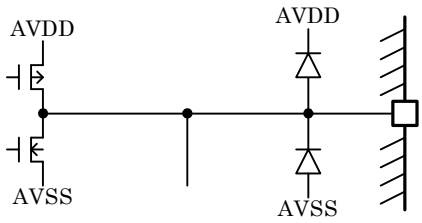
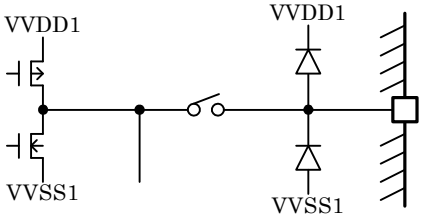
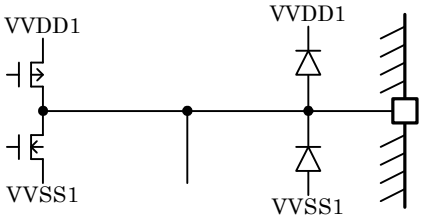
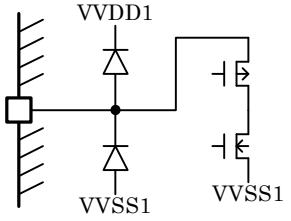
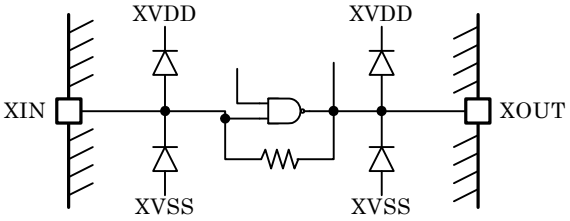
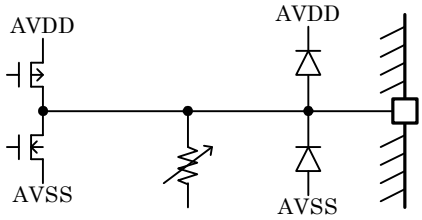
<Notes>
・Because the characteristics of oscillator could be changed according to the circuit board, ask evaluation with the individual original circuit board to the oscillator maker.
・Concerning about internal circuit for XIN/XOUT, refer to the "Analog Pin Internal Equivalent Circuits" section.

The XIN pin can also be supplied from an external clock instead of connecting the oscillator. In this case, XOUT pin must be left open.

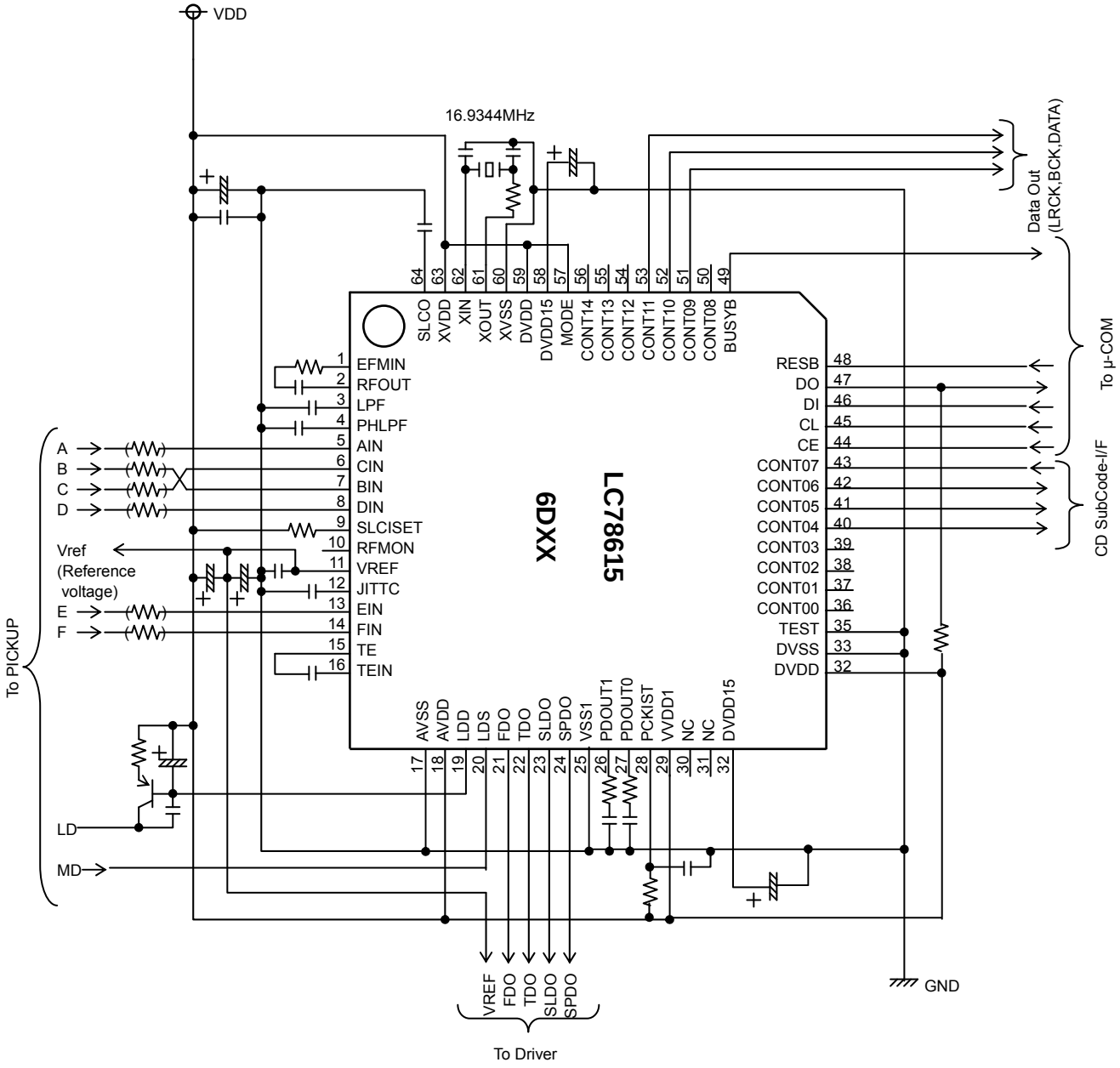
Analog Pin Internal Equivalent Circuits

Pin Name (Pin No.)	Equivalent Circuit
EFMIN (1)	
RFOUT (2)	
LPF (3)	
PHLPF (4)	
AIN (5) CIN (6) BIN (7) DIN (8)	
SLCISET (9)	
RFMON (10)	

Pin Name (Pin No.)	Equivalent Circuit
VREF (11)	
JITTC (12)	
EIN (13) FIN (14)	
TE (15)	
TEIN (16)	
LDD (19)	
LDS (20)	

Pin Name (Pin No.)	Equivalent Circuit
FDO (21) TDO (22) SLDO (23) SPDO (24)	
PDOUT1 (26)	
PDOUT0 (27)	
PCKIST (28)	
XOUT (61) XIN (62)	
SLCO (64)	

Application Circuit Example



* This sample circuit is only for CD servo block and each PLL block.
  The value of each component needs to be adjusted under the target conditions.
  The circuit for CD servo shown above could be changed depending on the CD mechanism used.

* In this sample circuit, CONT00 - CONT14 are used as 3lines outputs (LRCK, BCK, DATA) and CD-Subcode-I/F (SBCK,SBSY,SFSY,PW). For CONT00 - CONT14, use the appropriate pin function according to specifications.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC78615E-01US-H	PQFP64 14x14 / QIP64E (Pb-Free / Halogen Free)	300 / Tray Foam