Microphone Pre-Amplifer with Digital Output

Description

The AAP149B is a chip-scale device with digital output developed specifically for integrating in small form factor two terminal electret condenser microphones.

The AAP149B provides PDM bit stream output and can run with a clock frequency of 1MHz to 3MHz and it has incorporated of 4th order Sigma-Delta ADC. The ADC has a 20kHz signal bandwidth. The single bit modulator features an inherently linear output, as well as enabling noise shaping and shifting of quantization noise.

The AAP149B provides ultra-low input capacitance and noise performance, 5µVrms typical with shorted input to ground, and it also provides excellent RFI and EMI immunity.

The AAP149B has 20dB gain and low quiescent current in sleep mode. Sleep mode is automatically detected by the clock frequency falling below 100kHz.

Additionally, the AAP149B is configured to be compatible with stereo audio applications, with provision of a Left and Right channel select.

The AAP149B is provided in a chip scale 6pin SMD package. The package size is 810µm x 1200µm; with an overall height of 350µm including solder bumps. This extremely small package size and aspect ratio is optimum for use in small diameter microphones.

Available in tape & reel package.

Features

- Integrated 4th Order Sigma-Delta ADC, with 20kHz signal BW, PDM output and clock
- Frequency of 1MHz to 3MHz
- 20dB Gain
- Sleep Mode with low Quiescent Current < 40µA
- Low Input Capacitance 0.2pF typical
- Low Noise 5µV RMS typical Input Noise (A-weighted, input shorted)
- Stereo-Audio Compatible with L/R Channel Select
- RoHS Compliant & Halogen Free

Applications

- Small Diameter Electret Microphones with digital output

Functional Block Diagram

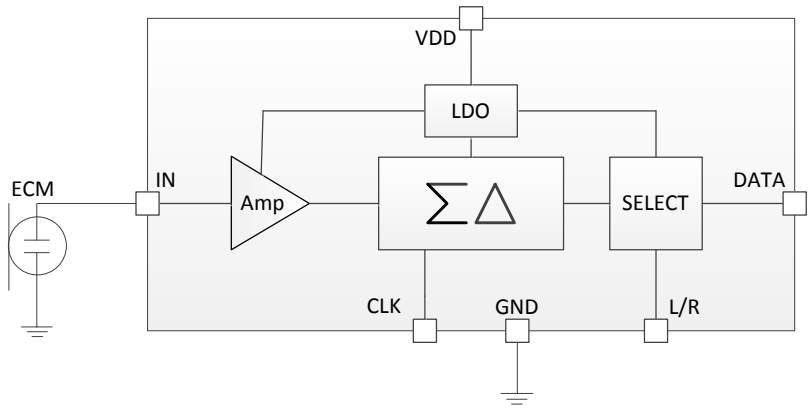


Figure 1 · Functional Block Diagram

Pin Configuration

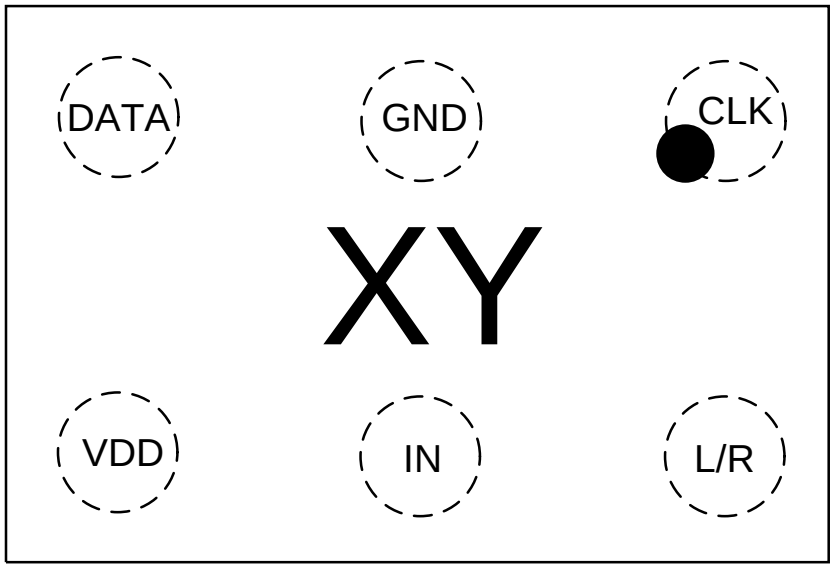


Figure 2 · Pinout (Top View)

- Top mark XY and pin 1 indicator (Laser mark)
  XY= Unique lot code assigned for each assembly order

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Packing Qty
-40°C to 85°C	RoHS2 compliant, Pb-free Halogen Free	CSP	AAP149BS-M6B-G-LF-TR	Tape and Reel	3500

Pin Description

Pin Designator	Description
CLK	ADC Clock input of 1MHz to 3MHz
GND	Ground
DATA	Data Output pin, selectable by L/R
VDD	Power input, 1.6V to 3.6V
IN	Analog signal input for Electret Condenser Microphone
L/R	Left or Right Channel Select. L/R sets low for Left channel, VDD for Right channel

Absolute Maximum Ratings

Parameter	Min	Max	Units
Power Supply (VDD)	-0.5	5	V
Analog Input (IN)	-0.5	0.5	V
Voltage on CLK (without loading clock)		5	V
Voltage on L/R		5	V
Maximum Operating Ambient Temperature	-40	85	°C
Maximum storage temperature	-65	100	°C
Peak package solder reflow temperature (40 seconds maximum exposure)		260	°C

Note: Exceeding any Absolute Maximum ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these, or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Typical Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Range	VDD	1.6	3.3	3.6	V
Operating Temperature Range	T_A	-4		45	°C
Clock Rise and Fall Time				10	ns

Electrical Characteristics

Note: Unless otherwise specified, all limits are guaranteed for T_A = 25°C, VDD= 3.3V, V_{IN} = -44dBV_{RMS}, f_{CLK}=2.4MHz, 50% duty, C_{MIC} =5pF

Parameter	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY					
Supply Voltage (VDD)		1.6	3.3	3.6	V
Supply Current	IN=GND, CLK=2.4MHz, No Load				
Normal Mode (I_{DD})	VDD=1.8V		510		µA
	VDD=3.3V		600		µA
Sleep Mode (I_{SB})	VDD=1.8V, f_{CLK}=GND		8.2	40	µA
	VDD=3.3V, f_{CLK}=GND		15.5	40	µA
PERFORMANCE					
Transfer Function (TF)			20		dBV/dBFS
Nominal Sensitivity	IN=1kHz, -44dBV		-24		dBFS
Signal-to-Noise Ratio (SNR)	IN=1kHz, -44dBV, A-weighted		60		dB(A)
Input Referred Noise (EIN)	20Hz to 20kHz, A-weighted,		5		μV_{RMS}
Dynamic Range	Derived from EIN and max acoustic input		90		dB
Band Width		25		20000	Hz
Frequency Response	Low Frequency -3dB point		33		Hz
	High Frequency -3dB point	20			kHz
THD & Noise (THD+N)			0.21		%
Overload Margin	@1% THD+N		81		mVpk
	@5% THD+N		91		mVpk
Input Capacitance (C_{IN})			0.2		pF
Input Resistance (R_{IN})		>20			GΩ
Maximum Acoustic Input			120		dBSPL
Power Supply Rejection Ratio (PSRR)	IN=GND, 217Hz, 100mVpp square wave superimposed on VDD=1.8V		-70		dBFS
DIGITAL INPUT/OUTPUT CHARACTERISTICS					
Input Voltage High (V_{IH})	I_{OUT}=1.8mA	0.65*VDD		VDD+0.3	V
Input Voltage Low (V_{IL})	I_{OUT}=1.8mA	-0.3		0.35*VDD	V
Output Voltage High (V_{OH})	I_{OUT}=1.8mA	0.65*VDD		VDD+0.3	V
Output Voltage Low (V_{OL})	I_{OUT}=1.8mA	-0.3		0.35*VDD	V
Noise Floor	20Hz to 20kHz, A-weighted		-83		dBFS
TIMING CHARACTERISTICS					
Start-Up Period (Note1)				5	ms
Sleep time (t_{SL}) (Note 3)	Time from CLK Falling < 100kHz			10	ms
Wake-Up time(t_{WU})(Note 2)	Time from CLK Rising > 100kHz, Power On			10	ms
Clock Frequency (f_{CLK})		1	2.4	3	MHz
Clock Duty Ratio		40	50	60	%

Parameter	Test Conditions	Min	Typ	Max	Units
Clock Rise/Fall time (t_{CF}, t_{CR})	R_L=1MΩ & C_L=15pF			10	ns
Time from CLK transition to data becoming valid (T_{DV})	On falling edge of CLK, L/R=GND, CL=15pF		20		ns
Time from CLK transition to data becoming Hi-Z (T_{DH})	On Rising edge of CLK, L/R=GND, CL=15pF		15		ns
Time from CLK transition to data becoming valid (T_{DV})	On Rising edge of CLK, L/R=VDD, CL=15pF		26		ns
Time from CLK transition to data becoming Hi-Z (T_{DH})	On falling edge of CLK, L/R=VDD, CL=15pF		14		ns
Load capacitance on Data (C_L)				100	pF

Notes:

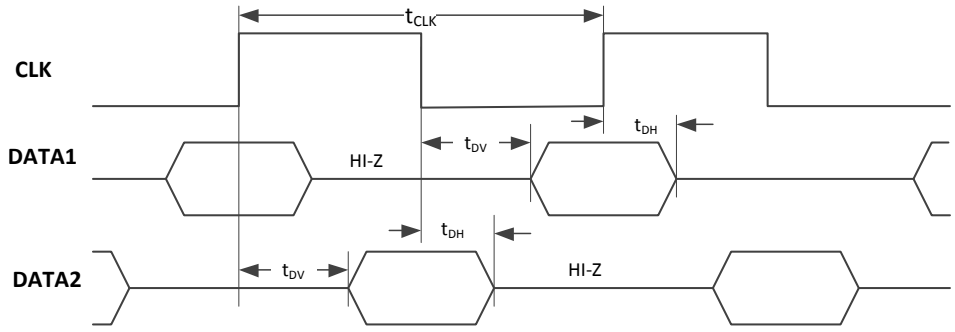
(1) Start-up period is measured when VDD becomes 3.3V to the time when transfer function settles within 1dB of its final value. After start-up period, the device can handle equivalent of 1Pa with THD <10%.

(2) The wake-up period is measured when the clock frequency is higher than 100kHz and the transfer function is settles within 1dB of its final value.

(3) Fall-sleep period is measured when the clock frequency falls below 100kHz and current drops to the stand-by current I_{SB}.

(4) The stand-by mode is entered when the clock frequency is below the specified clock frequency.

TIMING DIAGRAM



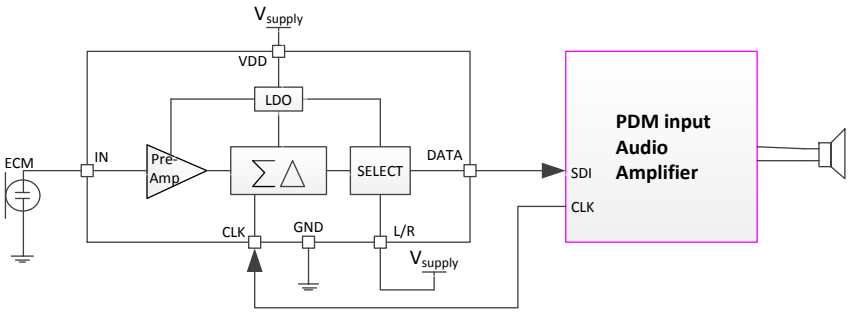
Timing diagram of CLK and DATA terminals

Applications Information

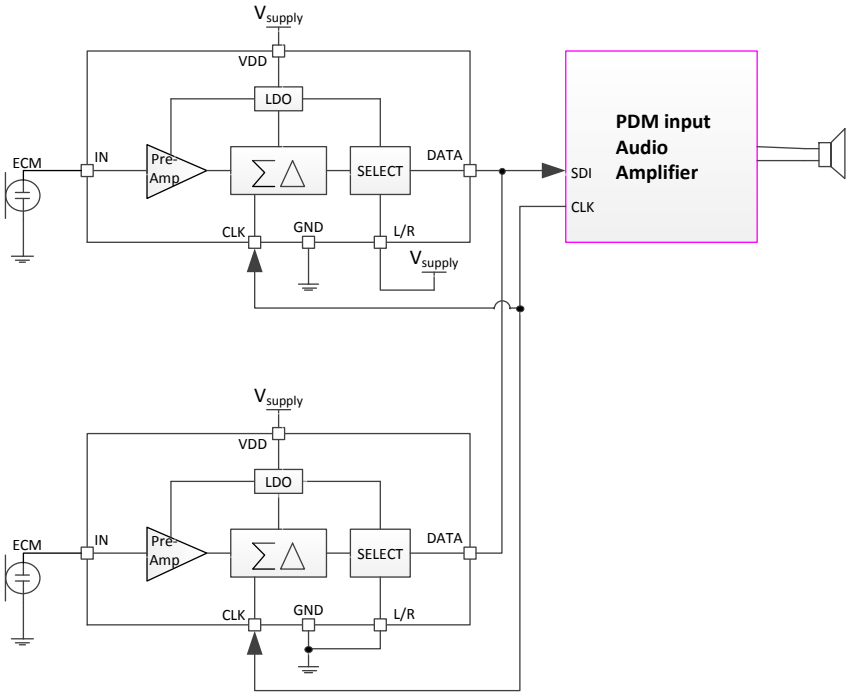
VDD is required to decouple using 0.1μF ceramic capacitor. It should be placed very close to the VDD pin and GND. Due to very high input impedance, careful consideration should be taken to remove all flux used during the reflow soldering process.

A 100Ω resistance is recommended on the clock output of the device driving AAP149B to minimize ringing and improve signal integrity.

For optimal PSRR, route a trace to the VDD pin. DO not place a VDD plane under the device.



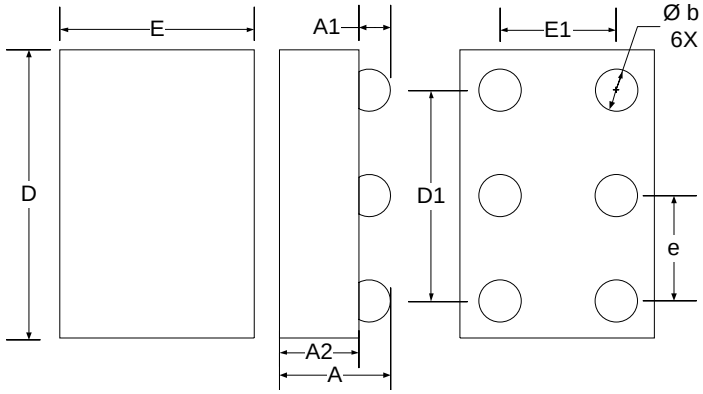
Mono Microphone Application Circuit



Stereo Microphone Application Circuit

Package Outline Dimensions

The package is halogen free and meets RoHS2 and REACH standards.

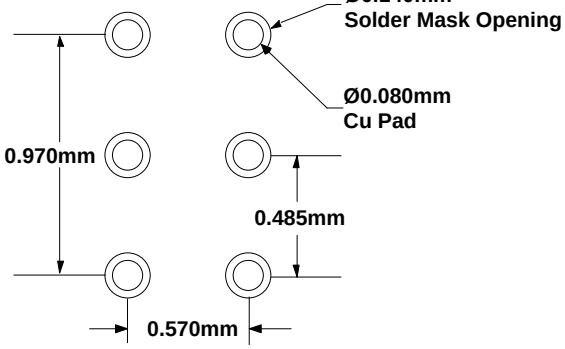


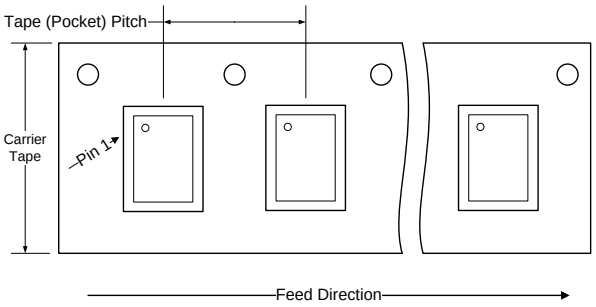
Dim	MILLIMETERS		INCHES	
	MIN	**MAX**	**MIN**	**MAX**
A	0.252	0.352	0.0099	0.0139
A1	0.065	0.095	0.0026	0.0037
A2	0.175	0.225	0.0069	0.0089
b	0.105		0.0041	
D1	0.970 BSC		0.0382 BSC	
D	1.200	1.225	0.0472	0.0482
e	0.485 BSC		0.0191 BSC	
E1	0.570 BSC		0.0224 BSC	
E	0.810	0.835	0.0319	0.0329

Note:

1. Solder ball composition is SnAg
2. Dimensions are in mm, inches for reference only.

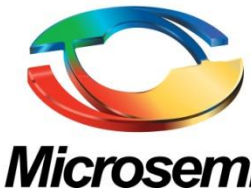
Figure 3 · 6 Bump X2CSP Micro SMD Package Dimensions





- Carrier tape width 8mm
- Reel Diameter 7”
- Devices per reel 3,500

Figure 4 · PCB Layout Footprint / Tape and Reel Information



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AAP149B-1.0/05.15