AK2346A

Two-way Radio Audio Processor

1. Features

- Audio processing
  - TX and RX amplifier
  - Pre/De-emphasis circuit
  - Compressor and Expander with no external components
  - Scrambler and De-scrambler in frequency inversion type with 16 different carrier clocks
  - Limiter with level adjuster
  - Splatter filter for wide and narrow band
  - Digital controlled amplifier for microphone, modulator and demodulator sensitivity

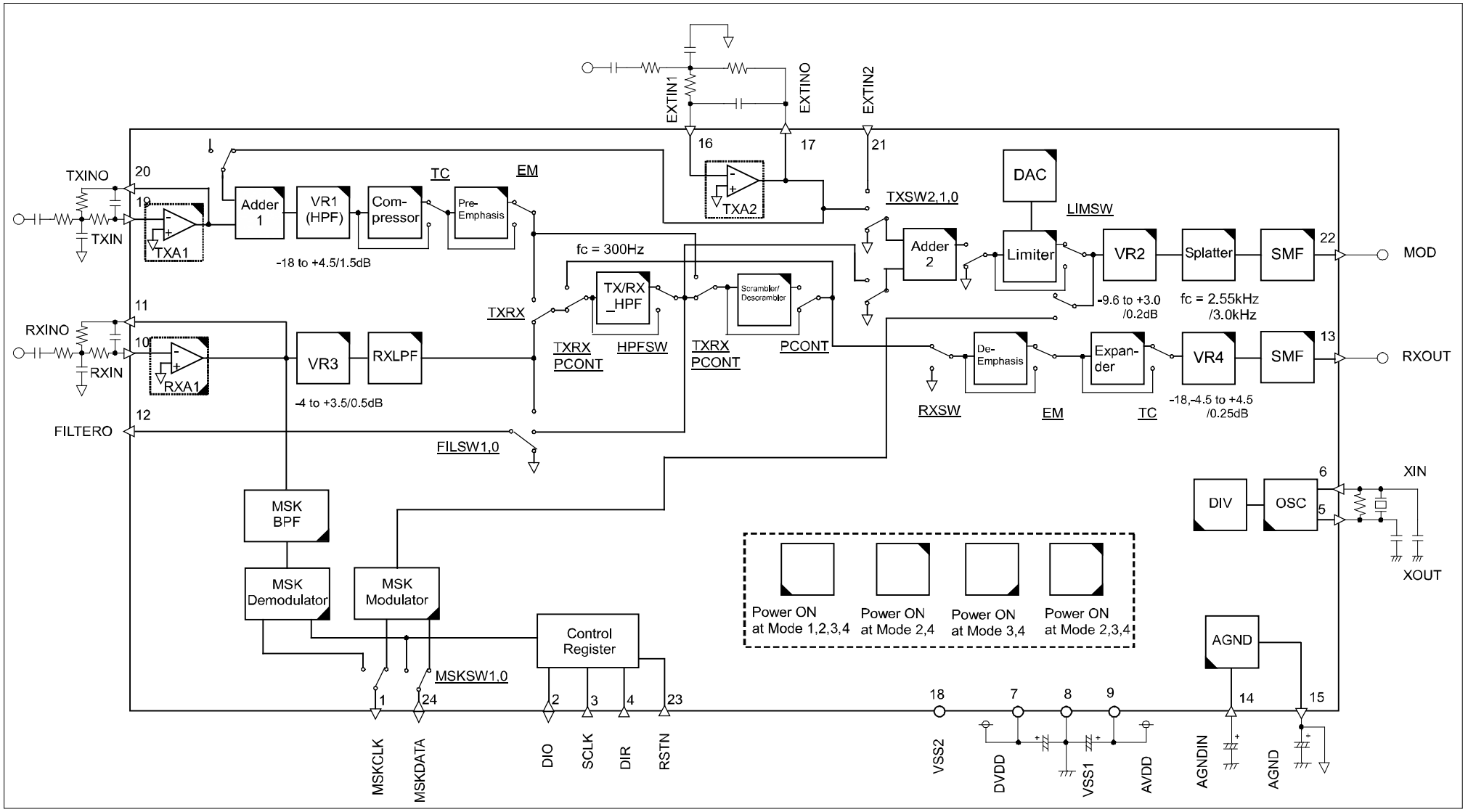
- 1200/2400bit/s MSK Modem with frame detection
- Wide range operation voltage: 2.6V to 5.5V, temperature: -40 to 85 °C
- Oscillator circuit for 14.7456MHz crystal
- Serial control interface operation
- Compact plastic packaging, 24-pin QFNJ (4.0 x 4.0 x 0.75mm 0.5mm pitch)

2. Description

AK2346A includes audio filter, limiter, splatter filter, Compandor, scrambler, MSK Modem, which is highly integrated two-way radio baseband functions for FRS and LMR.
Audio high-pass filter shows a high attenuation in magnitude response characteristics less than 250Hz that supports to eliminate a sub-audio tone clearly.
TX limiter for deviation control has a limiting level adjuster controlled by a 4-bit signal level adjuster.
Splatter filter has the magnitude response for narrowband (fc=2.55kHz) and wideband (3.0kHz) to meet various regulatory agencies in the world wide.
Compandor is no adjustment type because it includes all parametric components inside the chip.
Scrambler circuit is composed of frequency inversion circuit by double balanced mixer that has 16 different carrier clocks.
MSK Modem for data communication can be chosen either 2400bit/s or 1200bit/s. 2400bit/s data rate provides a high speed data transmission and 1200bit/s supports a low BER (bit error rate) performance that is suitable for under weak electrical field condition application.
There are four signal level adjusters for microphone, modulator and demodulator sensitivity by digital controlled amplifier (volume).

3. Contents

4. Block Diagram



5. Circuit Configuration

Block	Description
TXA1	The operational amplifier for transmit audio gain adjustment and for the filter to eliminate aliasing noise by the SCF(switched capacitor filter) in the following stage. Please select an external resistor and capacitor to set the gain less than 30dB and the cut-off frequency to about 10kHz.
VR1 (HPF)	Digitally controlled amplifier (volume) for transmit audio signal level which is adjustable in 1.5dB steps over a –18.0dB to +4.5dB range by setting VR13 to VR10 register.
Compressor	The circuit to compress transmits audio signal level by 1/2 in dB scale. Standard cross-point is –10dBx. TC register sets OFF/ON to the circuit.
Pre-emphasis	The circuit to emphasis the high-frequency component of transmit audio signal to improve S/N ratio of the modulation signal.
TX/RXHPF	The High-pass filter to eliminate the low-frequency component less than 250Hz for transmit and receive audio signal. This circuit is turned on and off by HPFSW register.
Scrambler/ Descrambler	Scramble/De-scramble circuit to inverse transmit and receive audio spectrum by 2.844 to 3.491kHz carrier signal. EM and PCONT register can set scramble/de-scramble or emphasis circuit. Both circuits can not be used simultaneously.
Adder1/2	The circuit to add audio signal and external tone signal. TXINSW,TXSW2,1,0 registers are used to set this block.
Limiter	An amplitude limiting circuit to suppress the frequency deviation of the modulation signal. The limitation level can be adjusted by internal DAC.
DAC	Digitally controlled amplifier (volume) for the limitation level of the limiter circuit which is adjustable in 0.5dB steps over a -17.6dB to -2.1dB range by setting LIMLV3 toLIMLV0 register.
VR2	Digitally controlled amplifier (volume) for MOD output level which is adjustable in 0.2dB steps over a –3.2dB to +3.0dB range by setting VR25 to VR20 register. VR25 is a –6.4/0dB coarse bit.
Splatter	The circuit to eliminate the high frequency component higher than 3kHz included in the limiter output signal or the MSK modulator signal. The cut-off frequency can be selected by SPL register.
SMF	The smoothing filter to eliminate the high frequency and clock component caused in SCF circuits.
RXA1	The operational amplifier for receives audio gain adjustment and for the filter to eliminate aliasing noise by the SCF in the following stage. Please select an external resistor and capacitor to set the gain less than 20dB and the cut-off frequency to about 40kHz.
VR3	Digitally controlled amplifier (volume) for receive audio signal level which is adjustable in 0.5dB steps over a –4.0dB to +3.5dB range by setting VR33 to VR30 register.
RXLPF	The Low-pass filter to eliminate the high frequency component higher than 3kHz for receive audio signal.
De-emphasis	The circuit to de-emphasis the emphasized signal by pre-emphasis circuit.
Expander	The circuit to expand the receive audio signal level to double in dB scale compressed by compressor Standard cross-point is –10dBx. TC register sets OFF/ON to the circuit.
VR4	Digitally controlled amplifier (volume) for Expander output level which is adjustable in 0.25dB, steps over a –18dB and –4.5dB to +4.5dB range by setting VR42 to VR40 register.
TXA2	The operational amplifier for transmit audio gain adjustment and for the filter to eliminate aliasing noise by the SCF(switched capacitor filter) in the following stage. Please select an external resistor and capacitor to set the gain less than 30dB and the cut-off frequency to about 10kHz.

Block	Description
MSK BPF	The Band-pass filter to eliminate the low and high frequency component for received MSK signal.
MSK Demodulator	The circuit to reproduce the 1200/2400bit/s receive clock and data from MSK signal at RXIN pin.
MSK Modulator	The circuit to generate a MSK signal according to the received digital data from MSKDATA pin.
AGND	The circuit to generate the reference voltage (1/2VDD) for internal analog signal.
OSC	The circuit to oscillate the 14.7456MHz reference clock with an external crystal oscillator and resistor and capacitors.
DIV	The circuit to generate 1/2,1/3 or 1/4 frequency-divided output When a signal whose frequency is twice, three times, or four times higher than 3.6864MHz is input from the outside, this circuit divides the signal frequency by two, three, or four. MCKSL[1:0] register is used to set this block.
Control Register	The control register controls the status of internal switches and digitally controlled amplifiers of IC by serial data that consists of 4 address bits and 8 data bits. The data buffer stores 8 bits of the MSK received data to smooth the signal interface with microprocessor. At the start up, RSTN-pin is used for system reset. SRST register is used for software reset. (Refer to the control register map)

6. Pin/Function

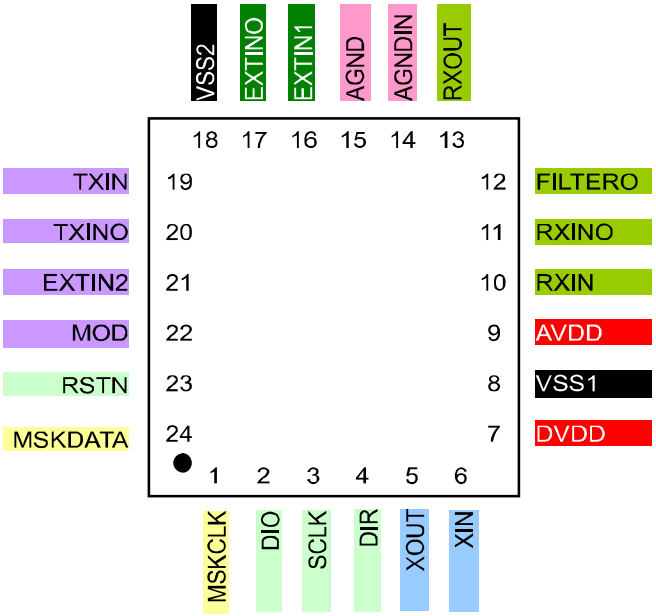
Package	Signal			Function
Pin No	Name	Type	Conditions at power down	
1	MSKCLK	DO	H	Clock input and output pin for MSK signal.
2	DIO	DB	Z	Serial data input and output pin. Input for register setting data and output for MSK receive data.
3	SCLK	DI	Z	Clock input pin for serial data I/O.
4	DIR	DI	Z	Serial data I/O control pin.
5	XOUT	DO	*2)	Crystal oscillator connecting input pin.
6	XIN	DI	*2)	Crystal oscillator connecting input and output pin. To connect a 14.7456MHz crystal oscillator between this pin and XOUT pin generates the reference clock internally. In case of externally supplied clock operation, connect to this pin. For more information, please refer to external application circuits.
7	DVDD	PWR	-	Digital VDD power supply pin. Normally connect to 2.6V to 5.5V power-supply. Also this pin must be decoupled to VSS pin by 0.1uF capacitor mounted close to the device pins.
8	VSS1	PWR	-	VSS power supply pin. Normally supply 0V to this pin.
9	AVDD	PWR	-	Analog VDD power supply pin. Normally connect to 2.6V to 5.5V power-supply. Also this pin must be decoupled to VSS pin by 0.1uF capacitor mounted close to the device pins. Applied voltage must be DVDD ≤ AVDD

Package	Signal			Function
Pin No	Name	Type	Conditions at power down	
10	RXIN	AI	Z	Demodulated audio signal input pin. This is the inverting input of RXA1. It composes a pre-filter with external resistor and capacitor.
11	RXINO	AO	Z	RXA1 feedback output pin.
12	FILTERO	AO	Z	RXLPF circuit and TX/RX_HPF circuit output pin. LPF output pin. This is a monitor pin for tone signal. 57.6kHz sampling-clock is included, so please eliminate this signal component by LPF externally.
13	RXOUT	AO	Z	Receive audio signal output pin.
14	AGNDIN	AI	*1)	Analog ground input pin. Connect the capacitor to stabilize the analog ground level.
15	AGND	AO	*1)	Analog ground output pin. Connect the capacitor to stabilize the analog ground level.
16	EXTIN1	AI	Z	TXA2 feedback input pin. This is the inverting input pin for TXA2. It composes a microphone amplifier with an external resistor and capacitor.
17	EXTINO	AO	Z	TXA2 feedback output pin.
18	VSS2	PWR	-	VSS power supply pin. Normally supply 0V to this pin.
19	TXIN	AI	Z	Transmit audio signal input pin. This is the inverting input pin for TXA1. It composes a microphone amplifier with an external resistor and capacitor.
20	TXINO	AO	Z	TXA1 feedback output pin.
21	EXTIN2	AI	Z	External input pin. This pin is available for external tone signal.
22	MOD	AO	Z	The modulated transmit signal output pin.
23	RSTN	DI	Z	Reset pin.
24	MSKDATA	DB	Z	MSK signal MSK signal transmitted and received data input and output pin. In transmission, AK2346A reads data synchronized with the rising edge of MSKCLK. This pin outputs 2 kinds of information according to the setting of FSL register. This pin puts out two types of signal that depends on the status of register named FSL. In case FSL equal “1”, it is received flag mode (RDF). So the pin puts out low level after 8 bits of MSK receive signal have been written to the internal register. In case FSL equal “0”, it is frame detection mode (FD). So the low pulse is put out after a frame pattern is detected. When MSKSW[1:0] register is set to “1/0”, RDATA signal is put out.

Note **A**: Analog, **D**: Digital, **PWR**: Power, **I**: Input, **O**: Output, **B**: Bidirectional, **Z**: High-Z, **L**: Low

*1) AGND level
*2) When XIN pin is set to low level, XOUT pin goes to high level.

• Pin Assignment



7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	AVDD	-0.3	6.5	V
	DVDD	-0.3	6.5	V
Ground Level	VSS	0	0	V
Input Voltage	V_{IN}	-0.3	AVDD+0.3	V
		-0.3	DVDD+0.3	V
Input Current (Except power supply pin)	I_{IN}	-10	+10	mA
Storage Temperature	T_{stg}	-55	130	°C

Note : All voltages with respect to the VSS pin.

Caution : Exceeding these maximum ratings can result in damage to the device.
Normal operation cannot be guaranteed under this extreme.

8. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating Temperature	Ta		-40		85	°C
Power Supply Voltage	AVDD		2.6	3.0	5.5	V
	DVDD	DVDD≤AVDD	2.6	3.0	5.5	V
Analog Reference Voltage	AGND			1/2AVDD		V
Output Load Resistance	R_{L1}	MOD, RXOUT, FILTEROO	10			kΩ
	R_{L2}	TXINO, RXINO, RXOUT	30			
Output Load Capacitance	C_{L1}	MOD, RXOUT, FILTEROO			50	pF
	C_{L2}	TXINO, RXINO, RXOUT			15	

Note : All voltages with respect to the VSS pin.

9. Digital DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High level input voltage	V_{IH}	DIO,SCLK,DIR,MSKDATA, RSTN	0.8VDD			V
Low level input voltage	V_{IL}	DIO,SCLK,DIR,MSKDATA, RSTN			0.2VDD	V
High level input current	I_{IH}	V_{IH}=DVDD DIO,SCLK,DIR,MSKDATA, RSTN			10	μA
Low level input current	I_{IL}	V_{IL}=0V DIO,SCLK,DIR,MSKDATA, RSTN	-10			μA
High level output voltage	V_{OH}	I_{OH}=+0.2mA MSKCLK,MSKDATA,DIO	VDD-0.4		VDD	V
Low level output voltage	V_{OL}	I_{OL}=-0.4mA MSKCLK,MSKDATA,DIO	0.0		0.4	V

10. Clock Input Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	MCK0	XIN,XOUT		14.7456		MHz	
	MCK1	XIN		3.6864 7.3728 11.0592 14.7456		MHz	*1), *2)
High level input voltage	V_{MCK1_IH}	XIN	1.5			V	*1)
Low level input voltage	V_{MCK1_IL}	XIN			0.4	V	*1)
Input amplitude	V_{MCK2}	XIN	0.2		1.0	V_{PP}	*2)

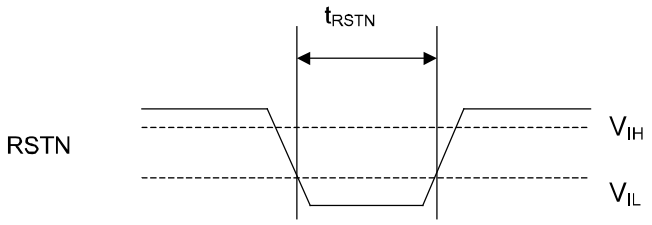
*1) These values apply when the clock signal is input on the XIN pin directly. For details, refer to 6), "Oscillator circuit", in "Recommended External Circuit Examples".

*2) These values apply when the clock signal is input on the XIN pin via DC cut. For details, refer to 6), "Oscillator circuit", in "Recommended External Circuit Examples".

11. System Reset

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Hardware reset signal input width	t_{RSTN}	RSTN pin	1			μs	*1)
Software reset		SRST register					*2)

*1) After power-on, be sure to perform a hardware reset operation (register initialization). The system is reset by a low pulse input of 1μs (min.) and enters the normal operation state. At this moment, the digital (DI) pins are set as follows: RSTN pin to high, MSKDATA pin to low, SCLK pin to high, DIR pin to low.



*2) When data 0xAA:10101010 is written to the SRST[7:0] register, software reset is performed. This setting initializes the registers and the operation mode is set to mode 0 (power down). After software reset is completed, this register comes to “0”.

12. Power Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Consumption Current	IDD0	Mode 0 OSC:OFF, Audio: OFF, Modem:OFF		0.1	0.3	mA
	IDD1	Mode 1 OSC:ON , Audio: OFF, Modem:OFF		0.8	1.5	
	IDD2	Mode 2 OSC:ON , Audio: ON , Modem:OFF		5.4	8.7	
	IDD3	Mode 3 OSC:ON , Audio: OFF, Modem:ON		1.8	3.2	
	IDD4	Mode 4 OSC:ON , Audio: ON , Modem:ON		6.0	9.5	

13. Analog Characteristics

For the following conditions unless otherwise specified: f=1kHz, Emphasis: on, Compandor: on, Scrambler: off, VR1=VR2=VR3=VR4=0dB with the external circuit shown in example page.33 to 35. "dBx" is standardized unit for 2.6V to 5.5V operation, 0dBx=-5+20log(VDD/2)dBm, 0dBm=0.775Vrms.

1) TX Audio System

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Standard Input Level	@TXINO		-10		dBx	
Absolute Gain	TXINO to MOD	-1.5	0	+1.5	dB	
Limit Level	EXTLIMIN to MOD	-8.6	-7.6	-6.6	dBx	
Compressor Linearity	TXINO to MOD TXINO=-44dBx TXINO=-50dBx Relative value to 0dB for MOD level of -10dBx TXINO.	 -20.0 -24.0	 -17.0 -20.0	 -14.0 -16.0	dB	
Compressor Distortion	TXINO to MOD TXINO=-10dBx 30kHz Low-pass filtering			-35	dB	
Noise Level with no signal input	TXINO to MOD C-Message filtering			-36.5	dBm	
VR1 Attenuation Error	TXINO to MOD -18.0 dB to 4.5dB, 1.5dB/step	-1.5		+1.5	dB	
VR2 ATT Error (VR24,23,22,21,20)	TXINO to MOD -3.2dB to +3.0dB, 0.2dB/step	-0.2		+0.2	dB	
VR2 ATT Error (VR25=0)	TXINO to MOD When -6.4dB setting Relative error for -6.4/0dB	-6.8	-6.4	-6.0	dB	
Limiter DAC Error (VR25=0)	MOD -10～+5.5dB, 0.5dB/step	-0.5		+0.5	dB	

2) RX Audio System

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Standard Input Level	@RXINO		-10		dBx	
Absolute Gain	RXINO to FILTERO	-1.5	0	+1.5	dB	
	RXINO to RXOUT	-1.5	0	+1.5	dB	
Expander Linearity	RXINO to RXOUT RXINO=-25dBx RXINO=-30dBx Relative value to 0dB for RXOUT level of -10dBx RXINO	 -33.0 -45.0	 -30.0 -40.0	 -27.0 -35.0	dB	
Expander Distortion	RXINO to RXOUT RXINO=-5dBx 30kHz Low-pass filtering			-35	dB	
Noise Level with no signal input	RXINO to RXOUT C-Message Filtering			-70	dBm	
VR3 Attenuation Error	RXIN0 to RXOUT -4.0dB to +3.5dB, 0.5dB/step	-0.5		+0.5	dB	
VR4 Attenuation Error	RXIN0 to RXOUT -4.5 to +4.5dB, 0.25dB/step	-0.25		+0.25	dB	
VR4 ATT Error (VR42,41,40=0,0,0)	RXIN0 to RXOUT When -18dB setting Relative error for -18/0dB	-20	-18	-16	dB	

3) Audio Filter Characteristics

3.1) Emphasis: **off**, Compandor: off, Scrambler: off (Design target values)

Parameter	Condition		Min.	Typ.	Max.	Units	Notes
TX overall characteristics	TXINO to MOD Relative value to gain at 1kHz	250Hz		-50	-38	dB	
		300Hz to 2.0kHz	-1.0		+1.0	dB	*SPL*=0 fc=2.55K
		2.5kHz	-1.5		+1.0		
		3.0kHz	-4.0		-1.0		
		6.0kHz		-38	-28		
		300Hz to 2.5kHz	-1.0		+1.0	dB	*SPL*=1 fc=3.0K
		3.0kHz	-1.5		+1.0		
		6.0kHz		-43	-22		
RX overall characteristics	RXINO to RXOUT Relative value to gain at 1kHz	250Hz		-49	-38	dB	
		300Hz	-1.5		+1.0		
		350Hz to 3.0kHz	-1.0		+1.0		
		6.0kHz		-38	-28		

3.2) Emphasis: **on**, Compandor: off, Scrambler: off

Parameter	Condition		Min.	Typ.	Max.	Units	Notes
TX overall characteristics	TXINO to MOD Relative value to gain at 1kHz	250Hz		-57	-40	dB	
		300Hz	-12.5		-9.5	dB	*SPL*=0 fc=2.55K
		2.5kHz	+6.0		+9.0		
		3.0kHz	+4.5		+8.5		
		6.0kHz		-29	-18		
		300Hz	-12.5		-9.5	dB	*SPL*=1 fc=3.0K
		2.5kHz	+6.0		+9.0		
		3.0kHz	+7.0		+10.5		
		6.0kHz		-34	-12		
RX overall characteristics	RXINO to RXOUT Relative value to gain at 1kHz	250Hz		-38	-26	dB	
		300Hz	+8.5		+11.5		
		3.0kHz	-11.5		-8.5		
		6.0kHz		-52	-40		

- Audio path frequency response (Emphasis:off)

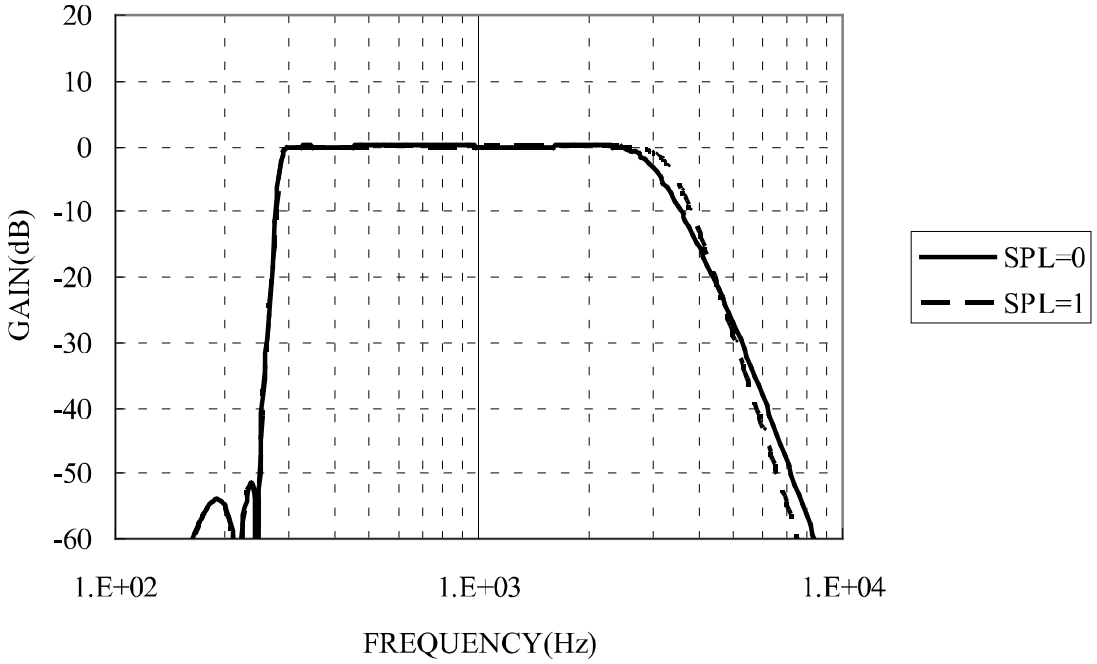


Figure 1: TX overall response without pre-emphasis.

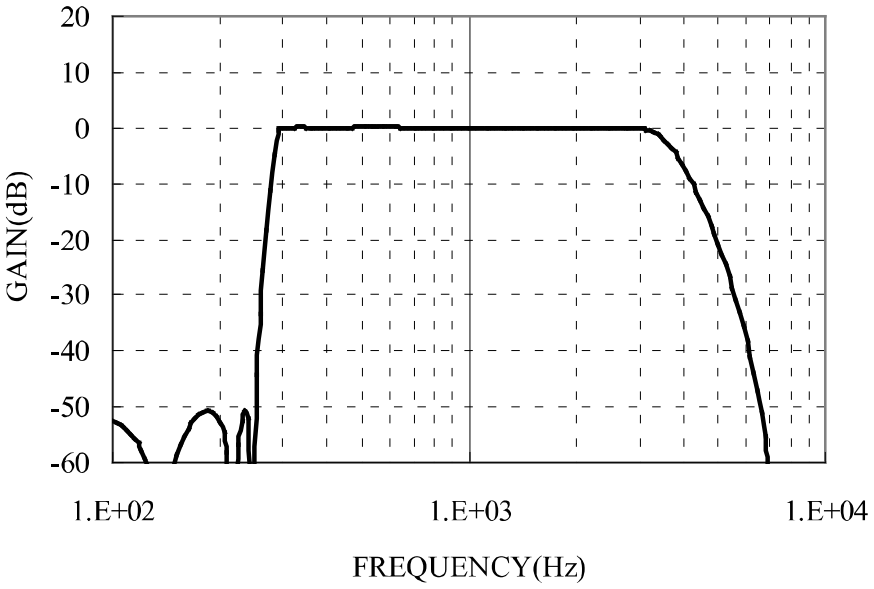


Figure 2: RX overall response without de-emphasis.

- Audio path frequency response (Emphasis:on)

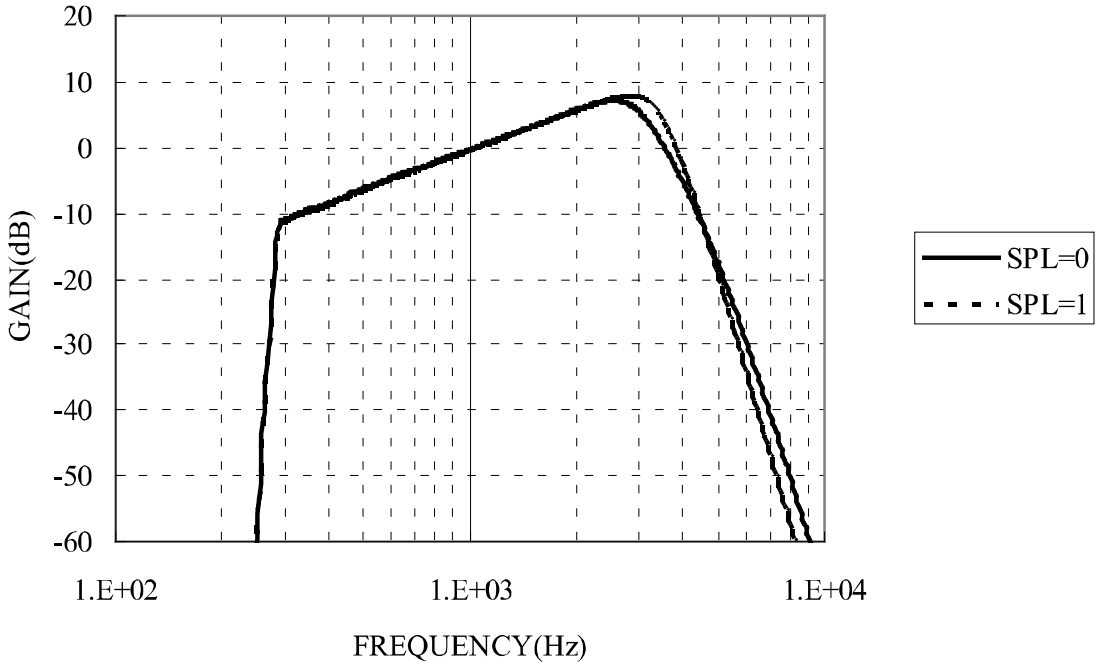


Figure 3: TX overall response with pre-emphasis.

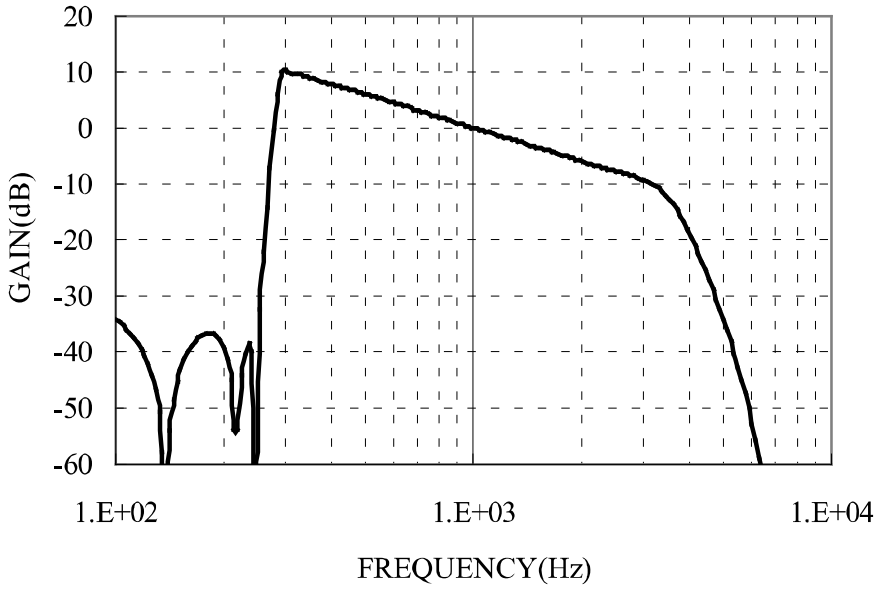


Figure 4: RX overall response with de-emphasis.

4) Scrambler Characteristics (Scrambler: **on**, Emphasis: off, Compandor: off)

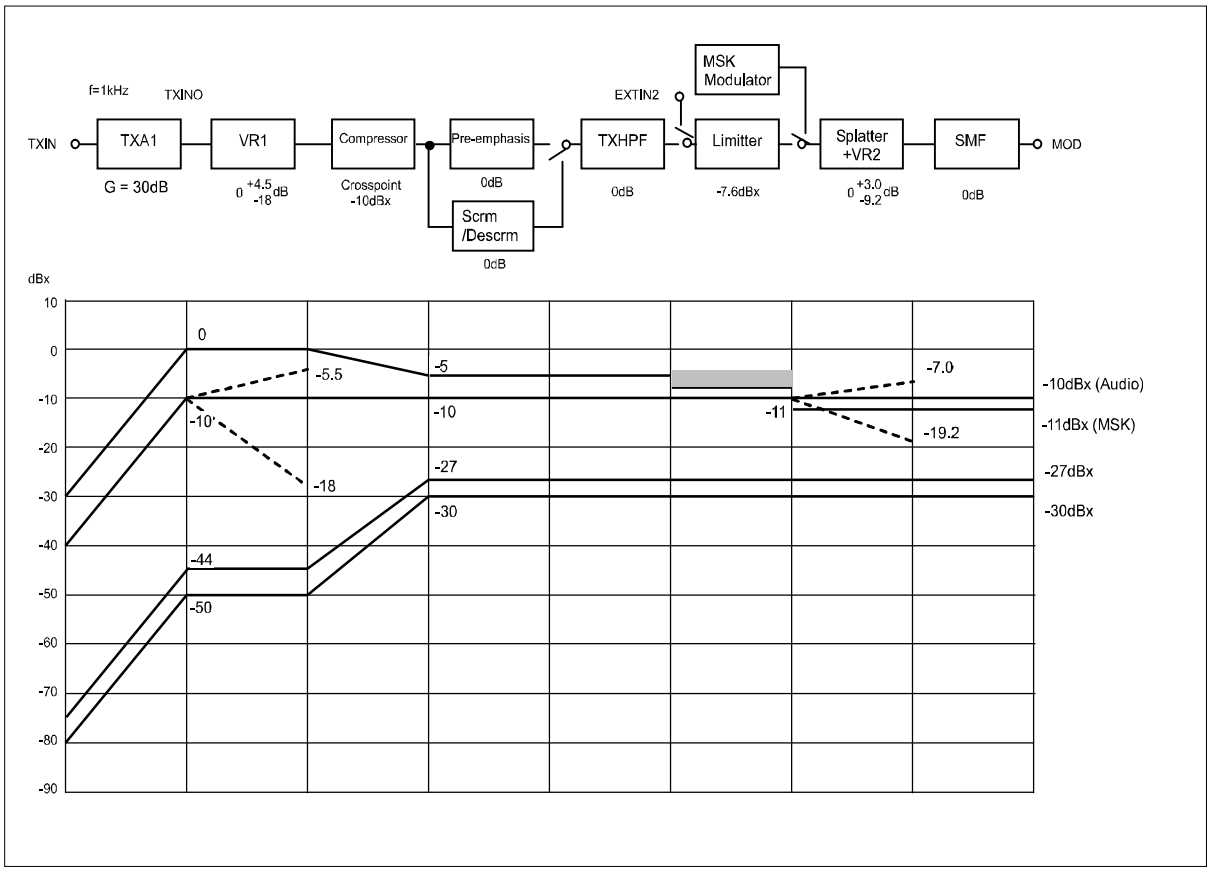
Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Carrier Frequency			3.388		kHz	
Modulated Output Level	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 2.388kHz	-12	-10	-8	dBx	
High Frequency Rejection Level	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 4.388kHz			-50	dBx	
Carrier Signal Leakage Level	TXINO to MOD, RXINO to RXOUT Input level No signal Measuring-freq. 3.388kHz			-50	dBx	
Original Signal Leakage Level	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 1.0kHz			-50	dBx	

5) MSK Modem Characteristics

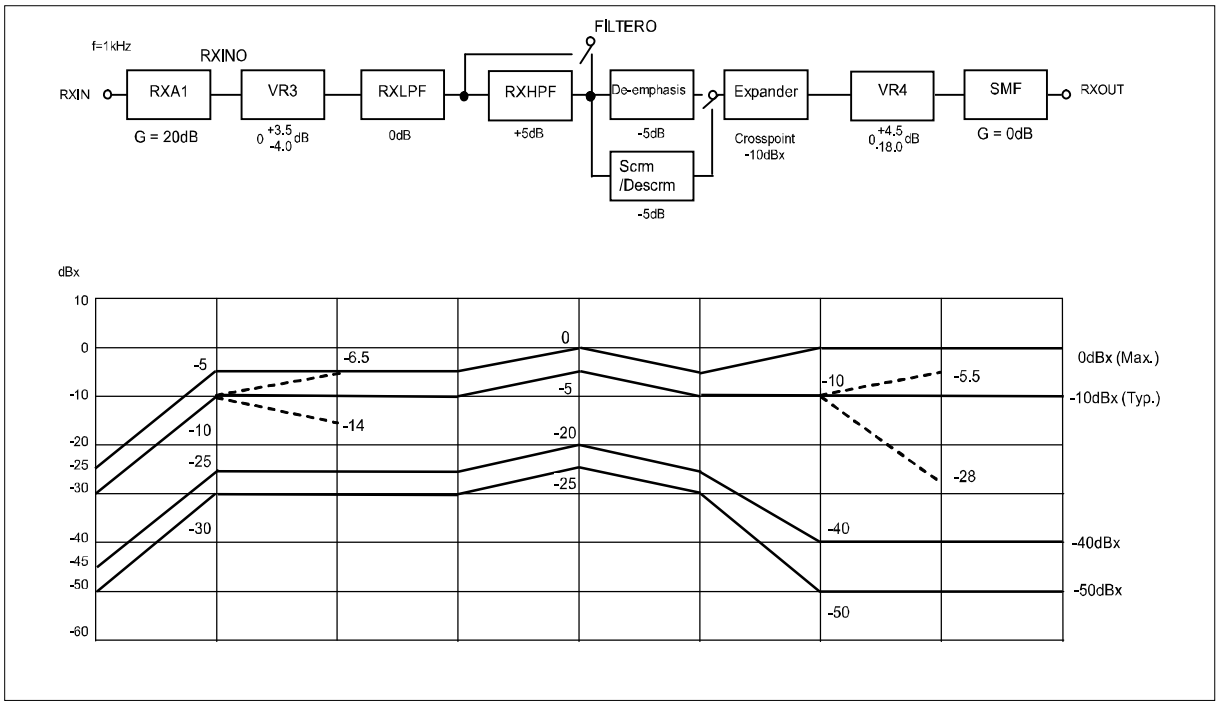
Parameter	Condition	Min.	Typ.	Max.	Units	Notes
TX Signal Level	@MOD 1.2kHz signal out	-12	-11	-10	dBx	
TX Signal Distortion	@MOD 1.2kHz signal out			-32	dB	
RX Signal Level	@RXINO 1.2kHz signal out	-17	-11	-1	dBx	

14. Level Diagram

1) TX audio system : *TXRX*=0



2) RX audio system : *TXRX*=1



"dBx" is standardized unit for 2.6V to 5.5V operation, 0dBx=-5+20log(VDD/2)dBm, 0dBm=0.775Vrms.

15. Serial Interface Configuration

1) Register Configuration

Address				Function	Data							
A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Control register 1	BS3	BS2	BS1	TXRX	TXINSW	TXSW2	TXSW1	TXSW0
0	0	0	1	Control register 2	FILSW1	FILSW0	RXSW	LIMSW	TC	EM	PCONT	SPL
0	0	1	0	Control register 3	0	TXA2PW	MSKSW1	MSKSW0	MSKSL	FCLN	FSL	HPFSW
0	0	1	1	Volume register 1	0	0	0	0	VR13	VR12	VR11	VR10
0	1	0	0	Volume register 2	0	0	VR25	VR24	VR23	VR22	VR21	VR20
0	1	0	1	Volume register 3	0	0	0	0	VR33	VR32	VR31	VR30
0	1	1	0	Volume register 4	0	0	VR45	VR44	VR43	VR42	VR41	VR40
0	1	1	1	Modem register 1	Lower 8 bit of Modem Flame pattern							
1	0	0	0	Modem register 2	Upper 8 bit of Modem Flame pattern							
1	0	0	1	Volume register 5	0	0	0	LIMLV4	LIMLV3	LIMLV2	LIMLV1	LIMLV0
1	0	1	0	Control register 4	0	0	0	0	SCR3	SCR2	SCR1	SCR0
1	0	1	1	Control register 5	0	0	0	0	0	MCKCNT	MCKSL1	MCKSL0
1	1	0	0	Software Reset	SRST[7:0]							
1	1	0	1	Test register 1	Test register 1 for LSI test operation (not accessible)							
1	1	1	0	Test register 2	Test register 2 for LSI test operation (not accessible)							
1	1	1	1	Test register 3	Test register 3 for LSI test operation (not accessible)							
				Modem register 3	Modem Receive data							

2) Register Map

2.1) Control Register 1

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	BS3	BS2	BS1	TXRX	TXINSW	TXSW2	TXSW1	TXSW0
Initial Value				0	0	0	1	1	1	1	1

2.1.1) Operation mode setting

BS3	BS2	BS1	Mode	OSC,AGND	TX, RX, Audio	Modem
0	0	0	Mode0(power OFF)	OFF	OFF	OFF
0	0	1	Mode1(Standby)	ON	OFF	OFF
0	1	0	Mode2	ON	ON	OFF
0	1	1	Mode3	ON	OFF	ON
1	0	0	Mode4	ON	ON	ON

Note : Do no set the combination of the code which is not defined in the table given above.

2.1.2) TX, RX Setting

Data	Function	Operation		Notes
		0	1	
TXRX	TX, RX Switch	TX Operation Note 1	RX Operation Note 2	Note 3
TXINSW	TX Signal	TXA1+TXA2 Operation	TXA1 Operation	Note 4

2.1.3) TX audio path setting

TXSW2	TXSW1	TXSW0	TX Audio	Modem	EXTINO Signal	EXTIN2 Signal
1	1	1	OFF	OFF	OFF	OFF
1	1	0	ON	OFF	OFF	OFF
1	0	1	OFF	ON	OFF	OFF
1	0	0	ON	OFF	ON	OFF
0	1	1	ON	OFF	OFF	ON
0	1	0	OFF	OFF	ON	OFF
0	0	1	OFF	OFF	OFF	ON

Note : Do no set the combination of the code which is not defined in the table given above.

Note 1: TXIN to RXOUT path is available by setting TXRX=0 and RXSW=1 in register.
However, Scrambler/Descrambler circuit does not work properly on this setting, so please set PCONT=1 (disable). To set RXSW=0 makes RXOUT pin mute in operation.

Note 2: RXIN to MOD path is available by setting
TXRX=1 and TXSW2/TXSW1/TXSW0=1/1/0 in register.
However, Scrambler/Descrambler circuit does not work properly on this setting, so please set PCONT=1 (disable). To set TXSW2/TXSW1/TXSW0=1/1/1 makes MOD pin mute in operation.

Note 3: Please set a gain level properly in each circuit block according to level diagram in page 16.

Note 4: In case of TXA1+TXA2 Operation (TXINSW=0),
please set the register to other than TXSW2/TXSW1/TXSW0=1/0/0 nor TXSW2/TXSW1/TXSW0=0/1/0

2.2) Control Register 2

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	FILSW1	FILSW0	RXSW	LIMSW	TC	EM	PCONT	SPL
Initial Value				1	1	1	1	1	1	1	1

FILSW1	FILSW0	Operation	Notes
1	1	FILTERO pin is mute	
0	1	RXLPF circuit signal to FILTERO pin	
0	0	TX/RX_HPF circuit signal to FILTERO pin	

Note : Do no set the combination of the code which is not defined in the table given above.

Data	Function	Operation		Notes
		0	1	
RXSW	RX Audio	mute	Normal operation	Note 5
LIMSW	Limiter	OFF (bypass)	ON (active)	
TC	Compressor/ Expander	OFF (bypass)	ON (active)	
SPL	Splatter cut-off frequency	2.55kHz	3.0kHz	

Note 5: FILTERO pin cannot be controlled by setting RXSW=0.

EM	PCONT	Operation	Notes
1	1	Emphasis : ON (enable) Scrambler : OFF(disable)	
0	1	Emphasis : OFF(disable) Scrambler : OFF(disable)	
0	0	Emphasis : OFF(disable) Scrambler : ON (enable)	

Note : Do no set the combination of the code which is not defined in the table given above.

2.3) Control Register 3

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	TXA2PW	MSKSW1	MSKSW0	MSKSL	FCLN	FSL	HPFSW
Initial Value				0	0	1	1	1	1	1	1

MSKSW1	MSKSW0	Operation		Notes
		MSKCLK pin	MSKDATA pin	
1	1	High output	High-Z Input High or Low	MSK transmission :OFF
0	1	TX clock (TCLK) is out put from MSKCLK pin.	TX data (MSKDATA) can be input from MSKDATA pin.	MSK transmission :ON
1	0	Rx clock (RCLK) is out put from MSKCLK pin.	RX data (RDATA) is output from MSKDATA pin.	
0	0	High output	RDF/FD signal is output from MSKDATA pin. Select MSK RX flag (RDF) and input clock to SCLK pin, then Rx data is output from DIO pin.	

Data	Function	Operation		Notes
		0	1	
TXA2PW	TXA2 power down control	TXA2 power down	TXA2 operation	However in case of mode0, TXA2 comes to power down.
MSKSL	Modem data rate	2400bit/s	1200bit/s	
FCLN	Modem flame detect	ON (enable)	OFF (disable)	
FSL	RDF/FD Switch	FD enable	RDF enable	
HPFSW	TX/RX_HPF	OFF (bypass)	ON (active)	

2.4) Volume Register 1

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	0	VR13	VR12	VR11	VR10
Initial Value				0	0	0	0	1	1	0	0

VR13	VR12	VR11	VR10	VR1 gain(dB)
0	0	0	0	-18.0
0	0	0	1	-16.5
0	0	1	0	-15.0
0	0	1	1	-13.5
0	1	0	0	-12.0
0	1	0	1	-10.5
0	1	1	0	-9.0
0	1	1	1	-7.5
1	0	0	0	-6.0
1	0	0	1	-4.5
1	0	1	0	-3.0
1	0	1	1	-1.5
1	1	0	0	0.0
1	1	0	1	+1.5
1	1	1	0	+3.0
1	1	1	1	+4.5

2.5) Volume Register 2

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	VR25	VR24	VR23	VR22	VR21	VR20
Initial Value				0	0	1	1	0	0	0	0

VR25	VR2 gain(dB)
0	-6.4
1	0.0

VR24	VR23	VR22	VR21	VR20	VR2 gain(dB)
0	0	0	0	0	-3.2
0	0	0	0	1	-3.0
0	0	0	1	0	-2.8
0	0	0	1	1	-2.6
0	0	1	0	0	-2.4
0	0	1	0	1	-2.2
0	0	1	1	0	-2.0
0	0	1	1	1	-1.8
0	1	0	0	0	-1.6
0	1	0	0	1	-1.4
0	1	0	1	0	-1.2
0	1	0	1	1	-1.0
0	1	1	0	0	-0.8
0	1	1	0	1	-0.6
0	1	1	1	0	-0.4
0	1	1	1	1	-0.2
1	0	0	0	0	0.0
1	0	0	0	1	+0.2
1	0	0	1	0	+0.4
1	0	0	1	1	+0.6
1	0	1	0	0	+0.8
1	0	1	0	1	+1.0
1	0	1	1	0	+1.2
1	0	1	1	1	+1.4
1	1	0	0	0	+1.6
1	1	0	0	1	+1.8
1	1	0	1	0	+2.0
1	1	0	1	1	+2.2
1	1	1	0	0	+2.4
1	1	1	0	1	+2.6
1	1	1	1	0	+2.8
1	1	1	1	1	+3.0

2.6) Volume Register 3

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	VR33	VR32	VR31	VR30
Initial Value				0	0	0	0	1	0	0	0

VR33	VR32	VR31	VR30	VR3 gain (dB)
0	0	0	0	-4.0
0	0	0	1	-3.5
0	0	1	0	-3.0
0	0	1	1	-2.5
0	1	0	0	-2.0
0	1	0	1	-1.5
0	1	1	0	-1.0
0	1	1	1	-0.5
1	0	0	0	0.0
1	0	0	1	+0.5
1	0	1	0	+1.0
1	0	1	1	+1.5
1	1	0	0	+2.0
1	1	0	1	+2.5
1	1	1	0	+3.0
1	1	1	1	+3.5

2.7) Volume Register 4

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	VR45	VR44	VR43	VR42	VR41	VR40
Initial Value				0	0	0	1	0	0	1	1

VR45	VR44	VR43	VR42	VR41	VR40	VR4 gain (dB)
0	0	0	0	0	0	-18.0
0	0	0	0	0	1	-4.50
0	0	0	0	1	0	-4.25
0	0	0	0	1	1	-4.00
0	0	0	1	0	0	-3.75
0	0	0	1	0	1	-3.50
0	0	0	1	1	0	-3.25
0	0	0	1	1	1	-3.00
0	0	1	0	0	0	-2.75
0	0	1	0	0	1	-2.50
0	0	1	0	1	0	-2.25
0	0	1	0	1	1	-2.00
0	0	1	1	0	0	-1.75
0	0	1	1	0	1	-1.50
0	0	1	1	1	0	-1.25
0	0	1	1	1	1	-1.00
0	1	0	0	0	0	-0.75
0	1	0	0	0	1	-0.50
0	1	0	0	1	0	-0.25
0	1	0	0	1	1	0.00
0	1	0	1	0	0	+0.25
0	1	0	1	0	1	+0.50
0	1	0	1	1	0	+0.75
0	1	0	1	1	1	+1.00
0	1	1	0	0	0	+1.25
0	1	1	0	0	1	+1.50
0	1	1	0	1	0	+1.75
0	1	1	0	1	1	+2.00
0	1	1	1	0	0	+2.25
0	1	1	1	0	1	+2.50
0	1	1	1	1	0	+2.75
0	1	1	1	1	1	+3.00
1	0	0	0	0	0	+3.25
1	0	0	0	0	1	+3.50
1	0	0	0	1	0	+3.75
1	0	0	0	1	1	+4.00
1	0	0	1	0	0	+4.25
1	0	0	1	0	1	+4.50

Note : Do no set the combination of the code which is not defined in the table given above.

2.8) Modem Register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	F07	F06	F05	F04	F03	F02	F01	F00
Initial Value				1	0	1	0	1	0	0	0
1	0	0	0	F15	F14	F13	F12	F11	F10	F09	F08
Initial Value				0	0	0	1	1	0	1	1

2.9) Volume Register 5

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	LIMLV4	LIMLV3	LIMLV2	LIMLV1	LIMLV0
Initial Value				0	0	0	0	1	0	1	1

LIMLV4	LIMLV3	LIMLV2	LIMLV1	LIMLV0	gain(dB)
0	0	0	0	0	5.5 (-2.1)
0	0	0	0	1	5.0 (-2.6)
0	0	0	1	0	4.5 (-3.1)
0	0	0	1	1	4.0 (-3.6)
0	0	1	0	0	3.5 (-4.1)
0	0	1	0	1	3.0 (-4.6)
0	0	1	1	0	2.5 (-5.1)
0	0	1	1	1	2.0 (-5.6)
0	1	0	0	0	1.5 (-6.1)
0	1	0	0	1	1.0 (-6.6)
0	1	0	1	0	0.5 (-7.1)
0	1	0	1	1	0 (-7.6dBx)
0	1	1	0	0	-0.5 (-8.1)
0	1	1	0	1	-1.0 (-8.6)
0	1	1	1	0	-1.5 (-9.1)
0	1	1	1	1	-2.0 (-9.6)
1	0	0	0	0	-2.5 (-10.1)
1	0	0	0	1	-3.0 (-10.6)
1	0	0	1	0	-3.5 (-11.1)
1	0	0	1	1	-4.0 (-11.6)
1	0	1	0	0	-4.5 (-12.1)
1	0	1	0	1	-5.0 (-12.6)
1	0	1	1	0	-5.5 (-13.1)
1	0	1	1	1	-6.0 (-13.6)
1	1	0	0	0	-6.5 (-14.1)
1	1	0	0	1	-7.0 (-14.6)
1	1	0	1	0	-7.5 (-15.1)
1	1	0	1	1	-8.0 (-15.6)
1	1	1	0	0	-8.5 (-16.1)
1	1	1	0	1	-9.0 (-16.6)
1	1	1	1	0	-9.5 (-17.1)
1	1	1	1	1	-10.0 (-17.6)

2.10) Control Register 4

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	0	SCR3	SCR2	SCR1	SCR0
Initial Value				0	0	0	0	1	1	0	1

SCR3	SCR2	SCR1	SCR0	Carrier Frequency (kHz)
0	0	0	0	2.844
0	0	0	1	2.880
0	0	1	0	2.916
0	0	1	1	2.954
0	1	0	0	2.992
0	1	0	1	3.032
0	1	1	0	3.072
0	1	1	1	3.114
1	0	0	0	3.156
1	0	0	1	3.200
1	0	1	0	3.245
1	0	1	1	3.291
1	1	0	0	3.339
1	1	0	1	3.388
1	1	1	0	3.439
1	1	1	1	3.491

2.11) Control Register 5

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	MCKCNT	MCKSL1	MCKSL0
Initial Value				0	0	0	0	0	1	1	1

Data	Function	Operation		Notes
		0	1	
MCKCNT	External input switch	External input	a crystal oscillator (14.7456MHz)	

MCKSL1	MCKSL0	Operation	Notes
0	0	Master Clock: 3.6864MHz	External input only
1	0	Master Clock: 7.3728MHz	External input only
0	1	Master Clock: 11.0592MHz	External input only
1	1	Master Clock: 14.7456MHz	

Note : Set MSKSL[1:0] register when Mode0 or Mode1.

2.12) Software Reset Register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	SRST[7:0]							
Initial Value				0	0	0	0	0	0	0	0

When data 0xAA:10101010 is written to the SRST[7:0] register, software reset is performed.
Refer to "System Reset" for further information.

2.13) Modem receive data register

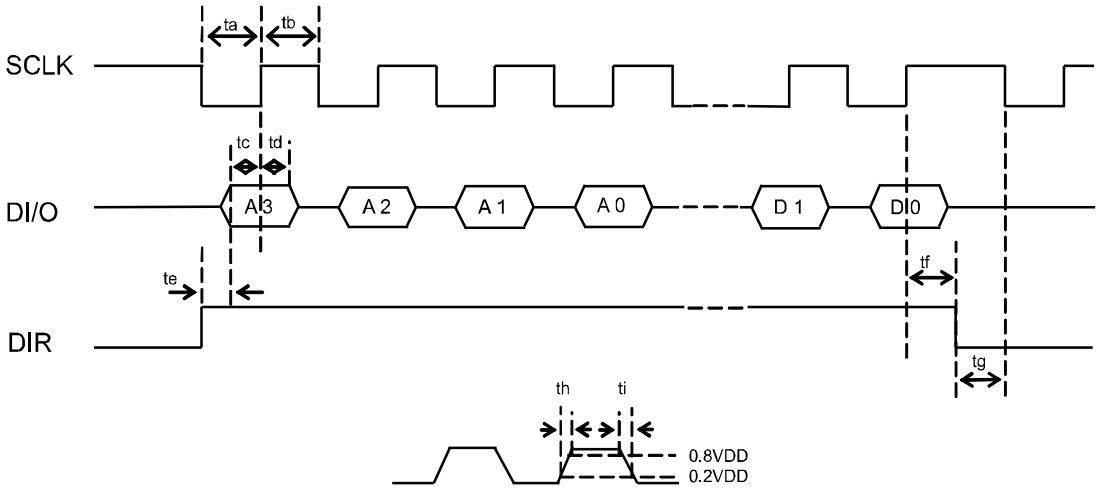
Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Data	Function	MSK receive data		Notes
		0	1	
RD7 to 0	MSKSL=0	2.4kHz	1.2kHz	Data received first is RD7.
	MSKSL=1	1.8kHz	1.2kHz	

16. Digital AC Timing

1) Serial Interface Timing

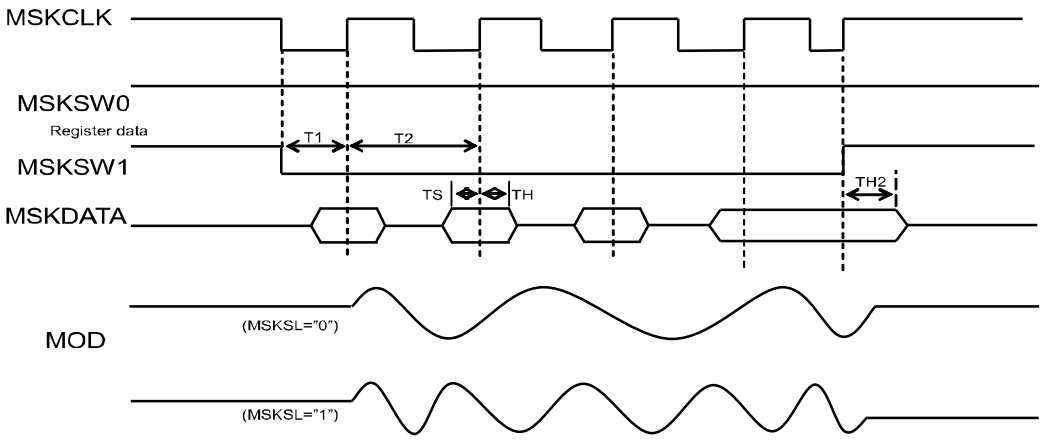
Parameter	Symbol	Min.	Typ.	Max.	Units
Clock pulse width 1 Clock pulse width 2	ta tb	500 500			ns
DIO Set up time DIO Hold time	tc td	100 100			ns
DIR Set up time DIR Hold time DIR Falling to SCLK Falling time	te tf tg	100 100 100			ns
SCLK Input rising time SCLK Input falling time	th ti			100 100	ns



SCLK waveform

2) MSK Modulator Timing

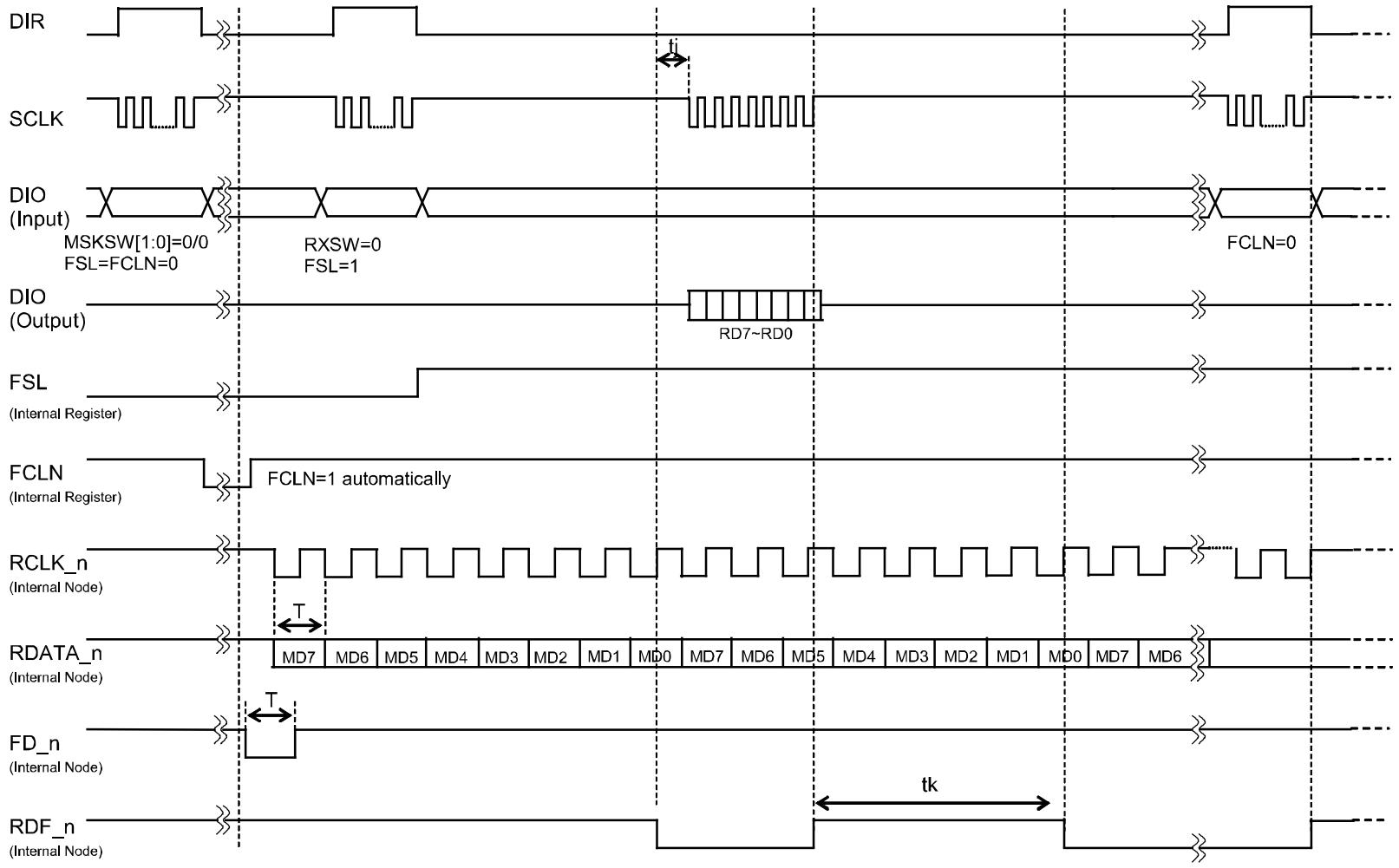
Parameter	Symbol	Min.	Typ.	Max.	Units
MSKSW1 Falling to MSKCLK Rising MSKSL="0" MSKSL="1"	T1		208.3 416.7		us
MSKCLK Period MSKSL="0" MSKSL="1"	T2		416.7 833.3		us
MSKDATA Set up time MSKDATA Hold time MSKDATA Hold time2	TS TH TH2	1 1 2			us



Note: The timing of setting the internal registers TXSW1 and TXSW2 is synchronized with the falling edge of DIR pin.

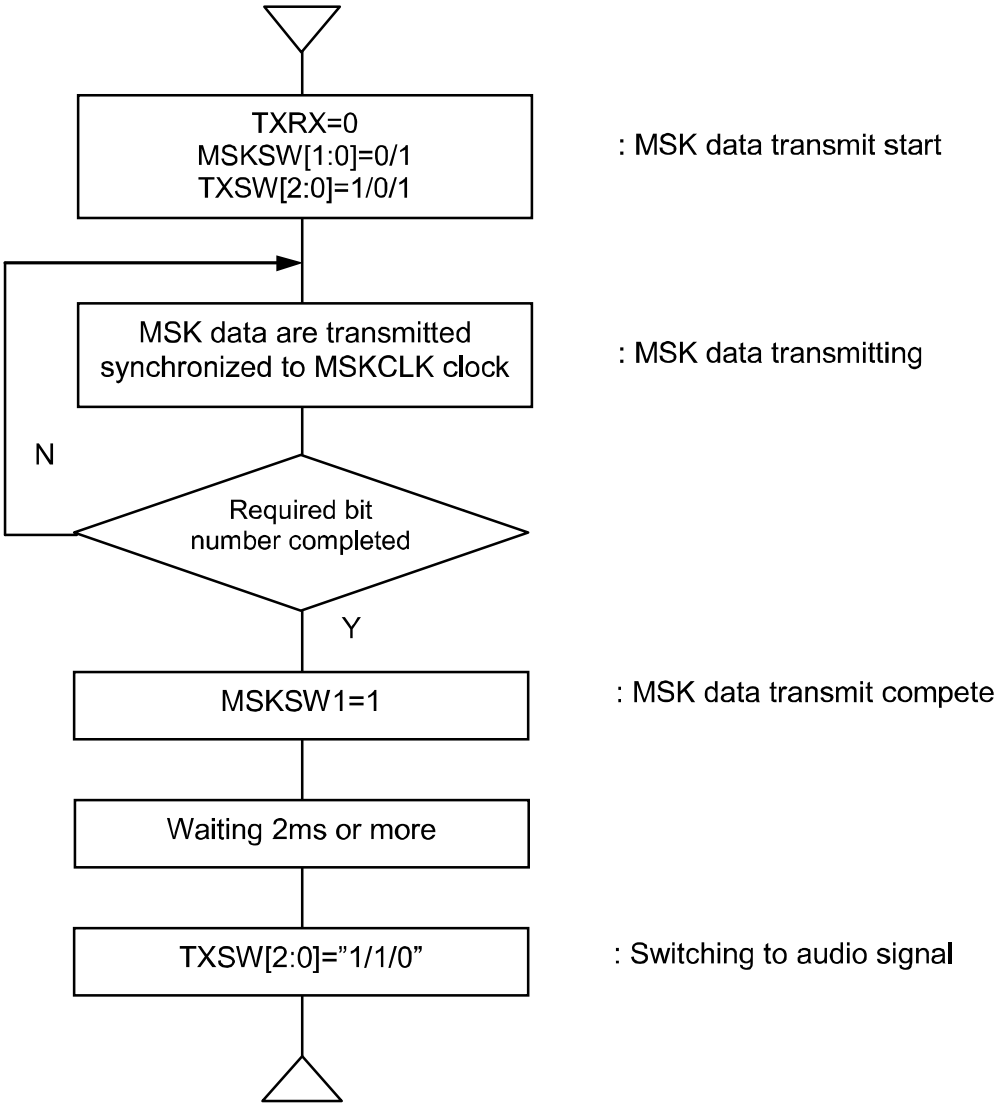
3) MSK Demodulator Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
RCLK Period and FD pulse width MSKSL="0" MSKSL="1"	T		416.7 833.3		us
RDF Falling to SCLK Falling time SCLK Rising to RDF Falling time	tj tk	100 600			ns


DIR
ti
SCLK
DIO
(Input)
MSKSW[1:0]=0/0
FSL=FCLN=0
RXSW=0
FSL=1
FCLN=0
DIO
(Output)
RD7~RD0
FSL
(Internal Register)
FCLN
(Internal Register)
FCLN=1 automatically
RCLK_n
(Internal Node)
T
RDATA_n
(Internal Node)
MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0 MD7 MD6
T
FD_n
(Internal Node)
tk
RDF_n
(Internal Node)

17. MSK Modem Description

1) MSK Modulator control flow
MSK data transmitter, Modulator interfaces with MSKCLK, MSKDATA and MOD pins and also TXRX, TXSW2, TXSW1, TXSW0, MSKSW1 and MSKSW0 register as below.

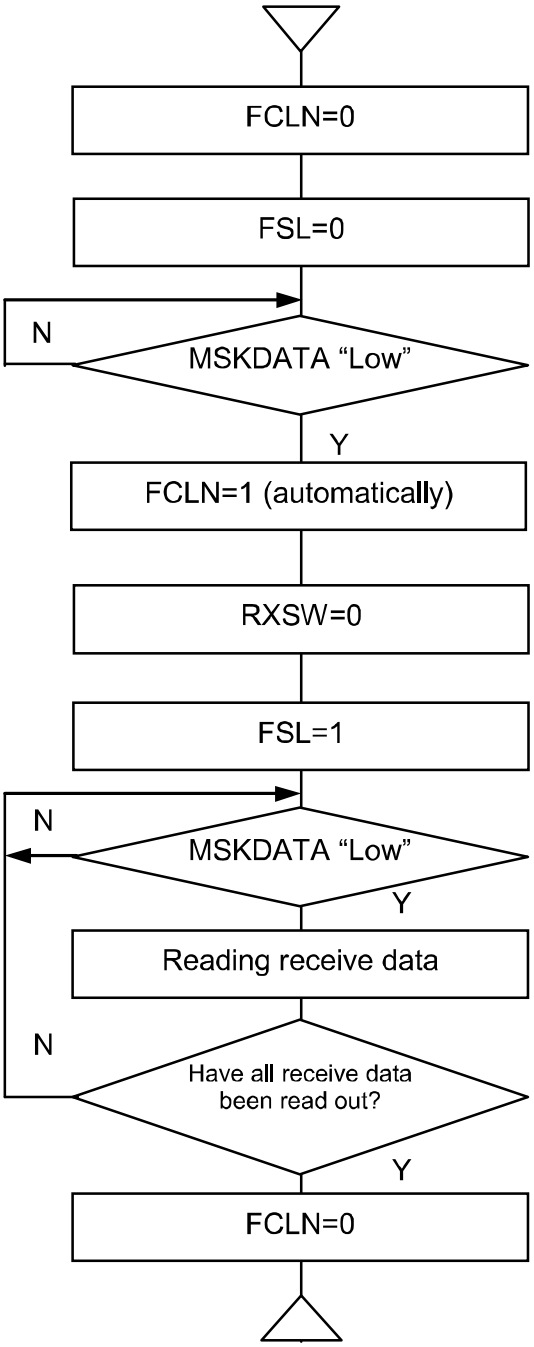


(1) Setting TXRX=0, MSKSW1=0, MSKSW0=1, TXSW2=1 and TXSW1=0, MSK data transmit is provided.
(2) A 1200/2400Hz clock is put out from MSKCLK pin. Synchronizing with the rising edge of MSKCLK,
AK2346A reads the MSK transmit data from MSKDATA pin and puts out them to MOD pin.
(3) After transmitting the necessary bit number, please set MSKSW1=1
(4) Afterwards, before switching to audio signal mode, please wait for at least 2ms after setting MSKSW1=1 to complete sending the MSK data final data bit transmit. Then set TXSW[2:0]="1/1/0".

2) MSK Demodulator control flow

2.1) When frame detection is used

MSK data receiver, Demodulator interfaces with RXIN, MSKDATA, SCLK, DIO and DIR pins and also FSL, RXSW and FCLN registers as below.



: Setting flame detect (FD) enable

: Setting for FD signal put out from MSKDATA pin.

: Synchronized frame pattern detect or not ?

: FD is disable automatically

: Receive audio mute

: Setting for received flag (RDF) signal put out from MSKDATA pin.

: 8 bit data received or not ?

: Having read 8bit data, MSKDATA pin puts out high level.

: Waiting for the next synchronized flame.

(1) Set MSKSW1=0 and MSKSW0=0 for flame detect mode.

(2) Setting FCLN=0 and FSL=0 and also SCLK pin sets high level and DIR pin sets low level, MSKDATA pin puts out high level and wait for synchronized frame.

(3) After a synchronized frame is detected, MSKDATA pin works as frame detect (FD) mode. FD goes to low level during the period of time "T", then FCLN is sets to "1" automatically.

(4) Monitoring low level of MSKDATA pin, set RXSW=0 for audio signal mute. Then set FSL=1 for received flag (RDF), signal put out from MSKDATA pin.

(5) After 8 bit received data (MD7…0) have been entered to the internal buffer from node RDATA, MSKDATA pin goes to low level as RDF mode.

(6) After CPU detects this low level at MSKDATA pin, please puts in 8 clock to SCLK pin. Then modulated data (RD7…0) put out from DIO pin synchronized with falling edge of SCLK clock.

(7) After 8 clock have been put into SCLK pin completely, MSKDATA pin goes to high level that shows all modulated data coming from DIO pin.

(8) By repeating the steps (5), (6), (7), the data come out from DIO pin continuously.

(9) After the necessary data have been read, DIR pin sets to high level and FCLN=0. Then internal node RCLK and RDATA are set to "1" for initializing and system waits for the next synchronization frame data.

This frame detection circuit does not have reset function. In case of stopping the sequence during the steps (1) to (8), please set again from the first step (1). Especially, when MSKDATA pin goes out low level on frame detecting, FCLN register is sets to "1" automatically as written in (2). If you set FCLN=0 during this operation, the date set "0" is ignored. So please set the data again after MSKDATA pin puts out high level.

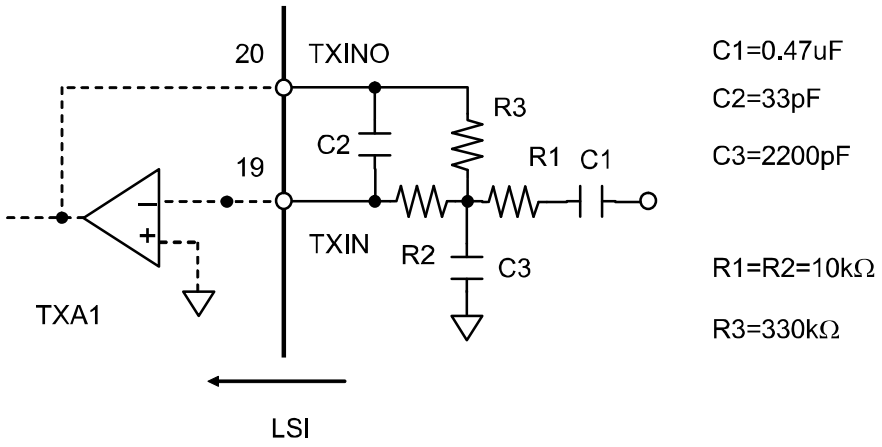
2.2) When frame detection is not used

(1) When frame detection is not used, set MSKSW1 to 1 and MSKSW0 to 0 to start MSK reception.
(2) When the MSK signal is received on the RXIN pin, demodulated data is output successively on the MSKDATA pin via MSK-BPF and MSK-Demodulator in synchronization with the falling edge of the 1200Hz or 2400Hz clock signal output on the MSKCLK pin.
(3) Setting MSKSW1=1 and MSKSW0=1, reception mode comes to a stop. High level is output on the MSKDATA pin and MSKSW0 comes to High-Z. At this time input High level or Low level to MSKDATA pin.

18. Recommended External Application Circuits

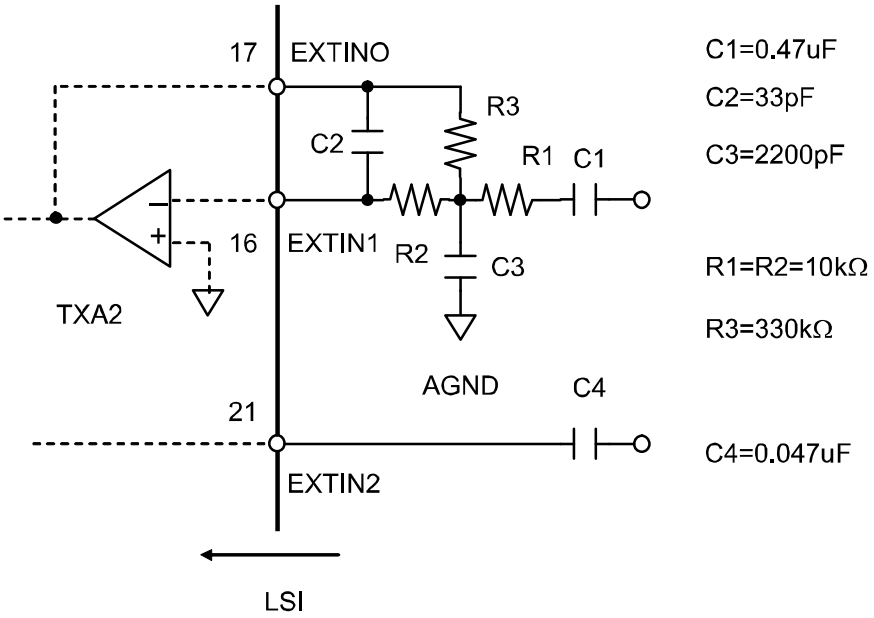
1) TXA1 Amplifier

This is an operational amplifier required for typical transmit microphone. The gain should be less than 30dB. To eliminate high frequency noise component over than 100kHz from input signal, please compose 1st or 2nd order anti-aliasing filter. The following simplified schematic shows an example of 2nd order anti-aliasing filter that has 30dB gain and 10kHz cut-off frequency.



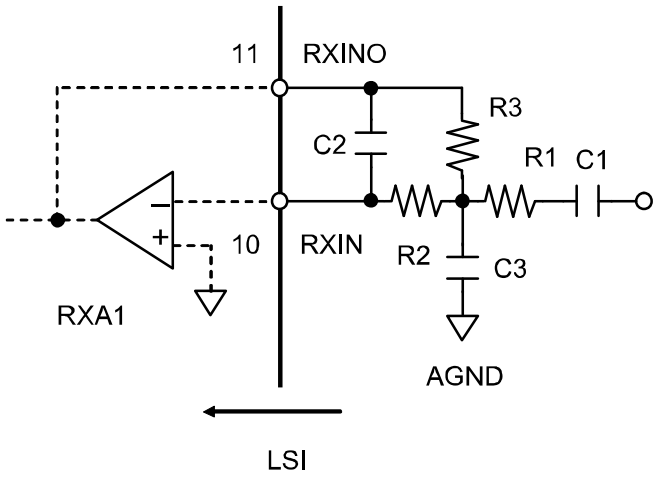
2) TXA2 amplifier

This amplifier is used for adjusting the gain of the external tone signal. The gain should be less than 30dB. To eliminate high frequency noise component over than 100kHz from input signal, please compose 1st or 2nd order anti-aliasing filter. The following simplified schematic shows an example of 2nd order anti-aliasing filter that has 30dB gain and 10kHz cut-off frequency.



3) RXA1 Amplifier

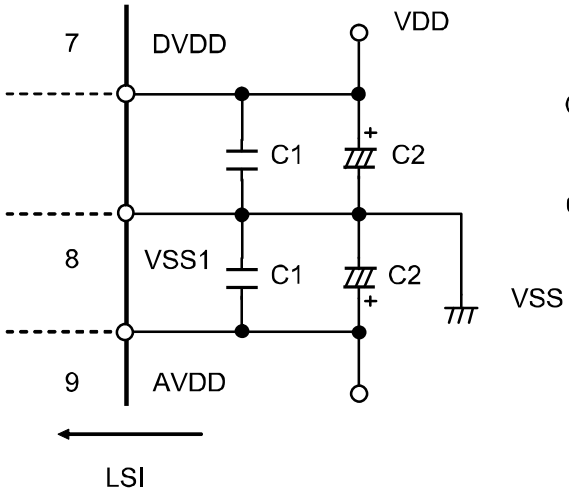
This is an operational amplifier suitable for receive gain adjuster and anti-aliasing filter to eliminate high frequency noise component over 100kHz The gain should be less than 20dB. The following simplified schematic shows an example of 2nd order anti-aliasing filter that has 20dB gain and 39kHz cut-off frequency.



C1=0.47uF
C2=33pF
C3=560pF
R1=10kΩ
R2=9.1kΩ
R3=100kΩ

4) Power supply stabilizing capacitors

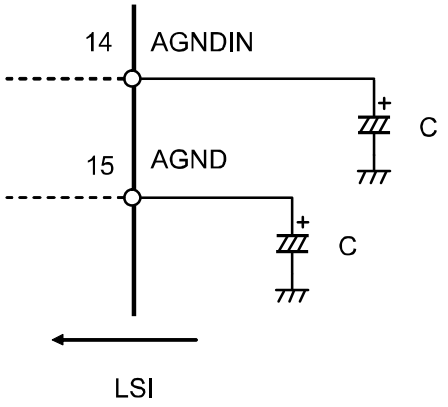
To connect capacitors between VDD and VSS pin reduce the ripple and noise included in power supply. These capacitors are mounted close to the device pins.



C1=0.1μF (Ceramic cap)
C2=10μF (Electrolytic cap)

5) AGND, AGNDIN pin stabilizing

Please decouple to VSS level by the 0.3uF or larger capacitor. These capacitors are mounted close to the device pins.



C=1μF (Electrolytic capacitor)

6) Clock Generation

The clock source can be chosen from either built-in crystal oscillator circuit or externally supplied.

When the built-in oscillator circuit is used, connect a 14.7456MHz crystal oscillator, a resistor, and capacitors as shown in Fig. 1. AK2346A is designed to get a stable oscillation for the electrical equivalent circuitry of quartz crystal unit: resonance resistance≤80Ω(Max.) and shunt capacitance≤1.5pF(Max.). It is recommended that external 12pF capacitors should be connected so that the total load capacitance does not exceed the load capacitance≤6pF (1.5pF+12pF//12pF) or less. These external components are mounted as close to the device pins as possible.

When a clock signal is supplied externally, not only 3.6864MHz but also 7.3728MHz (twice higher than 3.6864MHz), 11.0592MHz (three times higher than 3.6864MHz), and 14.7456MHz (four times higher than 3.6864MHz) are supported. However, the internal frequency must always be set to 3.6864MHz by selecting division by 2, 3, or 4 for the divider in the subsequent stage. Connect the clock signal as shown in Fig. 2 or Fig. 3 according to the clock amplitude level.

The circuit in the first stage of the XIN pin has a constant threshold voltage (0.8V). Therefore, if the high level of the input clock is 1.5V or higher and the low level is 0.5V or lower, connect the clock signal as shown in Fig. 2. If the input clock amplitude (p-p value) is between 0.2V and 1.0V, connect the clock signal as shown in Fig. 3.

When the clock is to be shared with peripheral ICs, the clock must be input and output on the XIN pin. The clock amplitude must not exceed the absolute maximum rating.

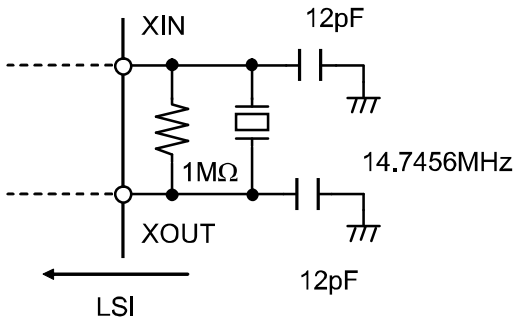


Fig. 1

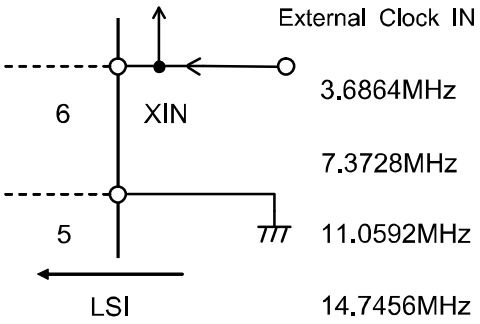


Fig. 2

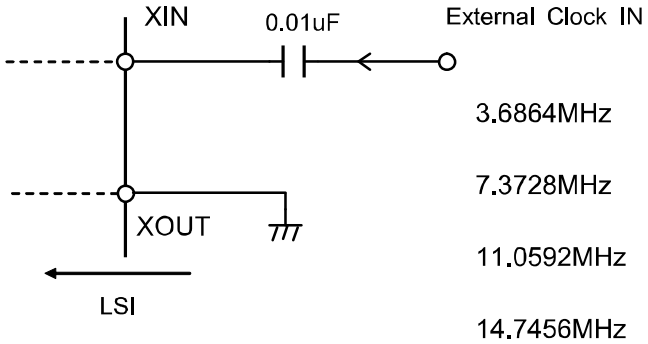
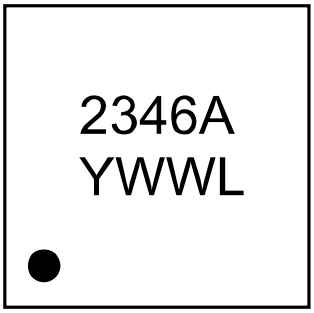


Fig. 3

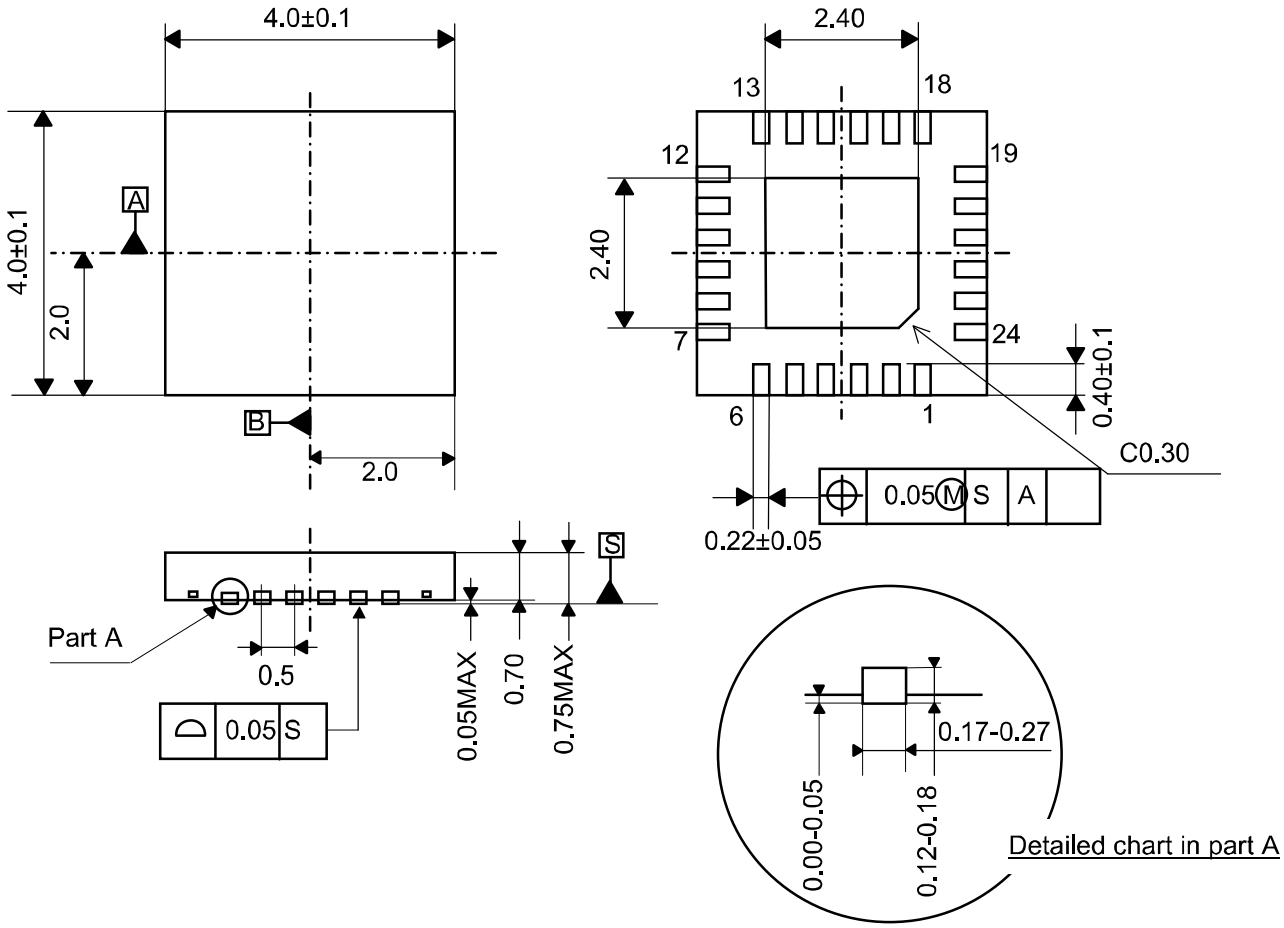
19. Packaging

- Marking



[Contents of XXXYZ]
Y : Date of manufacturing, Last digit of the year
WW : Date of manufacturing, 2 digits of week number
L : Production lot number

- 24-pin QFNJ Mechanical Outline (4.0 x 4.0 x 0.75mm, 0.5mm pitch)



Note: The exposed pad at the center of the back of the package must be connected to VSS or opened.

20. Important Notice

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