FAIRCHILD

SEMICONDUCTOR ™

DM74AS280
9-Bit Parity Generator/Checker

General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

The AS280 can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the AS280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and no internal connection at pin 3. This permits the AS280 to be substituted for the '180 in existing designs to produce identical function even if 'AS280s are mixed with existing '180s.

Features

- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for N-bits
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range

Connection Diagram

Dual-In-Line Package
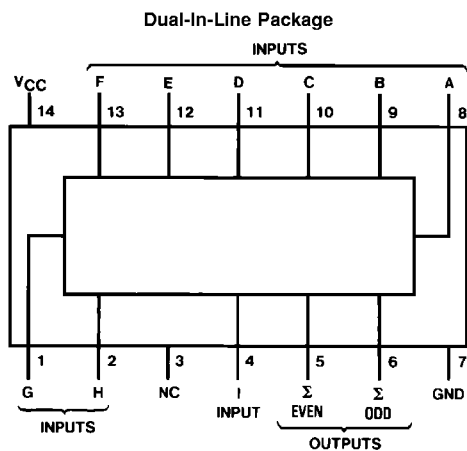
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Order Number DM74AS280M
or DM74AS280N
See Package Number M14A or N14A

Function Table

Number of Inputs (A thru I) that are High	Outputs	
	ΣEven	ΣOdd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

L = Low State
H = High State

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C

Storage Temperature Range	−65°C to +150°C
Typical θ$_{JA}$	
N Package	77.0°C/W
M Package	108.0°C/W

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V$_{CC}$	Supply Voltage	4.5	5	5.5	V
V$_{IH}$	High Level Input Voltage	2			V
V$_{IL}$	Low Level Input Voltage			0.8	V
I$_{OH}$	High Level Output Current			−2	mA
I$_{OL}$	Low Level Output Current			20	mA
T$_A$	Free-Air Operating Temperature	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

Over recommended free-air temperature range. All typical values are measured at V$_{CC}$ = 5V, T$_A$ = 25°C.

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
V$_{IK}$	Input Clamp Voltage	V$_{CC}$ = 4.5V, I$_I$ = −18 mA			−1.2	V
V$_{OH}$	High Level Output Voltage	I$_{OH}$ = −2 mA, V$_{CC}$ = 4.5V to 5.5V	V$_{CC}$ − 2			V
V$_{OL}$	Low Level Output Voltage	V$_{CC}$ = 4.5V, I$_{OL}$ = Max		0.35	0.5	V
I$_I$	Input Current @ Max Input Voltage	V$_{CC}$ = 5.5V, V$_{IH}$ = 7V			0.1	mA
I$_{IH}$	High Level Input Current	V$_{CC}$ = 5.5V, V$_{IH}$ = 2.7V			20	µA
I$_{IL}$	Low Level Input Current	V$_{CC}$ = 5.5V, V$_{IL}$ = 0.4V			−0.5	mA
I$_O$	Output Drive Current	V$_{CC}$ = 5.5V, V$_O$ = 2.25V	−30		−112	mA
I$_{CC}$	Supply Current	V$_{CC}$ = 5.5V		25	40	mA

Switching Characteristics

over recommended operating free air temperature range (Note 2)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t$_{PLH}$	Propagation Delay Time, Low to High Level Output	V$_{CC}$ = 4.5V to 5.5V, C$_L$ = 50 pF, R$_L$ = 500Ω	Data	ΣEven	3	12	ns
t$_{PHL}$	Propagation Delay Time, High to Low Level Output				3	11	ns
t$_{PLH}$	Propagation Delay Time, Low to High Level Output		Data	ΣOdd	3	12	ns
t$_{PHL}$	Propagation Delay Time, High to Low Level Output				3	11.5	ns

Note 2: See Section 5 for test waveforms and output load.

## Logic Diagram
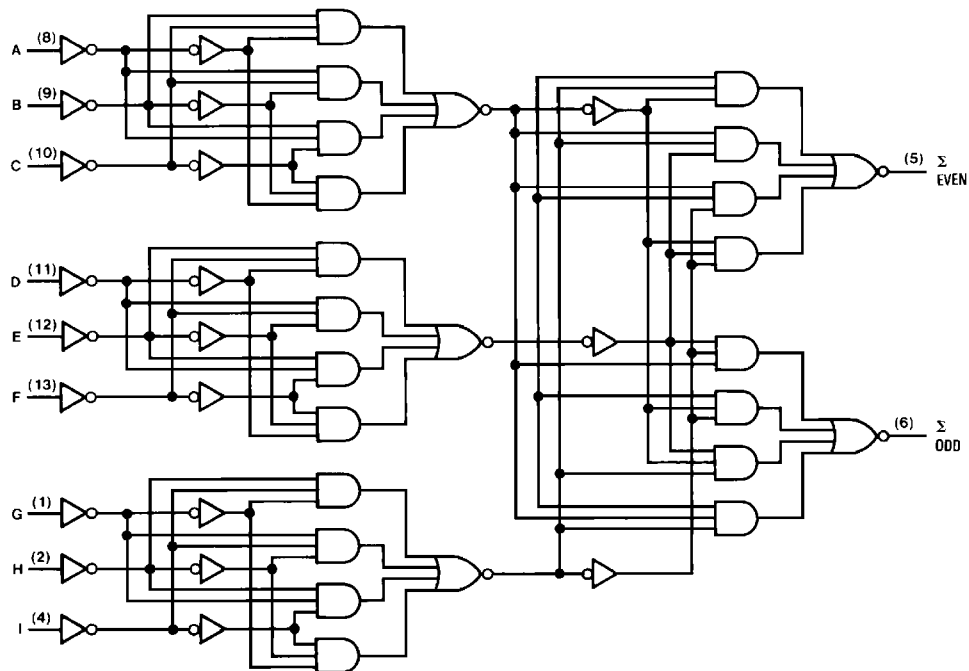
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Typical Applications

Three AS280s can be used to implement a 25-line parity generator/checker.

As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (AS86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.
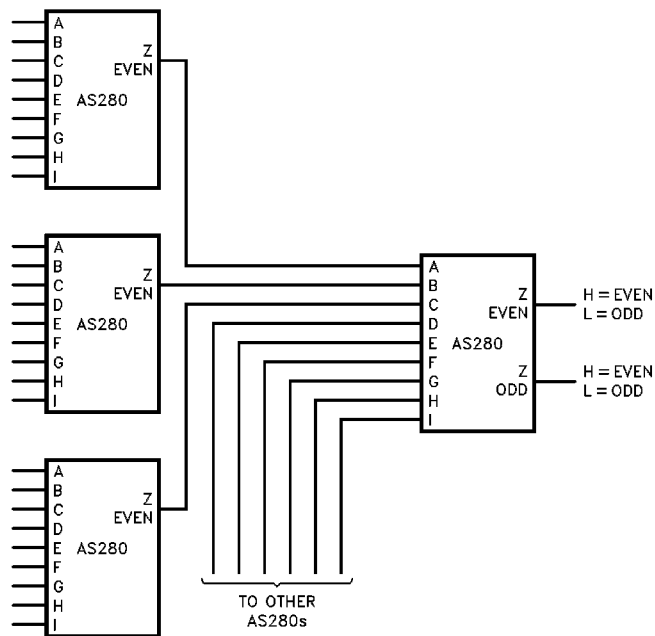
Longer word lengths can be implemented by cascading AS280s. As shown in *Figure 2*, parity can be generated for word lengths up to 81 bits.

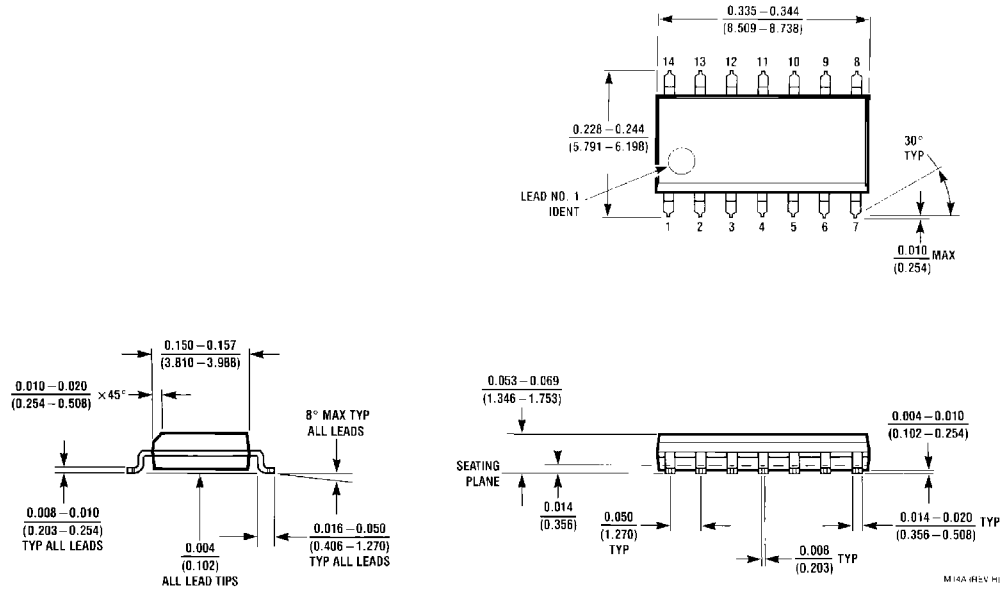## Typical Applications (Continued)
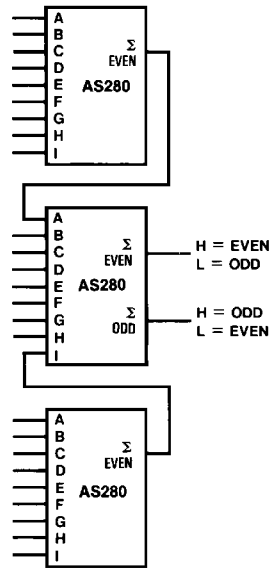
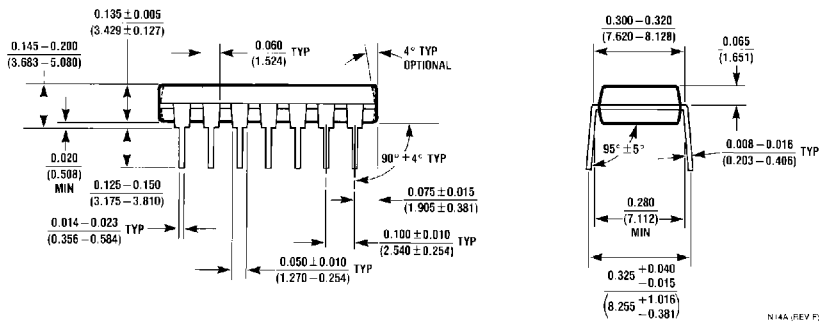DS006303-3

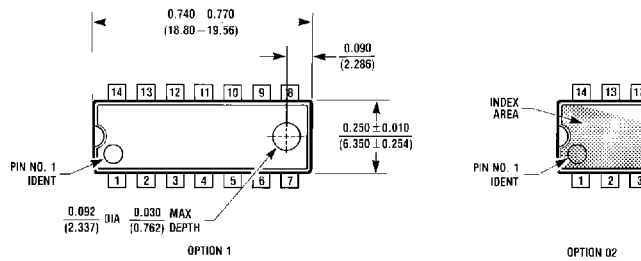**FIGURE 1. 25-Line
Parity/Generator Checker**

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FIGURE 2. 81-Line Parity/Generator Checker

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

LEAD NO. 1
IDENT

30°
TYP

1 2 3 4 5 6 7

0.010
(0.254) MAX

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)

S.O. Package (M)
Order Number DM74AS280M
Package Number M14A

0.740 0.770
(18.80 − 19.56)

0.090
(2.286)

14 13 12 11 10 9 8

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7

0.092
(2.337) DIA

0.030
(0.762) MAX DEPTH

OPTION 1

INDEX
AREA

14 13 12

PIN NO. 1
IDENT

1 2 3

OPTION 02

0.135 ± 0.005
(3.429 ± 0.127)

0.145 − 0.200
(3.683 − 5.080)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.020
(0.508)
MIN

0.125 − 0.150
(3.175 − 3.810)

90° + 4° TYP

0.014 − 0.023
(0.356 − 0.584) TYP

0.075 ± 0.015
(1.905 ± 0.381)

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.050 ± 0.010
(1.270 − 0.254) TYP

0.300 − 0.320
(7.620 − 8.128)

0.065
(1.651)

95° ± 5°

0.008 − 0.016
(0.203 − 0.406) TYP

0.280
(7.112)
MIN

0.325 +0.040
−0.015

(8.255 +1.016
−0.381)

N14A (REV F)

Molded Dual-In-Line Package (N)
Order Number DM74AS280N
Package Number N14A

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