# High Speed CMOS 9-Bit Parity Generator/Checker

**QS54/74FCT280T**

**QS54/74FCT1280T**

## FEATURES/BENEFITS

- QSFCT280BT faster than FAST™
- QSFCT1280T has I8 enable, registered outputs
- $I_{OL}$ = 48 mA COM, 32 mA MIL
- TTL-compatible input and output levels
- Military product compliant with MIL-STD 883
- 6.3 ns delay, Ix to $\Sigma$e for QSFCT280BT
- 2 ns setup, Ix to reg clock for QSFCT1280BT
- CMOS power levels <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- JEDEC standard pinouts

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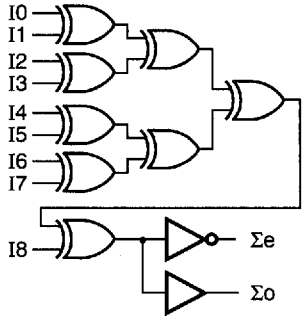
## DESCRIPTION

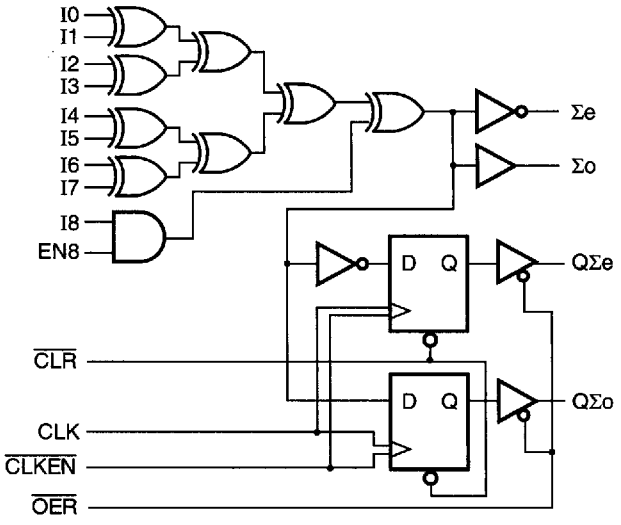
The QSFCT280/AT/BT and QSFCT1280/AT/BT are high-speed CMOS TTL-compatible 9-bit parity generator-checkers. Both odd and even parity outputs are available for generating or checking odd or even parity. The 1280 has I8 enable for parity bit generation and registered odd and even outputs for parity check on the following cycle. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

## FUNCTIONAL BLOCK DIAGRAM

**FCT280**

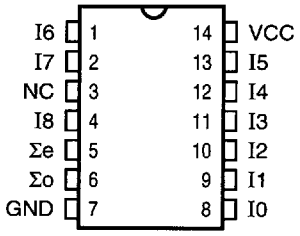



**FCT1280**

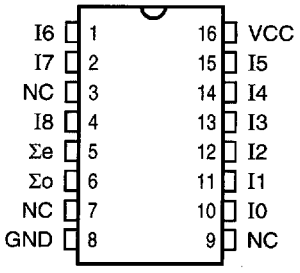


## FCT280 PIN CONFIGURATIONS (All Pins Top View)

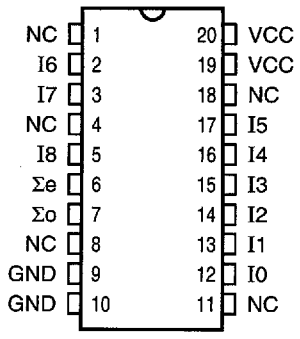
**DIP, SOIC**




**QSOP**

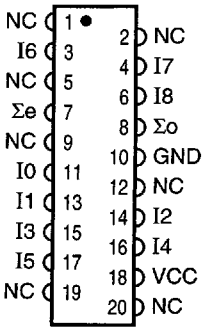



**HQSOP**




**Note:**
14-Pin SOIC is 150 mil wide (package code S1).

**ZIP**




## PIN DESCRIPTION

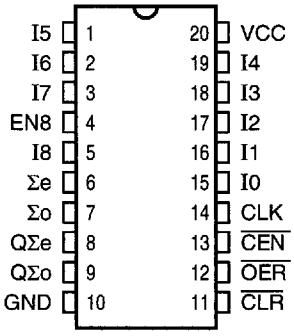
| Name | I/O | Description |
|---|---|---|
| I8-I0 | I | Data Inputs |
| Σe | O | Even Parity Out |
| Σo | O | Odd Parity Out |

## FUNCTION TABLE

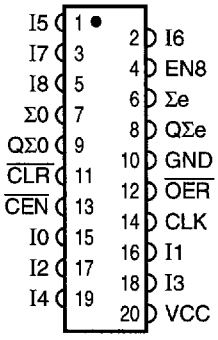
| Inputs I8-I0 | Outputs Σ even | Outputs Σ odd | Function |
|---|---|---|---|
| Number of Bits at TTL High = 0,2,4,6,8 | H | L | Parity is Even |
| Number of Bits at TTL High = 1,3,5,7,9 | L | H | Parity is Odd |

## FCT1280 PIN CONFIGURATIONS (All Pins Top View)

**PDIP, SOIC, QSOP, HQSOP**




**ZIP**

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## PIN DESCRIPTION

| Name | I/O | Description |
|---|---|---|
| I8-I0 | I | Data Inputs |
| EN8 | I | Enable I8 |
| CLK | I | Clock |
| $\overline{CEN}$ | I | Clock Enable |
| $\overline{CLR}$ | I | Clear |
| $\overline{OER}$ | I | Reg. Out Enable |
| Σe | O | Even Parity Out |
| Σo | O | Odd Parity Out |
| QΣe | O | Reg. Even Parity |
| QΣo | O | Reg. Odd Parity |

## FUNCTION TABLE

| Inputs I7-I0 | Inputs I8 | Inputs EN8 | Outputs Σe | Outputs Σo |
|---|---|---|---|---|
| Number of Bits at TTL High = 0,2,4,6,8 | X | L | H | L |
| | L | H | H | L |
| | H | H | L | H |
| Number of Bits at TTL High = 1,3,5,7,9 | X | L | L | H |
| | L | H | L | H |
| | H | H | H | L |

| Inputs $\overline{OER}$ | Inputs $\overline{CEN}$ | Inputs $\overline{CLR}$ | Inputs CLK | Outputs QΣe | Outputs QΣo | Function |
|---|---|---|---|---|---|---|
| H | X | X | X | Hi-Z | Hi-Z | Disable |
| L | X | L | X | L | L | Clear |
| L | H | H | ↑ | QΣen-1 | QΣon-1 | No Change |
| L | L | H | ↑ | Σen-1 | Σon-1 | Load Σe,Σo |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage to Ground | –0.5V to +7.0V |
| DC Output Voltage $V_{OUT}$ | –0.5V to +7.0V |
| DC Input Voltage $V_{IN}$ | –0.5V to +7.0V |
| AC Input Voltage (for a pulse width ≤ 20 ns) | –3.0V |
| DC Input Diode Current with $V_{IN} < 0$ | –20 mA |
| DC Output Diode Current with $V_{OUT} < 0$ | –50 mA |
| DC Output Current Max. Sink Current/Pin | 120 mA |
| Maximum Power Dissipation | 0.5 watts |
| $T_{STG}$ Storage Temperature | –65° to +150°C |

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

## FCT280 CAPACITANCE

$T_A$ = 25°C, f = 1 MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V

| **Pins** (14-Pin Package) | **SOIC** | **QSOP** | **PDIP** | **ZIP** | **Unit** |
|---|---|---|---|---|---|
| 1, 2, 4, 8-13 | 4 | 4 | 5 | 7 | pF |
| 5, 6 | 6 | 6 | 7 | 9 | pF |
| — | 8 | 8 | 9 | 10 | pF |

## FCT1280 CAPACITANCE

$T_A$ = 25°C, f = 1 MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V

| **Pins** | **SOIC** | **QSOP** | **PDIP** | **ZIP** | **Unit** |
|---|---|---|---|---|---|
| 1-5, 11-19 | 4 | 4 | 5 | 7 | pF |
| 6-9 | 6 | 6 | 7 | 9 | pF |
| — | 8 | 8 | 9 | 10 | pF |

**Note:** Capacitance is characterized but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0V ± 5%  Military $T_A$ = –55°C to 125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Logic HIGH for All Inputs | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | Logic LOW for All Inputs | — | — | 0.8 | V |
| $\Delta V_T$ | Input Hysteresis | $V_{TLH} - V_{THL}$ for All Inputs | — | 0.2 | — | V |
| $\lvert I_{IH} \rvert$<br>$\lvert I_{IL} \rvert$ | Input Current<br>Input HIGH or LOW | Vcc = Max., 0 ≤ $V_{IN}$ < Vcc | — | — | 5 | µA |
| $\lvert I_{OZ} \rvert$ | Off-State Output Current (Hi-Z) | Vcc = Max., 0 ≤ $V_{IN}$ ≤ Vcc | — | — | 5 | µA |
| $I_{OS}$ | Short Circuit Current | Vcc = Max., $V_{OUT}$ = GND(2,3) | –60 | — | — | mA |
| $V_{IC}$ | Input Clamp Voltage | Vcc = Min., $I_{IN}$ = –18 mA, $T_A$ = 25°C(3) | — | –0.7 | –1.2 | V |
| $V_{OH}$ | Output HIGH Voltage | Vcc = Min. $I_{OH}$ = –12 mA (MIL)<br>$I_{OH}$ = –15 mA (COM) | 2.4<br>2.4 | —<br>— | —<br>— | V |
| $V_{OL}$ | Output LOW Voltage | Vcc = Min. $I_{OL}$ = 32 mA (MIL)<br>$I_{OL}$ = 48 mA (COM) | —<br>— | —<br>— | 0.50<br>0.50 | V |

**Notes:**
1. Typical values indicate Vcc = 5.0V and $T_A$ = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions(1) | Min | Max | Unit |
|---|---|---|---|---|---|
| Icc | Quiescent Power Supply Current | Vcc = Max., freq = 0<br>0V ≤ $V_{IN}$ ≤ 0.2V or Vcc-0.2V ≤ $V_{IN}$ ≤ Vcc | — | 1.5 | mA |
| ΔIcc | Supply Current per Input @ TTL HIGH | Vcc = Max., $V_{IN}$ = 3.4V, freq = 0(2) | — | 2.0 | mA |
| Qccd | Supply Current per Input per MHz | Vcc = Max., Outputs Open and Enabled<br>One BitToggling @ 50% Duty Cycle<br>Other Inputs at GND or Vcc(3,4) | — | 0.25 | mA/ MHz |

**Notes:**
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN}$ = 3.4V).
3. For flip-flops, Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

## FCT280 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A$ = 0°C to 70°C, Vcc = 5.0V ± 5% Military $T_A$ = –55°C to 125°C, Vcc = 5.0V ± 10%
$C_{LOAD}$ = 50 pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| Symbol | Description | | 280T Min | 280T Max | 280AT Min | 280AT Max | 280BT Min | 280BT Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHLE}$ | Propagation Delay | Com | — | 10 | — | 7.5 | — | 6.3 | ns |
| $t_{PLHE}$ | I8-I0 to Σeven | Mil | — | 11 | — | 9 | — | 7.5 | |
| $t_{PHLO}$ | Propagation Delay | Com | — | 10 | — | 7.5 | — | 6.3 | ns |
| $t_{PLHO}$ | I8-I0 to Σodd | Mil | — | 11 | — | 9 | — | 7.5 | |

## FCT1280 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A$ = 0°C to 70°C, Vcc = 5.0V ± 5% Military $T_A$ = –55°C to 125°C, Vcc = 5.0V ± 10%
$C_{LOAD}$ = 50 pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| Symbol | Description | | 1280T Min | 1280T Max | 1280AT Min | 1280AT Max | 1280BT Min | 1280BT Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHLE}$ | Propagation Delay | Com | — | 10 | — | 7.5 | — | 6.3 | ns |
| $t_{PLHE}$ | I8-I0 to Σeven | Mil | — | 11 | — | 9 | — | 7.5 | |
| $t_{PHLO}$ | Propagation Delay | Com | — | 10 | — | 7.5 | — | 6.3 | ns |
| $t_{PLHO}$ | I8-I0 to Σodd | Mil | — | 11 | — | 9 | — | 7.5 | |
| $t_{OE}$ | Output Enable Time | Com(1) | 1.5 | 12.5 | 1.5 | 10 | 1.5 | 7.5 | ns |
| | $\overline{OER}$ to QΣe, QΣo | Mil(1) | 1.5 | 14 | 1.5 | 12 | 1.5 | 8.5 | |
| $t_{OZ}$ | Output Disable Time | Com(2) | 1.5 | 8 | 1.5 | 7 | 1.5 | 6.5 | ns |
| | $\overline{OER}$ to QΣe, QΣo | Mil(2) | 1.5 | 8 | 1.5 | 7 | 1.5 | 6.5 | |
| $t_{CPQ}$ | Clock to Output | Com | — | 10 | — | 9 | — | 7.5 | ns |
| | QΣe, QΣo | Mil | — | 11 | — | 10 | — | 8.5 | |
| $t_{CLR}$ | $\overline{CLR}$ to Output | Com | — | 13 | — | 11 | — | 8 | ns |
| | QΣe, QΣo | Mil | — | 15 | — | 13 | — | 10 | |
| $t_{CS}$ | $\overline{CEN}$ Setup Time | Com | 2.5 | — | 2 | — | 2 | — | ns |
| | $\overline{CEN}$ to CLK | Mil | 2.5 | — | 2 | — | 2 | — | |
| $t_{CH}$ | $\overline{CEN}$ Hold Time | Com | 3 | — | 2.5 | — | 2 | — | ns |
| | $\overline{CEN}$ to CLK | Mil | 3 | — | 2.5 | — | 2.5 | — | |
| $t_S$ | Data Setup Time | Com | 2.5 | — | 2 | — | 2 | — | ns |
| | Ix to CLK | Mil | 2.5 | — | 2 | — | 2 | — | |
| $t_H$ | Data Hold Time | Com | 3 | — | 2.5 | — | 2 | — | ns |
| | Ix to CLK | Mil | 3 | — | 2.5 | — | 2.5 | — | |
| $t_W$ | Clock Pulse Width | Com(2) | 7 | — | 7 | — | 5 | — | ns |
| | HIGH or LOW | Mil(2) | 7 | — | 7 | — | 6 | — | |

**Notes:**
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.