CY54/74FCT480T

Dual 8-Bit Parity Generator/Checker

Features

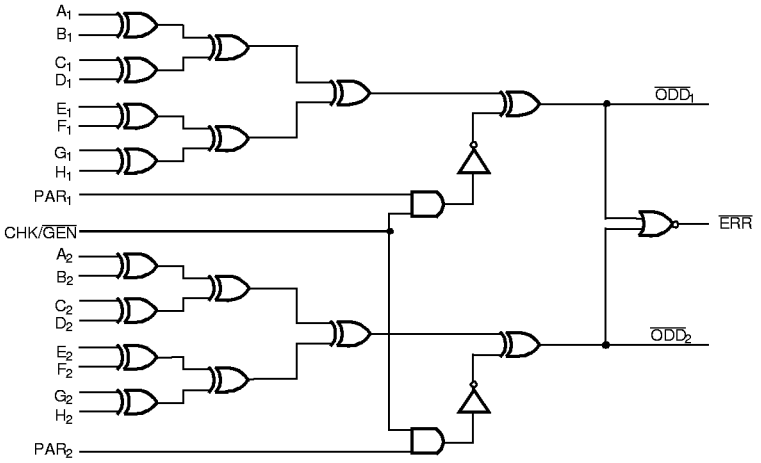
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-A speed at 7.5 ns max. (Com'l)**
  FCT-B speed at 5.6 ns max. (Com'l)
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink Current 64 mA (Com'l), 32 mA (Mil)**
  Source Current 32 mA (Com'l), 12 mA (Mil)
- **Two 8-bit parity generator/checkers**
- **Open drain Active LOW parity error output**
- **Expandable for larger word widths**

Functional Description

The FCT480T is a high-speed dual 8-bit parity generator/checker. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a sum and parity error output. The FCT480T can be used in ODD parity systems. The parity error output is open-drain, designed for easy expansion of the word width by a wired-OR connection of several FCT480T type devices. Since additional logic is not needed, the parity generation or checking times remain the same as for an individual FCT480T device.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

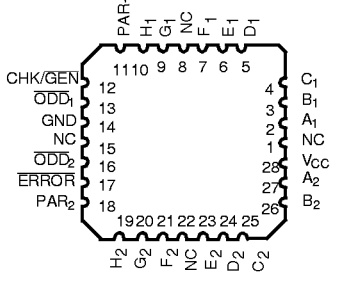
Logic Block Diagram



FCT480T–1

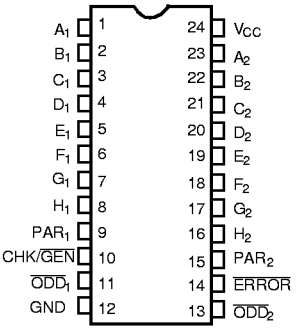
Pin Configurations

LCC
Top View



FCT480T-2

DIP/SOIC/QSOP
Top View



FCT480T-3

Function Table

Inputs					Outputs		
A_1 to H_1	A_2 to H_2	CHK/$\overline{GEN}$	PAR_1	PAR_2	$\overline{ODD}_1$	$\overline{ODD}_2$	$\overline{ERROR}$
Number of A_1 to H_1 Inputs HIGH is EVEN	Number of A_2 to H_2 Inputs HIGH is EVEN	H	H	H	L	L	H
			L	H	H	L	L
			H	L	L	H	L
			L	L	H	H	L
		L	X	X	H	H	L
	Number of Inputs HIGH A_2 to H_2 is ODD	H	H	H	L	H	L
			L	H	H	H	L
			H	L	L	L	H
			L	L	H	L	L
		L	X	X	H	L	L
Number of A_1 to H_1 Inputs HIGH is ODD	Number of A_2 to H_2 Inputs HIGH is EVEN	H	H	H	H	L	L
			L	H	L	L	H
			H	L	H	H	L
			L	L	L	H	L
		L	X	X	L	H	L
	Number of A_2 to H_2 Inputs HIGH is ODD	H	H	H	H	H	L
			L	H	L	H	L
			H	L	H	L	L
			L	L	L	L	H
		L	X	X	L	L	H

Maximum Ratings[1, 2]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –65°C to +135°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Input Voltage..... –0.5V to +7.0V

DC Output Voltage..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin)..... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	All	–40°C to +85°C	5V ± 5%
Military[3]	All	–55°C to +125°C	5V ± 10%

Notes:

1. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –32 mA	Com'l	2.0			V
		V_{CC} = Min., I_{OH} = –15 mA	Com'l	2.4	3.3		V
		V_{CC} = Min., I_{OH} = –12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 64 mA	Com'l		0.3	0.55	V
		V_{CC} = Min., I_{OL} = 32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[5]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				–10	µA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = 0.0V		–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC} = 0V, V_{OUT} = 4.5V				±1	µA

Capacitance[5]

Parameter	Description	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[7] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=2.5 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=2.5 MHz, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling at f_1=2.5 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.5	5.0[10]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling at f_1=2.5 MHz, V_{IN}=3.4V or V_{IN}=GND	6.5	21.0[10]	mA

Switching Characteristics Over the Operating Range

	Description	FCT480AT		FCT480BT		Unit
		Military	Com'l	Military	Com'l	
t_{PLH} t_{PHL}	Propagation Delay A to EVEN/ODD	9.5 9.0	7.5 7.0	7.0 6.6	5.6 5.6	ns
t_{PLH}[11] t_{PHL}	Propagation Delay A to $\overline{ERROR}$	9.0 10.5	7.0 8.5	7.0 8.1	5.6 6.5	ns
t_{PLH} t_{PHL}	Propagation Delay CHK/$\overline{GEN}$ to EVEN/ODD	8.5 10.0	6.5 7.5	6.3 7.4	5.9 5.9	ns
t_{PLH}[11] t_{PHL}	Propagation Delay CHK/$\overline{GEN}$ to $\overline{ERROR}$	9.5 9.0	7.5 7.0	7.1 6.9	5.7 5.5	ns

Notes:

7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_1 = Input signal frequency
   N_1 = Number of inputs changing at f_1
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. t_{PLH} is measured up to $V_{OUT}=V_{OL}+0.3V$

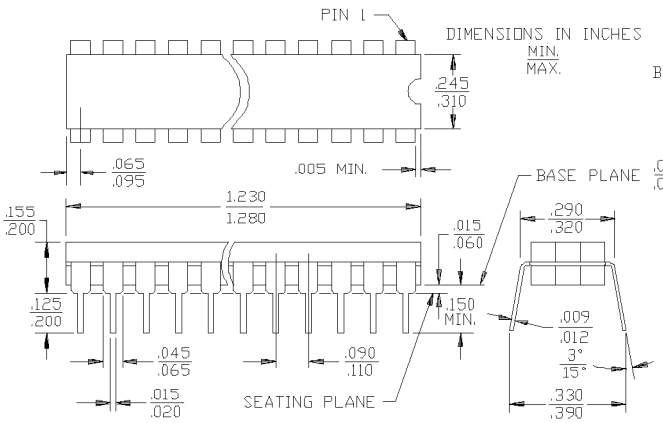
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.6	CY74FCT480BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT480BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT480BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT480BTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY74FCT480ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480ATQC	Q13	24-Lead (150-Mil) QSOP	

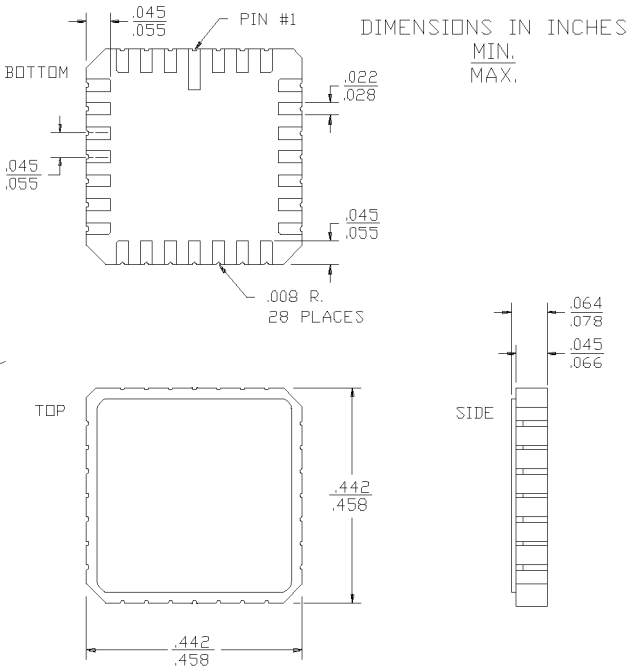
Document #: 38-00281-B

Package Diagrams

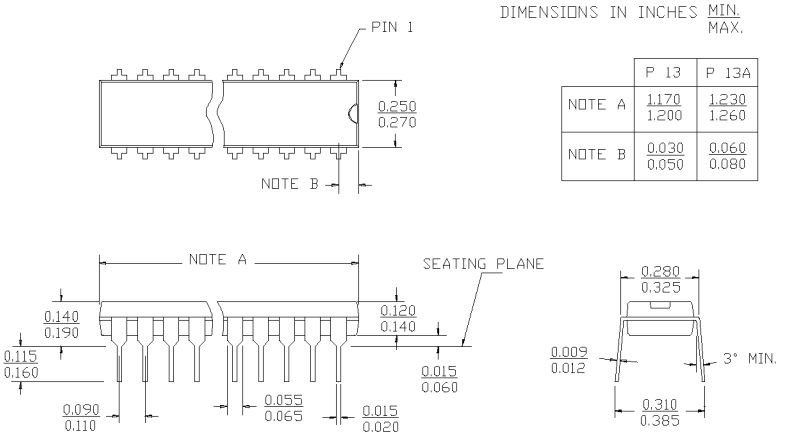
24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D-9 Config.A



28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4



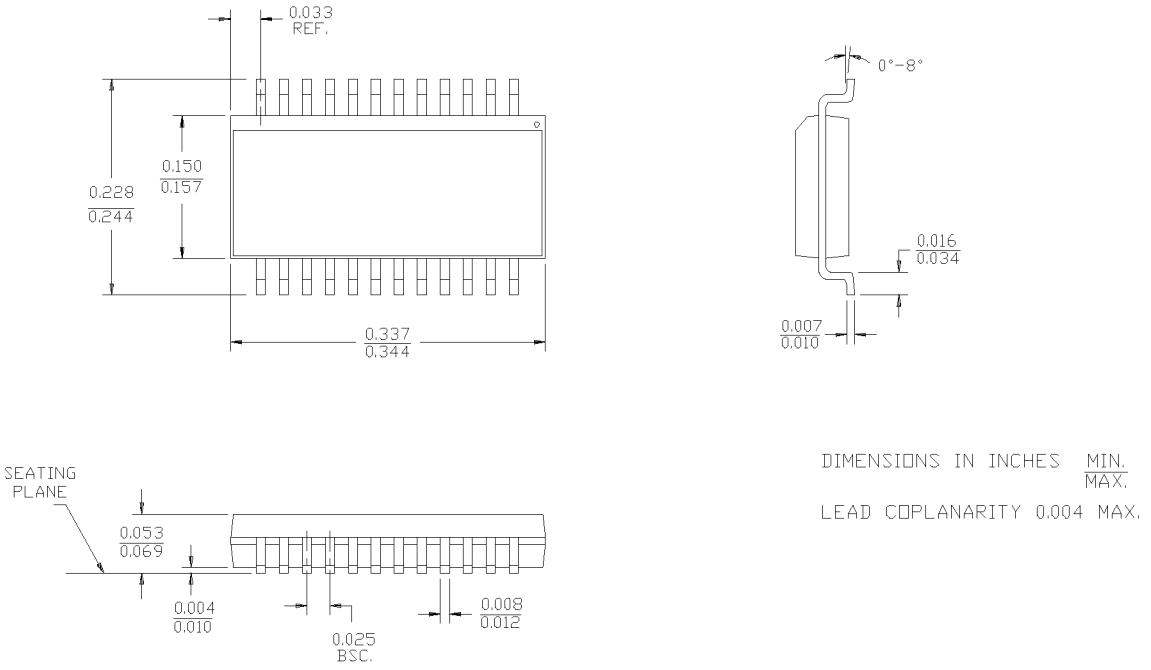
24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

Package Diagrams (continued)

24-Lead Quarter Size Outline Q13



24-Lead (300-Mil) Molded SOIC S13