FAIRCHILD SEMICONDUCTOR™

November 1988
Revised December 1998

74AC280
9-Bit Parity Generator/Checker

General Description

The AC280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

Features

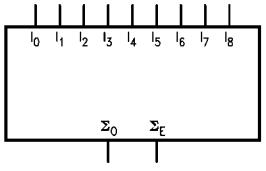
- I_{CC} reduced by 50%
- 9-bit width for memory applications
- AC280: 5962-92201

Ordering Code:

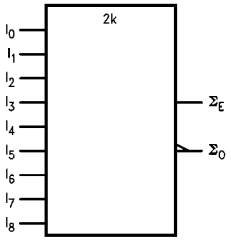
Order Number	Package Number	Package Description
74AC280SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols

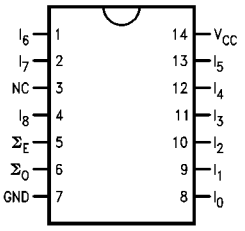


IEEE/IEC



Connection Diagram

Pin Assignment for DIP and SOIC



Pin Descriptions

Pin Names	Description
I_0–I_8	Data Inputs
Σ_O	Odd Parity Output
Σ_E	Even Parity Output

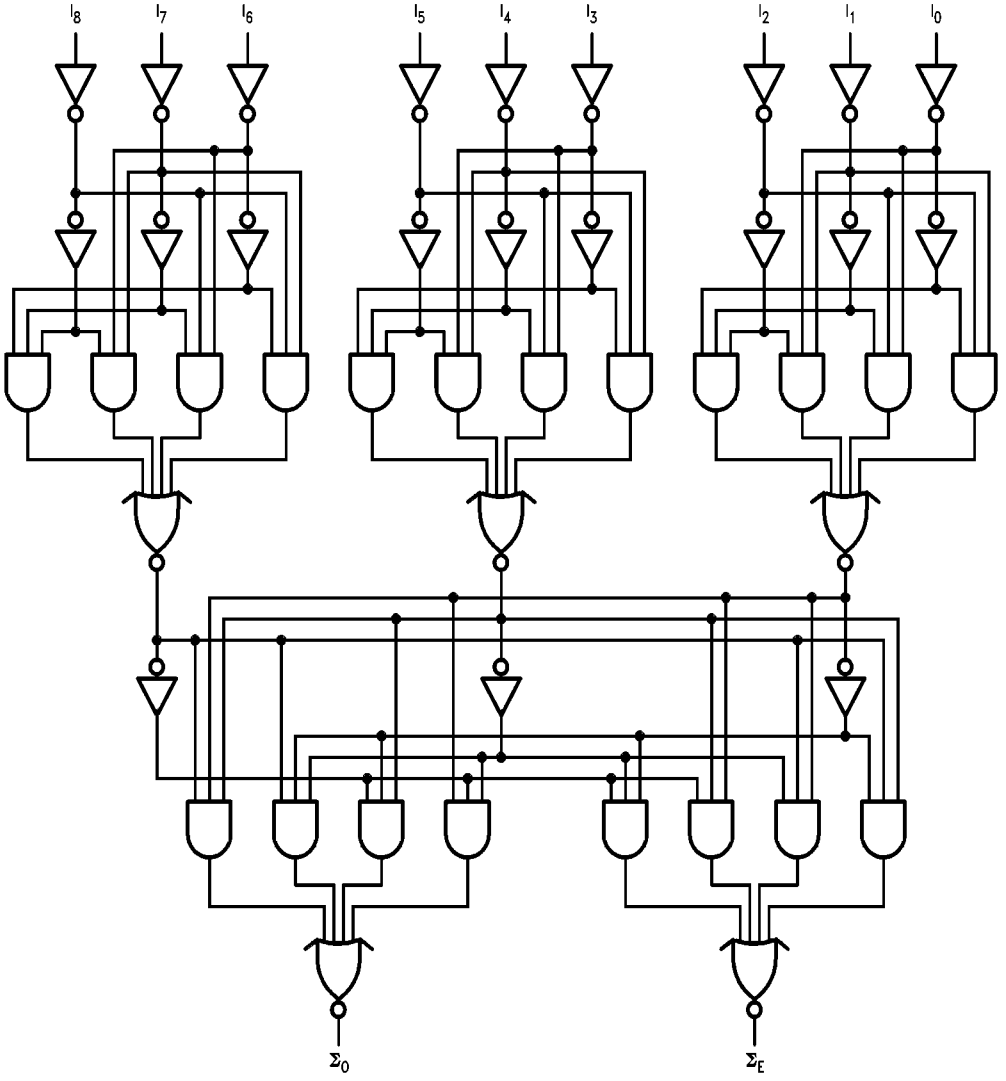
Truth Table

Number of HIGH Inputs I_0–I_8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J) PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Fairchild does not recommend operation of FACT circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74AC		54AC	74AC	Units	Conditions
			$T_A = +25°C$		$T_A = -55°C$ to $+125°C$	$T_A = -40°C$ to $+85°C$		
		(V)	Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1	2.1		$V_{OUT} = 0.1V$
	Input Voltage	4.5	2.25	3.15	3.15	3.15	V	or $V_{CC} - 0.1V$
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9	0.9		$V_{OUT} = 0.1V$
	Input Voltage	4.5	2.25	1.35	1.35	1.35	V	or $V_{CC} - 0.1V$
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9	2.9		$I_{OUT} = -50\ \mu A$
	Output Voltage	4.5	4.49	4.4	4.4	4.4	V	
		5.5	5.49	5.4	5.4	5.4		
								$V_{IN} = V_{IL}$ or V_{IH}
		3.0		2.56	2.4	2.46		$I_{OH} = -12$ mA
		4.5		3.86	3.7	3.76	V	$I_{OH} = -24$ mA
		5.5		4.86	4.7	4.76		$I_{OH} = -24$ mA (Note 2)
V_{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1	0.1		$I_{OUT} = 50\ \mu A$
	Output Voltage	4.5	0.001	0.1	0.1	0.1	V	
		5.5	0.001	0.1	0.1	0.1		
								$V_{IN} = V_{IL}$ or V_{IH}
		3.0		0.36	0.50	0.44		$I_{OL} = 12$ mA
		4.5		0.36	0.50	0.44	V	$I_{OL} = 24$ mA
		5.5		0.36	0.50	0.44		$I_{OL} = 24$ mA (Note 2)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic	5.5			50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 3)	5.5			−50	−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

AC Electrical Characteristics

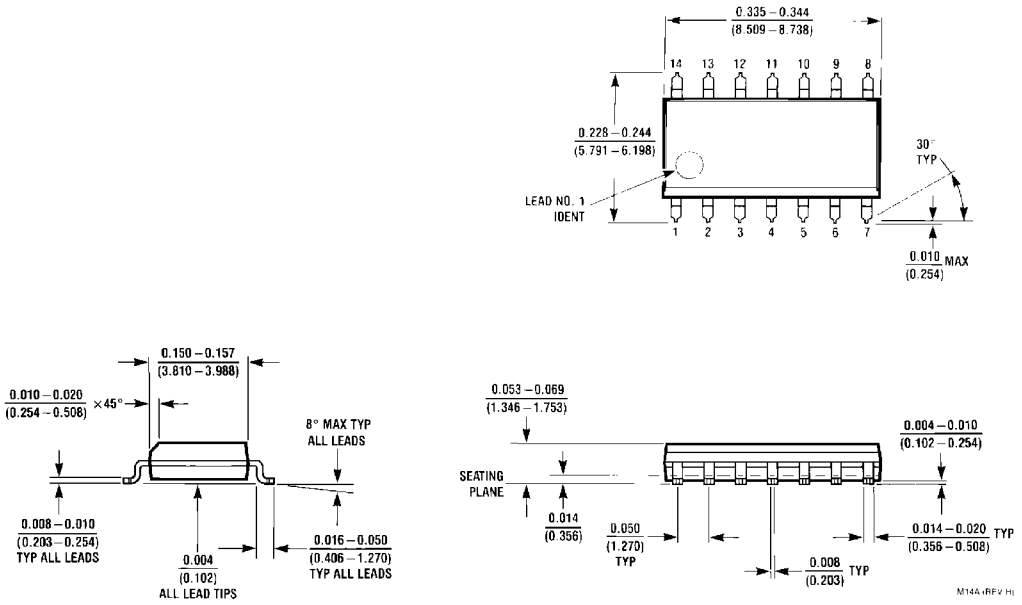
Symbol	Parameter	V_{CC} (V) (Note 5)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	5.0	10.5	17.0	1.0	20.0	4.0	18.5	ns
t_{PHL}	I_n to Σ_E	5.0	3.0	7.5	13.0	1.5	14.5	2.0	14.5	
t_{PLH}	Propagation Delay	3.3	5.0	12.0	17.0	1.0	20.0	4.0	18.5	ns
t_{PHL}	I_n to Σ_O	5.0	3.0	8.5	13.0	1.5	14.5	2.0	14.5	

Note 5: Voltage range 3.3 is 3.3V ±0.3V.
Voltage range 5.0 is 5.0V ±0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	75.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
Package Number M14A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com