

# 54F/74F280

## 9-Bit Parity Generator/Checker

### General Description

The 'F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

### Features

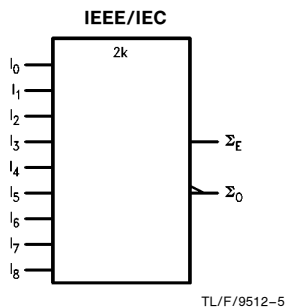
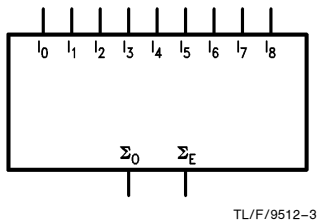
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F280PC		N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
	54F280DM (Note 2)	J14A	14-Lead Ceramic Dual-In-Line
74F280SC (Note 1)		M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F280SJ (Note 1)		M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F280FM (Note 2)	W14B	14-Lead Cerpack
	54F280LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

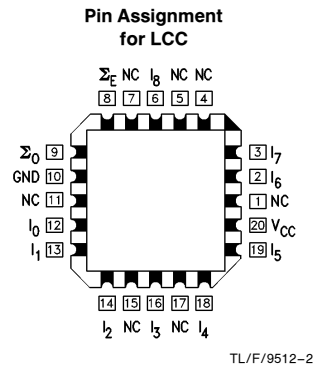
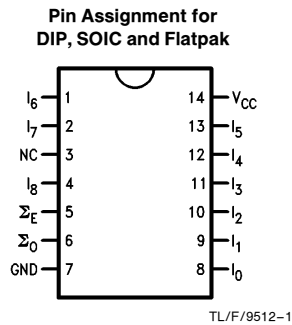
**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

### Logic Symbols



### Connection Diagrams



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## Unit Loading/Fan Out

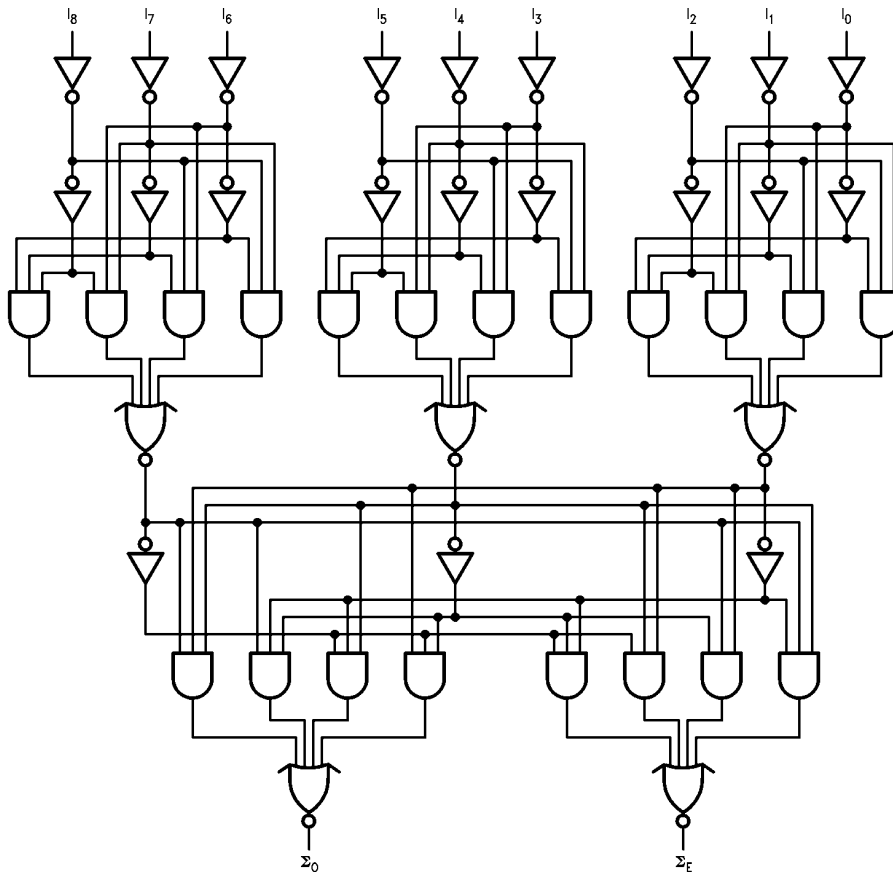
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_0-I_8$	Data Inputs	1.0/1.0	$20 \mu\text{A}/-0.6 \text{ mA}$
$\Sigma_O$	Odd Parity Output	50/33.3	$-1 \text{ mA}/20 \text{ mA}$
$\Sigma_E$	Even Parity Output	50/33.3	$-1 \text{ mA}/20 \text{ mA}$

## Truth Table

Number of HIGH Inputs $I_0-I_8$	Outputs	
	$\Sigma$ Even	$\Sigma$ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level  
L = LOW Voltage Level

## Logic Diagram



TL/F/9512-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

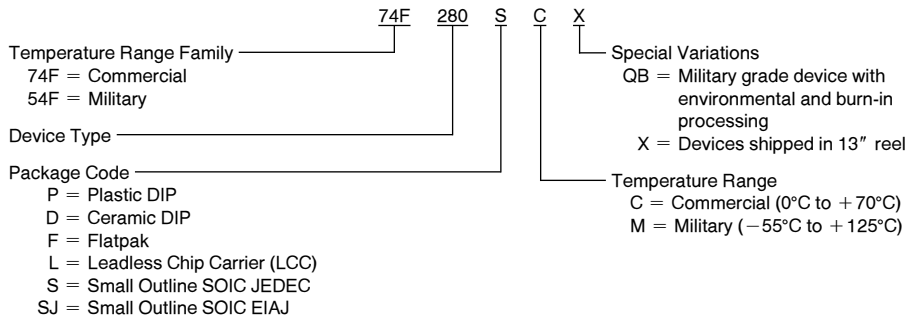
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				
		74F 5% V <sub>CC</sub>	2.7				
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current			-60	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		25	38	mA	Max	V <sub>O</sub> = HIGH

## AC Electrical Characteristics

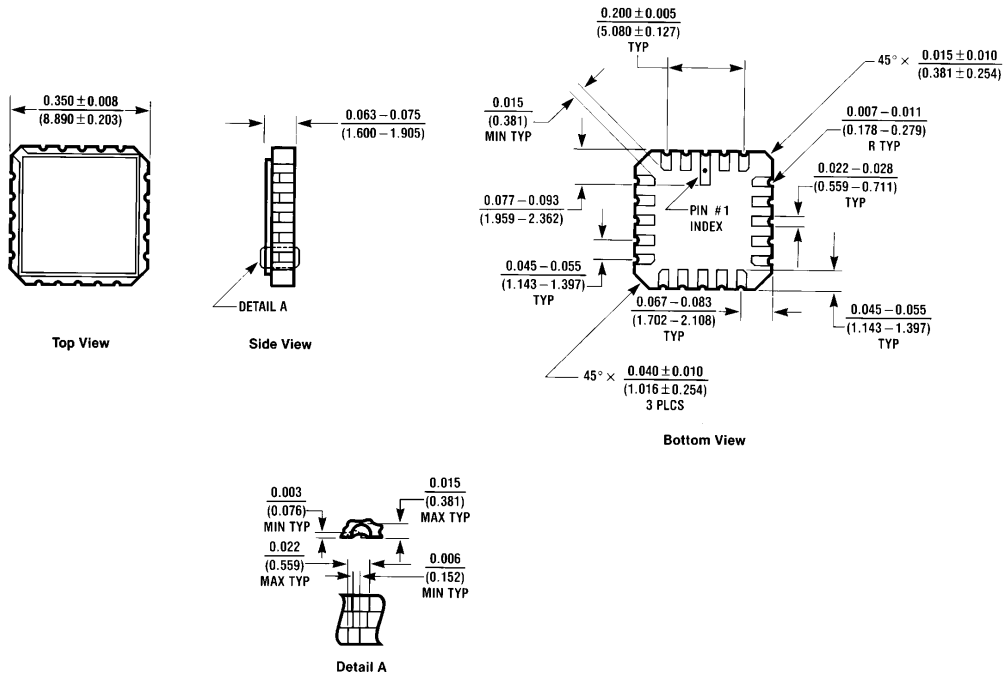
Symbol	Parameter	74F			54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	6.5	10.0	15.0	6.5	20.0	6.5	16.0	ns
t <sub>PHL</sub>	I <sub>n</sub> to Σ <sub>E</sub>	6.5	11.0	16.0	6.5	21.0	6.5	17.0	
t <sub>PLH</sub>	Propagation Delay	6.0	10.0	15.0	5.0	20.0	6.0	16.0	ns
t <sub>PHL</sub>	I <sub>n</sub> to Σ <sub>O</sub>	6.5	11.0	16.0	6.5	21.0	6.5	17.0	

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



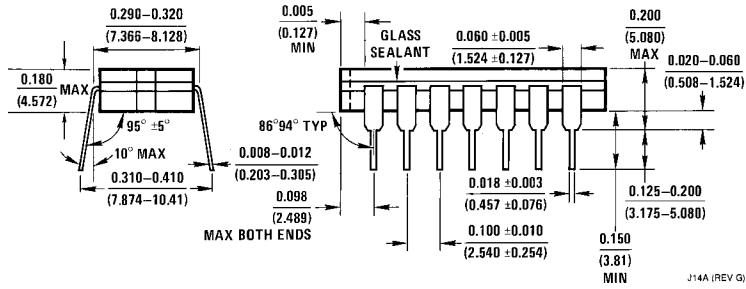
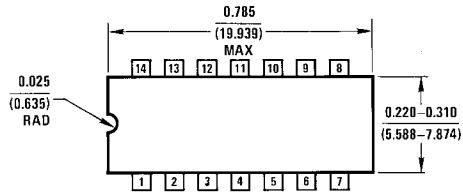
**Physical Dimensions** inches (millimeters)



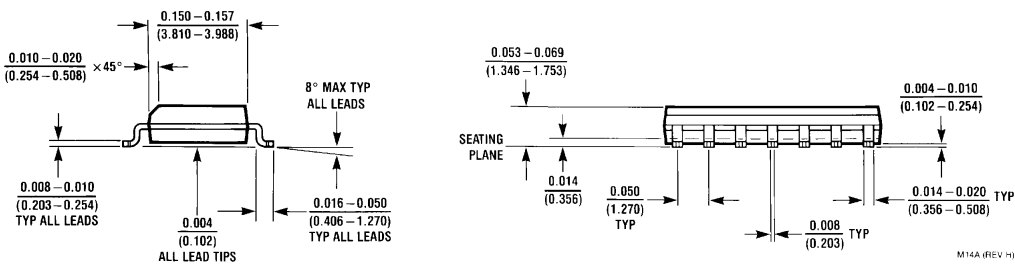
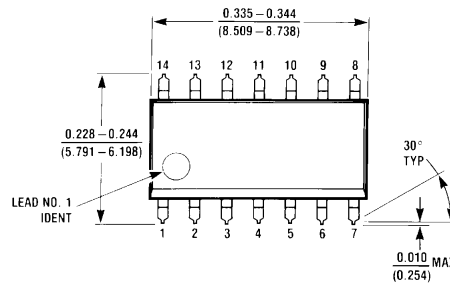
E20A (REV D)

**20-Lead Ceramic Leadless Chip Carrier (L)  
 NS Package Number E20A**

**Physical Dimensions** inches (millimeters) (Continued)

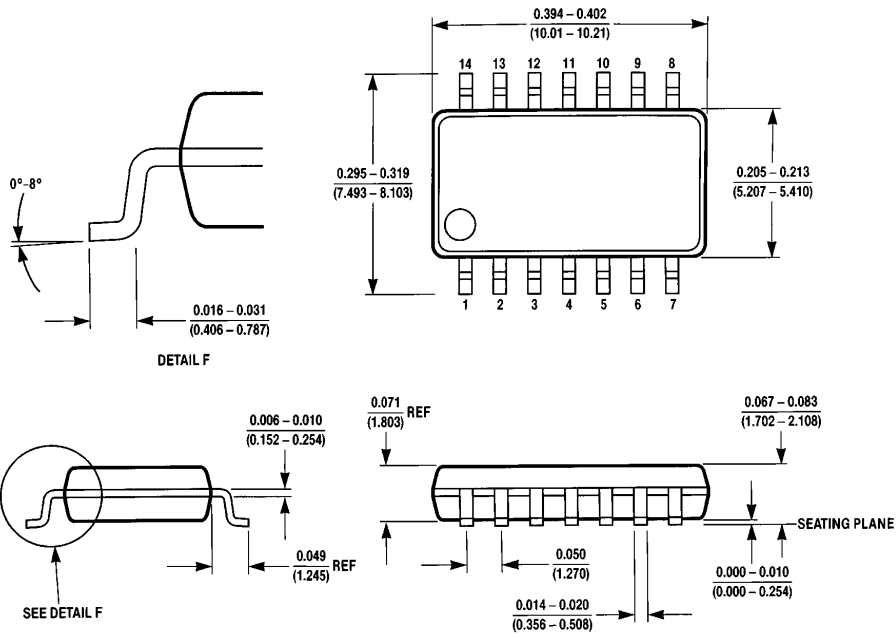


**14-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J14A



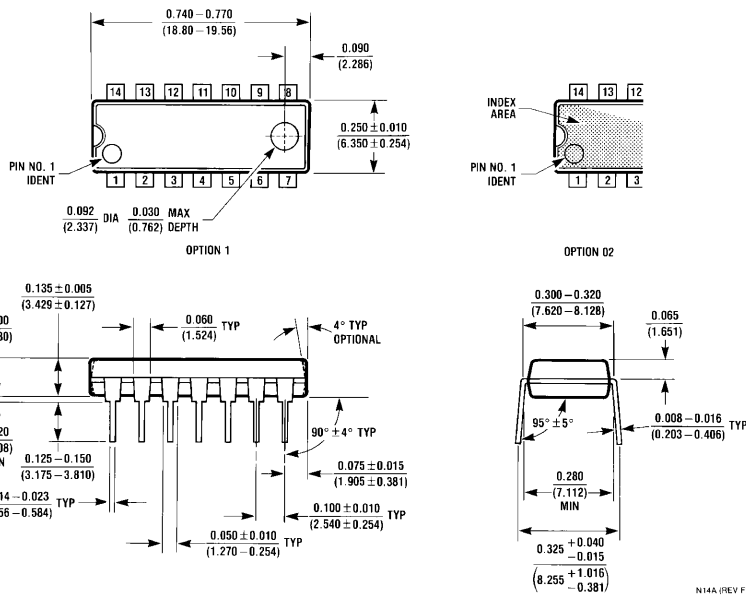
**14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)**  
NS Package Number M14A

**Physical Dimensions** inches (millimeters) (Continued)



M14D (REV A)

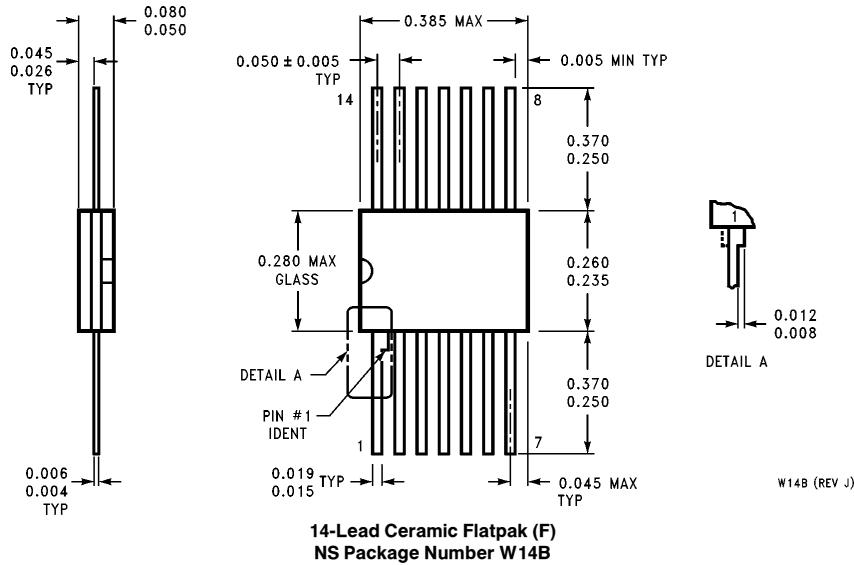
**14-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)**  
**NS Package Number M14D**



N14A (REV F)

**14-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
**NS Package Number N14A**

**Physical Dimensions** inches (millimeters) (Continued)



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## 54F280 9-Bit Parity Generator/Checker

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

### General Description

The 'F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

### Features

- Guaranteed 4000V minimum ESD protection


### Datasheet

Title	Size (in Kbytes)	Date	 View Online	 Download	 Receive via Email
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54F280 9-Bit Parity Generator/Checker	152 Kbytes	3-Dec-97	<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>
54F280 Mil-Aero Datasheet MN54F280-X	18 Kbytes		<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>

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## Package Availability, Models, Samples & Pricing

Part Number	Package		Status	Models		Samples & Electronic Orders	Budge Prici
	Type	# pins		SPICE	IBIS		Quantity
54F280LMQB	LCC	20	Full production	N/A	N/A	.	50+
54F280DM	Cerdip	14	Full production	N/A	N/A	.	50+
54F280DMQB	Cerdip	14	Full production	N/A	N/A		50+
54F280FMQB	Cerpack	14	Full production	N/A	N/A	.	50+
JM38510/34901B2	LCC	20	Full production	N/A	N/A	.	50+
JM38510/34901BC	Cerdip	14	Full production	N/A	N/A	.	50+
JM38510/34901BD	Cerpack	14	Full production	N/A	N/A	.	50+

54F280J-MLS	Cerdip	14	Preliminary	N/A	N/A	.	
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