![Harris Semiconductor logo]

CD74HC280,
CD74HCT280

High Speed CMOS Logic
9-Bit Odd/Even Parity Generator/Checker

November 1997

Features

- Typical Propagation Delay = 17ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C

- Replaces 74LS180 Types

- Easily Cascadable

- Fanout (Over Temperature Range)
  - Standard Outputs . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . 15 LSTTL Loads

- Wide Operating Temperature Range . . . -55°C to 125°C

- Balanced Propagation Delay and Transition Times

- Significant Power Reduction Compared to LSTTL Logic ICs

- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V

- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The Harris CD74HC280 and CD74HCT280 are 9-bit odd/even parity, generator checker devices. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated (ΣE output is high) when an even number of data inputs is high. Odd parity is indicated (ΣO output is high) when an odd number of data inputs is high. Parity checking for words larger than 9 bits can be accomplished by tying the ΣE output to any input of an additional HC/HCT280 parity checker.
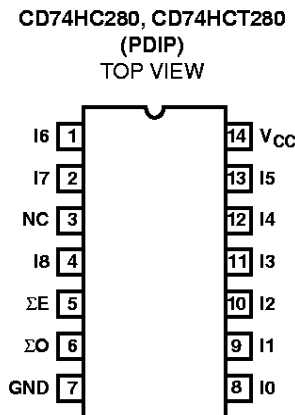
Ordering Information

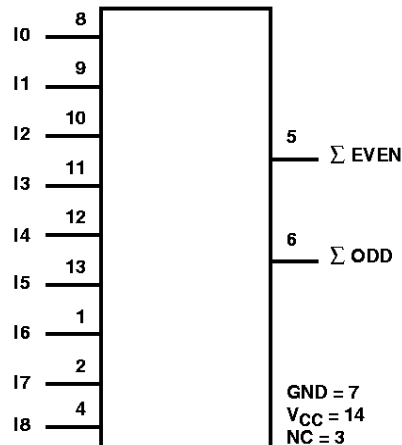| PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC280E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT280E	-55 to 125	14 Ld PDIP	E14.3

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

2. Wafer and die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

CD74HC280, CD74HCT280
(PDIP)
TOP VIEW

```
        ___ ___
I6 [1]  |  U  | [14] VCC
I7 [2]  |     | [13] I5
NC [3]  |     | [12] I4
I8 [4]  |     | [11] I3
ΣE [5]  |     | [10] I2
ΣO [6]  |     | [9]  I1
GND [7] |_____| [8]  I0
```

Functional Diagram

```
I0 ---8---|         |
I1 ---9---|         |
I2 ---10--|         |--5-- Σ EVEN
I3 ---11--|         |
I4 ---12--|         |--6-- Σ ODD
I5 ---13--|         |
I6 ---1---|         |
I7 ---2---|         |   GND = 7
I8 ---4---|         |   VCC = 14
          |_____|   NC = 3
```

File Number **1669.1**

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
   For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
   For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Drain Current, per Output, I_O
   For -0.5V < V_O < V_{CC} + 0.5V . . . . ±25mA
DC Output Source or Sink Current per Output Pin, I_O
   For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
   HC Types . . . . .2V to 6V
   HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
   2V . . . . 1000ns (Max)
   4.5V. . . . . 500ns (Max)
   6V . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package.	175

Maximum Junction Temperature . . . . .150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . .300°C
   (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	I_O (mA)	V_{CC} (V)	25°C MIN	TYP	MAX	-40°C TO 85°C MIN	MAX	-55°C TO 125°C MIN	MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications   (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	1

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Switching Specifications   Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, Any Input to ΣO	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	200	250	300	ns
			4.5	-	40	50	60	ns
			6	-	34	43	51	ns
		C_L = 15pF	5	17	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Propagation Delay, Any Input to ΣE	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	200	250	300	ns
			4.5	-	40	50	60	ns
			6	-	34	43	51	ns
		C_L = 15pF	5	17	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	58	-	-	-	pF
HCT TYPES								
Propagation Delay, Any Input to ΣO	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	45	56	68	ns
		C_L = 15pF	5	19	-	-	-	ns
Propagation Delay, Any Input to ΣE	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	42	53	63	ns
		C_L = 15pF	5	18	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	15	19	22	ns
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	58	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per package.

6. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.
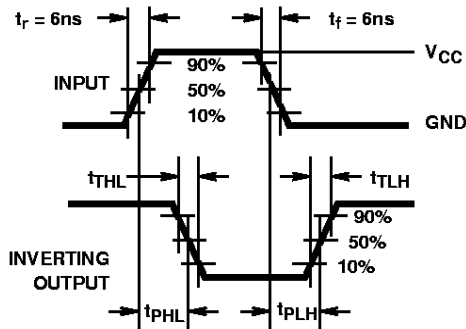
Test Circuits and Waveforms

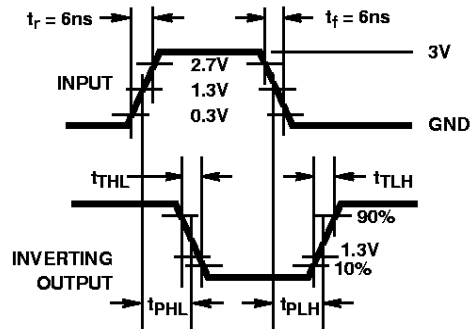FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC