

CD4528BC Dual Monostable Multivibrator

General Description

The CD4528BC is a dual monostable multivibrator. Each device is retriggerable and resettable. Triggering can occur from either the rising or falling edge of an input pulse, resulting in an output pulse over a wide range of widths. Pulse duration and accuracy are determined by external timing components Rx and Cx.

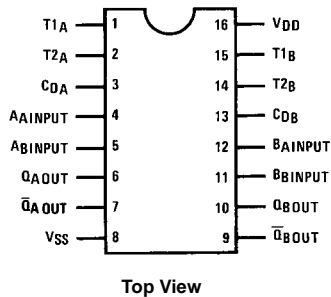
Features

- Wide supply voltage range: 3.0V to 18V
- Separate reset available
- Quiescent current = 5.0 nA/package (typ.) at 5.0 V_{DC}
- Diode protection on all inputs
- Triggerable from leading or trailing edge pulse
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range

Ordering Code:

Order Number	Package Number	Package Description
CD4528BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4528BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

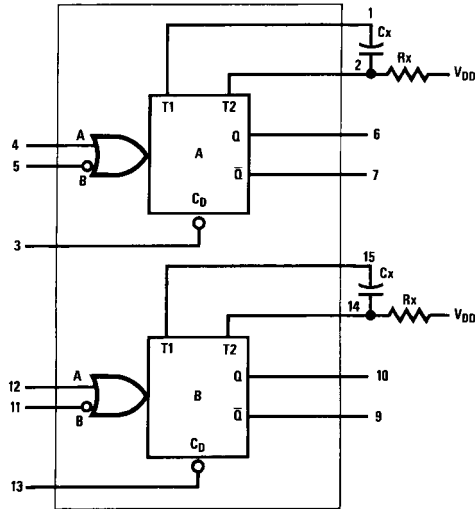


Truth Table

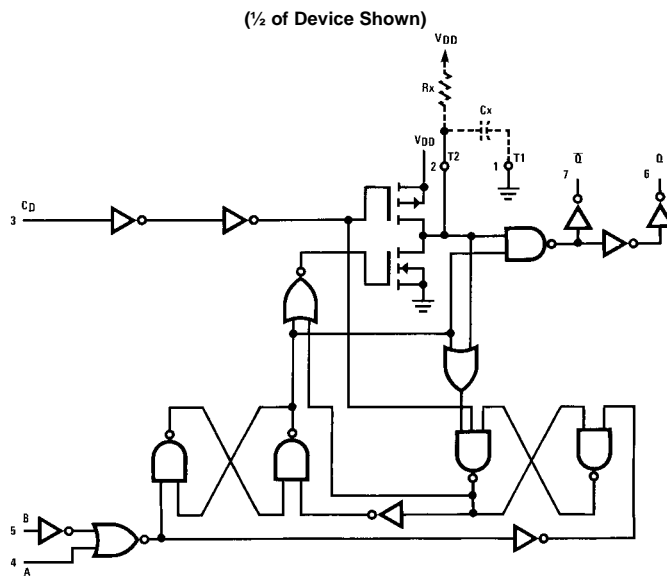
Clear	Inputs		Outputs	
	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⌊	⌋
H	↑	H	⌋	⌊

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⌊ = One HIGH Level Pulse
⌋ = One LOW Level Pulse
X = Irrelevant

Block Diagram



Logic Diagram



Note: Externally ground pins 1 and 15 to pin 8.

Absolute Maximum Ratings(Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	-0.5 V_{DC} to +18 V_{DC}
Input Voltage, All Inputs (V_{IN})	-0.5 V_{DC} to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	-55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5		0.005	5		150	μA
		$V_{DD} = 10V$		10		0.010	10		300	
		$V_{DD} = 15V$		20		0.015	20		600	
V_{OL}	LOW Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	
		$V_{DD} = 15V$		0.05			0.05		0.05	
V_{OH}	HIGH Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		
V_{IL}	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or 9V		3.0		4.50	3.0		3.0	
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0		6.75	4.0		4.0	
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0	5.50		7.0		
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0	8.25		11.0		
I_{OL}	LOW Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 4.6V$	-0.25		-0.2	-0.36		-0.14		mA
		$V_{DD} = 10V, V_O = 9.5V$	-0.62		-0.5	-0.9		-0.35		
		$V_{DD} = 15V, V_O = 13.5V$	-1.8		-1.5	-3.5		-1.1		
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10 ⁻⁵	-0.1		-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10 ⁻⁵	0.1		1.0	

Note 3: V_{SS} = 0V unless otherwise specified.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 5)						
T _A = 25°C, C _L = 50 pF, R _L = 200 kΩ, Input t _r = t _f = 20 ns, unless otherwise specified						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _r	Output Rise Time	t _r = (3.0 ns/pF) C _L + 30 ns, V _{DD} = 5.0V		180	400	ns
		t _r = (1.5 ns/pF) C _L + 15 ns, V _{DD} = 10.0V		90	200	
		t _r = (1.1 ns/pF) C _L + 10 ns, V _{DD} = 15.0V		65	160	
t _f	Output Fall Time	t _f = (1.5 ns/pF) C _L + 25 ns, V _{DD} = 5.0V		100	200	ns
		t _f = (0.75 ns/pF) C _L + 12.5 ns, V _{DD} = 10V		50	100	
		t _f = (0.55 ns/pF) C _L + 9.5 ns, V _{DD} = 15.0V		35	80	
t _{PLH} t _{PHL}	Turn-Off, Turn-On Delay A or B to Q or \bar{Q} C _x = 15 pF, R _x = 5.0 kΩ	t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 240 ns, V _{DD} = 5.0V		230	500	ns
		t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 8 ns, V _{DD} = 10.0V t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 65 ns, V _{DD} = 15.0V		100	250	
t _{PLH} t _{PHL}	Turn-Off, Turn-On Delay A or B to Q or \bar{Q} C _x = 100 pF, R _x = 10 kΩ	t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 620 ns, V _{DD} = 5.0V		230	500	ns
		t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 257 ns, V _{DD} = 10.0V t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 185 ns, V _{DD} = 15.0V		100	250	
t _{WL} t _{WH}	Minimum Input Pulse Width A or B C _x = 15 pF, R _x = 5.0 kΩ	V _{DD} = 5.0V		60	150	ns
		V _{DD} = 10.0V V _{DD} = 15V		20	50	
PW _{OUT}	Output Pulse Width Q or \bar{Q} For C _x < 0.01 μF (See Graph for Appropriate V _{DD} Level) C _x = 15 pF, R _x = 5.0 kΩ	V _{DD} = 5.0V		550		ns
		V _{DD} = 10.0V		350		
		V _{DD} = 15.0V		300		
t _{PLH} t _{PHL}	Reset Propagation Delay, t _{PLH} , t _{PHL} C _x = 15 pF, R _x = 5.0 kΩ	V _{DD} = 5.0V	15	29	45	μs
		V _{DD} = 10.0V	10	37	90	
		V _{DD} = 15.0V	15	42	95	
t _{PLH} t _{PHL}	C _x = 1000 pF, R _x = 10 kΩ	V _{DD} = 5.0V		7.0		μs
		V _{DD} = 10.0V		6.7		
		V _{DD} = 15.0V		6.7		
t _{RR}	Minimum Retrigger Time C _x = 15 pF, R _x = 5.0 kΩ	V _{DD} = 5.0V		0		ns
		V _{DD} = 10.0V		0		
		V _{DD} = 15.0V		0		
Pulse Width Match between Circuits in the Same Package C _x = 10,000 pF, R _x = 10 kΩ		V _{DD} = 5.0V		6	25	%
		V _{DD} = 10.0V		8	35	
		V _{DD} = 15.0V		8	35	

Note 5: AC parameters are guaranteed by DC correlated testing.

Pulse Widths

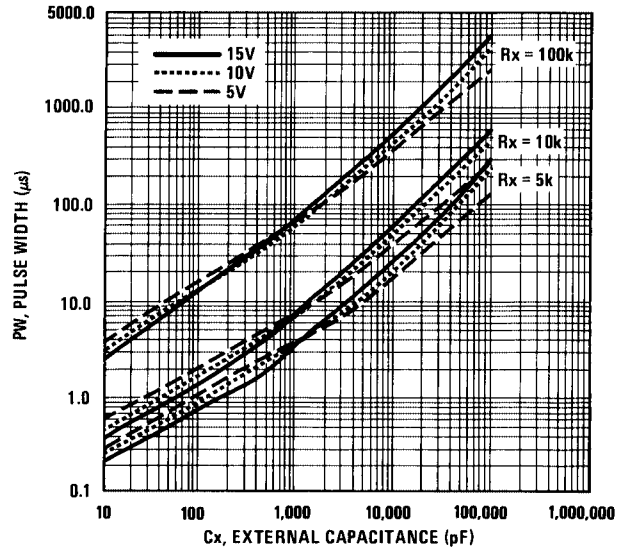


FIGURE 1. Pulse Width vs Cx

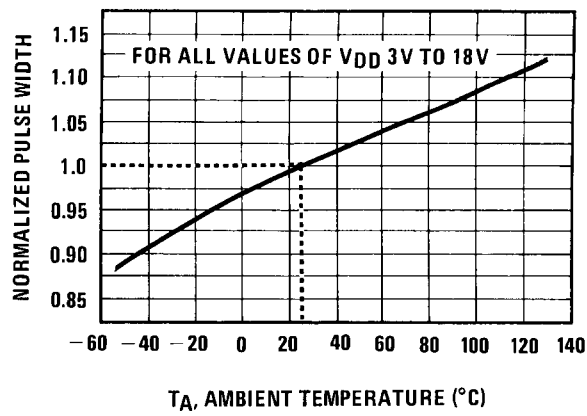
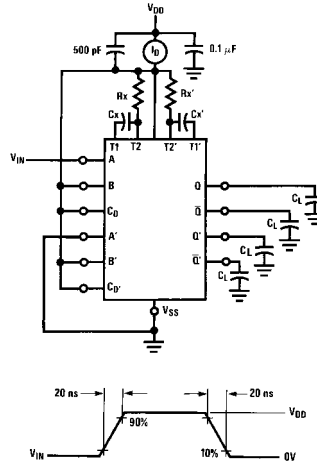


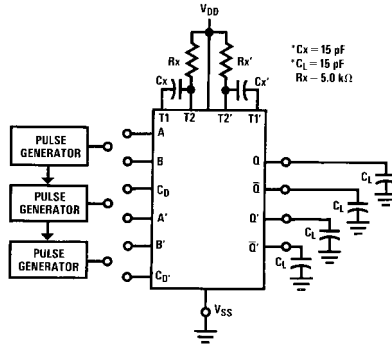
FIGURE 2. Normalized Pulse Width vs Temperature

AC Test Circuits and Waveforms



Duty Cycle = 50%

FIGURE 3. Power Dissipation Test Circuit and Waveforms



*Includes capacitance of probes, wiring, and fixture parasitic.
 Note: AC test waveforms for PG1, PG2, and PG3 in Figure 4.

Input Connections

Characteristics	C _D	A	B
t _{PLH} , t _{PHL} , t _r , t _f , PW _{out} , PW _{in}	V _{DD}	PG1	V _{DD}
t _{PLH} , t _{PHL} , t _r , t _f , PW _{out} , PW _{in}	V _{DD}	V _{SS}	PG2
t _{PLH(R)} , t _{PHL(R)} , PW _{in}	PG3	PG1	PG2

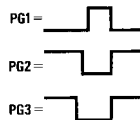


FIGURE 4. AC Test Circuit

AC Test Circuits and Waveforms (Continued)

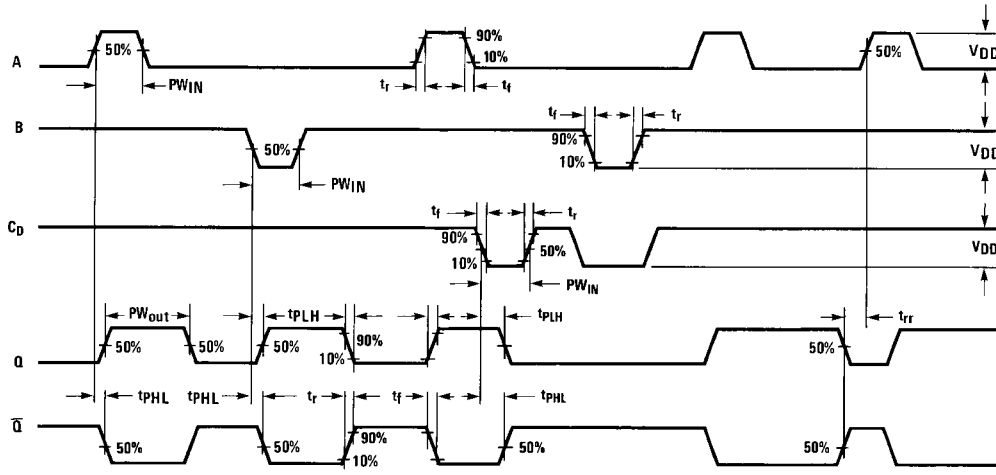
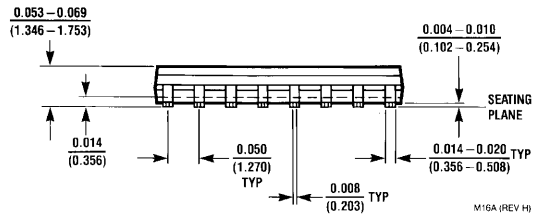
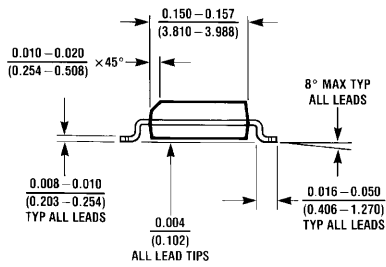
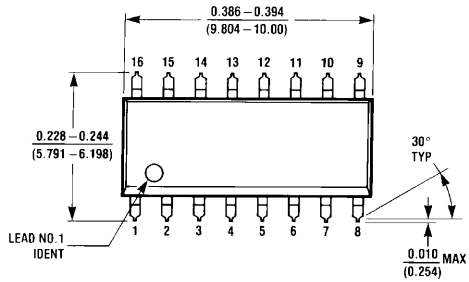


FIGURE 5. AC Test Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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