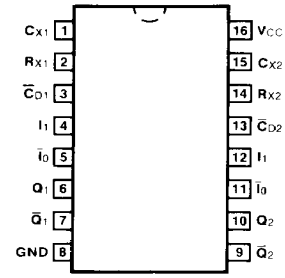
# 9602
# 96L02

## DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

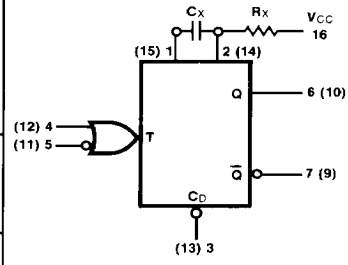
**DESCRIPTION** — The 9602 is a dual TTL monostable multivibrator with trigger mode selection, reset capability, rapid recovery, internally compensated reference levels and high speed capability. Output pulse duration and accuracy depend on external timing components, and are therefore under user control for each application. It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, frequency detectors, clock pulse generators and fixed-frequency dividers. Each input is provided with a clamp diode to limit undershoot and minimize ringing induced by fast fall times acting on system wiring impedances.

- **RETRIGGERABLE, 0% TO 100% DUTY CYCLE**
- **DC LEVEL TRIGGERING, INSENSITIVE TO TRANSITION TIMES**
- **LEADING OR TRAILING-EDGE TRIGGERING**
- **COMPLEMENTARY OUTPUTS WITH ACTIVE PULL-UPS**
- **PULSE WIDTH COMPENSATION FOR $\Delta V_{CC}$ AND $\Delta T_A$**
- **50 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **RESETTABLE, FOR INTERRUPT OPERATIONS**

**CONNECTION DIAGRAM**
PINOUT A




**LOGIC SYMBOL**




VCC = Pin 16
GND = Pin 8

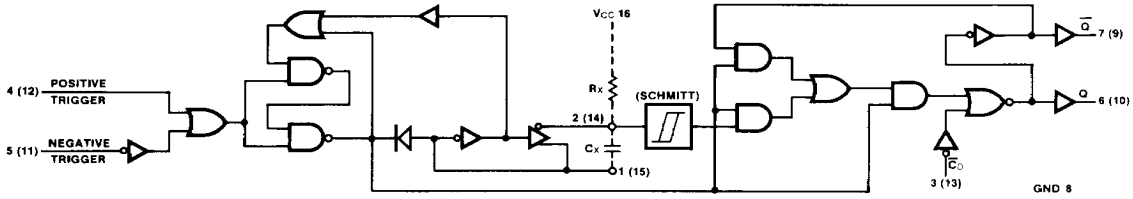
**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C | MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 9602PC, 96L02PC | | 9B |
| Ceramic DIP (D) | A | 9602DC, 96L02DC | 9602DM, 96L02DM | 6B |
| Flatpak (F) | A | 9602FC, 96L02FC | 9602FM, 96L02FM | 4L |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 96XX (U.L.) HIGH/LOW | 96L (U.L.) HIGH/LOW |
|---|---|---|---|
| $\bar{I}_0$ | Trigger Input (Active Falling Edge) | 1.5/1.0 | 0.5/0.25 |
| $I_1$ | Trigger Input (Active Rising Edge) | 1.5/1.0 | 0.5/0.25 |
| $\bar{C}_D$ | Direct Clear Input (Active LOW) | 1.5/1.0 | 0.5/0.25 |
| Q | Positive Pulse Output | 24/7.0 (6.2) | 9.0/3.0 |
| $\bar{Q}$ | Complementary Pulse Output | 24/7.0 (6.2) | 9.0/3.0 |

## FUNCTIONAL BLOCK DIAGRAM




### OPERATION NOTES

1. TRIGGERING — can be accomplished by a positive-going transition on pin 4 (12) or a negative-going transition on pin 5 (11). Triggering begins as a signal crosses the input $V_{IL}$:$V_{IH}$ threshold region; this activates an internal latch whose unbalanced cross-coupling causes it to assume a preferred state. As the latch output goes LOW it disables the gates leading to the Q output and, through an inverter, turns on the capacitor discharge transistor. The inverted signal is also fed back to the latch input to change its state and effectively end the triggering action; thus the latch and its associated feed-back perform the function of a differentiator.

   The emitters of the latch transistors return to ground through an enabling transistor which must be turned off between successive triggers in order for the latch to proceed through the proper sequence when triggering is desired. Pin 5 (11) must be HIGH in order to trigger at pin 4 (12); conversely, pin 4 (12) must be LOW in order to trigger at pin 5 (11).

2. RETRIGGERING — In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 2 (14). The delay will time out when the ramp voltage reaches the upper trigger point of a Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the output. The delay period can therefore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.

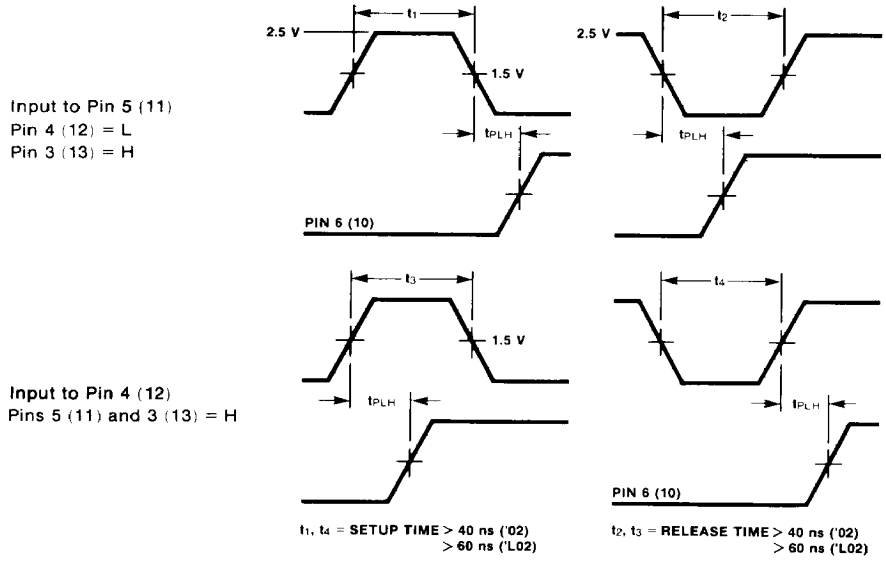
3. NON-RETRIGGERABLE OPERATION — Retriggering can be inhibited logically, by connecting pin 6 (10) back to pin 4 (12) or by connecting pin 7 (9) back to pin 5 (11). Either hook-up has the effect of keeping the latch-enabling transistor turned on during the delay period, which prevents the input latch from cycling as discussed above in the section on triggering.

4. OUTPUT PULSE WIDTH — An external resistor $R_X$ and an external capacitor $C_X$ are required, as shown in the functional block diagram. To minimize stray capacitance and noise pickup, $R_X$ and $C_X$ should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor, $R_X$ should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit. The output pulse width $t_w$ is defined as follows, where $R_X$ is in kΩ, $C_X$ is in pF and $t_w$ is in ns.

   (9602) $t_w = 0.31\ R_X C_X\ (1 + 1/R_X)$ for $C_X \geq 10^3$ pF
   $5\ k\Omega \leq R_X \leq 50\ k\Omega$ for 0°C to +75°C
   $5\ k\Omega \leq R_X \leq 25\ k\Omega$ for -55°C to +125°C
   (96L02) $t_w = 0.33\ R_X C_X\ (1 + 3/R_X)$ for $C_X \geq 10^3$ pF
   $16\ k\Omega \leq R_X \leq 220\ k\Omega$ for 0°C to +75°C
   $20\ k\Omega \leq R_X \leq 100\ k\Omega$ for -55°C to +125°C
   $C_X$ may vary from 0 to any value. For pulse widths with $C_X$ less than $10^3$ pF see *Figures a and b*.

**OPERATION NOTES** (Cont'd)

5. SETUP AND RELEASE TIMES — The setup times listed below are necessary to allow the latch-enabling transistor to turn off and the node voltages within the input latch to stabilize, thus insuring proper cycling of the latch when the next trigger occurs. The indicated release times (equivalent to trigger duration) allow time for the input latch to cycle and its signal to propagate.




6. RESET OPERATION — A LOW signal on $\overline{C}_D$, pin 3 (13), will terminate an output pulse, causing Q to go LOW and $\overline{Q}$ to go HIGH. As long as $\overline{C}_D$ is held LOW, a delay period cannot be initiated nor will attempted triggering cause spikes at the outputs. A reset pulse duration, in the LOW state, of 25 ns is sufficient to insure resetting. If the reset input goes LOW at the same time that a trigger transition occurs, the reset will dominate and the outputs will not respond to the trigger. If the reset input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

7. CAPACITOR LEAKAGE — For recommendations on electrolytic capacitors and larger values of $R_X$, please see the 9600 data sheet.

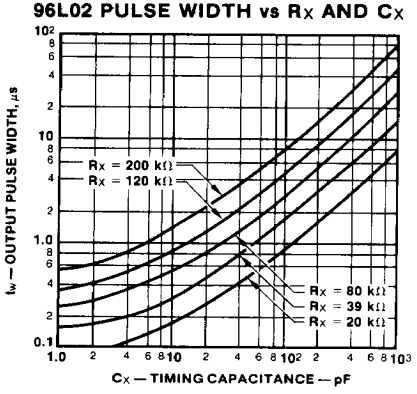



Fig. a

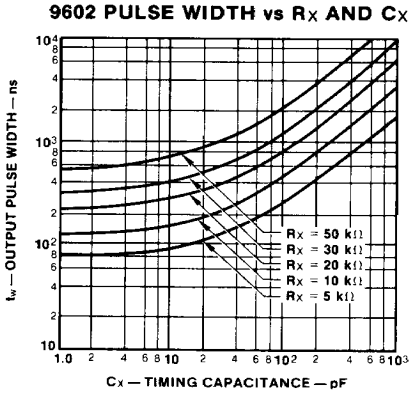
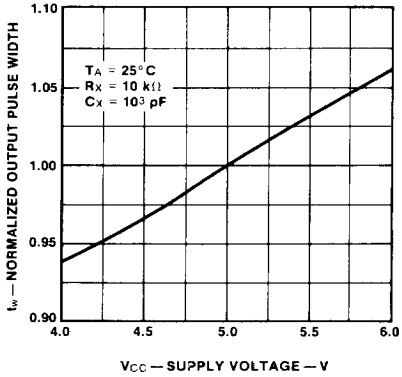


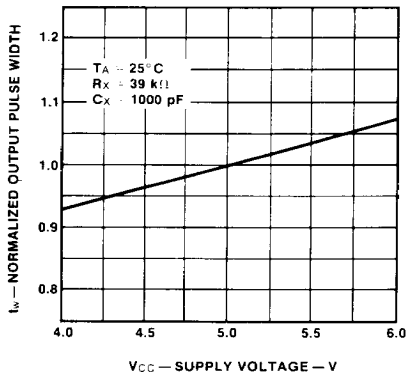

Fig. b

## TYPICAL CHARACTERISTICS

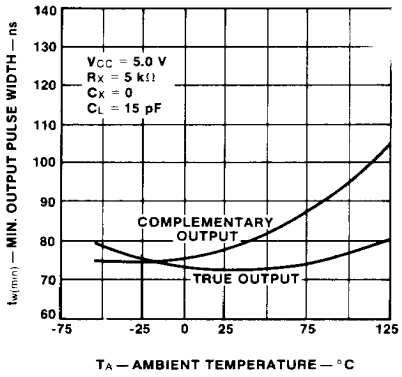
**9602 $t_w$ vs $V_{CC}$**



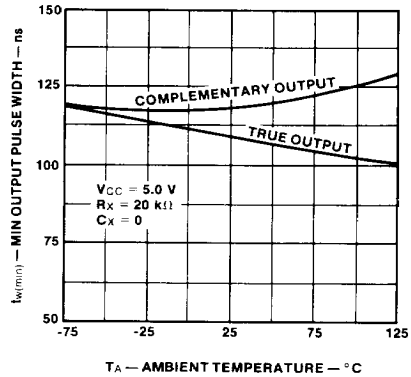

**96L02 $t_w$ vs $V_{CC}$**



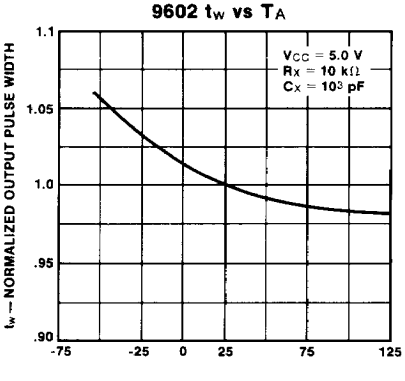

**9602 $t_{w(min)}$ vs $T_A$**



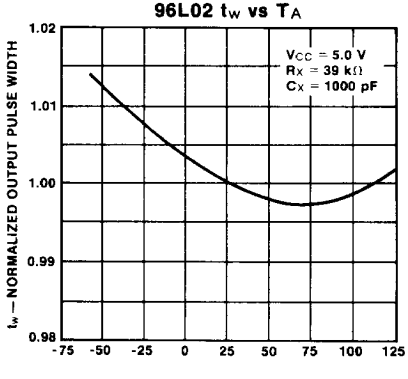

**96L02 $t_{w(min)}$ vs $T_A$**




**9602 $t_w$ vs $T_A$**




**96L02 $t_w$ vs $T_A$**

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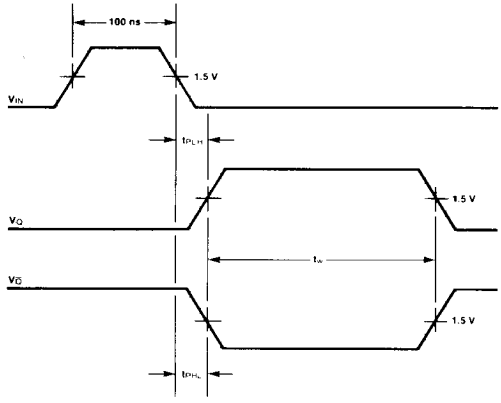
**DC AND AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | | 96XX Min | 96XX Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | | 12.4 | | V | $V_{CC}$ = Min, $I_{OH}$ = -9.6 mA |
| $V_{OL}$ | Output LOW Voltage | XM | | 0.4 | V | $V_{CC}$ = 4.5 V, $I_{OL}$ = 9.92 mA<br>$V_{CC}$ = 5.5 V, $I_{OL}$ = 12.8 mA |
| | | XC | | 0.45 | V | $V_{CC}$ = 4.75 V, $I_{OL}$ = 11.3 mA<br>$V_{CC}$ = 5.25 V, $I_{OL}$ = 12.8 mA |
| $V_{IH}$ | Input HIGH Voltage | XM | 2.0 | | V | Guaranteed Input HIGH Threshold |
| | | XC | 1.9 | | | |
| $V_{IL}$ | Input LOW Voltage | | | 0.85 | V | Guaranteed Input LOW Threshold |
| $I_{IL}$ | Input LOW Current | | | -1.6 | mA | $V_{CC}$ = Max, $V_{IN}$ = $V_{OL}$ |
| $I_{IL}$ | Input LOW Current | XM | | -1.24 | mA | $V_{CC}$ = Min, $V_{IN}$ = $V_{OL}$ |
| | | XC | | -1.14 | | |
| $I_{IH}$ | Input HIGH Current | | | 60 | $\mu$A | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V |
| $I_{OS}$ | Output Short Circuit Current | XM | | -25 | mA | $V_{CC}$ = Max, $V_{OUT}$ = 1.0 V |
| | | XC | | -35 | | |
| $I_{CC}$ | Power Supply Current | XM | | 45 | mA | $V_{CC}$ = 5.0 V |
| | | XC | | 52 | | |
| $t_{PLH}$ | Propagation Delay $\overline{I_0}$ to Q | XM | | 35 | ns | $R_X$ = 5 kΩ, $C_X$ = 0<br>$C_L$ = 15 pF, Fig. c |
| | | XC | | 40 | | |
| $t_{PHL}$ | Propagation Delay $\overline{I_0}$ to $\overline{Q}$ | XM | | 43 | ns | $R_X$ = 5 kΩ, $C_X$ = 0<br>$C_L$ = 15 pF, Fig. c |
| | | XC | | 48 | | |
| $t_w$ (min) | Minimum Output Pulse Width at Q | XM | | 90 | ns | $R_X$ = 5 kΩ, $C_X$ = 0<br>$C_L$ = 15 pF, Fig. c |
| | | XC | | 100 | | |
| | Minimum Output Pulse Width at $\overline{Q}$ | XM | | 100 | | |
| | | XC | | 110 | | |
| $t_w$ | Output Pulse Width | | 3.08 | 3.76 | $\mu$s | $R_X$ = 10 kΩ<br>$C_X$ = 1000 pF, Fig. c |
| $C_{STRAY}$ | Maximum Stray Capacitance from Pin 2 (14) to Gnd | | | 50 | pF | |
| $R_X$ | Timing Resistor Range | XM | 5.0 | 25 | kΩ | |
| | | XC | 5.0 | 50 | | |

**DC AND AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | | 96L Min | 96L Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | | 2.4 | | V | $V_{CC}$ = Min, $I_{OH}$ = -0.36 mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.3 | V | $V_{CC}$ = Min, $I_{OL}$ = 4.8 mA |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | V | Guaranteed Input HIGH Threshold |
| $V_{IL}$ | Input LOW Voltage | | | 0.7 | V | Guaranteed Input LOW Threshold |
| $I_{IH}$ | Input HIGH Current | | | 20<br>1.0 | $\mu$A<br>mA | $V_{IN}$ = 2.4 V<br>$V_{IN}$ = 5.5 V<br>$V_{CC}$ = Max |
| $I_{IL}$ | Input LOW Current | | | -0.4 | mA | $V_{CC}$ = Max, $V_{IN}$ = 0.3 V |
| $I_{OS}$ | Output Short Circuit Current | | -2.0 | -13 | mA | $V_{CC}$ = Max, $V_{OUT}$ = 1.0 V |
| $I_{CC}$ | Power Supply Current | | | 16 | mA | $V_{CC}$ = Max |
| $t_{PLH}$ | Propagation Delay $\overline{I_0}$ to Q | XM<br>XC | | 75<br>80 | ns | $V_{CC}$ = 5.0 V, $R_X$ = 20 kΩ<br>$C_X$ = 0, $C_L$ = 15 pF<br>$T_A$ = 25°C |
| $t_{PHL}$ | Propagation Delay $\overline{I_0}$ to $\overline{Q}$ | XM<br>XC | | 62<br>65 | ns | $V_{CC}$ = 5.0 V, $R_X$ = 20 kΩ<br>$C_X$ = 0, $C_L$ = 15 pF<br>$T_A$ = 25°C |
| $t_w$ (min) | Minimum Output Pulse Width at Q | | | 110* | ns | $V_{CC}$ = 5.0 V, $R_X$ = 20 kΩ<br>$C_X$ = 0, $C_L$ = 15 pF<br>$T_A$ = 25°C |
| $t_w$ | Output Pulse Width | | 12.4 | 15.2 | $\mu$s | $V_{CC}$ = 5.0 V, $R_X$ = 39 kΩ<br>$C_X$ = 1000 pF, $T_A$ = 25°C |
| $\Delta t$ | Change in Q Pulse Width Over Temperature | XC | | 1.6 | % | $R_X$ = 39 kΩ, $C_X$ = 1000 pF |
| $R_X$ | Timing Resistor Range | XM<br>XC | | 100<br>220 | kΩ | |

*Typical Value




INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 10$ ns

**Fig. c**

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