

74HC423; 74HCT423

Dual retriggerable monostable multivibrator with reset

Rev. 6 — 19 December 2011

Product data sheet

1. General description

74HC423; 74HCT423 are high-speed Si-gate CMOS devices that are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC423; 74HCT423 dual retriggerable monostable multivibrator with reset has two methods of output pulse width control.

1. The minimum pulse width is essentially determined by the selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}), see [Section 12.1](#).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\bar{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period ($nQ = \text{HIGH}$, $n\bar{Q} = \text{LOW}$) can be made as long as desired. When $n\bar{RD}$ is LOW, it forces the nQ output LOW, the $n\bar{Q}$ output HIGH and also inhibits the triggering. [Figure 10](#) and [Figure 11](#) illustrate pulse control by reset.

The $n\bar{A}$ and nB inputs' Schmitt trigger action makes them highly tolerant to slower input rise and fall times.

The 74HC423; 74HCT423 are identical to the 74HC123; 74HCT123 except that they cannot be triggered via the reset input.

2. Features and benefits

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC423N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT423N				
74HC423D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT423D				
74HC423BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT423BQ				
74HCT423DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT423PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

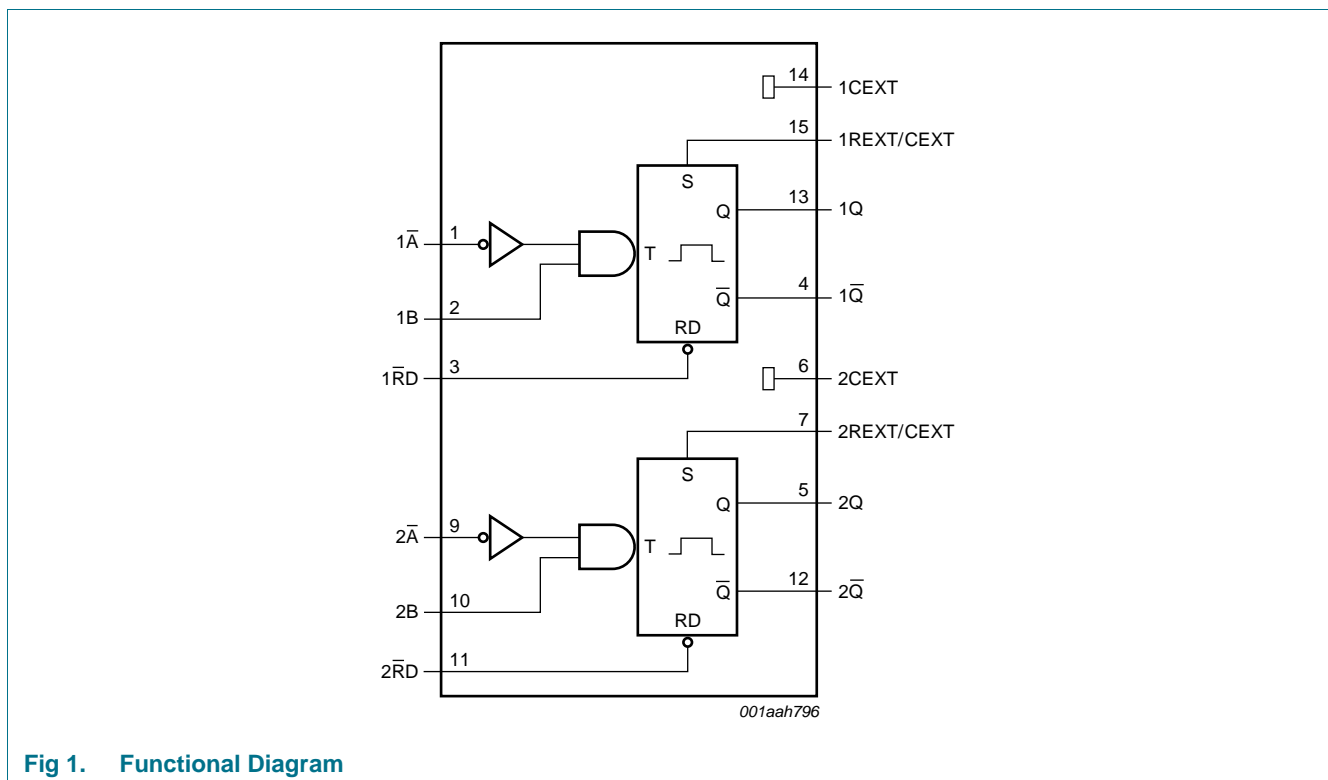


Fig 1. Functional Diagram

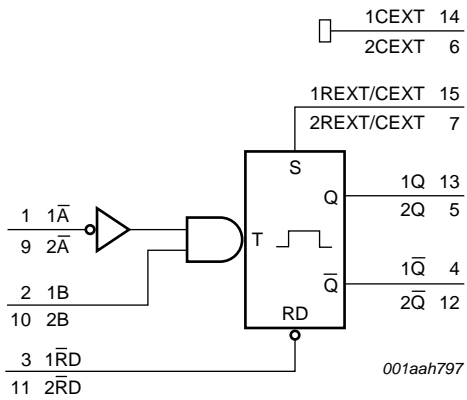


Fig 2. Logic symbol

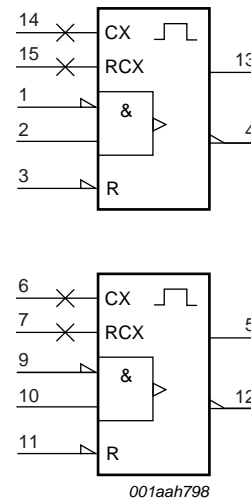


Fig 3. IEC Logic symbol

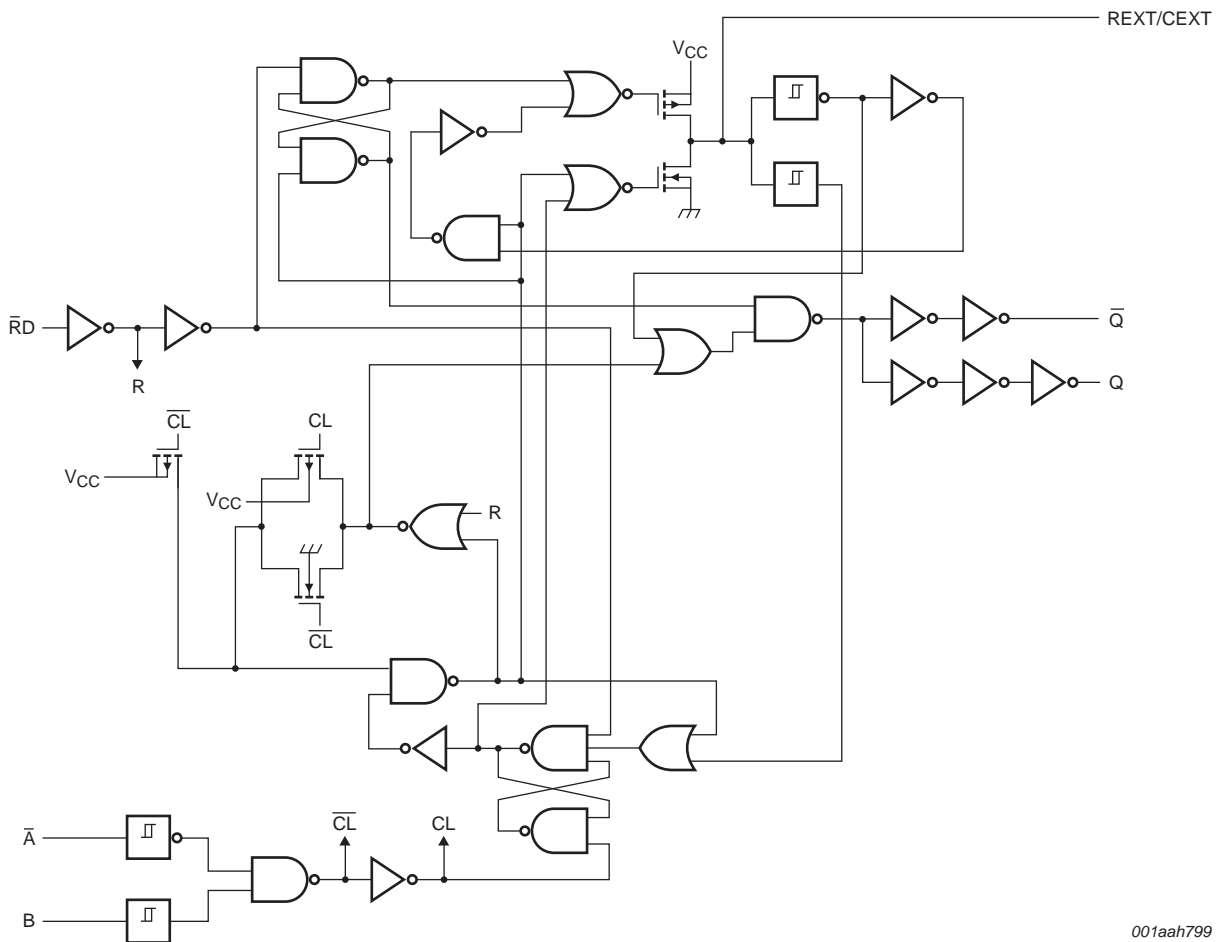
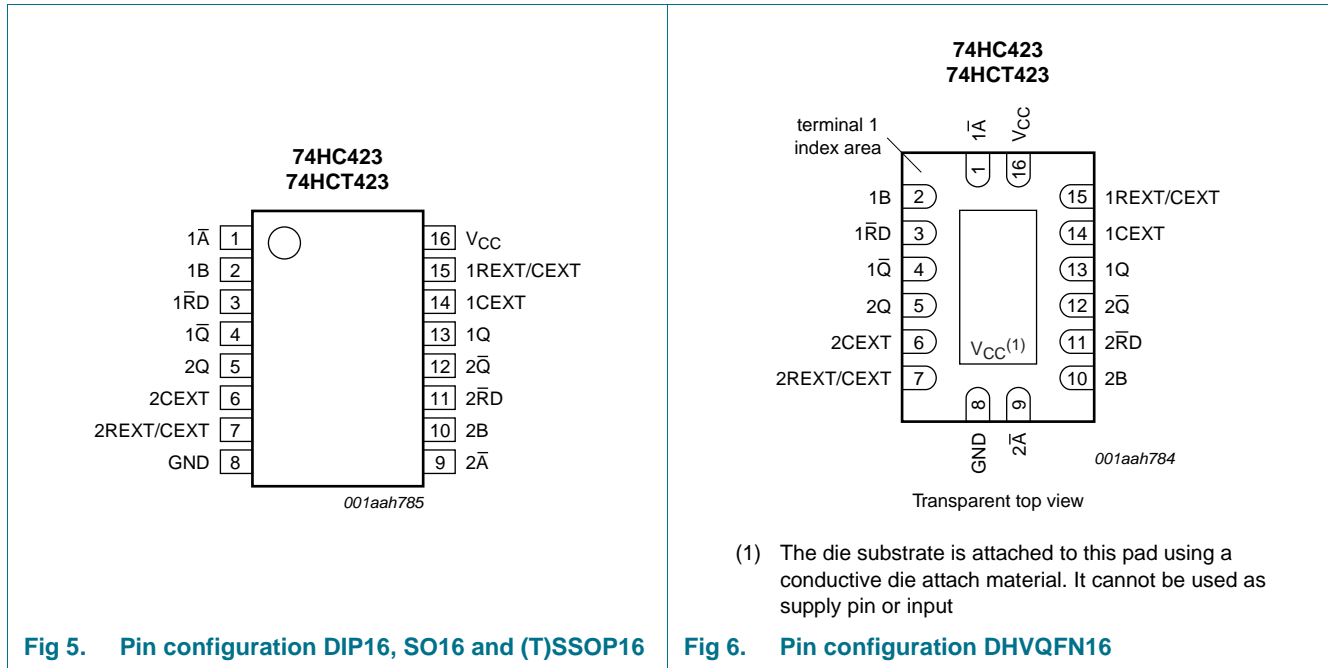


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning







5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1 \bar{A} , 2 \bar{A}	1, 9	trigger input (negative edge triggered)
1B, 2B	2, 10	trigger input (positive edge triggered)
1 $\bar{R}D$, 2 $\bar{R}D$	3, 11	direct reset (active LOW)
1 \bar{Q} , 2 \bar{Q}	4, 12	output (active LOW)
GND	8	ground (0 V)
1Q, 2Q	13, 5	output (active HIGH)
1CEXT, 2CEXT	14, 6	external capacitor connection
1REXT/CEXT, 2REXT/CEXT	15, 7	external resistor/capacitor connection
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Input			Output	
nRD	nA	nB	nQ	nQ
L	X	X	L	H
X	H	X	L ^[2]	H ^[2]
X	X	L	L ^[2]	H ^[2]
H	L	↑		
H	↓	H		

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH transition;
 ↓ = HIGH-to-LOW transition;

 = one HIGH level output pulse;

 = one LOW level output pulse.

- [2] If the monostable multivibrator was triggered before this condition was established, the pulse will continue as programmed.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	^[1] -	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	^[1] -	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	DIP16 package	^[2] -	750	mW
		SO16, SSOP16, TSSOP16 and DHVQFN16 packages	^[3] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly at 12 mW/K.

- [3] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K;
 For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K;
 For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC423			74HCT423			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC423										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT423										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}; V_{CC} = 4.5\text{ V}$								
		$I_O = -20\ \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}; V_{CC} = 4.5\text{ V}$								
		$I_O = 20\ \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 5.5\text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{CC}	supply current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 5.5\text{ V}; I_O = 0\text{ A}$	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}; I_O = 0\text{ A}$								
		nA, nB inputs	-	35	126	-	158	-	172	μA
		nRD input	-	50	180	-	225	-	245	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC423										
t_{pd}	propagation delay	$n\bar{A}$ or nB to nQ or $n\bar{Q}$; $R_{EXT} = 5\text{ k}\Omega$; $C_{EXT} = 0\text{ pF}$; see Figure 7	[1]							
		$V_{CC} = 2.0\text{ V}$	-	80	255	-	320	-	385	ns
		$V_{CC} = 4.5\text{ V}$	-	29	51	-	64	-	77	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	25	-	-	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	23	43	-	54	-	65	ns
		$n\bar{RD}$ to nQ or $n\bar{Q}$; see Figure 7	[1]							
		$V_{CC} = 2.0\text{ V}$	-	66	215	-	270	-	325	ns
		$V_{CC} = 4.5\text{ V}$	-	24	43	-	54	-	65	ns
t_t	transition time	see Figure 7	[2]							
		$V_{CC} = 2.0\text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns
t_W	pulse width	$n\bar{A}$ input LOW; see Figure 7 and Figure 8								
		$V_{CC} = 2.0\text{ V}$	100	11	-	125	-	150	-	ns
		$V_{CC} = 4.5\text{ V}$	20	4	-	25	-	30	-	ns
		$V_{CC} = 6.0\text{ V}$	17	3	-	21	-	26	-	ns
		nB input HIGH; see Figure 7 and Figure 8								
		$V_{CC} = 2.0\text{ V}$	100	17	-	125	-	150	-	ns
		$V_{CC} = 4.5\text{ V}$	20	6	-	25	-	30	-	ns
		$V_{CC} = 6.0\text{ V}$	17	5	-	21	-	26	-	ns
		$n\bar{RD}$ input LOW; see Figure 7 and Figure 8								
		$V_{CC} = 2.0\text{ V}$	100	14	-	125	-	150	-	ns
		$V_{CC} = 4.5\text{ V}$	20	5	-	25	-	30	-	ns
		$V_{CC} = 6.0\text{ V}$	17	4	-	21	-	26	-	ns
t_{trig}	retrigger time	nQ HIGH or $n\bar{Q}$ LOW; $V_{CC} = 5.0\text{ V}$; $R_{EXT} = 10\text{ k}\Omega$; $C_{EXT} = 100\text{ nF}$; see Figure 7 and Figure 8		450	-	-	-	-	-	μs
		nQ HIGH or $n\bar{Q}$ LOW; $V_{CC} = 5.0\text{ V}$; $R_{EXT} = 5\text{ k}\Omega$; $C_{EXT} = 0\text{ pF}$; $V_I = GND$ to V_{CC} ; see Figure 7 and Figure 8	[3]	75	-	-	-	-	-	ns
		$n\bar{A}$ or nB input; $V_{CC} = 5.0\text{ V}$; $R_{EXT} = 5\text{ k}\Omega$; $C_{EXT} = 0\text{ pF}$; see Figure 10	[4]	110	-	-	-	-	-	ns

Table 7. Dynamic characteristics ...continued
GND = 0 V; test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
R _{EXT}	external timing resistor	V _{CC} = 2.0 V; see Figure 8	10	-	1000	-	-	-	-	kΩ
		V _{CC} = 5.0 V	2	-	1000	-	-	-	-	kΩ
C _{EXT}	external timing capacitor	V _{CC} = 5.0 V; see Figure 8	no limits						pF	
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC}	-	54	-	-	-	-	-	pF

74HCT423

t _{pd}	propagation delay	n \bar{A} or nB to nQ or n \bar{Q} ; R _{EXT} = 5 kΩ; C _{EXT} = 0 pF; see Figure 7									
		V _{CC} = 4.5 V	[1]	-	30	51	-	64	-	77	ns
		V _{CC} = 5.0 V; C _L = 15 pF	[1]	-	26	-	-	-	-	-	ns
		n \bar{RD} to nQ or n \bar{Q} ; R _{EXT} = 5 kΩ; C _{EXT} = 0 pF; see Figure 7	[1]	-	26	48	-	60	-	72	ns
		V _{CC} = 4.5 V	[1]	-	26	48	-	60	-	72	ns
		V _{CC} = 5.0 V; C _L = 15 pF	[1]	-	22	-	-	-	-	ns	
t _t	transition time	V _{CC} = 4.5 V; Figure 7	[2]	-	7	15	-	19	-	22	ns
t _w	pulse width	trigger pulse; n \bar{A} input LOW; V _{CC} = 4.5 V; see Figure 7 and Figure 10	20	5	-	25	-	30	-	ns	
		trigger pulse; nB input HIGH; V _{CC} = 4.5 V; see Figure 7 and Figure 10	20	5	-	25	-	30	-	ns	
		reset pulse; n \bar{RD} input LOW; V _{CC} = 4.5 V; see Figure 7 and Figure 11	20	7	-	25	-	30	-	ns	
		output pulse; nQ HIGH or n \bar{Q} LOW; V _{CC} = 5.0 V; R _{EXT} = 10 kΩ; C _{EXT} = 100 nF; see Figure 7 , Figure 10 and Figure 11	-	450	-	-	-	-	-	-	μs
		output pulse; nQ HIGH or n \bar{Q} LOW; V _{CC} = 5.0 V; R _{EXT} = 5 kΩ; C _{EXT} = 0 pF; V _I = GND to V _{CC} - 1.5 V; see Figure 7 , Figure 10 and Figure 11	[3]	-	75	-	-	-	-	-	ns
t _{rtrig}	retrigger time	n \bar{A} or nB input; V _{CC} = 5.0 V; R _{EXT} = 5 kΩ; C _{EXT} = 0 pF; see Figure 10	-	110	-	-	-	-	-	ns	
R _{EXT}	external timing resistor	V _{CC} = 5.0 V; see Figure 8	2	-	1000	-	-	-	-	kΩ	
C _{EXT}	external timing capacitor	V _{CC} = 5.0 V; see Figure 8	no limits						pF		

Table 7. Dynamic characteristics ...continued
GND = 0 V; test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V [6]	-	56	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] For other R_{EXT} and C_{EXT} combinations see [Figure 8](#). If C_{EXT} > 10 pF, the next formula is valid:

t_W = K × R_{EXT} × C_{EXT} (typ.), where:

t_W = output pulse width in ns;

R_{EXT} = external resistor in kΩ;

C_{EXT} = external capacitor in pF;

K = 0.55 for V_{CC} = 2.0 V and 0.45 for V_{CC} = 5.0 V; see [Figure 9](#).

Inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[4] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

If C_{EXT} > 10 pF, the next formula (at V_{CC} = 5.0 V) for the set-up time of a retrigger pulse is valid:

t_{trig} = 30 + 0.19 × R_{EXT} × C_{EXT}^{0.9} + 13 × R_{EXT}^{1.05} (typ.); where:

t_{trig} = retrigger time in ns;

C_{EXT} = external capacitor in pF;

R_{EXT} = external resistor in kΩ.

Inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[5] When the device is powered-up, initiate the device via a reset pulse, when C_{EXT} < 50 pF.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o); where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

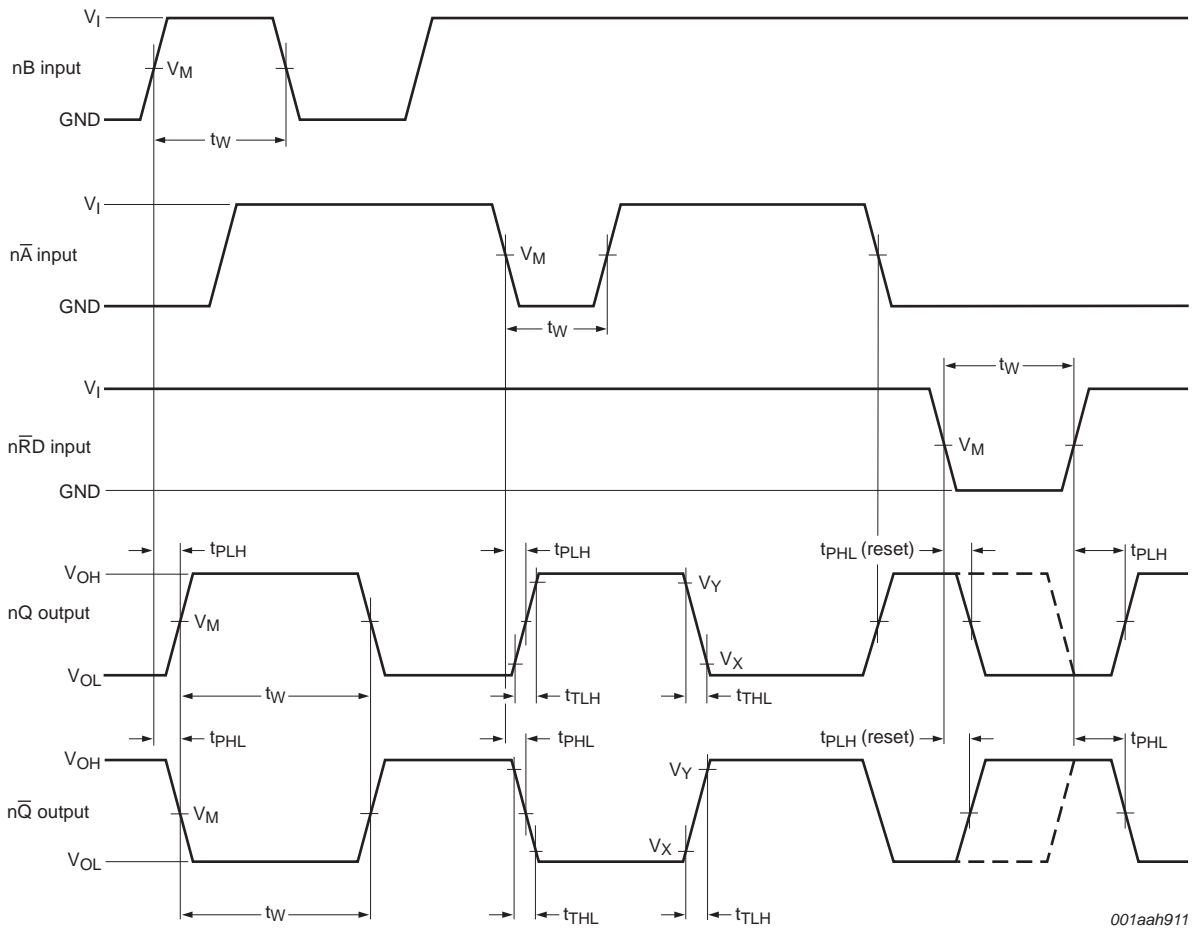
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

11. Waveforms



001aah911

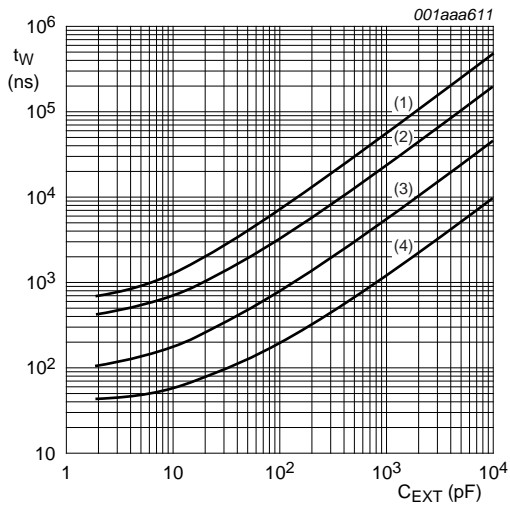
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Pulse widths, propagation delays from inputs (nA-bar, nB, nRD) to outputs (nQ, nQ-bar) and output transition times

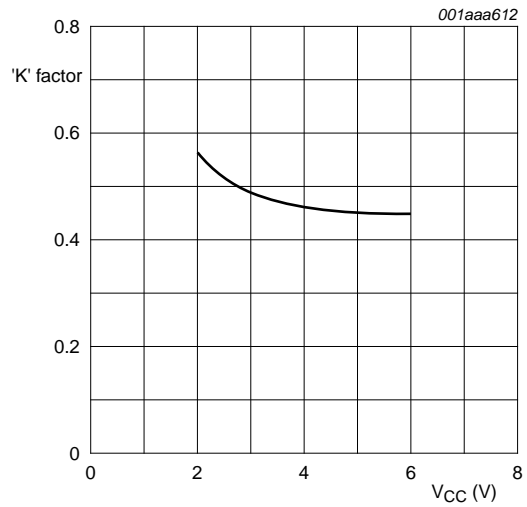
Table 8. Measurement points

Type	Input		Output		
	V _I	V _M	V _M	V _X	V _Y
74HC423	V _{CC}	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}
74HCT423	3 V	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}



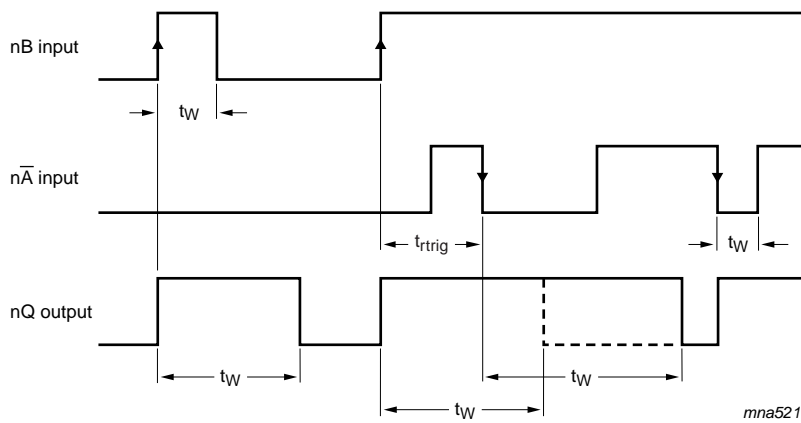
$V_{CC} = 5.0\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.
 (1) $R_{EXT} = 100\text{ k}\Omega$.
 (2) $R_{EXT} = 50\text{ k}\Omega$.
 (3) $R_{EXT} = 10\text{ k}\Omega$.
 (4) $R_{EXT} = 2\text{ k}\Omega$.

Fig 8. Typical output pulse width as a function of the external capacitor values



External capacitance = 10 nF,
 external resistance = 10 kΩ to 100 kΩ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig 9. Typical 'K' factor



$\overline{nRD} = \text{HIGH}$.

Fig 10. Output pulse control using retrigger pulse (t_{rtrig})

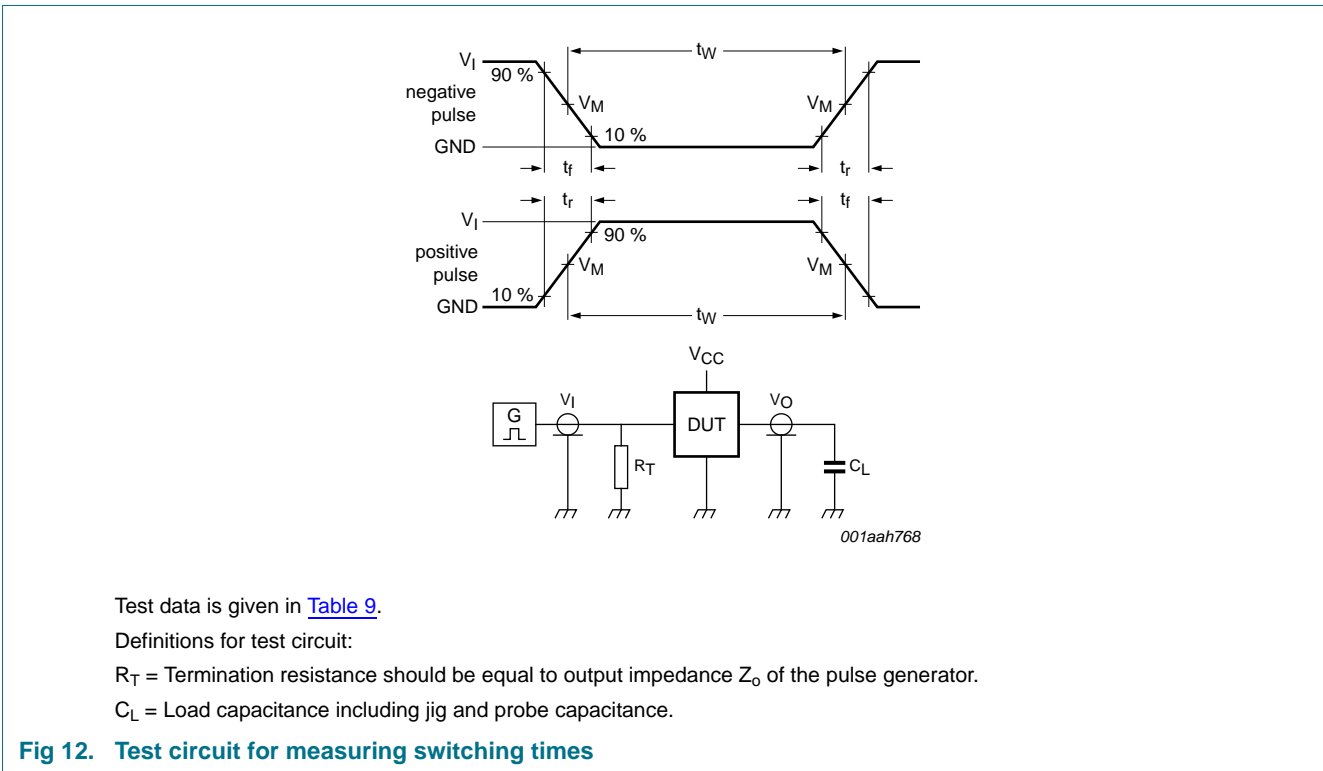
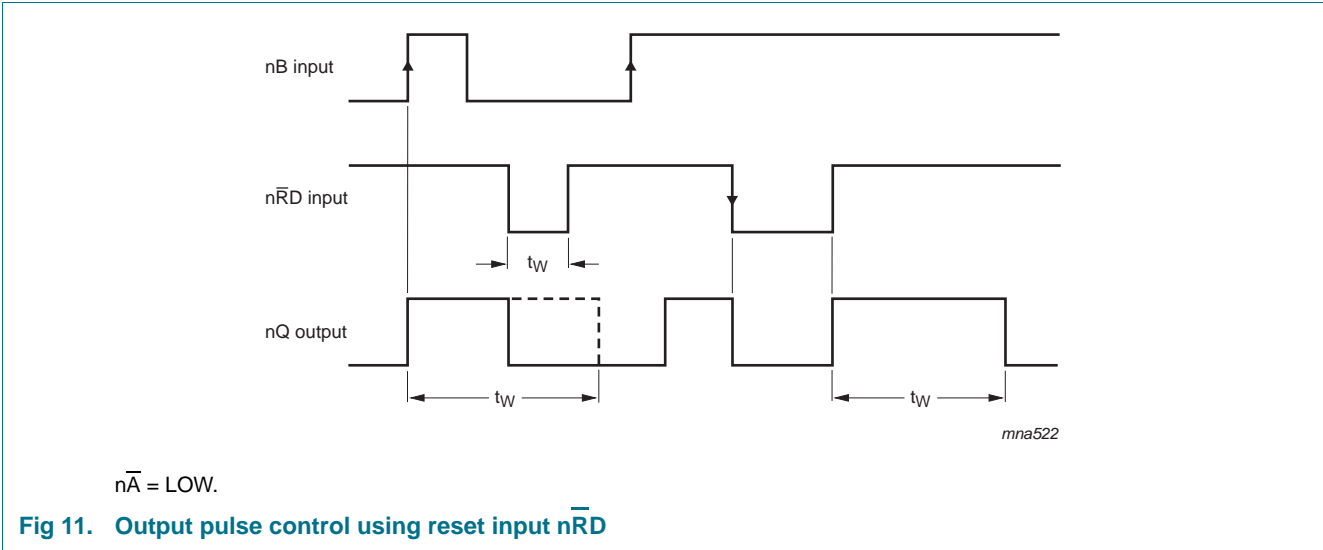


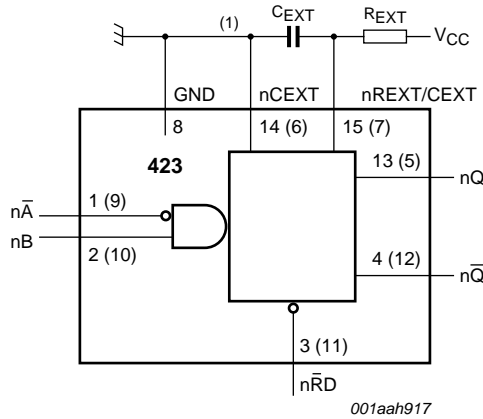
Table 9. Test data

Supply	Input	Load
V_{CC}	V_I	C_L
2.0 V to 6.0 V	V_{CC}	15 pF, 50 pF
		t_r, t_f
		6 ns

12. Application information

12.1 Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT} .



- (1) For minimum noise generation it is recommended that the nCEXT pins (6, 14) are connected to ground externally to the GND pin (8).

Fig 13. Timing component connections

12.1.1 Minimum monostable pulse width

To set the minimum pulse width, when $C_{EXT} < 10 \text{ nF}$, see [Figure 8](#) and when $C_{EXT} > 10 \text{ nF}$, the output pulse width is defined as:

$$t_W = 0.45 \times R_{EXT} \times C_{EXT} \text{ (typ.)}, \text{ where:}$$

t_W = pulse width in μs ;

R_{EXT} = external resistor in $\text{k}\Omega$;

C_{EXT} = external capacitor in nF .

12.2 Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT} , this output pulse can be eliminated using the circuit shown in [Figure 14](#).

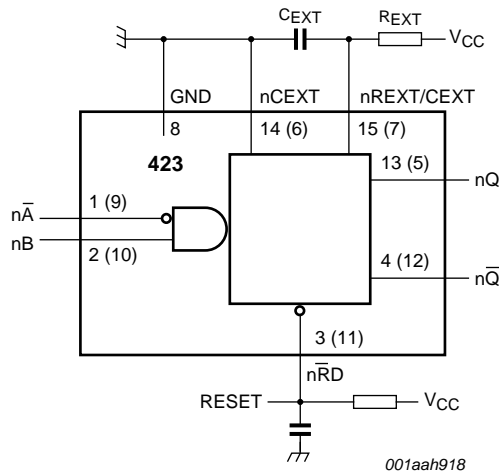


Fig 14. Power-up output pulse elimination circuit

12.3 Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the capacitor's stored energy. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode D_{EXT} preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in [Figure 15](#).

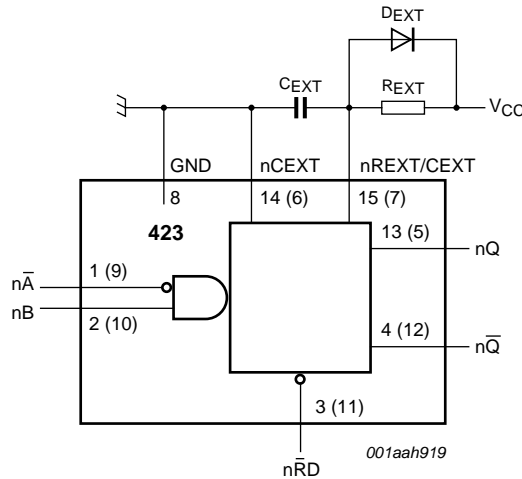


Fig 15. Power-down protection circuit

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

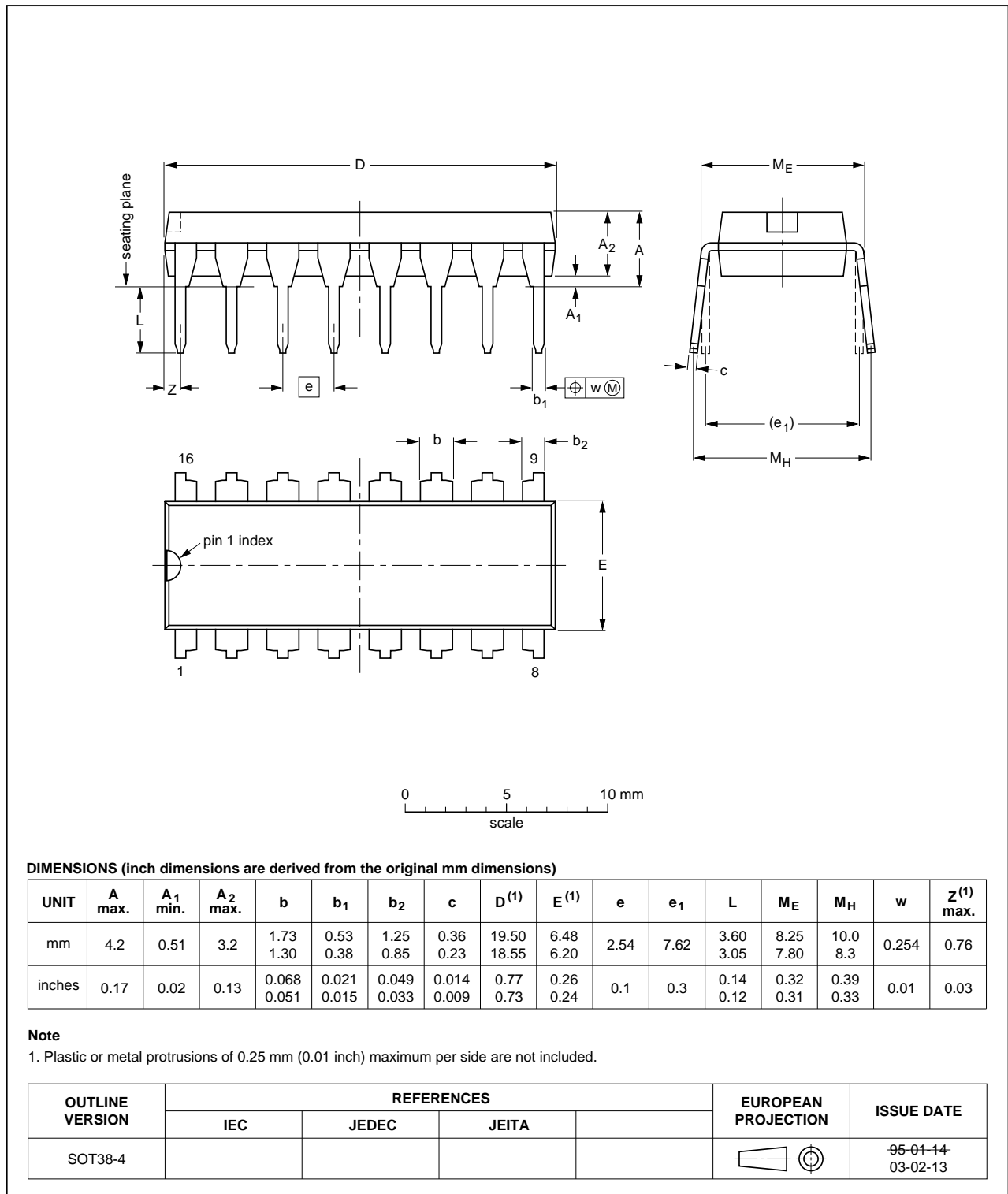


Fig 16. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

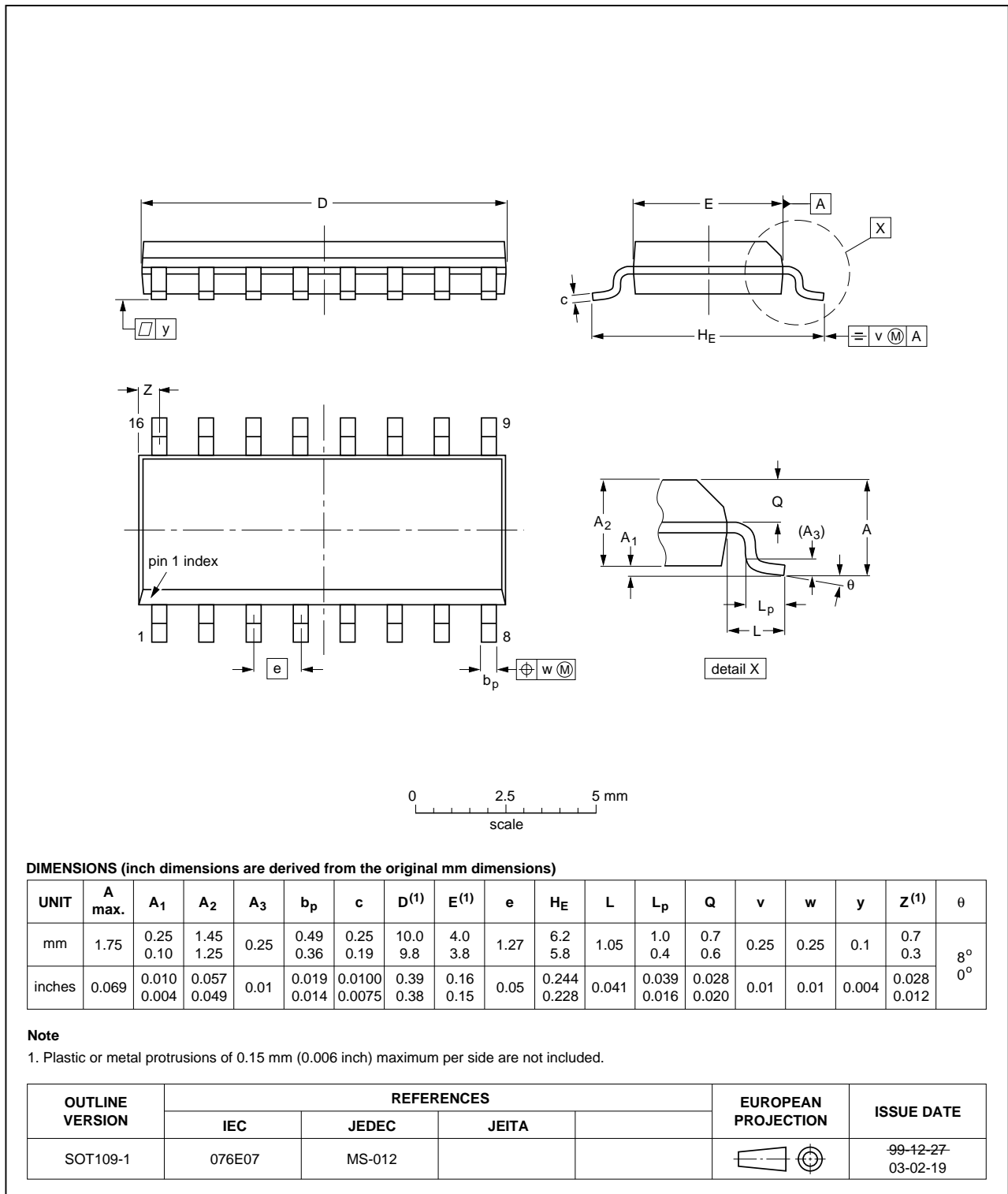


Fig 17. Package outline SOT109-1 (SO16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

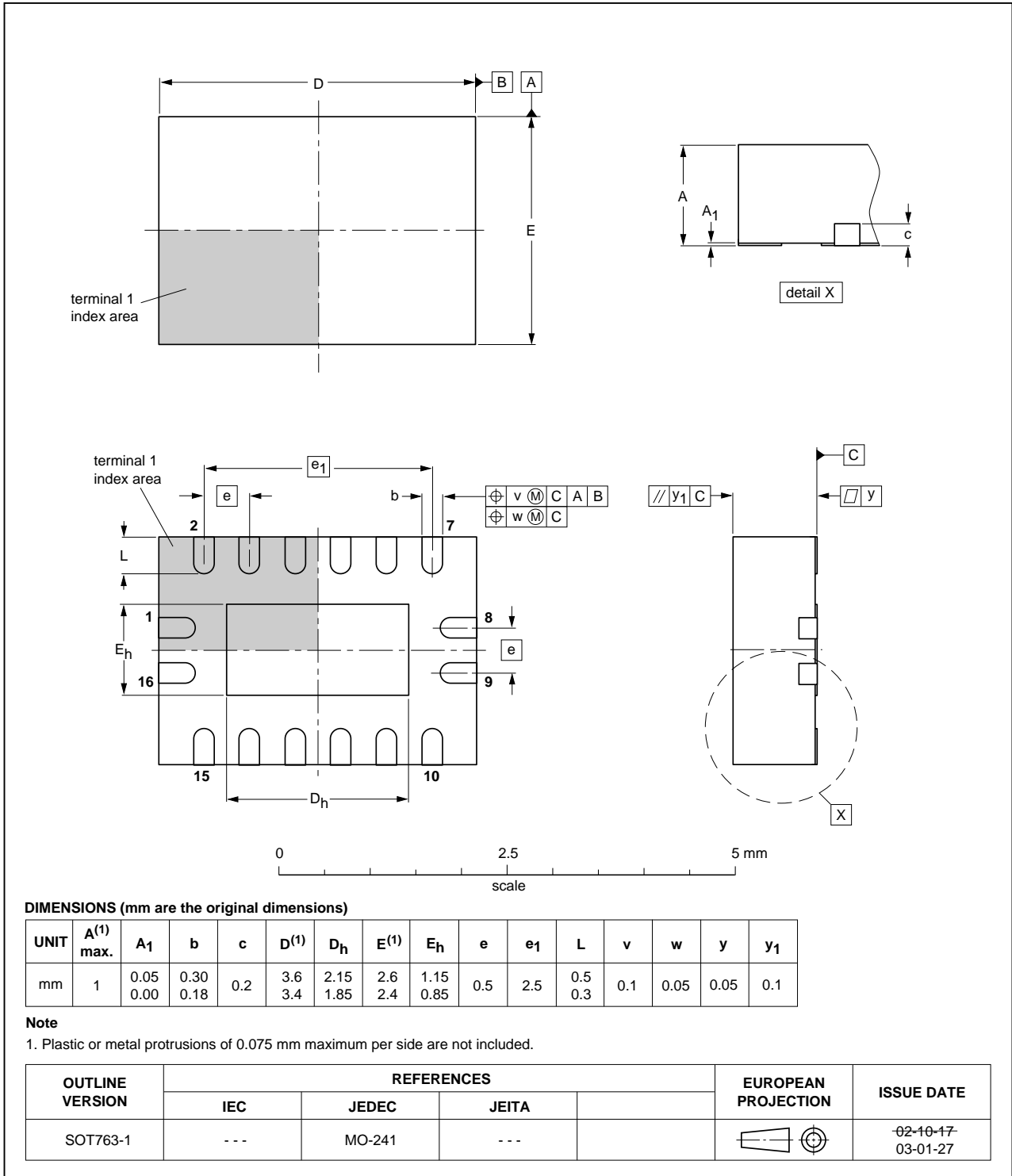


Fig 18. Package outline SOT763-1 (DHVQFN16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

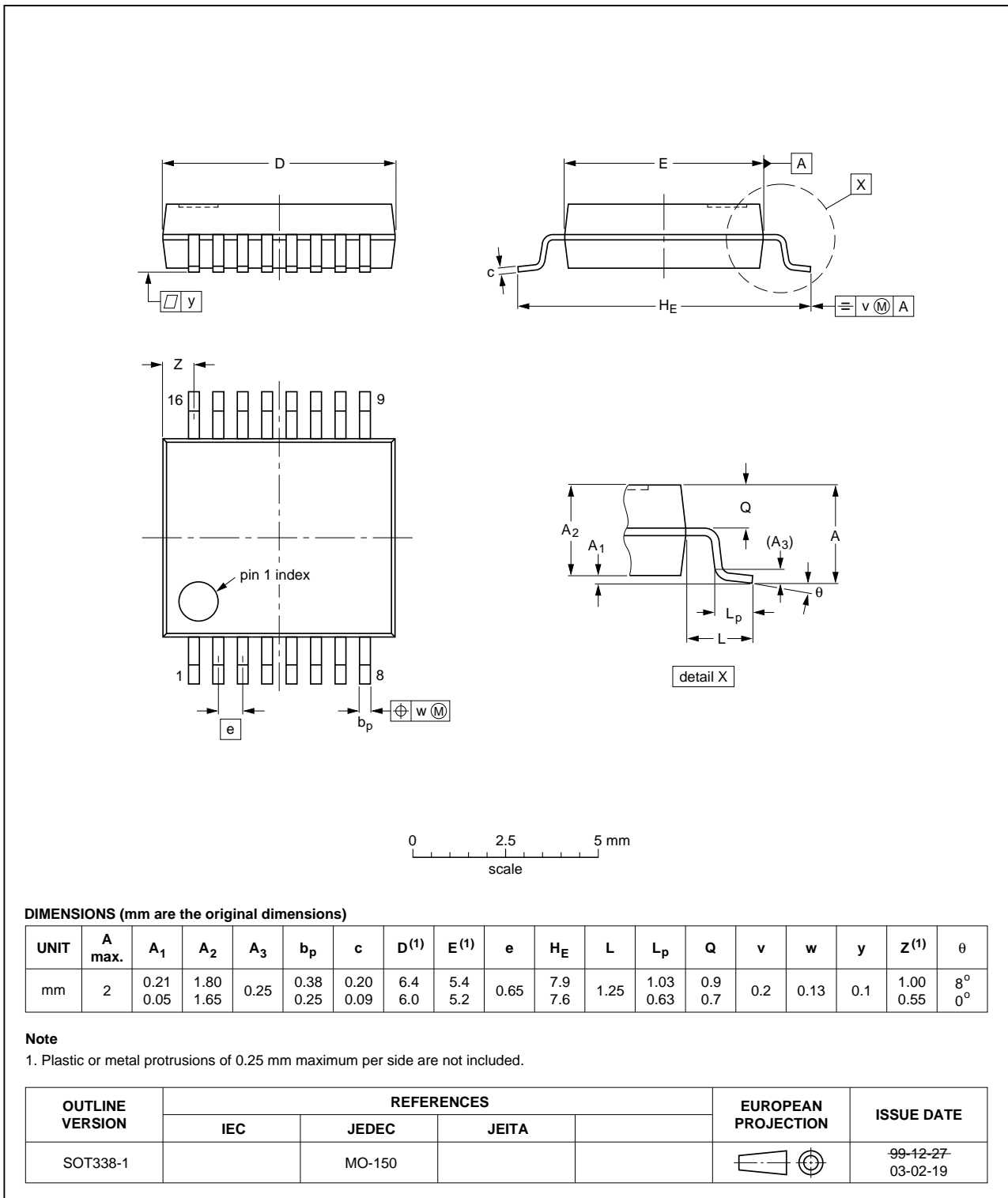


Fig 19. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

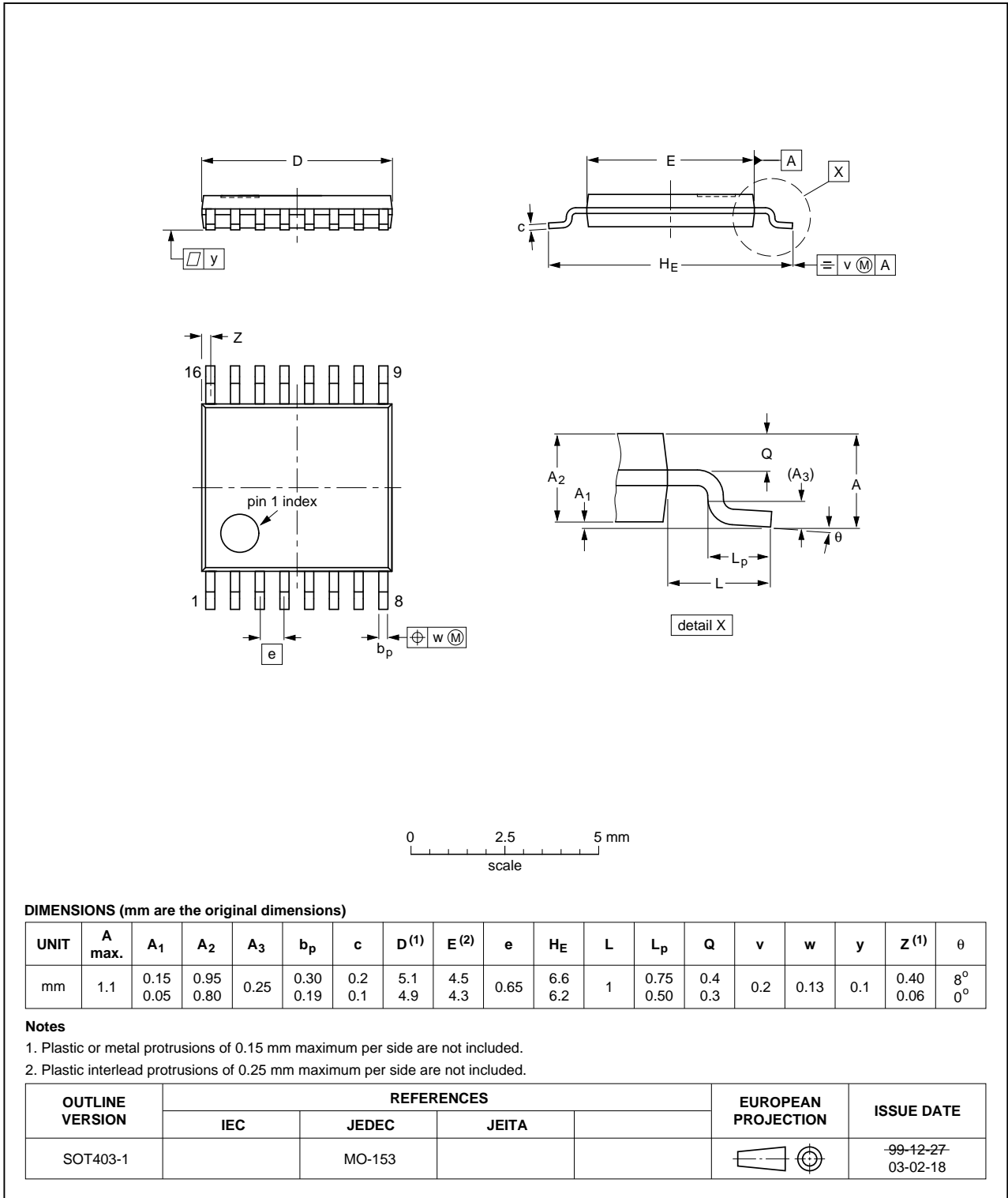


Fig 20. Package outline SOT403-1 (TSSOP16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT423 v.6	20111219	Product data sheet	-	74HC_HCT423 v.5
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74HC_HCT423 v.5	20110825	Product data sheet	-	74HC_HCT423 v.4
74HC_HCT423 v.4	20110318	Product data sheet	-	74HC_HCT423 v.3
74HC_HCT423 v.3	20080724	Product data sheet	-	74HC_HCT423_CNV v.2
74HC_HCT423_CNV v.2	19980708	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
7	Limiting values	5
8	Recommended operating conditions	6
9	Static characteristics	6
10	Dynamic characteristics	8
11	Waveforms	11
12	Application information	14
12.1	Timing component connections	14
12.1.1	Minimum monostable pulse width	14
12.2	Power-up considerations	14
12.3	Power-down considerations	15
13	Package outline	16
14	Abbreviations	21
15	Revision history	21
16	Legal information	22
16.1	Data sheet status	22
16.2	Definitions	22
16.3	Disclaimers	22
16.4	Trademarks	23
17	Contact information	23
18	Contents	24

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 19 December 2011

Document identifier: 74HC_HCT423