



# FAN8831

## Sinusoidal Piezoelectric Actuator Driver with Step-Up DC-DC Converter

### Features

#### Step-Up DC-DC Converter

- Integrated Step-up Power Switch up to 36 V
- Wide Operating Voltage Range of 2.7 to 5.5 V
- Adjustable Step-up Output Voltage
- Adjustable Step-up Current Limit
- Zero Current Detector (ZCD)
- Internal Soft-Start
- Built-in Protection Circuit
  - Over Voltage Protection (OVP)
  - Thermal Shutdown (TSD)

#### Piezo Actuator Driver

- Integrated Full-Bridge Switches ( $V_{DS}=75\text{ V}$ )
- Digitally Implemented Sine Modulator

#### Package Information

- Small 4.0 mm × 4.0 mm MLP

### Applications

- Piezo Actuator

### Description

The FAN8831 is a single-chip piezoelectric actuator driver consisting of step-up DC-DC converter with integrated 36 V boost switch and a full-bridge output stage. The device is capable of driving a Piezo bi-directionally at 120 V peak-to-peak from a single 3 V lithium cell. The step-up DC-DC converter operates in Critical Conduction Mode (CRM) and is optimized to work in a coupled inductor configuration to provide output voltages in excess of 60 V. Over-voltage protection, over-current protection and thermal shutdown are all provided. An internal ready is used to enable the full-bridge gate driver when step-up DC-DC converter output voltage reaches the proper level with hysteresis.

The boost voltage is set using external resistors, and step-up current limit is programmable via the external resistor at OCP pin.

The output H-bridge features four integrated 75 V P and N-channel for sine wave drive of the Piezo actuator.

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN8831MPX	-40°C to +125°C	24-Lead, MLP	Tape & Reel

### Application Diagram

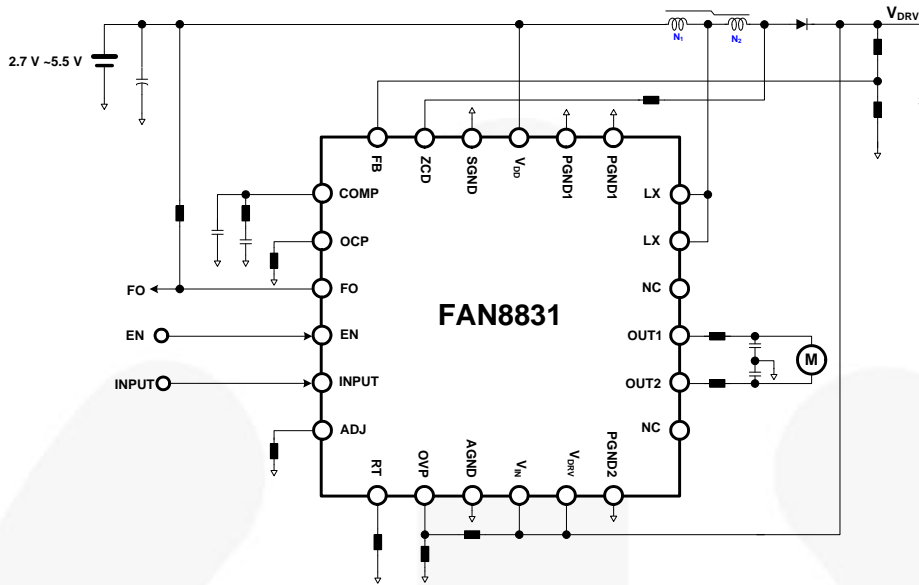


Figure 1. Typical Application Circuit for Piezo Actuator Driver

### Internal Block Diagram

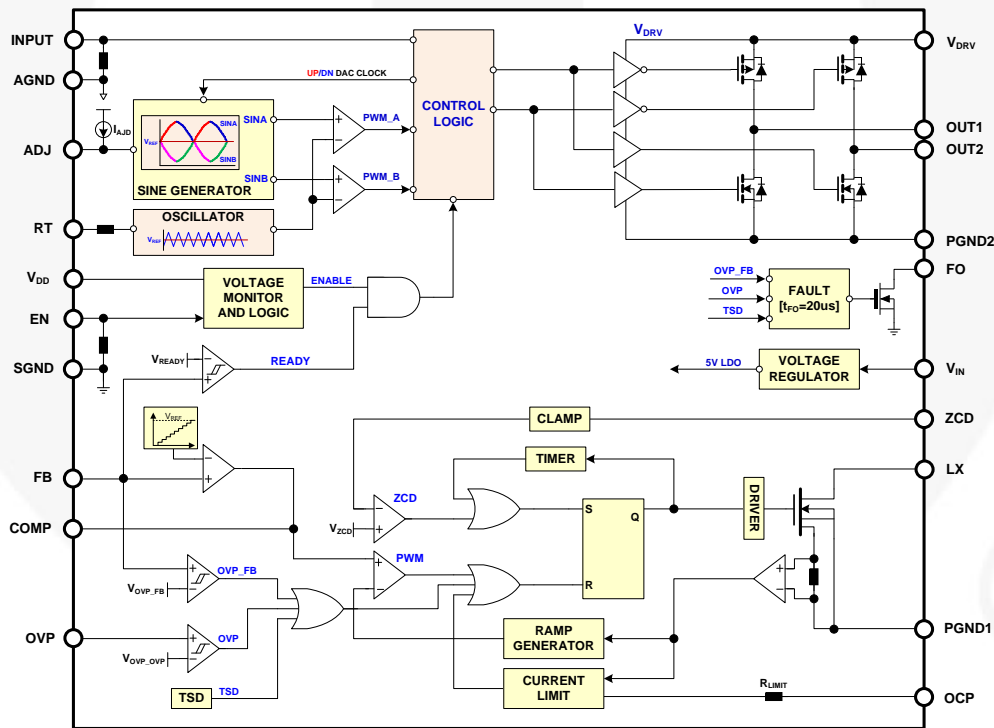


Figure 2. Functional Block Diagram

## Pin Configuration

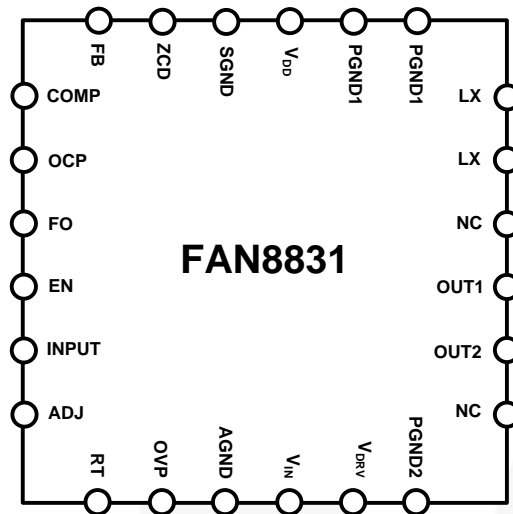


Figure 3. Pin Assignments

## Pin Definitions

Pin #	Name	Description
1,2	PGND1	Power Ground 1. It is connected to the source of the step-up switch.
3	V <sub>DD</sub>	Power supply of step-up DC-DC converter.
4	SGND	Signal Ground. The signal ground for step-up DC-DC converter circuitry.
5	ZCD	The input of the zero current detection.
6	FB	Step-up DC-DC converter output voltage feedback input.
7	COMP	Output of the transconductance error amplifier.
8	OCP	Sets Step-up DC-DC converter current limit.
9	FO	Fault Output.
10	EN	Enable pin to turn on and off the overall system. (Active Low Shutdown Mode).
11	INPUT	Logic input for sinusoidal waveform.
12	ADJ	Output voltage adjust control pin. Connect to internal current source to change output voltage using an external resistor. Connect a small capacitor (1 nF).
13	RT	Oscillator frequency control pin.
14	OVP	Voltage sense input of Step-up DC-DC converter for Over-Voltage Protection.
15	AGND	Analog Ground. The signal ground for full-bridge driver circuitry.
16	V <sub>IN</sub>	Power supply of 5 V LDO.
17	V <sub>DRV</sub>	Power supply of full-bridge driver.
18	PGND2	Power Ground 2. The power ground for full-bridge driver .
19	NC	Not Connected
20	OUT2	Output 2 for full-bridge driver.
21	OUT1	Output 1 for full-bridge driver.
22	NC	Not Connected
23, 24	L <sub>x</sub>	Switch Node. This pin is connected to the inductor.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V <sub>DRV</sub>	DC Link Input Voltage Drain-Source Voltage of each MOSFET			75	V
V <sub>DD</sub>	DC Supply Voltage for DC-DC Converter		-0.3	5.5	V
V <sub>IN,DCDC</sub>	EN, INPUT, FB and COMP to SGND		-0.3	V <sub>DD</sub> +0.3	V
V <sub>IN</sub>	DC Supply Voltage for LDO		-0.3	75	V
V <sub>LX</sub>	LX to PGND		-0.3	36	V
P <sub>D</sub>	Power Dissipation <sup>(2)</sup>	1S0P with thermal vias <sup>(3)</sup>		0.98	W
		1S2P with thermal vias <sup>(4)</sup>		2.9	
θ <sub>JA</sub>	Thermal Resistance Junction-Air <sup>(2)</sup>	1S0P with thermal vias <sup>(3)</sup>		127	°C/W
		1S2P with thermal vias <sup>(4)</sup>		43	
T <sub>A</sub>	Operating Ambient Temperature Range		-40	125	°C
T <sub>J</sub>	Operating Junction Temperature		-55	150	°C
T <sub>STG</sub>	Storage Temperature Range		-55	150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		2	KV
		Charged Device Model, JESD22-C101		500	V

### Notes:

1. All voltage values, except differential voltages, are given with respect to SGND, AGND and PGND pin.
2. JEDEC standard: JESD51-2, JESD51-3. Mounted on 76.2x114.3x1.6mm PCB (FR-4 glass epoxy material).
3. 1S0P with thermal vias: one signal layer with zero power plane and thermal vias.
4. 1S2P with thermal vias: one signal layer with two power plane and thermal vias.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DRV</sub>	Supply Voltage for Full-Bridge Driver	30		60	V
V <sub>LX</sub>	Boost Switch Voltage	10		30	V
V <sub>DD</sub>	Operating Voltage for DC-DC Converter	2.7	3.0	3.3	V
V <sub>IN</sub>	Operating Voltage for Voltage Regulator	10		60	V
R <sub>OCP</sub>	Current Limit Control Resistor	7.0		150	kΩ

## Electrical Characteristics

$V_{DD}=3.0\text{ V}$ ,  $V_{IN}=15.0\text{ V}$ ,  $V_{DRV}=60\text{ V}$ ,  $R_T=70\text{ K}\Omega$  and  $T_A=-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Typical values  $T_A=25^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Power Supply Section</b>						
$I_{Q,DD}$	Quiescent Current for $V_{DD}$ <sup>(5)</sup>	$V_{EN}=V_{COMP}=V_{DD}$ , $V_{FB}=1.0\text{ V}$ Device not switching		700	1200	$\mu\text{A}$
$I_{Q,IN}$	Quiescent Current for $V_{IN}$			300	500	$\mu\text{A}$
$I_{Q,DRV}$	Quiescent Current for $V_{DRV}$			200	300	$\mu\text{A}$
$I_{SD,DD}$	Shutdown Current for $V_{DD}$	$V_{EN}=0\text{ V}$ , $V_{DD}=V_{IN}=V_{DRV}=3\text{ V}$			1	$\mu\text{A}$
$I_{SD,IN}$	Shutdown Current for $V_{IN}$				1	$\mu\text{A}$
$I_{SD,DRV}$	Shutdown Current for $V_{DRV}$			5	10	$\mu\text{A}$
$V_{DDSTART}$	Start Threshold Voltage		2.6	2.7	2.8	V
$V_{DDUVHYS}$	$V_{DD}$ UVLO Hysteresis Voltage		0.1	0.2	0.3	V
<b>Error Amplifier Section</b>						
$V_{FB}$	Feedback Reference Voltage	$T_A=25^\circ\text{C}$	0.99	1.0	1.01	V
$I_{FB}$	FB pin Bias Current	$V_{FB}=0\text{ V} \sim 2\text{ V}$			1	$\mu\text{A}$
$\Delta V_{FB1}$	Feedback Voltage Line Regulation <sup>(6)</sup>	$2.7\text{ V} < V_{DD} < 5\text{ V}$		0.5	1.5	%/V
$G_m$	Transconductance	$T_A=25^\circ\text{C}$		800		$\mu\text{mho}$
<b>Zero Current Detect Section</b>						
$V_{ZCD}$	Input Voltage Threshold <sup>(7)</sup>		1.65	1.83	2.00	V
$V_{CLAMPH}$	Input High Clamp Voltage	$I_{DET}=2.3\text{ mA}$	3.0	3.5	4.0	V
$V_{CLAMPL}$	Input Low Clamp Voltage	$I_{DET}=-2.3\text{ mA}$	-0.30	0.12	0.50	V
$I_{ZCD,SR}$	Source Current Capability				-2.3	mA
$I_{ZCD,SK}$	Sink Current Capability				2.3	mA
$t_{ZCD,D}$	Delay From ZCD to Output Turn-On <sup>(7)</sup>			50	200	ns
<b>Maximum On-Time Section</b>						
$t_{ON,MAX}$	Maximum On-Time		15	25	35	$\mu\text{s}$
<b>Restart / Maximum Switching Frequency Limit Section</b>						
$t_{RST}$	Restart Timer		15	25	35	$\mu\text{s}$
$f_{MAX}$	Maximum Switching Frequency <sup>(7)</sup>			900	1000	KHz
<b>Soft-Start Timer Section</b>						
$t_{SS}$	Internal Soft-Start		16	28	40	ms
<b>Current Limit Comparator Section</b>						
$I_{OCP}$	OCP Trip Current	$R_{OCP}=3.3\text{ K}\Omega$ , $V_{DD}=3.3\text{ V}$	1.85	2.00	2.15	A
		$R_{OCP}=22\text{ K}\Omega$ , $V_{DD}=3.3\text{ V}$	0.9	1.0	1.1	A
$t_{CS\_BLANK}$	Comparator Leading-Edge Blanking Time <sup>(7)</sup>		80	130	180	ns

### Notes:

5. This is the  $V_{DD}$  current consumed when active but not switching. Does not include gate-drive current

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{1}{V_{OUT}}$$

6. The line regulation is calculated based on

7. This parameter, although guaranteed by design, is not tested in production.

## Electrical Characteristics

$V_{DD}=3.0\text{ V}$ ,  $V_{IN}=15.0\text{ V}$ ,  $V_{DRV}=60\text{ V}$ ,  $R_T=70\text{ K}\Omega$  and  $T_A=-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Typical values  $T_A=25^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Step-Up Switch Section</b>						
$R_{DS(on)}$	N-Channel On Resistance	$V_{DD}=3.3\text{ V}$ , $T_A=25^\circ\text{C}$		0.2	0.5	$\Omega$
$I_{LK\_LX}$	LX Leakage Current	$V_{LX}=36\text{ V}$			1.0	$\mu\text{A}$
<b>Oscillator Section</b>						
$f_{OSC}$	Operating Frequency	$R_T=58\text{ K}\Omega$	40	50	60	KHz
		$R_T=121\text{ K}\Omega$	20	25	30	KHz
<b>Logic (EN and INPUT) Section</b>						
$V_{INPUT+}$	INPUT Logic High Threshold Voltage		1.34			V
$V_{INPUT-}$	INPUT Logic Low Threshold Voltage				0.5	V
$I_{INPUT-}$	Input Low Current for INPUT and EN	$V_{EN}=0\text{ V}$			1	$\mu\text{A}$
$I_{INPUT+}$	Input High Current for INPUT and EN	$V_{EN}=V_{DD}$	8	12	16	$\mu\text{A}$
$R_{INPUT}$	Input Logic Pull-Down Resistance	$V_{EN}=V_{INPUT}=3\text{ V}$		250	375	$\text{K}\Omega$
$f_{INPUT}$	Input Logic Operating Frequency <sup>(8)</sup>		20		1000	Hz
<b>Full-Bridge Switch Section</b>						
$R_{DS,ONP}$	Output Upper-Side On Resistance	$T_A=25^\circ\text{C}$		3.0	5.0	$\Omega$
$R_{DS,ONN}$	Output Low-Side On Resistance	$T_A=25^\circ\text{C}$		3.0	5.0	$\Omega$
<b>Output Control Section</b>						
$V_{ADJ,MAX}$	Analog Output Control Maximum Voltage <sup>(8)</sup>	$V_{DRV}=100\%$ of Target		1.0		V
$V_{ADJ,MIN}$	Analog Output Control Minimum Voltage <sup>(8)</sup>			0.1		V
$I_{ADJ+}$	Internal Current Source for ADJ Pin	$T_A=25^\circ\text{C}$	9	10	11	$\mu\text{A}$
<b>Protection (Ready, OVP and TSD)</b>						
$V_{READY}$	Output Ready Threshold Voltage		0.75	0.80	0.85	V
$HY_{READY}$	Output Ready Hysteresis			0.2		V
$V_{OVP\_FB}$	OVP Threshold Voltage at FB Pin		1.05	1.10	1.15	V
$HY_{OVP\_FB}$	OVP Hysteresis Voltage at FB Pin			0.1		V
$V_{OVP\_OVP}$	OVP Threshold Voltage at OVP Pin		1.10	1.15	1.20	V
$HY_{OVP\_OVP}$	OVP Hysteresis Voltage at OVP Pin			0.15		V
$T_{SD}$	Thermal Shutdown Temperature <sup>(8)</sup>			150		$^\circ\text{C}$
$T_{HYS}$	Hysteresis Temperature of TSD <sup>(8)</sup>			50		$^\circ\text{C}$
$T_{FO}$	Fault Output Duration			20	30	$\mu\text{s}$
$V_{FOL}$	Fault Output Low Level Voltage	$R_{PU}=50\text{ K}\Omega$ , $V_{PU}=3\text{ V}$		0.1	0.4	V

### Note:

8. This parameter, although guaranteed by design, is not tested in production.

## Typical Performance Characteristics

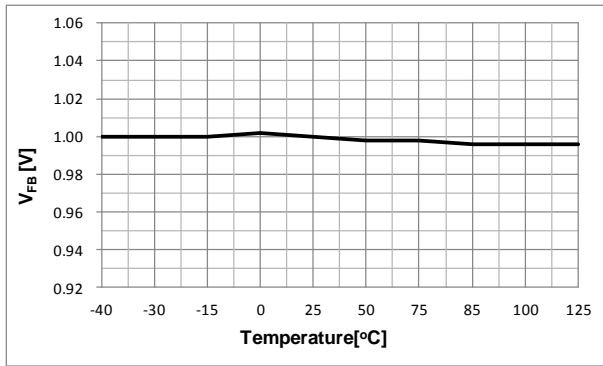


Figure 4. Reference Voltage vs. Temperature

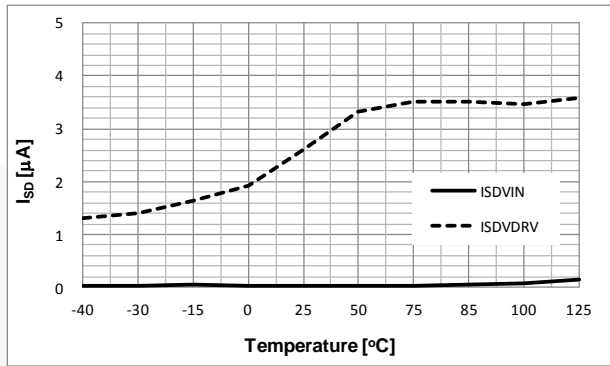


Figure 5. Shutdown Current for V<sub>DRV</sub> & V<sub>IN</sub> vs. Temperature

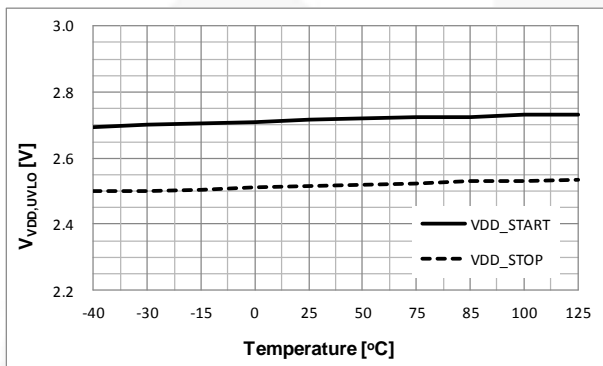


Figure 6. V<sub>DD</sub> UVLO vs. Temperature

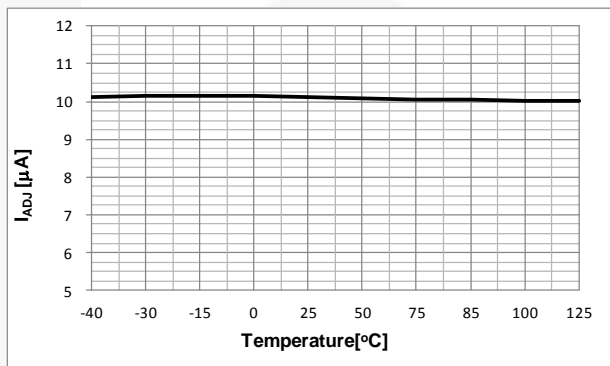


Figure 7. ADJ Current vs. Temperature

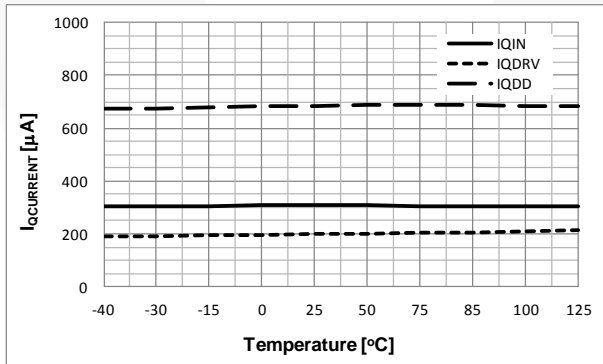


Figure 8. Quiescent Current for V<sub>DD</sub>, V<sub>DRV</sub>, & V<sub>IN</sub> vs. Temperature

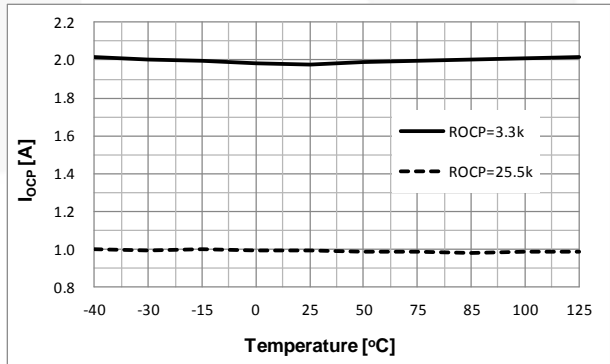


Figure 9. OCP Current vs. Temperature

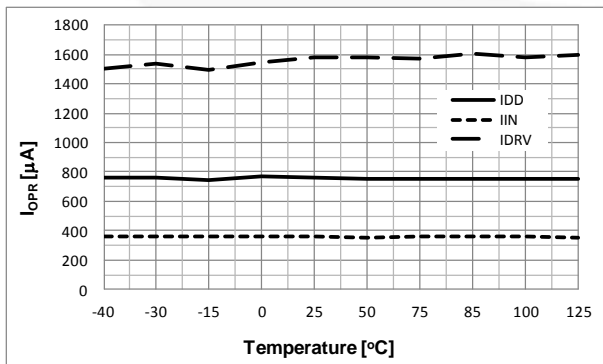


Figure 10. Operating Current for V<sub>DD</sub>, V<sub>DRV</sub>, & V<sub>IN</sub> vs. Temperature

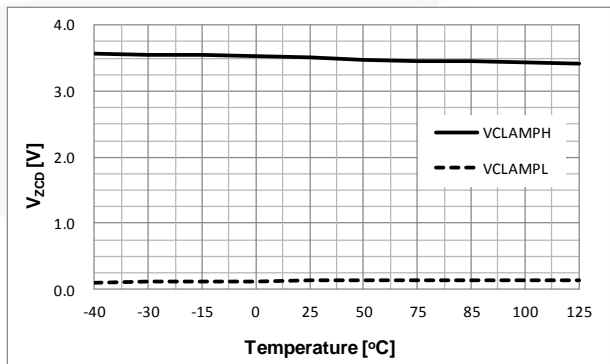


Figure 11. ZDC Clamp Voltage vs. Temperature

## Typical Performance Characteristics

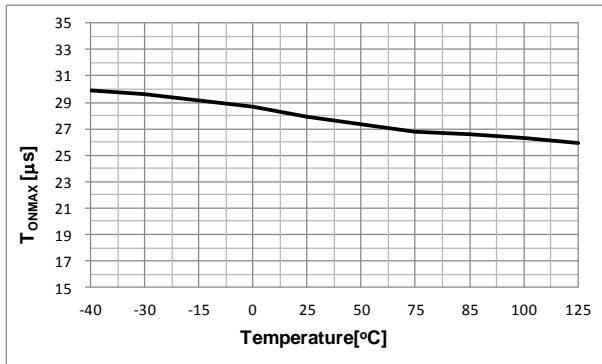


Figure 12. Maximum On-Time vs. Temperature

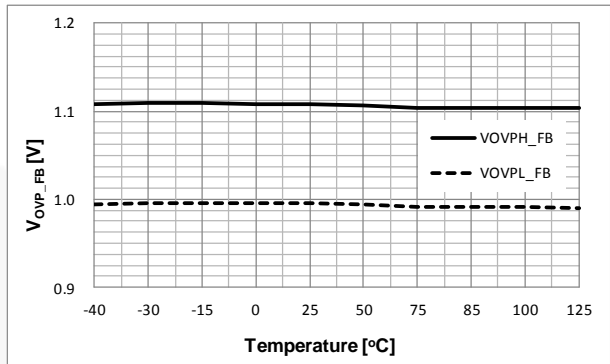


Figure 13. First OVP (FB) vs. Temperature

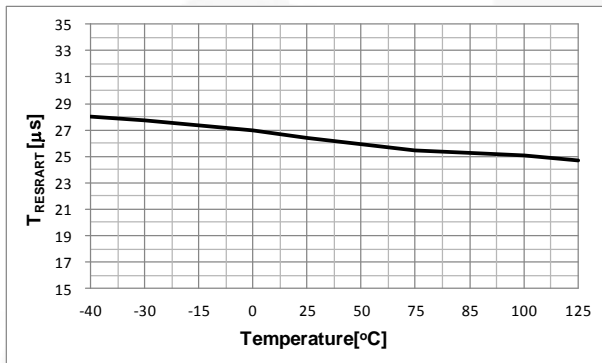


Figure 14. Restart-Time vs. Temperature

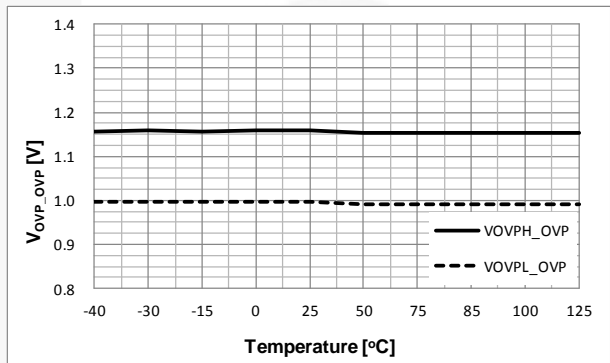


Figure 15. Second (OVP) vs. Temperature

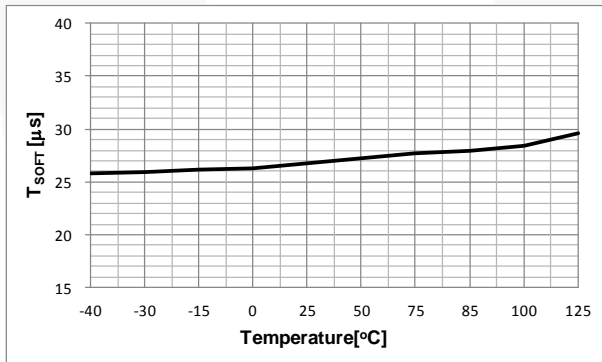


Figure 16. Soft-Start Time vs. Temperature

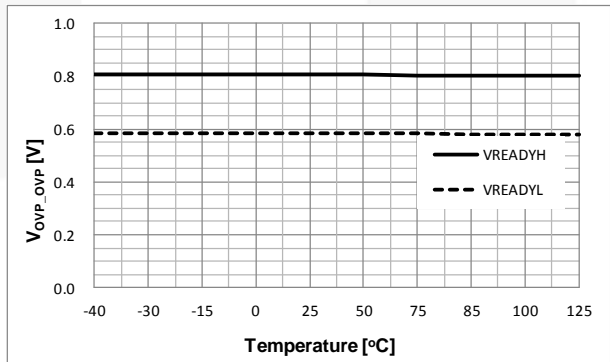


Figure 17. Ready Voltage vs. Temperature

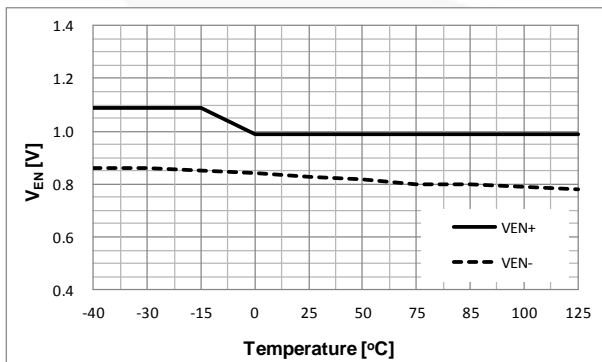


Figure 18. Enable (EN) Threshold Voltage vs. Temperature

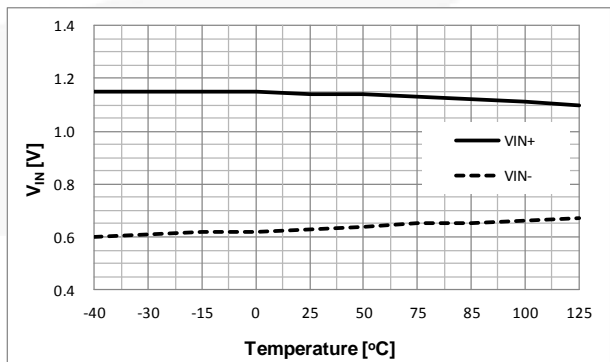


Figure 19. INPUT Threshold Voltage vs. Temperature



## Typical Performance Characteristics

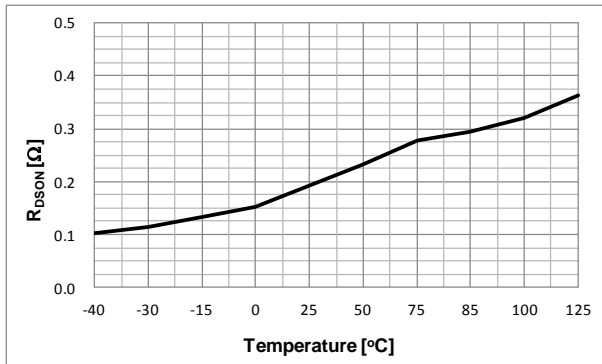


Figure 20. Boost Switch R<sub>DS(on)</sub> vs. Temperature

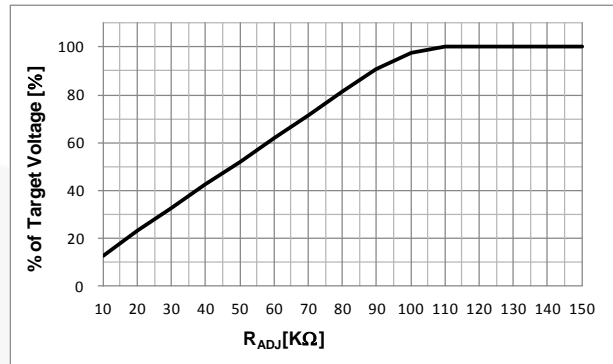


Figure 21. % of Sine Amplitude vs. R<sub>ADJ</sub>

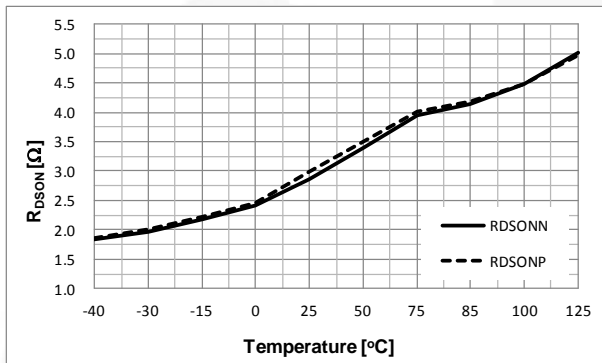


Figure 22. Full-Bridge Switch R<sub>DS(on)</sub> vs. Temperature

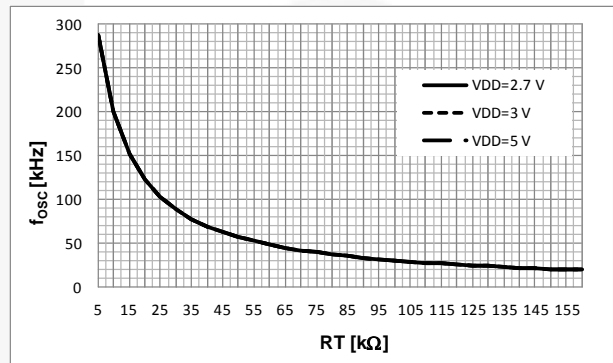


Figure 23. f<sub>osc</sub> vs. RT

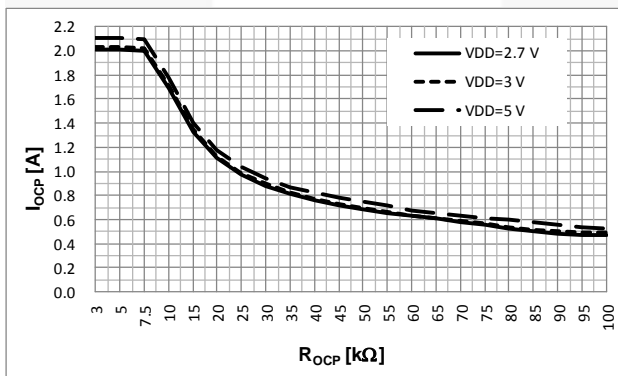
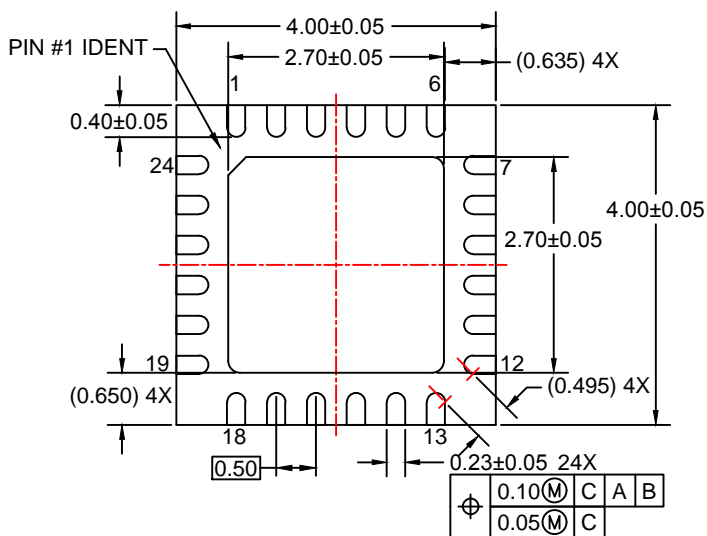
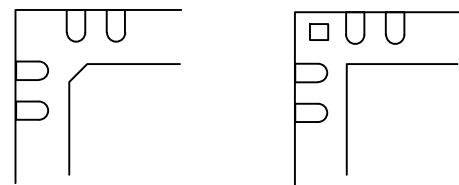
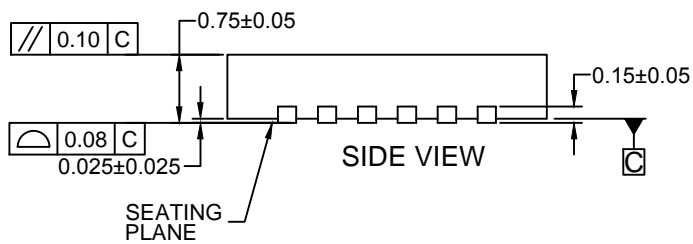
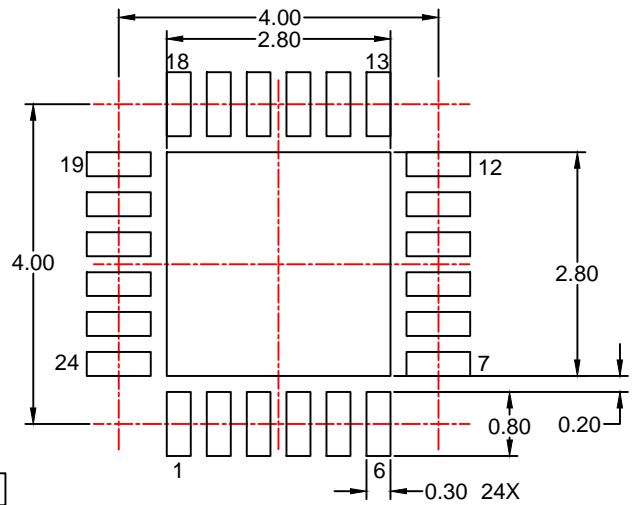
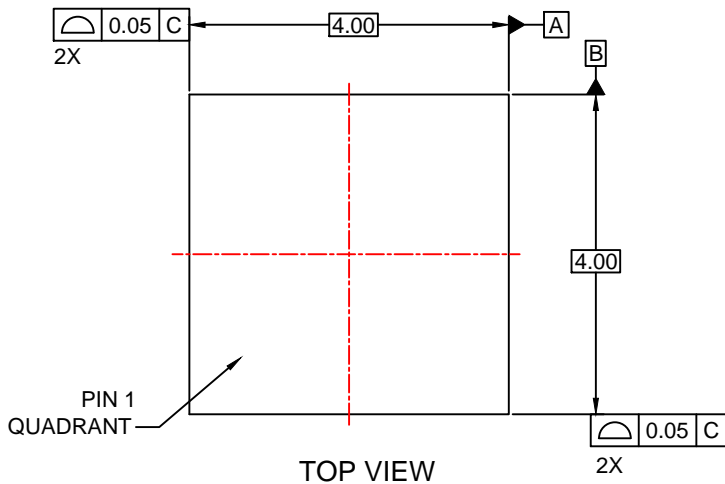


Figure 24. I<sub>OCP</sub> vs. R<sub>OCP</sub>



**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WGGD-6.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN IPC REFERENCE : QFN50P400X400X80-25W6N.
- E. DRAWING FILENAME: MKT-MLP24Erev5.





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- FETBench™
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- GTO™
- IntelliMAX™
- ISOPLANAR™
- Making Small Speakers Sound Louder and Better™
- MegaBuck™
- MICROCOUPLER™
- MicroFET™
- MicroPak™
- MicroPak2™
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- PowerXS™
- Programmable Active Droop™
- QFET®
- QS™
- Quiet Series™
- RapidConfigure™
- ™
- Saving our world, 1mW/W/kW at a time™
- SignalWise™
- SmartMax™
- SMART START™
- Solutions for Your Success™
- SPM®
- STEALTH™
- SuperFET®
- SuperSOT™-3
- SuperSOT™-6
- SuperSOT™-8
- SupreMOS®
- SyncFET™
- Sync-Lock™
- ®
- TinyBoost®
- TinyBuck®
- TinyCalc™
- TinyLogic®
- TINYOPTO™
- TinyPower™
- TinyPWM™
- TinyWire™
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- ™
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**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
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