89024
ARCHITECTURAL OVERVIEW
2400 BPS INTELLIGENT MODEM CHIP SET

- 300 to 2400 bps Full-Duplex Modem
- Operates with Public and Private Unconditioned Lines
- CCITT V.22 bis, V.22 A & B, V.21, Bell 212A, 103 Compatible
- DSP Implementation
- DTMF or Pulse Dialing with Automatic Adaptation to Network
- Call Progress Tone Detection for Most North American and European Networks
- Analog and Digital Loopback Diagnostics with Mark/Space Pattern Generation and Error Detection per V.54
- Programmable Output Level from −1 dBm to −16 dBm
- Automatic Dial and Redial Capability
- Two Chip Solution, no External Microcontroller Required
- Serial Command Set Compatible with Hayes Smartcom II Communication Software
- Easily Customized Command Set
- On-Chip 4 Wire to 2 Wire Hybrid Function with Disable Option
- On-Chip Serial Port and Handshake Signals for DTE Interface
- A Full Set of Control Signals for Telephone Line Control
- Telephone Line Audio Monitor Output
- Billing Delay Timer
- Auxiliary Relay Control Output
- Automatic Modem Type Recognition
- Low Power CHMOS/HMOS Devices

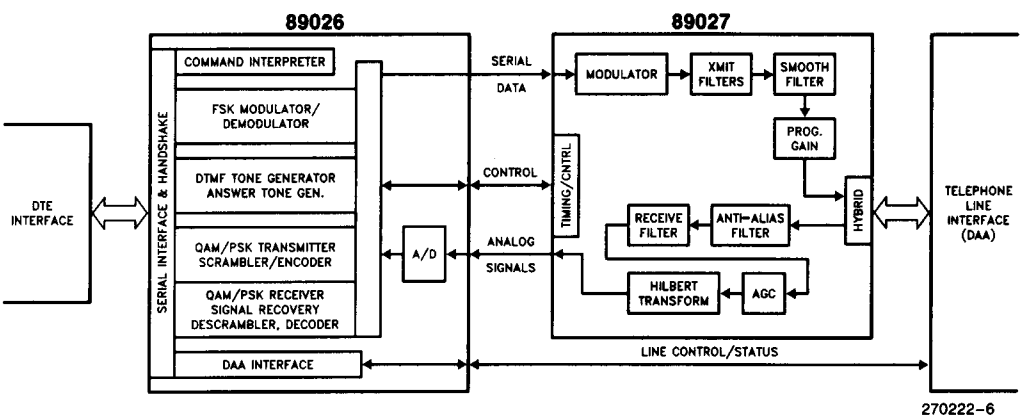

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Figure 1. System Block Diagram

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GENERAL DESCRIPTION

The Intel 89024 chip set is a high performance and highly integrated modem, providing a complete system in two chips. The system implements CCITT V.22 bis 2400 bps, V.22 A & B/ Bell 212A 1200 bps, and V.21/Bell 103 300 bps full-duplex modem functions. In addition to supporting a strict implementation of CCITT and Bell standards, a complete set of Hayes Smartmodem 2400 commands is also provided for modem configuration and user interface.

In stand-alone modem applications, the 89024 chip set along with a Data Access Arrangement (DAA) and RS-232 driver/receivers, represent the circuitry required for implementing an auto-dial, auto-answer, 300 to 2400 bps, full duplex modem.

In applications where user proprietary modem control commands may be required, the user can replace the 89024 internal command module with custom proprietary software resident in the 89026 microcontroller's on-chip ROM or an external memory device.

The 89024 system consists of a 16 bit application specific processor (89026) and an analog front end device (89027). The 89026 processor executes all "Digital Signal Processing" algorithms for the modem signals, as well as providing all modem control functions typically performed by an external processor. The analog front end provides the telephone line 2 wire to 4 wire interface, D/A conversion, and most of the complex filtering functions required in QAM/PSK/FSK modems. Refer to Figure 1 for a simplified block diagram of the system.

The chip set provides a comprehensive set of telephony functions designed to facilitate a simple interface to the telephone network.

89026 OVERVIEW

The 89026 processor performs most of modulation, demodulation and user interface functions. This chip is available in a standard 48 pin package. An optional 68 pin version supports an external ROM for user designed software. With this option, the signal processing algorithms resident in the 89026, can be controlled by the customer designed external software for proprietary modem control and call progress management applications. A block diagram of 89026 is provided in Figure 2.

This device contains a TTL compatible serial link to DTE/DCE equipment, along with a full complement of V.24/RS-232-C control signals. Alternatively, a UART or USART may be used to directly transfer data to/from a microcomputer bus. The device supports a complete set of Hayes compatible modem control commands. This compatibility facilitates communications between the 89024 and most PC software written for the Hayes Smartmodem 2400 product.

In the transmit direction, the 89026 synthesizes DTMF tones and the 300 bps FSK modem signal prior to transmitting them to the 89027 as digitized amplitude samples. During 1200 and 2400 bps operations, quadrature amplitude modulation (QAM) is used to send 2 or 4 bits of information at 600 baud to the 89027. Since the QAM coding technique is inherently a synchronous transmission mechanism, during a synchronous QAM transmission, the asynchronous data is synchronized by adding or deleting stop bits. Following the synchronization process, the 89026 transmits digitized phase and amplitude samples to the 89027 over a high speed serial link.

In the receive direction, the information is received by the 89026 from the 89027 as two signals which are 90 degrees phase shifted from each other. These analog signals are then digitized by the 89026's on-board A/D converter, and using DSP software algorithms the signals are gain adjusted, adaptively equalized for telephone line delay and amplitude distortion, and demodulated. Following the demodulation process by the 89026, the data is unscrambled, and if necessary, returned to asynchronous format.

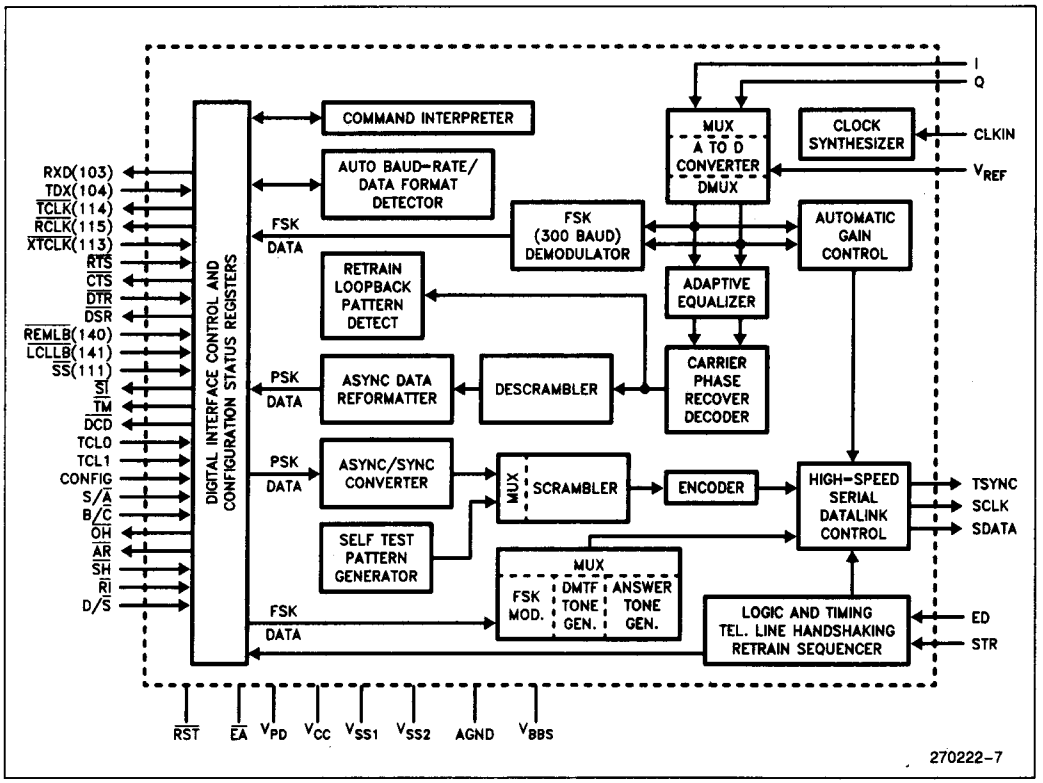

Figure 2. 89026 Block Diagram

89027 OVERVIEW

The 89027 is a 28 pin CHMOS analog front end device, which performs most of the complex filtering functions required in modem transmitters and receivers. A general block diagram of this chip is provided in Figure 3. Most of the analog signal processing functions in this chip are implemented with switched capacitor technology. The 89027 functions are controlled by the 89026, through a high speed serial data link.

During FSK transmit operation, the 89027 receives digitally synthesized mark and space sinusoid amplitude information from the 89026. The 89027 converts the signal to its analog equivalent, filters it, and transmits it to the telephone line. For QAM transmission, the signal constellation points are transferred to the 89027. This information is modulated into an analog signal, passed through spectral shaping filters, combined with the necessary guard tone, smoothed by a low pass filter, and transmitted to the line. Prior to transmitting either FSK or QAM signals to the telephone line, the 89027 adjusts the signal gain through a on-board programmable gain amplifier.

During the receive operation, the received QAM/PSK/FSK signals are passed through anti-alias filters, bandsplit filters, automatic gain control and carrier detect circuits, a Hibert transform filter, and the output sent to the 89026 processor as analog signals.

Other functions provided by the 89027 are: an on-board 2 wire to 4 wire circuit with disable capability, an audio monitor output with software configurable gain, and a programmable gain transmit signal.

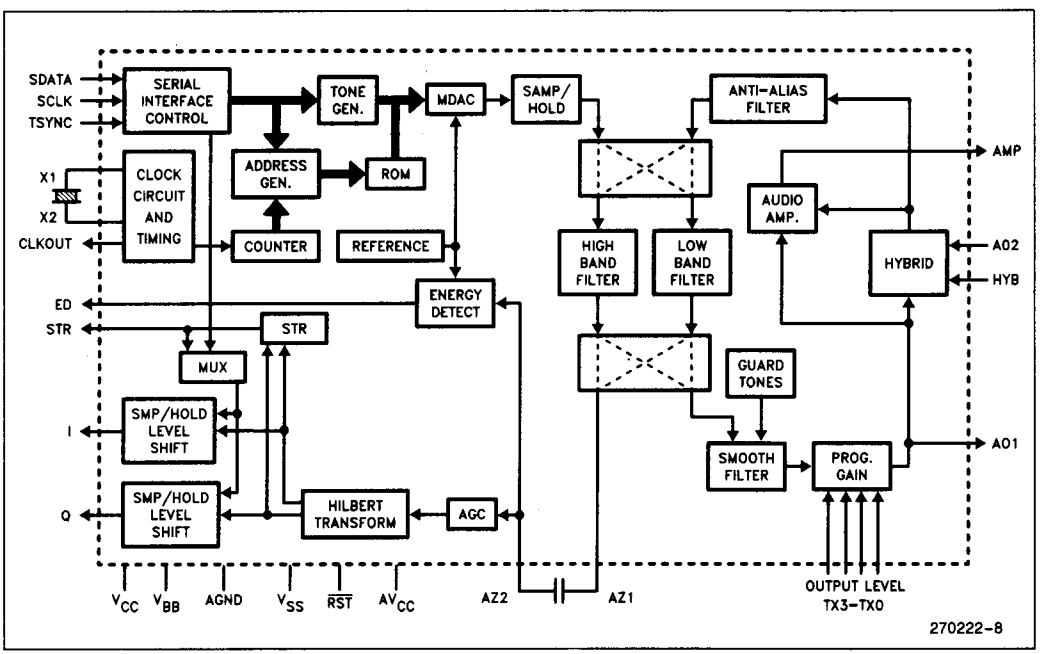

Figure 3. 89027 Block Diagram

APPLICATIONS OVERVIEW

The block diagram of a stand-alone 300 to 2400 bps Hayes compatible modem is depicted in Figure 4. The DAA section shown in this diagram may be obtained as an "FCC Part 68" approved module, or implemented using the suggested diagram in Figure 5.

In the above example, the modem conforms to CCITT and Bell data call set-up protocols, for identifying and connecting to remote modems. Because these protocols are quite different from each other and do not provide recognition of the remote modem type (i.e. V.22 bis/V.22 or 212A), the Intel chip set provides the additional capability to identify and adapt to remote modems without user intervention.

This feature is beneficial during the migration phase of the technology from 1200 bps to 2400 bps. In North America, where the installed base of 1200 bps modems is mostly made-up of 212A type, this feature allows a "Data Base Service Provider"to easily upgrade its existing 212A modems to 2400 bps V.22 bis standard, using the Intel 89024 system, entirely transparent to the current 212A users. Similarly, a user with a 89024 based modem system can automatically call data bases with either 212A or V.22 bis modems, without concern over the difference. This feature's benefits are realized in smooth upgrading of data links, with minimum cost and reduced disruption in services.

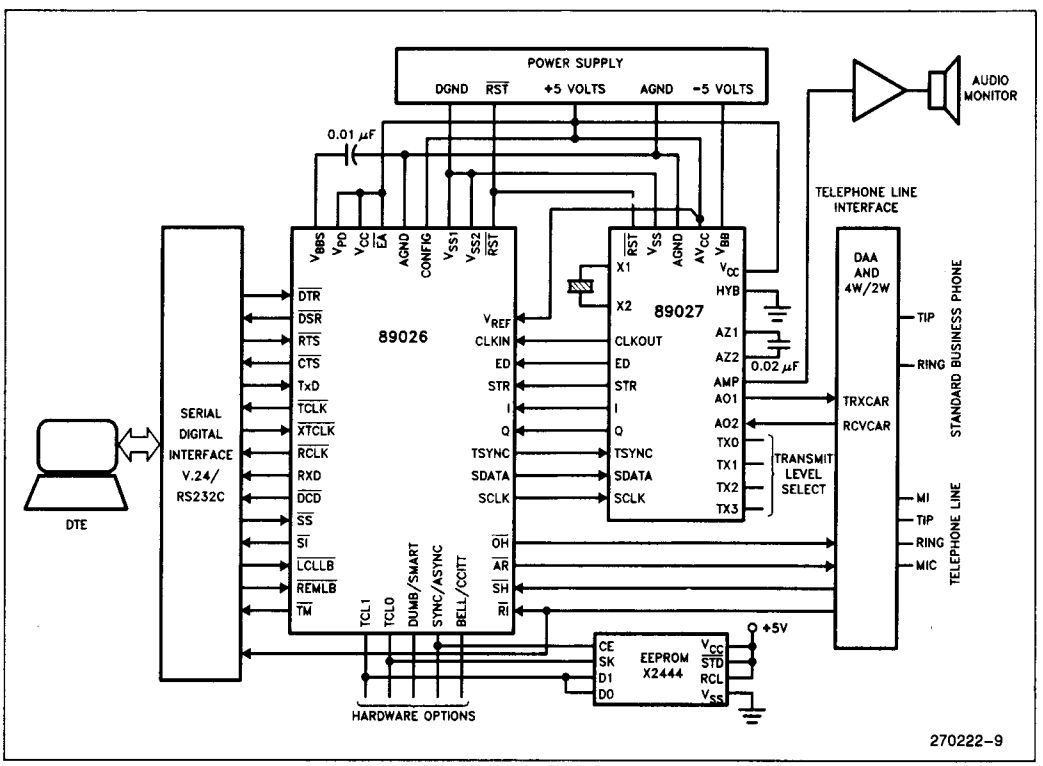

Figure 4. Typical Modem Configuration

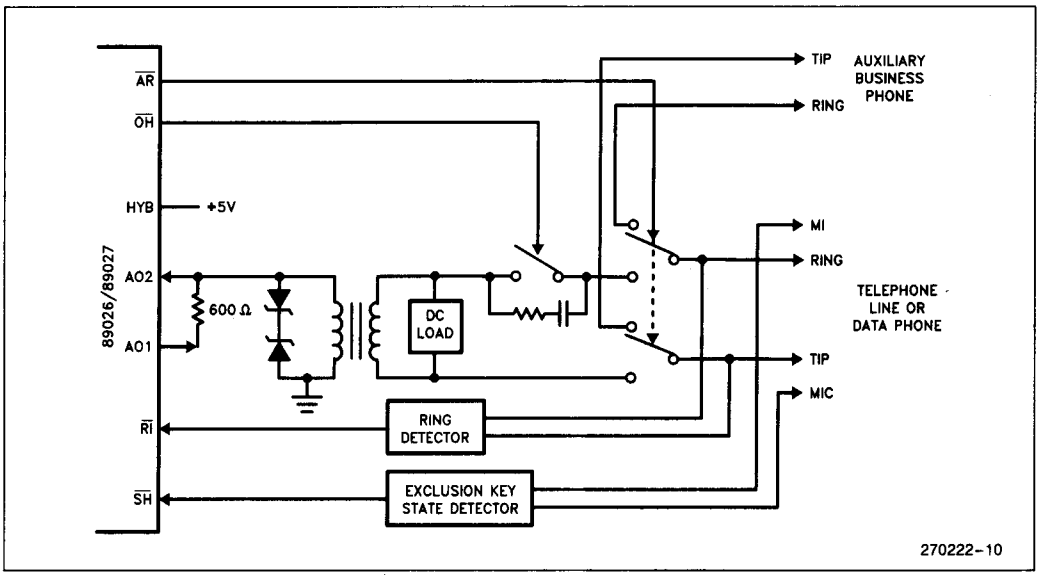

Figure 5. Typical Telephone Line Interface With Built-In Hybrid

PACKAGING

The standard 89026 is available in Intel's 48 pin plastic DIP, and the optional 68 pin device (for external memory applications) is available in PLCC packaging. The 89027 is available in 28 pin plastic DIP and PLCC packages. The assignment of pins for both devices is given below, along with the pin names and a brief explanation of their function.

89026 PINOUT

Symbol	Function (89026)	Direction	Pin No.	
			48 pin	68 pin
CLKIN	12.96 MHz master clock from 89027	In	36	67
$\overline{RST}$	Chip reset (active low)	In	48	16
I	In-phase received signal	In	43	11
Q	Quadrature-phase received signal	In	42	10
STR	Symbol Timing from 89027	In	3	24
ED	Energy Detect input	In	41	9
TSYNC	Transmitter sync pulse to 89027	Out	10	35
SDATA	Serial Data to 89027	Out	1	17
SCLK	Serial Clock to 89027	Out	2	18
$\overline{OH}$	Off-Hook control to DAA	Out	26	33
$\overline{SH}$	Switch-Hook from dataphone	In	28	44
$\overline{RI}$	Ring Indicator from DAA	In	27	42
$\overline{AR}$	Aux Relay control to DAA	Out	25	38

89026 PINOUT (Continued)

Symbol	Function (89026)	Direction	Pin No.	
			48 pin	68 pin
TCL1	NVRAM Data I/O	I/O	23	20
TCL0	NVRAM SK	Out	24	19
B/$\overline{C}$	103/V.21 default option	In	47	15
S/$\overline{A}$	NVRAM CE	Out	22	21
D/$\overline{S}$	Dumb/$\overline{S}$mart mode select	In	32	6
CONFIG	Custom Firmware Disable	In	40	8
$\overline{TM}$	Test Mode Indicator	Out	13	39
TXD	Transmitted data from DTE	In	6	27
RXD	Received data to DTE	Out	8	29
$\overline{RTS}$	Request to send from DTE	In	21	22
$\overline{CTS}$	Clear to Send to DTE	Out	20	23
$\overline{DSR}$	Data Set Ready to DTE	Out	19	30
$\overline{DCD}$	Data Carrier Detect to DTE	Out	18	31
$\overline{DTR}$	Data Terminal Ready from DTE	In	4	25
$\overline{RCLK}$	Received clock to DTE	Out	9	34
$\overline{TCLK}$	Transmit clock to DTE	Out	7	28
$\overline{XTCLK}$	External timing clock from DTE	In	5	26
$\overline{SI}$	Speed Indicator to DTE	Out	17	32
$\overline{SS}$	Speed select from DTE(4)	In	31	5
$\overline{REMLB}$	Remote Loopback Command from DTE	In	30	7
$\overline{LCLLB}$	Local Loopback Command from DTE	In	29	4
V_{CC}	Positive power supply (+5V)	+5V	38	1
V_{PD}	Ram back-up power	+5V	46	14
V_{REF}	A/D converter reference	+5V	45	13
V_{SS1}	Digital ground	GND	11	36
V_{SS2}	Digital ground	GND	37	68
AGND	Analog ground	AGND	44	12
V_{BBS}	Back-bias generator output	Out	12	37
$\overline{EA}$	External Memory enable	In	39	2
AD0-AD15	External memory access address/data(5)	I/O	—	60–45
$\overline{AA}$	Auto answer, ring indicator	Out	—	60
$\overline{JS}$	Jack select	Out	—	59
NMI	Non-maskable Interrupt (V_{SS})(1)	In	—	3
X2	Crystal output (NC)(2)	Out	35	66
CLKOUT	Clock output (NC)(2)	Out	—	65
$\overline{TEST}$	Factory test (V_{CC})(3)	In	—	64
INST	External memory instruction fetch	Out	—	63
ALE	Address latch enable	Out	34	62
$\overline{RD}$	External memory read	Out	33	61
READY	External memory ready (V_{CC})(3)	In	16	43
$\overline{BHE}$	External memory bus high enable	Out	15	41
$\overline{WR}$	External memory write	Out	14	40

NOTES:
1. Pins marked with (V_{SS}) must be connected to V_{SS}.
2. Pins marked with (NC) are to be left unconnected.
3. Pins marked with (V_{CC}) must be connected to V_{CC}.
4. $\overline{SS}$ pin reserved for future use.
5. With internal ROM enabled, AD0-AD1 are used as $\overline{AA}$ and $\overline{JS}$.

89027 PINOUT

Symbol	Function (89027)	Direction	Pin No.
V_{CC}	Positive Power Supply (Digital)	+5V	28
V_{BB}	Negative Power Supply	−5V	15
V_{SS}	Digital Ground	DGND	24
AGND	Analog Ground	AGND	21
AV_{CC}	Positive Power Supply (Analog)	+5	7
X1	Xtal Oscillator	In	23
X2	Xtal Oscillator	Out	25
CLKOUT	12.96 MHz Clock output to 89026	Out	26
$\overline{RST}$	Chip reset (active low)	In	20
HYB	Enable on-chip hybrid	In	10
AZ1	Auto-zero capacitor input	Out	16
AZ2	Auto-zero capacitor input	In	17
SDATA	Serial data from 89026	In	2
SCLK	Serial clock from 89026	In	1
TSYNC	Transmitter sync from 89026	In	3
STR	Symbol timing to 89026	Out	27
ED	Receiver energy detect to 89026	Out	18
I	In phase received signal to 89026	Out	13
Q	Quadrature-phase received signal to 89026	Out	14
AO1	Transmitter output	Out	6
AO2	Receiver input	In	12
AMP	Output to monitor speaker	Out	11
TX0	Transmitter level control	In	9
TX1	Transmitter level control	In	8
TX2	Transmitter level control	In	5
TX3	Transmitter level control	In	4

Unused pins:19, 22 must be left unconnected.

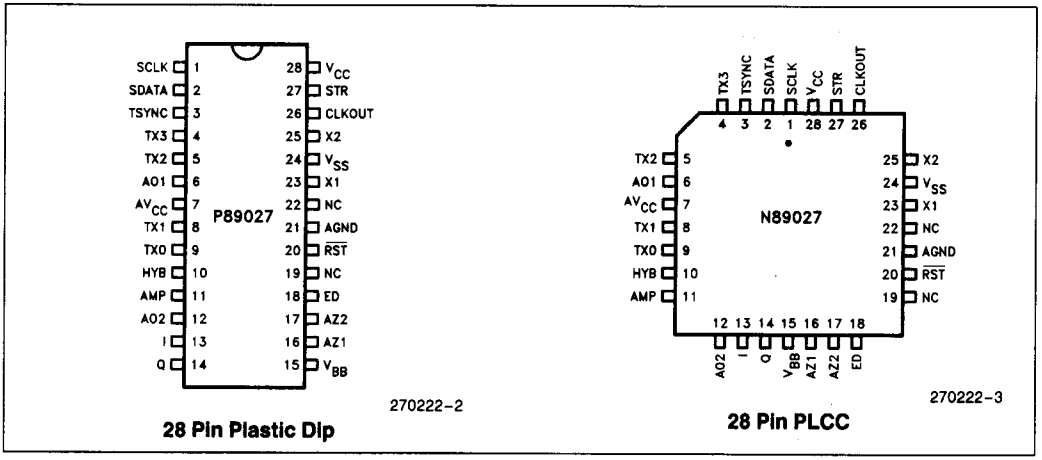

Figure 6a. 89027 Packages

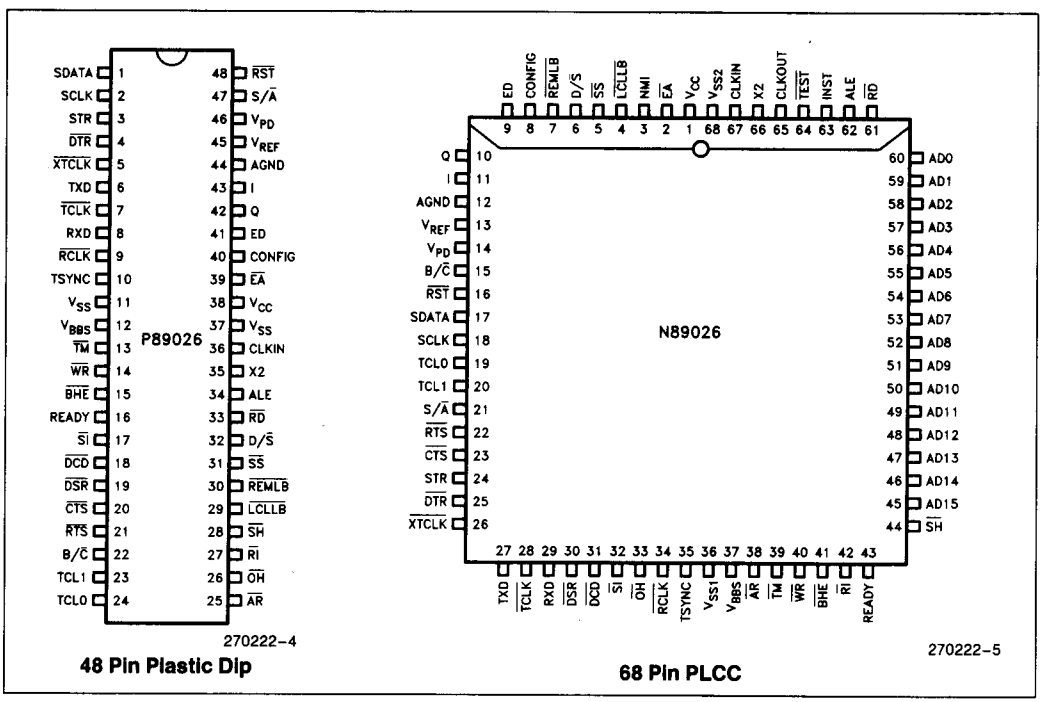

Figure 6b. 89026 Packages

OVERVIEW

The 89024 Reference Manual details design information for the 89024 Modem Chip Set. It provides descriptions and specifications of the two chips comprising the 89024, the 89026 and the 89027. In addition, it describes the control interface between the two chips.

The reference manual also provides a full description of all the "AT" commands and S-registers supported by the 89024 Modem Chip Set.

ORDERING INFORMATION

Intel literature number: 296235-001