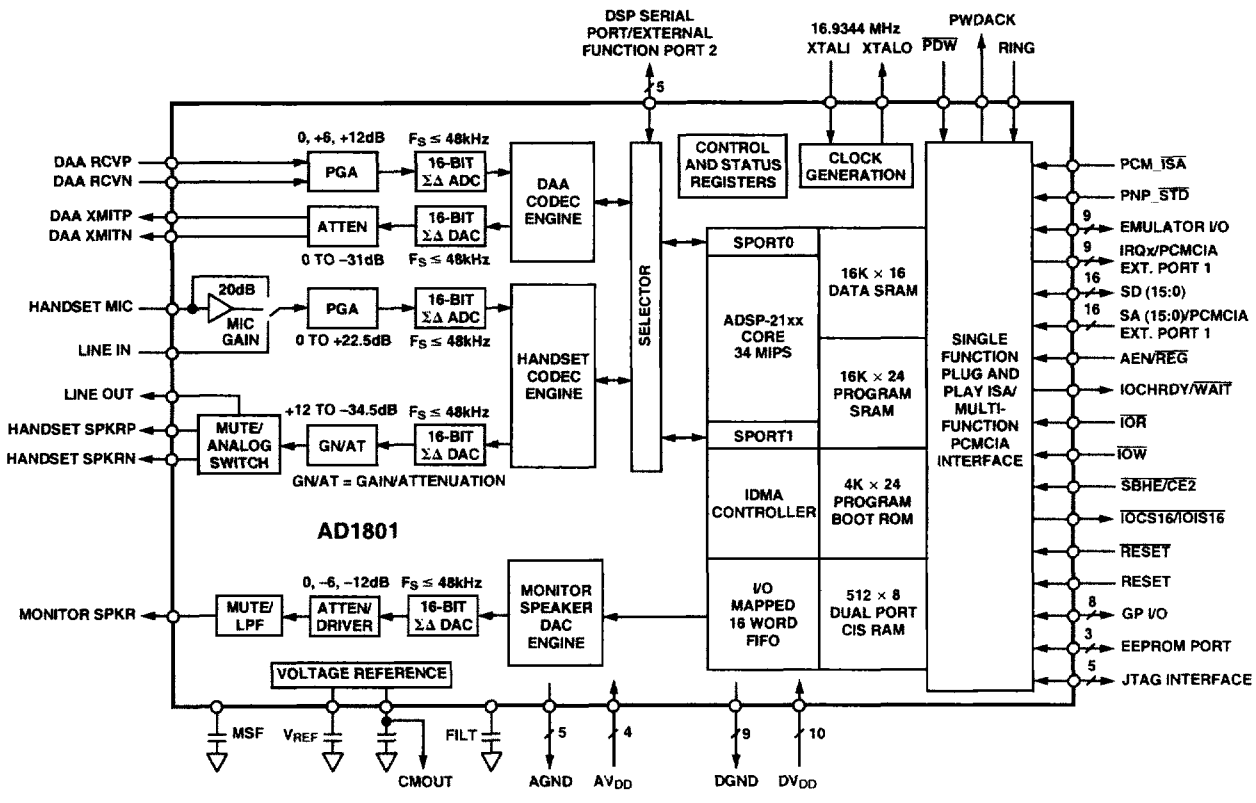
Single-Chip Fax/Data/Voice Modem

AD1801

FEATURES

- Single-Chip Integrated Fax/Data/Voice Modem
- Two Channel ΣΔ ADC and Three Channel ΣΔ DAC
- Supports V.34+, V.17 and Fallback Modem/Fax Standards and V.70 DSVD
- ADSP-21xx 34 MIPS DSP Core with SPORTs and IDMA Controller
- 16K Words Data Memory (RAM), 20K Words Program Memory (RAM and ROM), 512 Byte CIS RAM
- PC'97-Compliant Single Function Plug and Play ISA/Multifunction PCMCIA Parallel Interfaces
- Single 16.9344 MHz Clock Input
- Two Analog Inputs and Three Analog Outputs
- Eight Programmable I/O Pins
- Bidirectional Programmable Interrupt Structure
- Three Pin Serial Memory Port Interface/ICE-Port™ Emulator Interface/JTAG Boundary Scan Test Interface
- Programmable Gain, Attenuation and Mute
- On-Chip Signal Filters
  - Digital Interpolation and Decimation
  - Analog Output Low Pass
- 1 Hz Resolution Programmable Audio (Handset) Sample Rates from 5.4 kHz to 48 kHz, Modem Sample Rates from 5.4 kHz to 48 kHz, with 1 Hz, 8/7 Hz and 10/7 Hz Resolution
- 128-Lead PQFP and 128-Lead TQFP Packages
- Operation from Single +5 V Supply
- Advanced Power Management

FUNCTIONAL BLOCK DIAGRAM



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REV. 0

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AD1801–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25°C
Digital Supply (V_{DD})	5.0 V
Analog Supply (V_{CC})	5.0 V
Sample Rate (F_S)	48 kHz
Input Signal	1008 Hz
Analog Output Passband	20 Hz to 20 kHz
ADC FFT Size	2048
DAC FFT Size	8192
V_{IH}	2.0 V
V_{IL}	0.8 V
V_{OH}	2.4 V
V_{OL}	0.4 V
I_{OH}	–2 mA
I_{OL}	2 mA

Output Conditions
Autocalibrated
0 dB Attenuation
0 dB Output Relative to Full Scale
16-Bit Linear Mode
600 Ω DAA Load
1 kΩ Handset Load
10 kΩ Line Out Load
Mute Off
All DAA Transmit and Handset Speaker Specifications are Measured Differentially

Input Conditions
MIC 20 dB Gain Disabled
Autocalibrated
–1.0 dB Input Relative to Full Scale
16-Bit Linear Mode

DAA RECEIVE PATH

	Min	Typ	Max	Units
Full-Scale Input Voltage (RMS Values Assume Sine Wave Input, PGA Gain = 0 dB, Offset Error = 0% of FS)				
DAA Receive Differential Input		2		V rms
	4.523	5.656	6.787	V p-p
Resistance—DAA RCV Input†	40			kΩ
Capacitance—DAA RCV Input†		15		pF
Programmable Gain Amplifier (Relative to Full-Scale Input Voltage)				
Gain = +6 dB	5.5	6	6.5	dB
Gain = +12 dB	11	12	13	dB
Analog-to-Digital Converter				
Differential Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, 4 kHz Analog Output Passband, F_S = 12.0 kHz, PGA Gain = 0 dB)	81	84		dB
Differential Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, 4 kHz Analog Output Passband, F_S = 12.0 kHz, PGA Gain = +6 dB)	78	81		dB
Differential Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, 4 kHz Analog Output Passband, F_S = 12.0 kHz, PGA Gain = +12 dB)	75	78		dB
Differential THD+N (–1.0 dB Referenced to Full Scale,			0.02	%
4 kHz Analog Output Passband, F_S = 12.0 kHz)		–80	–74	dB
Differential Signal-to-Intermodulation Distortion† [CCIF Method]		–90	–80	dB
Single-Ended Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, 4 kHz Analog Output Passband, F_S = 12.0 kHz, PGA Gain = 0 dB [Effectively –6 dB PGA Gain; See Below*])	81	84		dB
Single-Ended Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, 4 kHz Analog Output Passband, F_S = 12.0 kHz, PGA Gain = +6 dB [Effectively 0 dB PGA Gain; See Below*])	78	81		dB
Single-Ended Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, 4 kHz Analog Output Passband, F_S = 12.0 kHz, PGA Gain = +12 dB [Effectively +6 dB PGA Gain; See Below*])	75	78		dB
Single-Ended THD+N (–1.0 dB Referenced to Full Scale, 4 kHz			0.02	%
Analog Output Passband, F_S = 12.0 kHz)		–80	–74	dB
Single-Ended Signal-to-Intermodulation Distortion† [CCIF Method]		–90	–80	dB
Crosstalk* (DAA RCV Input to Handset MIC/Line Input)			–80	dB
Offset Error (0 V Differential Analog Input)				
PGA Gain = 0 dB		30	100	LSBs
PGA Gain = +6 dB†		30		LSBs
PGA Gain = +12 dB†		30		LSBs

*When the DAA Receive ADC is used in a single-ended input circuit configuration, the user would apply a full-scale input of 1 V rms to RCVP and connect RCVN via a 1 μF capacitor to ground. However, this will result in an output word that is –6 dB down from full scale when the PGA is set for 0 dB, because the ADC input sees half the signal swing compared to when the ADC is driven differentially. Therefore, the effective PGA gain of the ADC, when used single-ended, is 6 dB less than when used differentially. To get a full-scale output with a 1 V rms input, the PGA should be programmed for 6 dB gain, which is an effective single-ended gain of 0 dB.

HANDSET MIC/LINE INPUT PATH

	Min	Typ	Max	Units
Full-Scale Input Voltage (RMS Values Assume Sine Wave Input)		0.1		V rms
Handset MIC Single-Ended Input with [illegible] dB Gain	0.226	0.2828	0.339	V p-p
		1		V rms
Handset MIC Single-Ended Input with 0 dB Gain	2.26	2.828	3.39	V p-p
		1		V rms
Line Single-Ended Input	2.26	2.828	3.39	V p-p
	20			kΩ
Resistance—Handset MIC Input†	20			kΩ
Resistance—Line Input†		15		pF
Capacitance—Handset MIC, LINE Input†		1.5		dB
Programmable Gain Amplifier Step Size (0 dB to 22.5 dB) (All Steps Tested)	21.5	22.5	23.5	dB
Gain Range Span†				
Analog-to-Digital Converter				dB
Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, A-Weighted)	70	83		%
THD+N (–1.0 dB Referenced to Full Scale)			0.03	dB
		–80	–70	dB
Signal-to-Intermodulation Distortion† [CCIF Method]		–100	–80	dB
Crosstalk† (Handset MIC/Line Input to DAA RCV Input)			–80	dB
Offset Error (Relative to Full-Scale Analog Input, PGA Gain = 0 dB)		400	2048	LSBs

DAA TRANSMIT PATH

	Min	Typ	Max	Units
Digital-to-Analog Converter				
Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, 4 kHz Analog Output Passband, Output Gain = 0 dB, F_S = 12.0 kHz)	81	90		dB
THD+N (–1.0 dB Referenced to Full Scale, 4 kHz Analog Output Passband, Output Gain = 0 dB, F_S = 12.0 kHz)			0.016	%
		–78.5	–74	dB
Signal-to-Intermodulation Distortion† [CCIF Method]		–90	–80	dB
Crosstalk† (DAA XMIT Output to Handset Speaker/Line Output)		–100	–80	dB
Total Out-of-Band Energy† (Measured from 0.555 × F_S to 100 kHz)			–60	dB
Audible Out-of-Band Energy†				
(Measured from 0.555 × F_S to 22 kHz, Tested at F_S = 8.0 kHz)			–80	dB
Common-Mode DC Offset (Referenced to Voltage Reference [CMOUT] Output)		20		mV
Differential DC Offset		10	50	mV
Programmable Attenuator				
Step Size (0 dB to –31.0 dB) (All Steps Tested)	0.487	1.0	1.513	dB
Output Attenuation Span†	30.487	31.0	31.513	dB
Full-Scale Output Voltage				
(RMS Values Assume Sine Wave Output) DAA XMIT Differential Output		2.121		V rms
	5.1	6.0	6.9	V p-p
			<2	Ω
Output Source Impedance—DAA XMIT†	600			Ω
External Load Impedance—DAA XMIT			15	pF
Pin Capacitance—DAA XMIT†			100	pF
Load Capacitance—DAA XMIT†				

HANDSET SPEAKER/LINE OUTPUT PATH

	Min	Typ	Max	Units
Digital-to-Analog Converter				
Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, A-Weighted)	78	86		dB
THD+N (–1.0 dB Referenced to Full Scale)			0.03	%
		–83	–70	dB
Signal-to-Intermodulation Distortion† [CCIF Method]		–90	–80	dB
DAC Crosstalk† (Handset Speaker/Line Output to DAA XMIT Output)		–100	–80	dB
Total Out-of-Band Energy† (Measured from $0.6 \times F_S$ to 100 kHz)			–60	dB
Audible Out-of-Band Energy†				
(Measured from $0.6 \times F_S$ to 22 kHz, Tested at F_S = 8.0 kHz)			–80	dB
Handset Speaker Common-Mode DC Offset (Relative to Voltage Reference				
[CMOUT] Output)		20		mV
Line Output Common-Mode DC Offset (Relative to Voltage Reference				
[CMOUT] Output)		40		mV
Differential DC Offset		10	50	mV
Programmable Amplifier/Attenuator				
Step Size (+12.0 dB to –34.5 dB) (All Steps Tested)	1.0	1.5	2.0	dB
Output Attenuation Span†	43.5	46.5	49.5	dB
Mute Attenuation†		–100		dB
Full-Scale Output Voltage				
(RMS Values Assume Sine Wave Output)				
Handset Speaker Differential Output		1.414		V rms
	3.1	4.0	4.8	V p-p
Line Out Single-Ended Output (10 kΩ Load)		0.707		V rms
	1.56	2.0	2.44	V p-p
Output Source Impedance—Handset Speaker†			<2	Ω
Output Source Impedance—Line Out†		400	600	Ω
External Load Impedance—Handset Speaker	1	1.2		kΩ
External Load Impedance—Line Out†	10			kΩ
Pin Capacitance—Handset Speaker			15	pF
Pin Capacitance—Line Out†			15	pF
Load Capacitance—Handset Speaker†			100	pF
Load Capacitance—Line Out†			100	pF

MONITOR SPEAKER PATH

	Min	Typ	Max	Units
Digital-to-Analog Converter				
THD+N (Referenced to Full Scale)		0.316	1.0	%
		–50	–40	dB
Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, A-Weighted)		50		dB
Programmable Attenuator				
Step Size (0 dB, –6 dB, –12 dB) (All Steps Tested)	–6.513	–6	–5.487	dB
Output Attenuation Span†	–12.513	–12	–11.487	dB
Mute Attenuation†		–80		dB
Full-Scale Output Voltage				
(RMS Values Assume Sine Wave Output) Monitor Speaker Output		0.707		V rms
	1.7	2.0	2.3	V p-p
Output Source Impedance–Monitor Speaker†			<1	Ω
External Load Impedance—Monitor Speaker†	8			Ω
Pin Capacitance—Monitor Speaker†			15	pF
Load Capacitance—Monitor Speaker†			100	pF

DIGITAL DECIMATION AND INTERPOLATION FILTERS—MODEM MODE 0†

	Min	Typ	Max	Units
Passband Edge (–0.220 dB Point)	0		$0.445 \times F_S$	Hz
Passband (–3.0 dB Point)	0		$0.490 \times F_S$	Hz
Passband Ripple	0		–0.17	dB
Transition Band	$0.445 \times F_S$		$0.555 \times F_S$	Hz
Stopband Edge[1]	$0.555 \times F_S$			Hz
Stopband Rejection (Plus 3 dB Rolloff)	78.0			dB
Group Delay			$19/F_S$	s
Group Delay Variation Over Passband			0.0	µs
Sample Rate			48	kHz

DIGITAL DECIMATION AND INTERPOLATION FILTERS—MODEM MODE 1†

	Min	Typ	Max	Units
Passband Edge (–0.24 dB Point)	0		$0.400 \times F_S$	Hz
Passband (–3.0 dB Point)	0		$0.453 \times F_S$	Hz
Passband Ripple	0		–0.24	dB
Transition Band	$0.400 \times F_S$		$0.555 \times F_S$	Hz
Stopband Edge[2]	$0.555 \times F_S$			Hz
Stopband Rejection (Plus 3 dB Rolloff)	52.8			dB
Group Delay			$10/F_S$	s
Group Delay Variation Over Passband			0.0	µs
Sample Rate			48	kHz

DIGITAL DECIMATION AND INTERPOLATION FILTERS—AUDIO MODE†

	Min	Typ	Max	Units
Passband Edge (–0.18 dB Point)	0		$0.400 \times F_S$	Hz
Passband (–3.0 dB Point)	0		$0.462 \times F_S$	Hz
Passband Ripple	0		–0.18	dB
Transition Band	$0.400 \times F_S$		$0.600 \times F_S$	Hz
Stopband Edge[3]	$0.600 \times F_S$			Hz
Stopband Rejection (Plus 3 dB Rolloff)	78.0			dB
Group Delay			$11/F_S$	s
Group Delay Variation Over Passband			0.0	µs
Sample Rate			48	kHz

DIGITAL INTERPOLATION FILTERS—MONITOR SPEAKER†

	Min	Typ	Max	Units
Passband Edge (–0.74 dB Point)	0		$0.350 \times F_S$	Hz
Passband (–3.0 dB Point)	0		$0.412 \times F_S$	Hz
Passband Ripple	0		–0.74	dB
Transition Band	$0.350 \times F_S$		$0.650 \times F_S$	Hz
Stopband Edge[4]	$0.650 \times F_S$			Hz
Stopband Rejection (Plus 12 dB Rolloff)	55.5			dB
Group Delay			$10/F_S$	s
Group Delay Variation Over Passband			0.0	µs
Sample Rate			48	kHz

NOTES

[1]The stopband repeats itself at multiples of $64 \times F_S$ where F_S is the sampling frequency. Thus the modem mode 0 digital filter will attenuate to –78.0 dB or better across the frequency spectrum, except for a range $\pm 0.555 \times F_S$ wide at multiples of $64 \times F_S$.

[2]The stopband repeats itself at multiples of $64 \times F_S$ where F_S is the sampling frequency. Thus the modem mode 1 digital filter will attenuate to –52.8 dB or better across the frequency spectrum, except for a range $\pm 0.555 \times F_S$ wide at multiples of $64 \times F_S$.

[3]The stopband repeats itself at multiples of $64 \times F_S$ where F_S is the sampling frequency. Thus the audio mode digital filter will attenuate to –78.0 dB or better across the frequency spectrum, except for a range $\pm 0.600 \times F_S$ wide at multiples of $64 \times F_S$.

[4]The stopband repeats itself at multiples of $64 \times F_S$ where F_S is the sampling frequency. Thus the audio mode digital filter will attenuate to –55.5 dB or better across the frequency spectrum, except for a range $\pm 0.650 \times F_S$ wide at multiples of $64 \times F_S$.

Specifications subject to change without notice.

VOLTAGE REFERENCE

	Min	Typ	Max	Units
CMOUT	2.0	2.45	2.7	V
External CMOUT Load Current†			10	μA
CMOUT Output Impedance†		4		kΩ

SYSTEM SPECIFICATIONS

	Min	Typ	Max	Units
System Frequency Response Ripple† (Line In to Line Out)			±0.5	dB
Differential Nonlinearity†			±1	Bit
Phase Linearity Deviation†			5	Degrees

STATIC DIGITAL SPECIFICATIONS

	Min	Typ	Max	Units
High-Level Input Voltage (V_{IH})				
Digital Inputs, Except XTALI	2.0		DV_{DD} + 0.3	V
XTALI	3.5		DV_{DD} + 0.3	V
Low-Level Input Voltage (V_{IL})				
Digital Inputs, Except XTALI	–0.3		0.8	V
XTALI	–0.3		1.5	V
High-Level Output Voltage (V_{OH})	2.4			V
Low-Level Output Voltage (V_{OL})			0.4	V
Input Leakage Current (GO/NOGO Tested)	–10		10	μA
Output Leakage Current (GO/NOGO Tested)	–10		10	μA

TIMING PARAMETERS (Guaranteed Over Operating Temperature and Digital Supply Range)

	Min	Typ	Max	Units
$\overline{\text{RESET}}$ LO Pulse Width (t_{RPWL})	100			ns
$\overline{\text{IOR}}$/$\overline{\text{IOW}}$ Strobe Width (t_{STW})	100			ns
AEN Setup to $\overline{\text{IOR}}$/$\overline{\text{IOW}}$ Falling (t_{AESU})	10			ns
AEN Hold from $\overline{\text{IOR}}$/$\overline{\text{IOW}}$ Rising (t_{AEHD})	0			ns
Address Setup to $\overline{\text{IOR}}$/$\overline{\text{IOW}}$ Falling (t_{ADSU})	10			ns
Address Hold from $\overline{\text{IOR}}$/$\overline{\text{IOW}}$ Rising (t_{ADHD})	0			ns
Data Hold from $\overline{\text{IOR}}$ Rising (t_{DHD1})			20	ns
Data Hold from $\overline{\text{IOW}}$ Rising (t_{DHD2})	15			ns
$\overline{\text{IOR}}$ Falling to Valid Read Data (t_{RDDV})			40	ns
Write Data Setup to $\overline{\text{IOW}}$ Rising (t_{WDSU})	10			ns

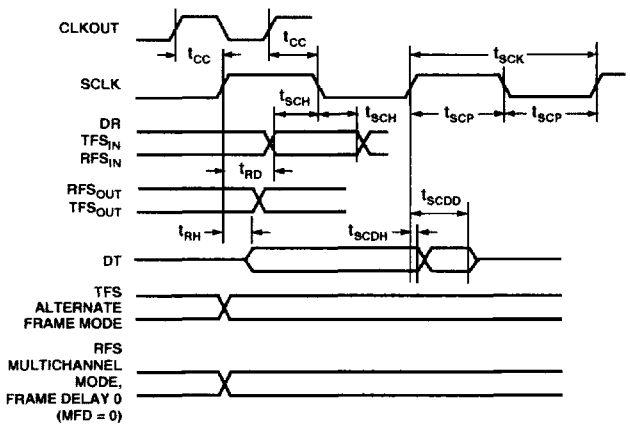


Figure 1. Serial Port Timing

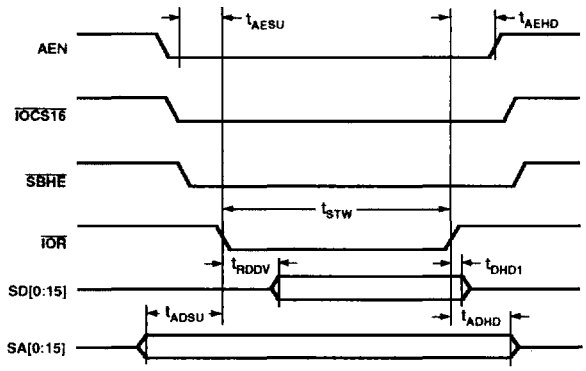


Figure 2. ISA PIO Read Cycle

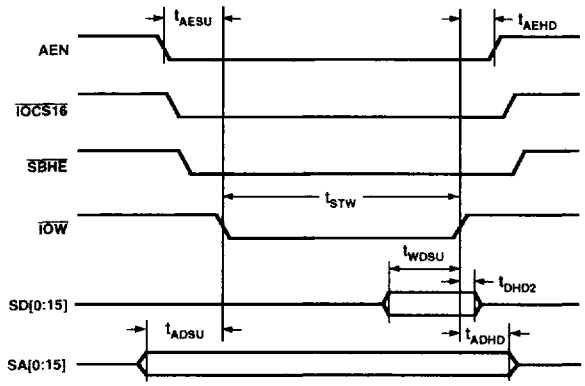


Figure 3. ISA PIO Write Cycle

POWER SUPPLY

	Min	Typ	Max	Units
Power Supply Range—AV_{DD} and DV_{DD}	4.75		5.25	V
Power Supply Current—5.0 AV_{DD} and DV_{DD} Operating		175	250	mA
Power Supply Current—5.0 AV_{DD} and DV_{DD} Power-Down			40	mA
Power Dissipation—5.0 AV_{DD} and DV_{DD} Operating (Current × Nominal Supply)			1000	mW
Power Dissipation—5.0 AV_{DD} and DV_{DD} Power-Down (Current × Nominal Supply)			200	mW
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)† (At Both Analog and Digital Supply Pins, for ADC and DAC)	40			dB

CLOCK SPECIFICATIONS†

	Min	Typ	Max	Units
Input Crystal/Clock Frequency		16.9344		MHz
Input Clock Duty Cycle (When an External Clock Is Used Instead of a Crystal)	25/75		75/25	%
Initialization Sample Rate Change Time (Neglecting Pipeline Delay of ≈ 1/4 Sample Period)			0	ms

†Guaranteed, not tested.
Specifications subject to change without notice.

PACKAGE CHARACTERISTICS

	Typ	Units
PQFP θ_{JA} (Thermal Resistance [Junction-to-Ambient])	35.9	°C/W
PQFP θ_{JC} (Thermal Resistance [Junction-to-Case])	8.38	°C/W
TQFP θ_{JA} (Thermal Resistance [Junction-to-Ambient])	36.1	°C/W
TQFP θ_{JC} (Thermal Resistance [Junction-to-Case])	3.81	°C/W

ABSOLUTE MAXIMUM RATINGS*

The AD1801 analog and digital power pins (AV_{DD} and DV_{DD}) must be powered by the same supply. The analog and digital power pins must always be at the same dc potential, or the AD1801 could be permanently damaged.

	Min	Max	Units
Power Supply			
Digital (V_{DD})	–0.3	6.0	V
Analog (V_{CC})	–0.3	6.0	V
Input Current			
(Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	–0.3	AV_{DD} + 0.3	V
Digital Input Voltage (Signal Pins)	–0.3	DV_{DD} + 0.3	V
Ambient Temperature (Operating)	0	+85	°C
Storage Temperature	–65	+150	°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD1801JS	0°C to +85°C	128-Lead PQFP	S-128A
AD1801JST	0°C to +85°C	128-Lead TQFP	ST-128
AD1801JST-REEL	0°C to +85°C	128-Lead TQFP	ST-128 Tape and Reel

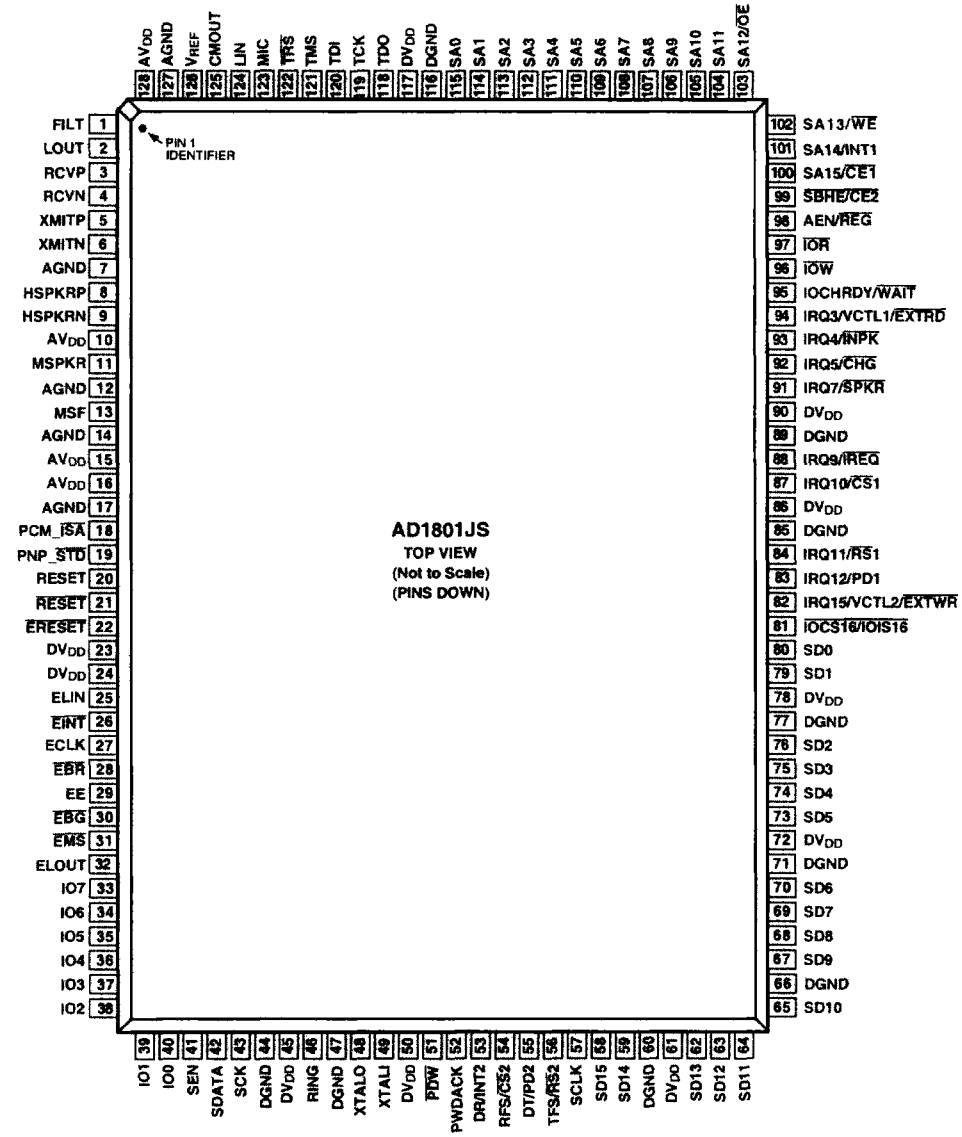
*S = Plastic Quad Flatpack; ST = Thin Quad Flatpack.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1801 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

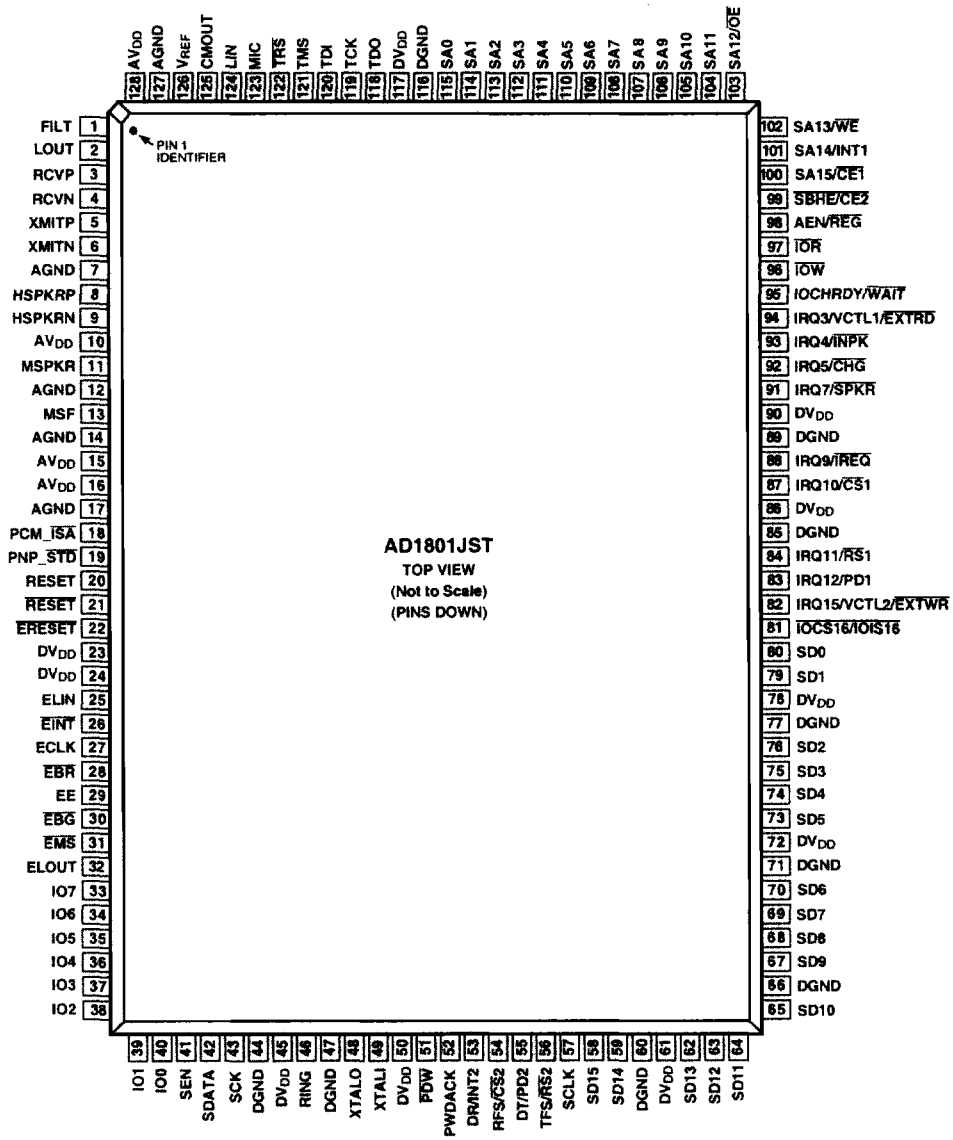
PIN CONFIGURATION

S-128A
128-Lead PQFP



PIN CONFIGURATION

ST-128
128-Lead TQFP



PIN FUNCTION DESCRIPTIONS

Device Configuration Signals

Pin Name	PQFP	TQFP	I/O	Description
PCM_$\overline{ISA}$	18	18	I	PCMCIA or ISA Host PC Bus Select Control. This pin has a weak internal pull-up device. See below for more information.
PNP_$\overline{STD}$	19	19	I	PnP or Standard Mode Select Control. When the AD1801 is configured in PCMCIA mode (i.e., when the PCM_$\overline{ISA}$ pin is HI), then the PNP_$\overline{STD}$ pin can be used as a general purpose input. The PNP_STDZ register bit can be used to monitor the state of this general purpose input under those conditions. This pin has a weak internal pull-up device. See below for more information.

DSP Core ICE-Port Emulator Interface

Pin Name	PQFP	TQFP	I/O	Description
EE	29	29	I	Emulator Enable.
$\overline{EBR}$	28	28	I	Emulator Bus Request.
$\overline{EBG}$	30	30	O	Emulator Bus Grant.
$\overline{ERESET}$	22	22	I	Emulator Reset.
$\overline{EMS}$	31	31	O	Emulator Memory Select.
$\overline{EINT}$	26	26	I	Emulator Interrupt.
ECLK	27	27	I	Emulator Clock.
ELIN	25	25	I	Emulator Input.
ELOUT	32	32	O	Emulator Output.

Ring Indicator

Pin Name	PQFP	TQFP	I/O	Description
RING	46	46	I	Phone Ring Indicator.

I/O Port

Pin Name	PQFP	TQFP	I/O	Description
IO7	33	33	I/O/Z	DSP Controlled Programmable I/O Bit 7. This pin has a weak internal pull-up device. See below for more information.
IO6	34	34	I/O/Z	DSP Controlled Programmable I/O Bit 6. This pin has a weak internal pull-up device. See below for more information.
IO5	35	35	I/O/Z	DSP Controlled Programmable I/O Bit 5. This pin has a weak internal pull-up device. See below for more information.
IO4	36	36	I/O/Z	DSP Controlled Programmable I/O Bit 4. This pin has a weak internal pull-up device. See below for more information.
IO3	37	37	I/O/Z	DSP Controlled Programmable I/O Bit 3. This pin has a weak internal pull-up device. See below for more information.
IO2	38	38	I/O/Z	DSP Controlled Programmable I/O Bit 2. This pin has a weak internal pull-up device. See below for more information.
IO1	39	39	I/O/Z	DSP Controlled Programmable I/O Bit 1. This pin has a weak internal pull-up device. See below for more information.
IO0	40	40	I/O/Z	DSP Controlled Programmable I/O Bit 0. This pin has a weak internal pull-up device. See below for more information.

Serial Memory (EEPROM) Port

Pin Name	PQFP	TQFP	I/O	Description
SCK	43	43	I/O/Z	Serial Data Clock. This pin has a weak internal pull-up device. See below for more information.
SEN	41	41	I/O/Z	Serial Data Enable Control. This pin has a weak internal pull-up device. See below for more information.
SDATA	42	42	I/O/Z	Bidirectional Serial Data. This pin has a weak internal pull-up device. See below for more information.

ISA Interface/PCMCIA Interface

Pin Name	PQFP	TQFP	I/O	Description
SD15	58	58	I/O/Z	System Data Bus Bit 15.
SD14	59	59	I/O/Z	System Data Bus Bit 14.
SD13	62	62	I/O/Z	System Data Bus Bit 13.
SD12	63	63	I/O/Z	System Data Bus Bit 12.
SD11	64	64	I/O/Z	System Data Bus Bit 11.
SD10	65	65	I/O/Z	System Data Bus Bit 10.
SD9	67	67	I/O/Z	System Data Bus Bit 9.
SD8	68	68	I/O/Z	System Data Bus Bit 8.
SD7	69	69	I/O/Z	System Data Bus Bit 7.
SD6	70	70	I/O/Z	System Data Bus Bit 6.
SD5	73	73	I/O/Z	System Data Bus Bit 5.
SD4	74	74	I/O/Z	System Data Bus Bit 4
SD3	75	75	I/O/Z	System Data Bus Bit 3.
SD2	76	76	I/O/Z	System Data Bus Bit 2.
SD1	79	79	I/O/Z	System Data Bus Bit 1.
SD0	80	80	I/O/Z	System Data Bus Bit 0.
SA11	104	104	I	System Address Bus Bit 11.
SA10	105	105	I	System Address Bus Bit 10.
SA9	106	106	I	System Address Bus Bit 9.
SA8	107	107	I	System Address Bus Bit 8.
SA7	108	108	I	System Address Bus Bit 7.
SA6	109	109	I	System Address Bus Bit 6.
SA5	110	110	I	System Address Bus Bit 5.
SA4	111	111	I	System Address Bus Bit 4.
SA3	112	112	I	System Address Bus Bit 3.
SA2	113	113	I	System Address Bus Bit 2.
SA1	114	114	I	System Address Bus Bit 1.
SA0	115	115	I	System Address Bus Bit 0.
$\overline{IOR}$	97	97	I	System I/O Read Strobe.
$\overline{IOW}$	96	96	I	System I/O Write Strobe.

Pin Name	PQFP	TQFP	I/O	ISA Description	PCMCIA Description
$\overline{IOCS16}/\overline{IOIS16}$	81	81	O/Z	System 16-Bit I/O Card Indicator.	System 16-Bit I/O Card Indicator.
SA12/$\overline{OE}$	103	103	I	System Address Bus Bit 12.	System Attribute Space Read Control.
SA13/$\overline{WE}$	102	102	I	System Address Bus Bit 13.	System Memory Space Write Control.
SA14/INT1	101	101	I	System Address Bus Bit 14.	Function 1 Interrupt Request.
SA15/$\overline{CE1}$	100	100	I	System Address Bus Bit 15.	System Card Enable 1.
$\overline{SBHE}/\overline{CE2}$	99	99	I	System Byte High Enable.	System Card Enable 2.
AEN/$\overline{REG}$	98	98	I	System Address Valid Indicator.	System Attribute Space Select.
IRQ9/$\overline{IREQ}$	88	88	O/Z	System Interrupt Request Mapped to IRQ9.	System Interrupt Request/Ready Indicator.
IOCHRDY/$\overline{WAIT}$	95	95	O/Z	System Bus Cycle Extension Control.	System Bus Cycle Extension Control.
IRQ3/VCTL1/ $\overline{EXTRD}$	94	94	O/Z	System Interrupt Request Mapped to IRQ3.	Reflects the opposite state of PCMCIA COR1 Register Bit 3. COR1 Bit 3 defaults as "0," so this pin defaults as HI. Read Strobe for interfacing to External Functions, such as the SMC91C94. See below for more information.
IRQ4/$\overline{INPK}$	93	93	O/Z	System Interrupt Request Mapped to IRQ4.	System Read Cycle Acknowledgment.
IRQ5/$\overline{CHG}$	92	92	O/Z	System Interrupt Request Mapped to IRQ5.	System Status Bit.
IRQ7/$\overline{SPKR}$	91	91	O/Z	System Interrupt Request Mapped to IRQ7.	Digital Audio Binary Waveform for Driving Host's Loudspeaker.

ISA Interface/PCMCIA Interface (Continues)

Pin Name	PQFP	TQFP	I/O	ISA Description	PCMCIA Description
IRQ10/$\overline{CS1}$	87	87	O/Z	System Interrupt Request Mapped to IRQ10.	Function 1 Chip Select.
IRQ11/$\overline{RS1}$	84	84	O/Z	System Interrupt Request Mapped to IRQ11.	Function 1 Reset.
IRQ12/PD1	83	83	O/Z	System Interrupt Request Mapped to IRQ12.	Function 1 Power-Down Control.
IRQ15/VCTL2/ $\overline{EXTWR}$	82	82	O/Z	System Interrupt Request Mapped to IRQ15.	Reflects the opposite state of PCMCIA COR2 Register Bit 3. COR2 Bit 3 defaults as "0," so this pin defaults as HI. Write Strobe for interfacing to External Functions, such as the SMC91C94. See below for more information.

Reset Signals

Pin Name	PQFP	TQFP	I/O	Description
RESET	20	20	I	ISA Bus Reset. RESET is active HI. The assertion of this signal will initialize the on-chip registers to their default values.
$\overline{RESET}$	21	21	I	Power-Up Reset. $\overline{RESET}$ is active LO. The assertion of this signal will initialize the on-chip registers to their default values.

DSP Serial Port (SPORT)/External Function Port 2

Pin Name	PQFP	TQFP	I/O	SPORT Interface	External Function Port 2
SCLK	57	57	I/O	Serial Clock.	
RFS/$\overline{CS2}$	54	54	I/O	Receive Frame Sync.	Function 2 Chip Select.
TFS/$\overline{RS2}$	56	56	I/O	Transmit Frame Sync.	Function 2 Reset.
DR/INT2	53	53	I	Serial Data Receive.	Function 2 Interrupt Request.
DT/PD2	55	55	O	Serial Data Transmit.	Function 2 Power-Down Control.

Boundary Scan JTAG Interface

Pin Name	PQFP	TQFP	I/O	Description
TMS	121	121	I	Boundary Scan Function Mode Select. This pin has a weak internal pull-up device. See below for more information.
TCK	119	119	I	Boundary Scan Function Clock. This pin has a weak internal pull-up device. See below for more information.
TDI	120	120	I	Boundary Scan Function Data Input. This pin has a weak internal pull-up device. See below for more information.
TDO	118	118	O	Boundary Scan Function Data Output.
$\overline{TRS}$	122	122	I	Boundary Scan Function Reset. This pin has a weak internal pull-up device. See below for more information. $\overline{TRS}$ must be connected to digital ground (dissipates a small amount of power) or to $\overline{RESET}$ (recommended) to ensure reliable operation.

Analog Signals

Pin Name	PQFP	TQFP	I/O	Description
RCVP	3	3	I	DAA Receive Line Input Positive Differential Signal.
RCVN	4	4	I	DAA Receive Line Input Negative Differential Signal.
MIC	123	123	I	Handset Microphone Mono Input. This signal can be either line level or –20 dB from line level.
LIN	124	124	I	Line Level Single-Ended Input.
HSPKRP	8	8	O	Handset Speaker Output Positive Differential Signal.
HSPKRN	9	9	O	Handset Speaker Output Negative Differential Signal.
LOUT	2	2	O	Line Level Single-Ended Output.
XMITP	5	5	O	DAA Transmit Output Positive Differential Signal.
XMITN	6	6	O	DAA Transmit Output Negative Differential Signal.
MSPKR	11	11	O	Monitor Speaker Single-Ended Output.

Crystal and Power-Down Signals

Pin Name	PQFP	TQFP	I/O	Description
XTALI	49	49	I	16.9344 MHz Crystal Input. When using a crystal as the clock source, the crystal should be connected between the XTALI and XTALO pins. This crystal should be 16.9344 MHz for the normal sampling rate range, i.e., 5.4 kHz to 44.1 kHz. A clock input may be driven into XTALI in place of a crystal.
XTALO	48	48	O	16.9344 MHz Crystal Output. When using a crystal as the clock source, the crystal should be connected between the XTALI and XTALO pins. If a clock is driven directly into XTALI, then XTALO should be left unconnected.
$\overline{PDW}$	51	51	I	Power-Down Control. $\overline{PDW}$ is active LO.
PWDACK	52	52	O	Power-Down Acknowledge.

Voltage Reference

Pin Name	PQFP	TQFP	I/O	Description
CMOUT	125	125	O	Common-Mode Voltage Output. Nominal 2.25 volt reference available externally for dc coupling and level-shifting. CMOUT should not be used where it will sink or source current. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor is required.
V_{REF}	126	126	I	Voltage Reference Filter. Voltage reference filter point for external bypassing only. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor is required.

Filter Connections

Pin Name	PQFP	TQFP	I/O	Description
FILT	1	1	I	Filter. This pin requires a 1.0 µF capacitor to analog ground for proper operation.
MSF	13	13	I	Monitor Speaker Filter. This pin requires a 1.0 nF capacitor to analog ground for proper operation.

Power Supplies and No Connects

Pin Name	PQFP	TQFP	I/O	Description
AV_{DD}	10, 15 16, 128	10, 15 16, 128	I	Analog Supply Voltage (+5 V ± 5%).
AGND	7, 12 14, 17 127	7, 12 14, 17 127	I	Analog Ground.
DV_{DD}	23, 24 45, 50 61, 72 78, 86 90, 117	23, 24 45, 50 61, 72 78, 86 90, 117	I	Digital Supply Voltage (+5 V ± 5%).
DGND	44, 47 60, 66 71, 77 85, 89 116	44, 47 60, 66 71, 77 85, 89 116	I	Digital Ground.

Pull-Up Resistors: Pins PCM-$\overline{ISA}$, PNP_$\overline{STD}$, IO[7:0], SEN, SDATA, SCK, TCK, TDI, TMS and $\overline{TRS}$ have internal pull-up devices. The pull-up device consists of a weak PMOS transistor that will source anywhere from 170 µA to 340 µA of current when the pin is held at 0 volts, depending on operating temperature and voltage.

MIXED SIGNAL FUNCTIONAL DESCRIPTION

FEATURES

Modem AFE

V.34/V.34bis modem codec (Analog Front-End [AFE]) with 1 Hz, 8/7 Hz, and 10/7 Hz programmable sample rates from 5.4 to 48 kHz, using 64 times oversampled, single-bit sigma-delta data conversion.

Support for all V.34 symbol and sample rates, including 8/7 and 10/7 symbol rates from single external 16.9344 MHz DSP crystal or clock.

Differential analog I/O to/from modem AFE for highest signal quality.

Programmable gain amplifier on modem receive ADC input with 0 dB, +6 dB or +12 dB gain.

Programmable attenuator on modem transmit DAC output, 0 dB to –31 dB with 1.0 dB typical step size.

Handset AFE

Full featured audio/handset codec (AFE) with 1 Hz programmable sample rates from 5.4 kHz to 48 kHz, using 64 times oversampled, single-bit sigma-delta data conversion.

Selectable 20 dB gain block for condenser microphones and selectable line input.

Selectable line output and differential analog output to handset speaker.

Programmable gain amplifier on ADC input, 0 dB to +22.5 dB with 1.5 dB typical step size.

Programmable gain amplifier/attenuator on DAC output +12 dB to –34.5 dB with 1.5 dB typical step size and full analog mute.

Monitor Speaker DAC

Sixteen word DSP output FIFO to minimize DSP overhead.

Sigma-delta DAC with sample rates tied to either modem codec or handset codec.

Programmable attenuator on DAC output with 0 dB, –6 dB or –12 dB attenuation, and full analog mute.

Output buffer to drive 8 Ω external monitor speaker.

DIGITAL FUNCTIONAL DESCRIPTION

FEATURES

ADSP-2181 DSP microcomputer core: 16.9344 MHz crystal, 33.8688 MIPS sustained performance.

Internal memory: 4K × 24 bits boot/program ROM, 16K × 24 bits of program RAM, 16K × 16 bits of data RAM, and a 512 × 8 bits dual port RAM for PCMCIA card configuration (Card Information Structure [CIS]) data tables or ISA Plug and Play (PnP) resource data.

Host PC bus interface option: 16-bit ISA bus or 16-bit PCMCIA PC Card bus.

PC 97 compliant single function Plug and Play (PnP) option.

PCMCIA PC Card bus interface and multifunction card configuration controller (PC Card 95 multifunction compliant).

PCMCIA interface supports two external card function ports for interfacing to communications ICs, e.g., ethernet controllers and ISDN devices.

Five pin synchronous serial port (SPORT) option over the second external function port for external serial communications with the DSP (communication to modem and handset ADC and DAC are lost).

Internal DMA controller for handling host PC program code download and data download/upload operations into and out of internal DSP memory.

Eight programmable I/O lines under DSP control.

Power management: hardware and software controlled power-down modes with ring awakening option.

Programmable interrupt requests.

DIGITAL ARCHITECTURAL OVERVIEW

The AD1801 comprises a 21xx family core, 16K × 16 data memory, 16K × 24 program memory, 512 bytes of CIS RAM and 4K × 24 words of boot/program ROM. Please refer to the ADSP-2181 DSP Microcomputer data sheet (Analog Devices publication C2041a-4-12/95) for additional information on the ADSP-2181 core, memory and peripheral features, and functions. This data sheet makes no attempt to document the ADSP-2181 core in the AD1801. Figure 4 illustrates the ADSP-2181 functional block diagram.

Figure 5 is a functional block diagram of the unique Windows® modem function of the AD1801. The DMA controller interfaces directly to the ADSP-2181's Internal DMA (IDMA) port.

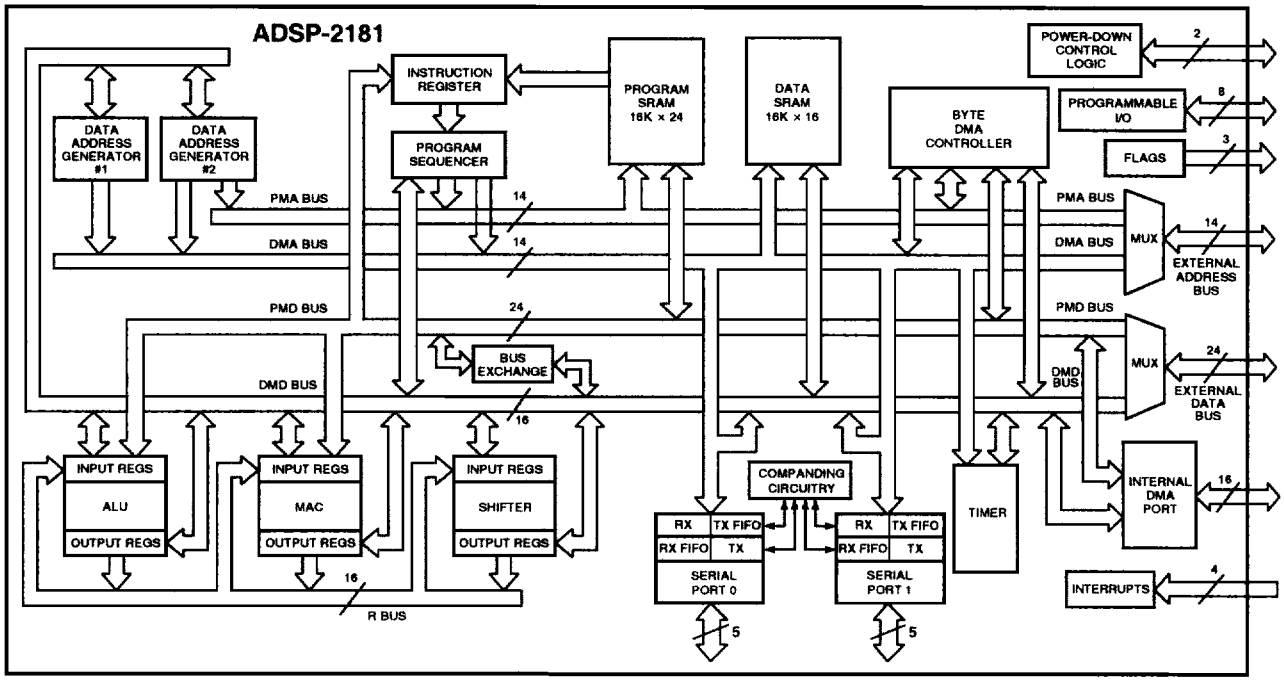


Figure 4. ADSP-2181 Block Diagram

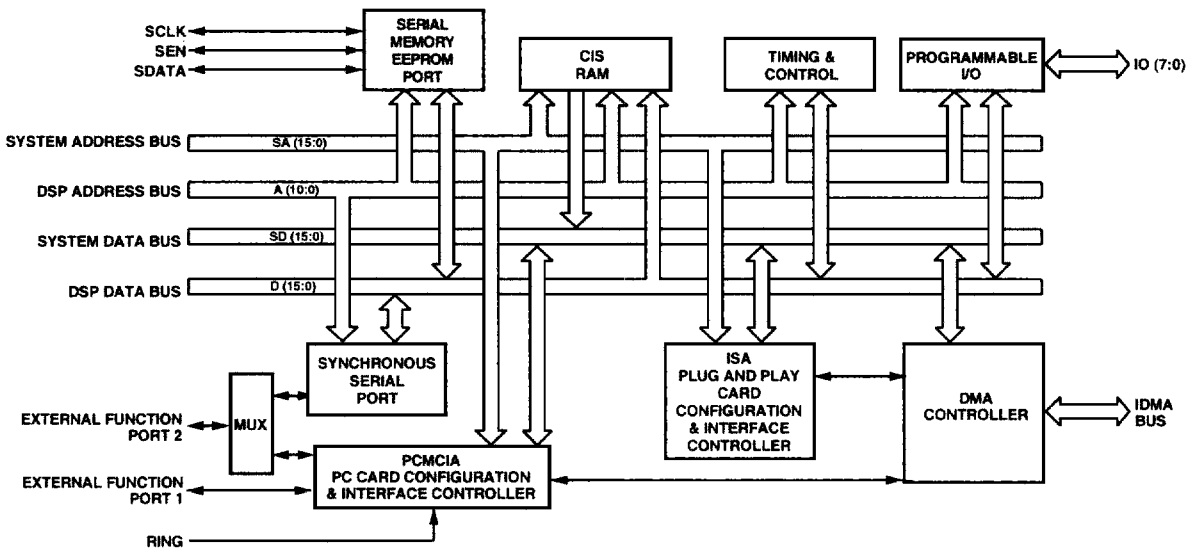


Figure 5. AD1801 Windows Modem Functional Block Diagram

Windows is a registered trademark of the Microsoft Corporation.

ADSP-2181 (DSP) INTERFACE

External Bus

The Windows modem function block interfaces to the ADSP-2181's external bus as an I/O peripheral to give the DSP access to control registers, status bits and the I/O ports. Note that the physical connections for this interface are made completely inside the AD1801. A 7-bit base address A[10:4], starting at address 0x000 (see Table VII), plus a 4-bit destination address, A[3:0], is decoded inside the Windows modem function. An I/O operation is qualified by an active $\overline{IOMS}$ signal initiated by the DSP. Up to 16 bits of the DSP external data bus, D[15:0], are used for passing data into and out of the Windows modem block; the direction is determined by DSP memory and enables controls $\overline{RD}$ and $\overline{WE}$. No wait states are required for internal DSP I/O operations.

Internal DMA Port

The Windows modem function block interfaces to the ADSP-2181's internal DMA port to provide the host PC with the means to access on-chip program and data memory. This communications path is crucial to the operation of the AD1801; it handles back-to-back host PC read or write operations for the active bus interface, i.e., it sustains data transfers of 4.17 Mbytes/s over the ISA 16-bit data bus and 8 Mbytes/s over the PC Card 16-bit data bus. This interface consists of a 16-bit multiplexed address/data bus (IAD[15:0]), port read ($\overline{IRD}$), write ($\overline{IWR}$), address latch (IAL) and start ($\overline{IS}$) control pins plus an acknowledge ($\overline{IACK}$) output.

Timing and Control

The Windows modem block of the AD1801 uses the maximum 33.8688 MHz clock output generated by the DSP core from an external 16.9344 MHz source. An external power-on reset circuit or the host PC Bus reset provides a reset to both the core DSP and Windows modem blocks; this forces the DSP to reboot from the internal ROM, rebuild the CIS table in the small internal RAM, and initialize various Windows modem programmable registers. The RING input is used as one interrupt to the DSP; a second interrupt is generated in the Windows modem Timing and Control block under host PC program control. The DSP can selectively enable/disable the ring detection interrupt via a bit in the DSP Control Register.

ISA Platform Compatible Host PC

The AD1801 is targeted for use in ISA add-on I/O slave card designs. It provides a glueless interface to the ISA bus whenever the PCM_$\overline{ISA}$ control input is tied LO. All bus drivers are compliant with ISA interface, electrical switching and drive capability specifications. In particular, "fast" outputs are not used as collectively they can induce glitches onto other bus controls when they are simultaneously switched.

ISA 16-Bit Data Bus Interface

The AD1801's ISA bus interface meets the timing specifications defined for 16-bit data ISA I/O standard access cycles. This interface consists of a 16-bit address bus (SA[15:0]), 16-bit data bus (SD[15:0]), I/O read and write strobes ($\overline{IOR}$ and $\overline{IOW}$), hardware reset RESET, IOCHRDY/$\overline{WAIT}$, $\overline{IOCS16}$/$\overline{IOIS16}$, and nine interrupt requests. One of the interrupts is selected for use by the card when it is configured; the others remain in a high impedance state to allow other cards their use. One bit in the AD1801's DSP Control register serves as the interrupt request to the PC. Its logic state is totally under DSP program control. A bit in the PC Control register allows the host PC to disable interrupt requests.

Plug And Play Card Configuration Controller

The AD1801 Plug And Play (PnP) module provides nine output enables to the interrupt request pins, only one of which is active after a PnP configuration session. The PnP module also determines the card's 7-bit I/O memory base address and provides an internal "card select" signal whenever the host PC accesses an AD1801 programmable register or the general purpose I/O port. The PNP_$\overline{STD}$ control input can be left unconnected or tied HI to enable this function.

The single function PnP module in the AD1801 meets Microsoft's PC 97 requirements. This means that it provides a minimum of seven I/O base locations and 7 interrupts as well as performing a full 16-bit I/O address decode. Since in PCMCIA mode only a single interrupt request is required, all but one of the ISA interrupt request pins are redefined when the AD1801 is configured for PCMCIA mode. These dual function pins are listed in Table I below. Since PCMCIA pin requirements exceed the minimum ISA requirements, two additional ISA interrupt requests can be readily accommodated as is reflected in the table.

In addition, the AD1801 provides the core DSP with the means to take the PnP function "off line" and permit the DSP access to the PnP internal registers. This allows the DSP the option of configuring the card at power-up, effectively bypassing the PnP card configuration sequence.

Table I. ISA IRQ to PCMCIA Signal Mapping

AD1801 Pin Name	ISA Bus Signal	PCMCIA Bus Signal	External Function Port-1 Signal
IRQ9/$\overline{IREQ}$	IRQ9	$\overline{IREQ}$	
IRQ3	IRQ3		
IRQ4/$\overline{INPK}$	IRQ4	$\overline{INPACK}$	
IRQ5/$\overline{CHG}$	IRQ5	$\overline{STSCHG}$	
IRQ7/$\overline{SPKR}$	IRQ7	$\overline{SPKR}$	
IRQ10/$\overline{CS1}$	IRQ10		$\overline{CS1}$
IRQ11/$\overline{RS1}$	IRQ11		$\overline{RS1}$
IRQ12/PD1	IRQ12		PD1
IRQ15	IRQ15		

The AD1801's PnP data address is maintained in the Timing & Control block, and the DMA Controller can be used to access the PnP data from the DSP's data memory without interrupting the DSP, thus stealing no more than a single DSP cycle per transfer. This is desirable since a PnP data request can occur at any time during normal operations.

ISA Standard Mode Compatibility

The PnP or Standard mode select input, PNP_$\overline{STD}$, is used to enable/disable the PnP logic module. It can be tied to DV_{DD} or left unconnected to enable the PnP logic or tied to DGND if PnP is not to be supported. An internal pull-up ensures that a HI state is seen when the pin is left unconnected. This input is available for the DSP to read. This allows the implementation of schemes that require the DSP to determine a suitable PC I/O space base address and PC interrupt for the I/O slave card when the standard mode is active. The DSP must program a 13-bit Default Base Address register with a 13-bit I/O Memory Base address and a 4-bit Default Interrupt Select register for selecting the active IRQ output. These registers are located in the AD1801's Timing & Control block and are active whenever inputs PNP_$\overline{STD}$ and PCM_$\overline{ISA}$ are tied to DGND.

PCMCIA Platform Compatible Host PC
The AD1801 is also targeted for use in PCMCIA's PC Card Standard slave card designs. It provides a glueless interface to the PC Card bus whenever the PCM_ISA control input is unconnected or tied to DV_{DD}. An internal pull-up allows this pin to be left unconnected in this mode.

PCMCIA 16-Bit PC Card Bus Interface
The AD1801's PC Card Bus interface meets the timing specifications defined for PCMCIA's PC Card Bus Standard '95 for both memory and I/O access cycles. This interface consists of a 12-bit address bus (SA[11:0]), 16-bit data bus (SD[15:0]), I/O read and write strobes ($\overline{IOR}$ and $\overline{IOW}$), card enables ($\overline{CE1}$ and $\overline{CE2}$), hardware reset (RESET), memory read and write strobes ($\overline{OE}$ and $\overline{WE}$), attribute and I/O memory select ($\overline{REG}$), PC interrupt/ready control ($\overline{IOIS16}$) and a read cycle acknowledge control ($\overline{INPK}$).

PCMCIA Card Configuration Controller
This module supports up to three card functions. Multiple function PC Cards require a separate set of Configuration registers per function. A Primary CIS common to all functions plus separate Secondary CIS's, one per function, are also required. Data for the Card Information Structures (CISs) is loaded into the internal 512-byte CIS RAM by the DSP during bootstrap loading. The DSP can obtain the data it needs from both its internal ROM and, for card-specific data, from an external serial EEPROM. The DSP sets a control bit in the AD1801 to indicate that RAM initialization has completed. The DSP does not have read access to the CIS memory.

The host PC can read the CIS memory at any time. If needed, the $\overline{WAIT}$ control can be activated to extend the read operation to meet bus cycle timing specifications. The host PC does not have write access to the CIS memory.

The card's modem function is implemented primarily within the AD1801. The RING input can be used to activate the PCMCIA's $\overline{STSCHG}$ status line to notify the host PC of ringing on the phone line. The host PC must set the Req_AttnEnab and SigChg bits in the AD1801's Extended Status register and Card Configuration and Status register, respectively, to activate this feature. A binary audio waveform, $\overline{SPKR}$, is available for use in lieu of the AUD output. This bus signal is intended to drive the host's loudspeaker. The 1.4 Mb/sec bitstream from the monitor speaker sigma delta engine provides the binary audio data stream for this pin. The host PC must set the Audio bit in the Card Configuration & Status register to enable this output.

The AD1801 provides two external function ports for supporting limited control of communications ICs, such as ethernet controller and ISDN devices, for example. Each external function port will consist of a function reset, chip select, address latch control, power-down control, and a function interrupt input. This interrupt will be passed on to the host PC if its particular function enable and interrupt enable controls are activated. The AD1801 also generates read and write strobes to facilitate data transfers between the host PC and the communication IC. Strobe timing is designed to meet the timing requirements of Standard Microsystems Corporation's SMC91C94 Ethernet Controller whenever External Function 1 is accessed by the host PC. The host PC's read and write strobes will be passed through the AD1801 whenever External Function 2 is accessed by the host PC. Table II identifies the PCMCIA Function Configuration registers needed to support each card function.

Table II. PCMCIA Function Configuration Registers

Function Configuration Registers			Required Registers and Bits		
Name	Bit Number	Bit Name	Internal Modem Function	External Function Port-1	External Function Port-2
Configuration Option Register	7	SRESET	Yes	Yes	Yes
	6	LevlREQ	1	1	1
	5	vendor option	0	0	0
	4	vendor option	0	0	0
	3	vendor option	0	0	0
	2	IREQ EN	Yes	Yes	Yes
	1	I/O BASE EN	Yes	Yes	Yes
	0	FUNC. EN	Yes	Yes	Yes
Card Configuration & Status Register	7	Chng	Yes	No	No
	6	SigChg	Yes	No	No
	5	IOis8	0	0	0
	4	not defined	0	0	0
	3	Audio	Yes	No	No
	2	PwrDn	Yes	Yes	Yes
	1	Intr	Yes	Yes	Yes
	0	IntrAck	Yes	Yes	Yes
Pin Replacement Register	7	CBVD1	*	*	*
	6	CBVD2	*	*	*
	5	CRdy	*	*	*
	4	CWProt	*	*	*
	3	RBVD1	*	*	*
	2	RBVD2	*	*	*
	1	RREADY	*	*	*
	0	RWProt	*	*	*
Socket and Copy Register	7	reserved (0)	*	*	*
	6				
	5	3-BIT COPY NUMBER	*	*	*
	4				
	3				
	2	3-BIT SOCKET NUMBER	*	*	*
	1				
	0				
Extended Status Register	7	RsvdEvt3	0	*	*
	6	RsvdEvt2	0	*	*
	5	RsvdEvt1	0	*	*
	4	ReqAttnEvt	Yes	*	*
	3	RsvdEnab3	0	*	*
	2	RsvdEnab2	0	*	*
	1	RsvdEnab1	0	*	*
	0	ReqAttnEnab	Yes	*	*
I/O Base Address Registers (4)	(7:0)	IO BASE 0	Yes	Yes	Yes
	(15:8)	IO BASE 1	Yes	Yes	Yes
	(23:16)	IO BASE 2	*	*	*
	(31:24)	IO BASE 3	*	*	*
I/O Size Register	(7:0)	IO SIZE	Yes	Yes	Yes

*Not Implemented, Reads 0, Writes Ignored.

All registers in PCMCIA Attribute Memory Space (0x200 to 0x27F) will read 0 and ignore writes unless specifically documented in the sections below.

Table III. PCMCIA Bus Transaction

Transaction Type	$\overline{IORD}$	$\overline{IOWR}$	$\overline{OE}$	$\overline{WE}$	$\overline{REG}$
I/O Read	0	1	1	1	0
I/O Write	1	0	1	1	0
Attribute Memory Read	1	1	0	1	0
Attribute Memory Write	1	1	1	0	0

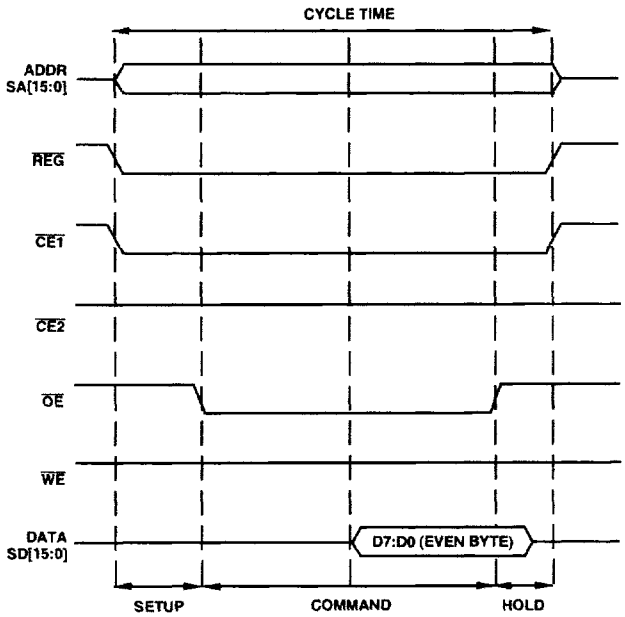


Figure 6. PCMCIA Attribute Memory Read Transfer

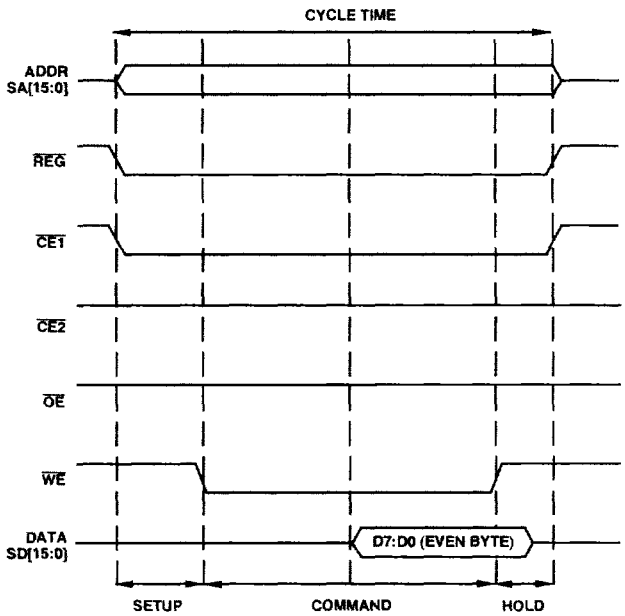


Figure 7. PCMCIA Attribute Memory Write Transfer

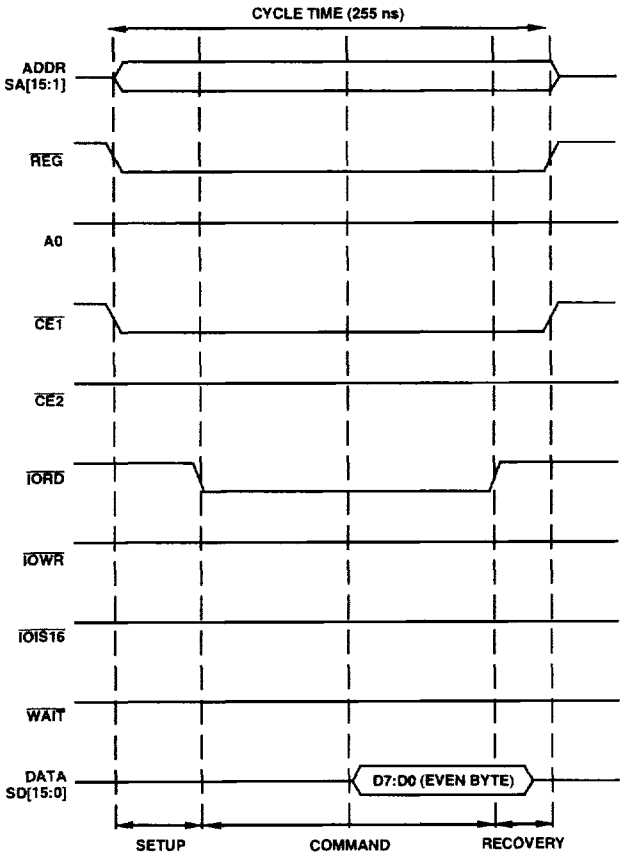


Figure 8. PCMCIA Default Read Cycle

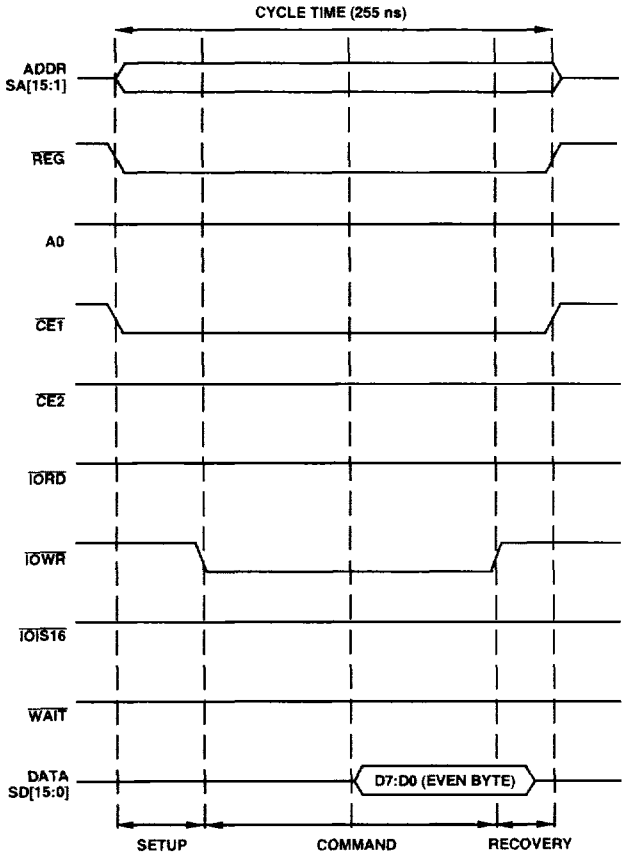


Figure 9. PCMCIA Default Write Cycle

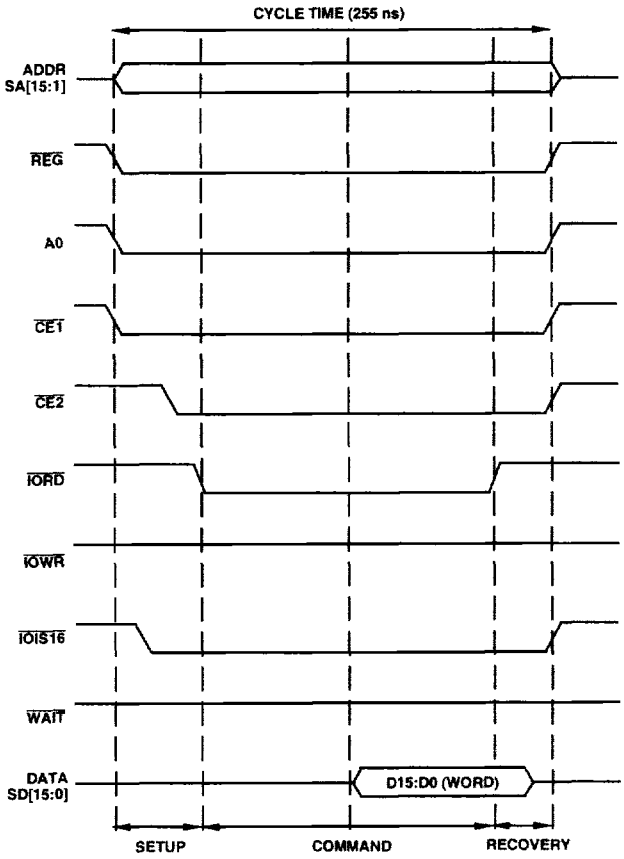


Figure 10. PCMCIA 16-Bit Word I/O Read Cycle

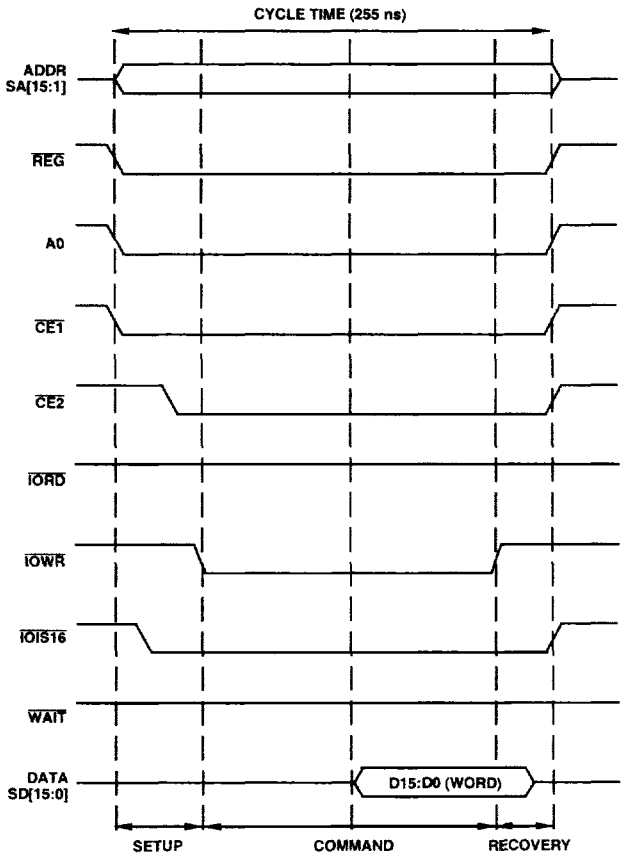


Figure 11. PCMCIA 16-Bit Word I/O Write Cycle

Interrupt Architecture
The signals used in generating interrupts are shown in Table IV.

Table IV. Interrupt Architecture

Pins	Description
PCM_$\overline{ISA}$	Indicates that the AD1801 is in PCMCIA mode or ISA mode.
RING	Falling edge signal indicates a ring interrupt.
INT1	External Function 1 interrupt request pin. Assumed to be a level signal if IntrACK1 = 0. Can be edge if IntrACK1 = 1.
INT2	External Function 2 interrupt request pin. Assumed to be a level signal if IntrACK2 = 0. Can be edge if IntrACK2 = 1.

PCMCIA/ PnP Signals	Description
Func0En	In PCMCIA mode, the Func0En bit is the "Enable Function" bit in the Configuration Option Register, COR0[0]. In PnP mode, the Func0En bit is the "active" bit for logical device zero.
Func1En	In PCMCIA mode, the Func1En bit is the "Enable Function" bit in the Configuration Option Register, COR1[0]. In PnP mode, the Func1En bit is deasserted.
Func2En	In PCMCIA mode, the Func2En bit is the "Enable Function" bit in the Configuration Option Register, COR2[0]. In PnP mode, the Func2En bit is deasserted.
IntrACKx	PCMCIA defined bit that determines the mode for clearing interrupts. When IntrACKx = 0, interrupts are cleared at the function (i.e., by the DSP or Host writing to ACK bits). When IntrACKx = 1, interrupts are cleared via the Intr bit (CSRx[1]). IntrACKx is CSRx[0]. The assertion of any of the three IntrACKs (from the three CSR registers) will cause the entire part to behave as if all three IntrACKs were asserted. Reads of the IntrACK bits will always return what was written.
Intr0	CSR0[1]. Reads of Intr0 indicate if the DSP/RING interrupt is asserted even if the interrupt pin enable 0 (IREQ0En) is deasserted.
Intr1	CSR1[1]. Reads of Intr1 indicate if the external Function 1 interrupt is asserted even if the interrupt pin enable 1 (IREQ1En) is deasserted.
Intr2	CSR2[1]. Reads of Intr2 indicate if the external Function 2 interrupt is asserted even if the interrupt pin enable 2 (IREQ2En) is deasserted.
Intr0 (WR = 0)	A write of "0" to the Intr0 bit, CSR0[1]. When IntrACK0 = 1, this causes both the DSP and RING interrupts to clear. When IntrACKx = 0, the write has no effect.
Intr1 (WR = 0)	A write of "0" to the Intr1 bit, CSR1[1]. When IntrACK1 = 1, this causes the External Function 1 (INT1) interrupt to clear. When IntrACK1 = 0, the write has no effect.
Intr2 (WR = 0)	A write of "0" to the Intr2 bit, CSR2[1]. When IntrACK2 = 1, this causes the External Function 2 (INT2) interrupt to clear. When IntrACK2 = 0, the write has no effect.
IREQ0En	Host writable bit (in the PCMCIA control registers) that enables DSP/RING interrupts on the IREQ# pin. PCMCIA mode only. (Created from COR0[2].)
IREQ1En	Host writable bit (in the PCMCIA control registers) that enables External Function 1 interrupts on the IREQ# pin. PCMCIA mode only. (Created from COR1[2].)
IREQ2En	Host writable bit (in the PCMCIA control registers) that enables External Function 2 interrupts on the IREQ# pin. PCMCIA mode only. (Created from COR2[2].)
IRQSELn	Nine versions of this signal exists for each of the nine ISA interrupt levels possible; assertion is mutually exclusive. IRQSELn signals are created from the PnP IRQ level register.

Table IV. Interrupt Architecture (Continued)

DSP Accessible Signals	Description
PCIRQ	DSP writable bit to request an interrupt on the system bus.
DSPIX	DSP writable bit to acknowledge/clear the DSP interrupt. Interrupt is acknowledged/cleared when DSPIX is set to "1." Writing this bit has no effect when in PCMCIA mode with IntrACK0 = 1.
RNGIX	DSP writable bit to acknowledge/clear the RING interrupt. Writing this bit has no effect when in PCMCIA mode with IntrACK0 = 1.

Host Accessible Signal (Not Including Those in PCMCIA/PnP Registers)	Description
DSPIE	Host writable bit which enables DSP interrupts.
RNGIE	Host writable bit which enables RING interrupts.
DSPI	Host readable bit which indicates whether an interrupt is pending from the DSP.
RNGI	Host readable bit which indicates whether an interrupt is pending from the RING pin.
DSPIA	Host writable bit to acknowledge/clear the DSP interrupt. Writing this bit has no effect when in PCMCIA mode with IntrACK0 =1.
RNGIA	Host writable bit to acknowledge/clear the RING interrupt. Writing this bit has no effect when in PCMCIA mode with IntrACK0 =1.

Table V. DSP Interrupt Mapping

Interrupt Source	Interrupt Vector Address	Comment
RESET	0x2000 (ROM)	Highest Priority
Power Down	0x002C (RAM)	
Host PC (IRQ2)	0x0004 (RAM)	Triggered by Writing "1" to PD Bit in PCC Register
IO0 Pin (IRQL1)	0x0008 (RAM)	Triggered by Rising or Falling Edge of IO0 Pin
PCMCIA Power-Down (IRQL0)	0x000C (RAM)	Triggered While PWRDN = 1 in CSR0 or $\overline{\text{PDW}}$ Pin LO
SPORT 0 Transmit	0x0010 (RAM)	
SPORT 0 Receive	0x0014 (RAM)	
RING Pin (IRQE)	0x0018 (RAM)	Triggered by Falling Edge on RING Pin
SPORT 1 Transmit	0x0020 (RAM)	
SPORT 1 Receive	0x0024 (RAM)	
Timer	0x0028 (RAM)	Lowest Priority

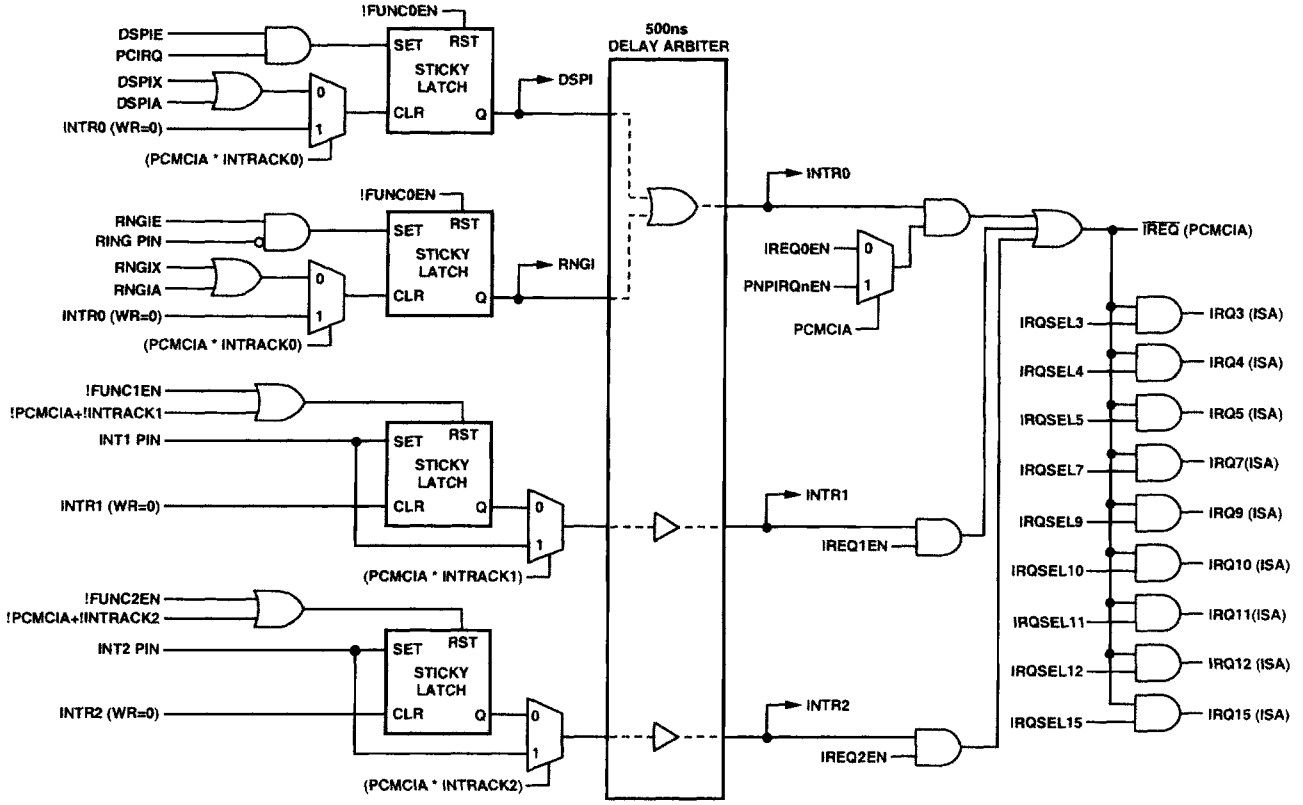


Figure 12. Interrupt Structure

DMA Controller

The AD1801's DMA Controller block ensures that both program code and data supplied by the host PC is loaded into on-chip memory in an efficient manner. The address counter in the IDMA Port can facilitate block transfers using the auto incrementing mechanism.

The host PC uses two locations in its I/O memory map for transferring data to and from on-chip program/data memory. One location allows the host PC effective access to the IDMA Control (IDMAC) register. This register is used by the host PC to program the 14-bit memory address counter (register bits 13:0) and 1-bit destination indicator (Register Bit 14). This register needs only to be programmed once for block transfers to/from the same type of memory, since the address counter is automatically incremented for each IDMA read/write operation. The destination indicator is programmed to a 1 whenever the host PC wishes to access data memory, otherwise program memory will be accessed. The second I/O location is reserved for the 16-bit data word provided to or supplied by the host PC. This location is mapped to a read-only Memory Data Input (MDI) register and to a write-only Memory Data Output (MDO) register.

When accessing the 24-bit program memory, two host PC read or write cycles from MDI or to MDO, respectively, are required. The first program memory access, or any odd numbered access following an IDMAC register update applies to the Most Significant (MS) 16 bits of the 24-bit program data word (Bits 23:8). The second access, or any even numbered access following an IDMAC register update applies to the Least Significant (LS) eight bits of the 24-bit program word (Bits 7:0). Bits MDO(15:8) are ignored by the AD1801 in this case for write operations; the host PC will receive valid data on MDI(7:0) for read operations. The IDMA address counter is not incremented until after the LS byte portion of the 24-bit program data word has been addressed. If the IDMAC register is updated before the second half of a program data read/write operation is executed, the capability to access the LS byte for the previous address value will be lost; the DMA controller will access the MS 16 bits of the data at the new address during the following program memory read/write operations.

When accessing data memory, only a single read or write cycle is required since the 16-bit memory words are accommodated by the DMA bus, IAD(15:0), and the host PC data bus, SD(15:0); however, the IDMAC register must be programmed first to let the DMA controller know that the next host PC initiated memory access cycles are targeted for data memory and to define a starting address. The IDMAC register is incremented upon completion of each successive write/read operation to/from the memory data registers, MDO and MDI.

The DMA Controller is able to provide the host PC with data without use of wait states for back-to-back read and write operations. The DSP continues to run at full speed while synchronization is achieved over a DMA bus cycle request; only then is a single DMA cycle stolen from the DSP. The entire DMA bus

cycle can take from 2.5 to a maximum of 3.5 DSP cycles to complete. One or two cycles are required for synchronization, then there is a half cycle setup time for the $\overline{IACK}$ control, followed by the single data transfer cycle.

If data cannot be presented onto the PC Card Bus within 100 ns from the falling edge of a read strobe using either the long or short IDMA Read Cycle timing, a data prefetch mechanism for every address counter update will be required. Internal holding registers can be used, essentially, to create a 1-word deep FIFO or to create a word register pair employing a ping-pong access arrangement, in order to meet PC Card Bus timing requirements.

Synchronous Serial Port

The AD1801 provides an external synchronous serial port (identical to the SPORT module in the ADSP-2181) that can be optionally selected in place of the second external function under the PCMCIA module's control. The Port Mode (PM) bit in the DSP Control register is used to select the enable option.

Power-Down Modes

The power-down control pins, $\overline{PWD}$ and PWDACK, available on the ADSP-2181, are brought out of the AD1801 to provide a hardware option for putting the DSP core in a low power state. The active HI PWDACK control indicates when the processor is powered down; it is deactivated when the processor has completed its power-up sequence. A logic LO on this pin also indicates that the processor's CLKOUT signal is valid and that program execution has begun.

General Purpose I/O Port

The AD1801 provides eight bits of general I/O, IO(7:0), that can be programmed by the DSP. The I/O Port Control (IPC) register determines port bit direction; a logic "0" sets a port bit to an output while a logic "1" sets a port bit to an input. Each port bit is tied to an internal weak pull-up resistor.

The AD1801 provides a single 8-bit output port register that is programmed by the DSP. Input port bits are not registered; they are simply passed onto the DSP data bus (D[15:0]) during active read operations accessing the DSP Input Port. Note that the DSP will read the internally generated output port bits that are active along with the active externally supplied input port bits.

The eight programmable I/O pins on the AD1801 (Pins 33 through 40) will source between 170 μA and 340 μA when they are three-stated. This feature provides weak pull-up capability from power-on. This current sourcing capacity should only be used to determine how fast the AD1801 will pull up the pin and how much current devices driving the AD1801's I/O pins need to sink to drive to logic LO.

When configured as outputs, the I/O pins will source 0.5 mA at 2.4 V (HI level output voltage) and will sink 2.0 mA at 0.4 V (LO level output voltage). They are conservative ratings for 10 ns edge transitions with a 50 pF load.

JTAG Scanning Logic

JTAG boundary scan logic is included in the AD1801.

The AD1801 is compliant with IEEE std. 1149.1a-1993. Only the mandatory instructions are supported. These are: BYPASS, SAMPLE/PRELOAD, and EXTEST. Scan order, from first in to last in, as follows.

Table VI. JTAG Scan Order

0 PCM_$\overline{ISA}$	43 RFS/CS2 OutEn	86 IRQ15/VCTL2
1 PNP_$\overline{STD}$	44 RFS/$\overline{CS2}$	87 IRQ12/PD1 OutEn
2 RESET	45 DT/PD2 OutEn	88 IRQ12/PD1
3 $\overline{RESET}$	46 DR/PD2	89 IRQ11/$\overline{RS1}$ OutEn
4 $\overline{ERESET}$	47 TFS/$\overline{RS2}$ OutEn	90 IRQ11/$\overline{RS1}$
5 TESTB (DV_{DD})	48 TFS/$\overline{RS2}$	91 IRQ10/$\overline{CS1}$ OutEn
6 ELIN	49 SCLK OutEn	92 IRQ10/$\overline{CS1}$
7 $\overline{EINT}$	50 SCLK	93 IRQ9/$\overline{IREQ}$ OutEn
8 ECLK	51 SD15 OutEn	94 IRQ9/$\overline{IREQ}$
9 $\overline{EBR}$	52 SD15	95 IRQ7/$\overline{SPKR}$ OutEn
10 EE	53 SD14 OutEn	96 IRQ7/$\overline{SPKR}$
11 $\overline{EBG}$	54 SD14	97 IRQ5/$\overline{CHG}$ OutEn
12 $\overline{EMS}$ OutEn	55 SD13 OutEn	98 IRQ5/$\overline{CHG}$
13 $\overline{EMS}$	56 SD13	99 IRQ4/$\overline{INPK}$ OutEn
14 ELOUT	57 SD12 OutEn	100 IRQ4/$\overline{INPK}$
15 IO7 OutEn	58 SD12	101 IRQ3/VCTL1 OutEn
16 IO7	59 SD11 OutEn	102 IRQ3/VCTL
17 IO6 OutEn	60 SD11	103 IOCHRDY/$\overline{WAIT}$ OutEn
18 IO6	61 SD10 OutEn	104 IOCHRDY/$\overline{WAIT}$
19 IO5 OutEn	62 SD10	105 $\overline{IOW}$
20 IO5	63 SD9 OutEn	106 $\overline{IOR}$
21 IO4 OutEn	64 SD9	107 AEN/$\overline{REG}$
22 IO4	65 SD8 OutEn	108 $\overline{SBHE}$/$\overline{CE2}$
23 IO3 OutEn	66 SD8	109 SA15/$\overline{CE1}$
24 IO3	67 SD7 OutEn	110 SA14/INT1
25 IO2 OutEn	68 SD7	111 SA13/$\overline{WE}$
26 IO2	69 SD6 OutEn	112 SA12/$\overline{OE}$
27 IO1 OutEn	70 SD6	113 SA11
28 IO1	71 SD5 OutEn	114 SA10
29 IO0 OutEn	72 SD5	115 SA9
30 IO0	73 SD4 OutEn	116 SA8
31 SEN OutEn	74 SD4	117 SA7
32 SEN	75 SD3 OutEn	118 SA6
33 SDATA OutEn	76 SD3	119 SA5
34 SDATA	77 SD2 OutEn	120 SA4
35 SCK OutEn	78 SD2	121 SA3
36 SCK	79 SD1 OutEn	122 SA2
37 RING	80 SD1	123 SA1
38 XTALI	81 SD0 OutEn	124 SA0
39 XTALO	82 SD0	
40 $\overline{PDW}$	83 $\overline{IOCS16}$/$\overline{IOIS16}$ OutEn	
41 PWDACK	84 $\overline{IOCS16}$/$\overline{IOIS16}$	
42 DR/INT2	85 IRQ15/VCTL2 OutEn	

NOTE
The JTAG input $\overline{TRS}$ (Pin 122) must be connected to digital ground (which dissipates a small amount of power due to the on-chip weak pull-up device) or to $\overline{RESET}$ (recommended) to ensure reliable AD1801 operation.

Emulation Mode (EZ-ICE® Port)

Unlike the ADSP-2181, which ignores its normal (non-emulator) reset pin when in emulator mode, all AD1801 reset sources are still functional when in emulator mode. This includes the RESET pin (ISA reset), the $\overline{\text{RESET}}$ pin (power-up reset), the RST (Host PC reset) bit in I/O mapped register PCC, PnP reset, and PCMCIA reset. As a result, in order to avoid erroneous emulator results, care must be taken to prevent the assertion of any of these resets during periods of time when the emulator actually takes control of the DSP core.

The 14-pin EZ-ICE port interface should be connected to the AD1801 as indicated below.

Table VII. Emulator Connections

EZ-ICE Connector Pin	AD1801 Connection
1 GND	Digital GND (Not Analog Supply)
2 $\overline{\text{BG}}$	No Connect
3 $\overline{\text{EBG}}$	$\overline{\text{EBG}}$ (Pin 30)
4 $\overline{\text{BR}}$	Digital V_{DD} (Not Analog Supply)
5 $\overline{\text{EBR}}$	$\overline{\text{EBR}}$ (Pin 28)
6 $\overline{\text{EINT}}$	$\overline{\text{EINT}}$ (Pin 26)
7 "key"	No Connect
8 ELIN	ELIN (Pin 25)
9 ELOUT	ELOUT (Pin 32)
10 ECLK	ECLK (Pin 27)
11 EE	EE (Pin 29)
12 $\overline{\text{EMS}}$	$\overline{\text{EMS}}$ (Pin 31)
13 $\overline{\text{RESET}}$	Digital V_{DD} (Not Analog Supply)
14 $\overline{\text{ERESET}}$	$\overline{\text{ERESET}}$ (Pin 22)

As with the ADSP-2181, all AD1801 emulation pins (Pins 22 and 25–32) should be floated when not connected to the EZ-ICE port. Within the AD1801 there is a pull-down resistor on the EE (emulation enable) pin which disables emulation mode when the EE pin is floated.

Note that the ADSP-2181 chip includes two emulator signals not found (and not required) on the AD1801 $\overline{\text{BG}}$ (Bus Grant) and $\overline{\text{BR}}$ (Bus Request). Under normal ADSP-2181 operation, and external device can interrupt the DSP to use its bus. This is done with the $\overline{\text{BR}}$ and $\overline{\text{BG}}$ pins; the external device asserts $\overline{\text{BR}}$, and the ADSP-2181 asserts $\overline{\text{BG}}$ when the bus is available. In the same scenario with an EZ-ICE in the system, the EZ-ICE takes the $\overline{\text{BR}}$ signal, ORs in its own bus request, and generates $\overline{\text{EBR}}$ to the ADSP-2181. The ADSP-2181 then asserts $\overline{\text{EBG}}$, which the emulator may pass on to the external device as $\overline{\text{BG}}$. During emulator mode, the ADSP-2181 ignores $\overline{\text{BR}}$ and three-states $\overline{\text{BG}}$ (so that the emulator can drive it instead). Since the AD1801 does not allow any external devices to be connected to the DSP core, there is no need for the $\overline{\text{BR}}$ and $\overline{\text{BG}}$ signals. When using an emulator, $\overline{\text{BR}}$ should be wired deasserted (HI) on the emulator connector.

PC AND DSP I/O MAPPED REGISTER DESCRIPTIONS

PC I/O Memory Map

The AD1801 bus interface uses the base address determined during an initialization period to allow host PC access to its internal registers and ports according to the table below. The base address will correspond to system address bits SA (15:3) when the AD1801 is in "ISA" mode and to bits SA (11:3) when the AD1801 is in "PCMCIA" mode.

Table VIII. PC I/O Memory Map

System Address Bits SA [11:3]	Resource Accessed Reads	Writes	Function
Base Addr + 0	PCS	PCC	Host PC Status and Control
Base Addr + 2	Reserved	IDMAC	Internal DMA Address
Base Addr + 4	MDI	MDO	Memory Data I/O
Base Addr + 6	TM	TM	Test Mode

PC Attribute Memory Map

Attribute memory space is defined for PCMCIA AD1801 configurations only.

All registers in PCMCIA Attribute Memory Space (0x200 to 0x27F) will read 0 and ignore writes unless specifically documented.

The AD1801 provides three PCMCIA Functions. Function 0 is completely contained on the AD1801 chip (i.e., the fax/data/voice modem), while Functions 1 and 2 are implemented externally to the AD1801 and are supported with I/O pins.

Table IX. PC Attribute Memory Map

System Address	Register/RAM Accessed Name	Valid Operation
0x000–0x3FF	CIS RAM	Read Only
0x400	COR0	Read/Write
0x402	CSR0	Read/Write
0x406	SCR0	Read/Write
0x408	ESR0	Read/Write
0x40A	IOBL0	Read/Write
0x40C	IOBH0	Read/Write
0x412	IOS0	Read/Write
0x440	COR1	Read/Write
0x442	CSR1	Read/Write
0x446	SCR1	Read/Write
0x44A	IOBL1	Read/Write
0x44C	IOBH1	Read/Write
0x452	IOS1	Read/Write
0x480	COR2	Read/Write
0x482	CSR2	Read/Write
0x48A	IOBL2	Read/Write
0x48C	IOBH2	Read/Write
0x492	IOS2	Read/Write

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PCMCIA Configuration Option Registers

COR0: PCMCIA Function 0 Configuration Register **Access: Read/Write** **Address: 0x400**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
SRESET	LevlReq	ConfIndex[5]	ConfIndex[4]	ConfIndex[3]	ConfIndex[2]	ConfIndex[1]	ConfIndex[0]

SRESET — Function 0 Software Reset. Setting this bit to "1" places the AD1801 in the reset state. This is equivalent to assertion of the hardware RESET signal except that this bit is not cleared. Resetting this bit to "0" leaves the AD1801 in the same state that follows a hardware reset. This bit is reset to "0" by power-up and hardware reset. This bit is sticky.

LevlReq — Function 0 Level Mode $\overline{IREQ}$. Level mode interrupts are defined when this bit is "1." Pulse mode (edge triggered) interrupts are defined when this bit is "0." This bit is hardcoded to "1" (level mode interrupts).

ConfIndex[5:3] — Configuration Index Bits 5 through 3 are defined as "vendor specific" and are not used to control anything on the AD1801. These bits can be written and read for general scratchpad purposes.

ConfIndex[2] — Configuration Index Bit 2 enables $\overline{IREQ}$ routing. When set to "1," $\overline{IREQ}$ interrupts are enabled for Function 0. When reset to "0," $\overline{IREQ}$ interrupts are disabled for Function 0. This bit is valid only when ConfIndex[0] (Function Enable) is set to "1" (enabled).

ConfIndex[1] — Configuration Index Bit 1 specifies the I/O addressing used. When set to "1," I/O addresses specified by the base and limit registers are passed to Function 0. When reset to "0," all host I/O addresses are passed to Function 0. This bit is valid only when ConfIndex[0] (Function Enable) is set to "1" (enabled).

ConfIndex[0] — Configuration Index Bit 0 enables or disables Function 0. When set to "1," Function 0 is enabled. When reset to "0," Function 0 is disabled and does not decode I/O addresses or generate $\overline{IREQ}$.

COR1: PCMCIA Function 1 Configuration Register **Access: Read/Write** **Address: 0x420**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
SRESET	LevlReq	ConfIndex[5]	ConfIndex[4]	ConfIndex[3]	ConfIndex[2]	ConfIndex[1]	ConfIndex[0]

SRESET — Function 1 Software Reset. Setting this bit to "1" drives the IRQ11/$\overline{RS1}$ output signal from the AD1801 LO. IRQ11/$\overline{RS1}$ is the Function 1 reset signal when the AD1801 is configured in PCMCIA mode.

LevlReq — Function 1 Level Mode $\overline{IREQ}$. Level mode interrupts are defined when this bit is "1." Pulse mode (edge triggered) interrupts are defined when this bit is "0." This bit is hardcoded to "1" (level mode interrupts).

ConfIndex[5:3] — Configuration Index Bits 5 through 3 are defined as "vendor specific" and are not used to control anything on the AD1801. These bits can be written and read for general scratchpad purposes.

ConfIndex[2] — Configuration Index Bit 2 enables $\overline{IREQ}$ routing. When set to "1," $\overline{IREQ}$ interrupts are enabled for Function 1. When reset to "0," $\overline{IREQ}$ interrupts are disabled for Function 1. This bit is valid only when ConfIndex[0] (Function Enable) is set to "1" (enabled).

ConfIndex[1] — Configuration Index Bit 1 specifies the I/O addressing used. When set to "1," I/O addresses specified by the base and limit registers are passed to Function 1. When reset to "0," all host I/O addresses are passed to Function 1. This bit is valid only when ConfIndex[0] (Function Enable) is set to "1" (enabled).

ConfIndex[0] — Configuration Index Bit 0 enables or disables Function 1. When set to "1," Function 1 is enabled. When reset to "0," Function 1 is disabled and does not decode I/O addresses or generate $\overline{IREQ}$.

COR2: PCMCIA Function 2 Configuration Register **Access: Read/Write** **Address: 0x440**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
SRESET	LevlReq	ConfIndex[5]	ConfIndex[4]	ConfIndex[3]	ConfIndex[2]	ConfIndex[1]	ConfIndex[0]

SRESET — Function 2 Software Reset. Setting this bit to "1" drives the TFS/$\overline{RS2}$ output signal from the AD1801 LO. SCLK/$\overline{RS2}$ is the Function 2 reset signal when the AD1801 is configured in PCMCIA mode.

LevlReq — Function 2 Level Mode $\overline{IREQ}$. Level mode interrupts are defined when this bit is "1." Pulse mode (edge triggered) interrupts are defined when this bit is "0." This bit is hardcoded to "1" (level mode interrupts).

ConfIndex[5:3] — Configuration Index Bits 5 through 3 are defined as "vendor specific" and are not used to control anything on the AD1801. These bits can be written and read for general scratchpad purposes.

ConfIndex[2] — Configuration Index bit 2 enables $\overline{IREQ}$ routing. When set to "1," $\overline{IREQ}$ interrupts are enabled for Function 2. When reset to "0," $\overline{IREQ}$ interrupts are disabled for Function 2. This bit is valid only when ConfIndex[0] (Function Enable) is set to "1" (enabled).

ConfIndex[1] Configuration Index bit 1 specifies the I/O addressing used. When set to "1," I/O addresses specified by the base and limit registers are passed to Function 2. When reset to "0," all host I/O addresses are passed to Function 2. This bit is valid only when ConfIndex[0] (Function Enable) is set to "1" (enabled).

ConfIndex[0] Configuration Index bit 0 enables or disables Function 2. When set to "1," Function 2 is enabled. When reset to "0," Function 2 is disabled and does not decode I/O addresses or generate $\overline{\text{IREQ}}$.

PCMCIA Card Configuration and Status Registers

CSR0: PCMCIA Function 0 Configuration and Status Register **Access: Read/Write** **Address: 0x402**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
Chng	SigChg	IOis8	Res(0)	Audio	PwrDn	Intr	IntrAck

Chng Status Change Detected. This bit indicates that one or more of the Pin Replacement register bits (CBVD1, CBVD2, CRDY or CWProt) is set to one, normally causing the $\overline{\text{CHG}}$ signal (Pin 92) to be asserted; however, if the SigChg bit (see below) is "1," and the card is configured for an I/O interface, the $\overline{\text{CHG}}$ pin is asserted when this bit is set.

SigChg Signal Change Enable/Disable. This bit is set and reset by the host to enable and disable a status change signal from the status register. When this bit is set and the card is configured for the I/O interface, the Chng bit controls Pin 92 ($\overline{\text{CHG}}$). If no status change signal is desired, the bit should be set to zero and the $\overline{\text{CHG}}$ signal will be held deasserted when the card is configured for I/O.

IOis8 I/O Cycles Occur Only as 8-Bit Transfers. When the host can provide I/O cycles only using the SD7:SD0 data path, the PCMCIA software will set this bit to a 1. The card is guaranteed that accesses to 16-bit registers will occur as two byte accesses rather than a single 16-bit access. This information is useful when 16-bit and 8-bit registers overlap.

On the AD1801, this bit is hardcoded to "0" (16-bit transfers allowed).

Res Reserved bits must be 0.

Audio Audio Enable. This bit enables audio information to be sent to the Host Bus Adapter via the speaker pin $\overline{\text{SPKR}}$ (Pin 91) when configured for an I/O interface.

PwrDn Power-Down. This bit is set to one to request that Function 0 enter a power-down state. PCMCIA software must not place Function 0 into a power-down state while the Function's READY pin in the LO (busy) state.

Intr Interrupt Request Pending. This bit represents the internal state of the interrupt request. This value is available whether or not interrupts have been configured. How the Intr bit is cleared is dependent up on how the IntrAck bit is configured.

IntrAck = 0—Intr reflects the function's interrupt request status. If the interrupt is cleared within the function, Intr is reset by the function.

IntrAck = 1—Intr remains set even though the interrupt condition has been cleared (i.e., sticky). It is reset by system software to indicate it is ready to receive another interrupt (implemented to support interrupt sharing).

IntrAck Interrupt Acknowledge. This bit determines the response of the Intr bit. The functionality associated with the IntrAck bit permits two or more functions to share the PC Card's $\overline{\text{IREQ}}$ pin.

IntrAck = 0—When IntrAck is reset, Intr functions as described above to support a single interrupt implementation.

IntrAck = 1—This causes the Intr bit to remain set even though the interrupt service routine has already serviced the interrupt. Normally, the interrupt service routine clears the interrupt pending bit in a function specific register, causing the Intr also to be cleared; however, to support interrupt sharing, the Intr bit is not cleared until PCMCIA specific software is ready to handle the next interrupt request. When cleared by the PCMCIA software, other interrupt requests that are pending can now be asserted over the PC Card's $\overline{\text{IREQ}}$ pin.

CSR1: PCMCIA Function 1 Configuration and Status Register **Access: Read/Write** **Address: 0x422**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
Chng	SigChg	IOis8	Res(0)	Audio	PwrDn	Intr	IntrAck

Chng Status Change Detected. This bit indicates that one or more of the Pin Replacement register bits (CBVD1, CBVD2, CRDY or CWProt) is set to one, normally causing the $\overline{\text{CHG}}$ signal (Pin 92) to be asserted. However, if the SigChg bit (see below) is "1," and the card is configured for an I/O interface, the $\overline{\text{CHG}}$ pin is asserted when this bit is set.

In the AD1801, Chng is "0" for Function 1.

SigChg — Signal Change Enable/Disable. This bit is set and reset by the host to enable and disable a status change signal from the status register. When this bit is set, and the card is configured for the I/O interface, the Chng bit controls Pin 92 ($\overline{CHG}$). If no status change signal is desired, the bit should be set to zero and the $\overline{CHG}$ signal will be held deasserted when the card is configured for I/O.

In the AD1801, SigChg is "0" for Function 1.

IOis8 — I/O cycles occur only as 8-bit transfers. When the host can provide I/O cycles only using the SD7:SD0 data path, the PCMCIA software will set this bit to a 1. The card is guaranteed that accesses to 16-bit registers will occur as two byte accesses rather than a single 16-bit access. This information is useful when 16-bit and 8-bit registers overlap.

On the AD1801, this bit is hardcoded to "0" (16-bit transfers allowed).

Res — Reserved bits must be 0.

Audio — Audio Enable. This bit enables audio information to be sent to the Host Bus Adapter via the speaker pin $\overline{SPKR}$ (Pin 91) when configured for an I/O interface.

In the AD1801, Audio is "0" for Function 1.

PwrDn — Power-Down. This bit is set to one to request that Function 1 enter a power-down state. PCMCIA software must not place Function 1 into a power-down state while the Function's READY pin is in the LO (busy) state.

Intr — Interrupt Request Pending. This bit represents the internal state of the interrupt request. This value is available whether or not interrupts have been configured. How the Intr bit is cleared is dependent up on how the IntrAck bit is configured.

IntrAck = 0—Intr reflects the function's interrupt request status. If the interrupt is cleared within the function, then Intr is reset by the function.

IntrAck = 1—Intr remains set even though the interrupt condition has been cleared (i.e., sticky). It is reset by system software to indicate it is ready to receive another interrupt (implemented to support interrupt sharing).

IntrAck — Interrupt Acknowledge. This bit determines the response of the Intr bit. The functionality associated with the IntrAck bit permits two or more functions to share the PC Card's $\overline{IREQ}$ pin.

IntrAck = 0—When IntrAck is reset, Intr functions as described above to support a single interrupt implementation.

IntrAck = 1—This causes the Intr bit to remain set even though the interrupt service routine has already serviced the interrupt. Normally, the interrupt service routine clears the interrupt pending bit in a function specific register, causing the Intr also to be cleared; however, to support interrupt sharing, the Intr bit is not cleared until PCMCIA specific software is ready to handle the next interrupt request. When cleared by the PCMCIA software, other interrupt requests that are pending can now be asserted over the PC Card's $\overline{IREQ}$ pin.

CSR2: PCMCIA Function 2 Configuration and Status Register **Access: Read/Write** **Address: 0x442**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
Chng	SigChg	IOis8	Res(0)	Audio	PwrDn	Intr	IntrAck

Chng — Status Change Detected. This bit indicates that one or more of the Pin Replacement register bits (CBVD1, CBVD2, CRDY or CWProt) is set to one, normally causing the $\overline{CHG}$ signal (Pin 92) to be asserted. However, if the SigChg bit (see below) is "1" and the card is configured for an I/O interface, the $\overline{CHG}$ pin is asserted when this bit is set.

In the AD1801, Chng is "0" for Function 2.

SigChg — Signal Change Enable/Disable. This bit is set and reset by the host to enable and disable a status change signal from the status register. When this bit is set and the card is configured for the I/O interface, the Chng bit controls Pin 92 ($\overline{CHG}$). If no status change signal is desired, the bit should be set to zero and the $\overline{CHG}$ signal will be held deasserted when the card is configured for I/O.

In the AD1801, SigChg is "0" for Function 2.

IOis8 — I/O Cycles Occur Only as 8-Bit Transfers. When the host can provide I/O cycles using only the SD7:SD0 data path, the PCMCIA software will set this bit to a 1. The card is guaranteed that accesses to 16-bit registers will occur as two byte accesses rather than a single 16-bit access. This information is useful when 16-bit and 8-bit registers overlap.

On the AD1801, this bit is hardcoded to "0" (16-bit transfers allowed).

Res — Reserved bits must be 0.

Audio — Audio Enable. This bit enables audio information to be sent to the Host Bus Adapter via the speaker pin $\overline{SPKR}$ (Pin 91) when configured for an I/O interface.

In the AD1801, Audio is "0" for Function 2.

PwrDn — Power-Down. This bit is set to one to request that Function 2 enter a power-down state. PCMCIA software must not place Function 2 into a power-down state while the Function's READY pin is in the LO (busy) state.

Intr — Interrupt Request Pending. This bit represents the internal state of the interrupt request. This value is available whether or not interrupts have been configured. How the Intr bit is cleared is dependent upon how the IntrAck bit is configured.

IntrAck = 0—Intr reflects the function's interrupt request status. If the interrupt is cleared within the function, Intr is reset by the function.

IntrAck = 1—Intr remains set even though the interrupt condition has been cleared (i.e., sticky). It is reset by system software to indicate it is ready to receive another interrupt (implemented to support interrupt sharing).

In the AD1801, Intr is "0" for Function 2.

IntrAck — Interrupt Acknowledge. This bit determines the response of the Intr bit. The functionality associated with the IntrAck bit permits two or more functions to share the PC Card's $\overline{IREQ}$ pin.

IntrAck = 0—When IntrAck is reset, Intr functions as described above to support a single interrupt implementation.

IntrAck = 1—This causes the Intr bit to remain set even though the interrupt service routine has already serviced the interrupt. Normally the interrupt service routine clears the interrupt pending bit in a function specific register, causing the Intr to also be cleared; however, to support interrupt sharing, the Intr bit is not cleared until PCMCIA specific software is ready to handle the next interrupt request. When cleared by the PCMCIA software, other interrupt requests that are pending can now be asserted over the PC Card's $\overline{IREQ}$ pin.

In the AD1801, IntrAck is ignored for Function 2.

PCMCIA Extended Status Register

ESR0: PCMCIA Function 0 Extended Status Register **Access: Read/Write** **Address: 0x408**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
Event3	Event2	Event1	Req Attn	Enable3	Enable 2	Enable1	Re Attn Enable

Event3 — Reserved for future expansion/definition—must be reset (0).

Event2 — Reserved for future expansion/definition—must be reset (0).

Event1 — Reserved for future expansion/definition—must be reset (0).

Req Attn — This bit is latched within one (1) ms of an event occurring on the PC Card, such as the start of each cycle of the ring frequency to indicate the presence of ringing on the phone line in the case of a modem card. When this bit is set to a one (1), and the Req Attn Enable bit is set to a one (1), the Changed bit in the Configuration and Status register will also be set to a one (1), and if the SigChg bit in the Configuration and Status register has also been set by the host, the $\overline{CHG}$ pin (Pin 91) will be asserted. The host writing a one (1) to this bit will reset it to zero (0). Writing a zero (0) to this bit will not have any effect.

Enable3 — Reserved for future expansion/definition—must be reset (0).

Enable2 — Reserved for future expansion/definition—must be reset (0).

Enable1 — Reserved for future expansion/definition—must be reset (0).

Req Attn Enable — Setting this bit to a one (1) enables the setting of the Changed bit in the Configuration and Status register when the Req Attn bit is set. When this bit is reset to a zero (0), this feature is disabled. The state of the Req Attn bit is not affected by the Req Attn Enable bit.

PCMCIA I/O Base Registers

IOBL0: PCMCIA Function 0 I/O Low Base Register **Address: 0x40A**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
IOBL0[7]	IOBL0[6]	IOBL0[5]	IOBL0[4]	IOBL0[3]	IOBL0[2]	IOBL0[1]	IOBL0[0]

IOBL0[7:0] — Low order byte of I/O base for Function 0.

IOBL1: PCMCIA Function 1 I/O Low Base Register **Address: 0x42A**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
IOBL1[7]	IOBL1[6]	IOBL1[5]	IOBL1[4]	IOBL1[3]	IOBL1[2]	IOBL1[1]	IOBL1[0]

IOBL1[7:0] — Low order byte of I/O base for Function 1.

PwrDn — Power-Down. This bit is set to one to request that Function 2 enter a power-down state. PCMCIA software must not place Function 2 into a power-down state while the Function's READY pin is in the LO (busy) state.

Intr — Interrupt Request Pending. This bit represents the internal state of the interrupt request. This value is available whether or not interrupts have been configured. How the Intr bit is cleared is dependent upon how the IntrAck bit is configured.

IntrAck = 0—Intr reflects the function's interrupt request status. If the interrupt is cleared within the function, Intr is reset by the function.

IntrAck = 1—Intr remains set even though the interrupt condition has been cleared (i.e., sticky). It is reset by system software to indicate it is ready to receive another interrupt (implemented to support interrupt sharing).

In the AD1801, Intr is "0" for Function 2.

IntrAck — Interrupt Acknowledge. This bit determines the response of the Intr bit. The functionality associated with the IntrAck bit permits two or more functions to share the PC Card's $\overline{IREQ}$ pin.

IntrAck = 0—When IntrAck is reset, Intr functions as described above to support a single interrupt implementation.

IntrAck = 1—This causes the Intr bit to remain set even though the interrupt service routine has already serviced the interrupt. Normally the interrupt service routine clears the interrupt pending bit in a function specific register, causing the Intr to also be cleared; however, to support interrupt sharing, the Intr bit is not cleared until PCMCIA specific software is ready to handle the next interrupt request. When cleared by the PCMCIA software, other interrupt requests that are pending can now be asserted over the PC Card's $\overline{IREQ}$ pin.

In the AD1801, IntrAck is ignored for Function 2.

PCMCIA Extended Status Register

ESR0: PCMCIA Function 0 Extended Status Register **Access: Read/Write** **Address: 0x408**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
Event3	Event2	Event1	Req Attn	Enable3	Enable2	Enable1	Re Attn Enable

Event3 — Reserved for future expansion/definition—must be reset (0).

Event2 — Reserved for future expansion/definition—must be reset (0).

Event1 — Reserved for future expansion/definition—must be reset (0).

Req Attn — This bit is latched within one (1) ms of an event occurring on the PC Card, such as the start of each cycle of the ring frequency to indicate the presence of ringing on the phone line in the case of a modem card. When this bit is set to a one (1), and the Req Attn Enable bit is set to a one (1), the Changed bit in the Configuration and Status register will also be set to a one (1), and if the SigChg bit in the Configuration and Status register has also been set by the host, the $\overline{CHG}$ pin (Pin 91) will be asserted. The host writing a one (1) to this bit will reset it to zero (0). Writing a zero (0) to this bit will not have any effect.

Enable3 — Reserved for future expansion/definition—must be reset (0).

Enable2 — Reserved for future expansion/definition—must be reset (0).

Enable1 — Reserved for future expansion/definition—must be reset (0).

Req Attn Enable — Setting this bit to a one (1) enables the setting of the Changed bit in the Configuration and Status register when the Req Attn bit is set. When this bit is reset to a zero (0), this feature is disabled. The state of the Req Attn bit is not affected by the Req Attn Enable bit.

PCMCIA I/O Base Registers

IOBL0: PCMCIA Function 0 I/O Low Base Register **Address: 0x40A**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
IOBL0[7]	IOBL0[6]	IOBL0[5]	IOBL0[4]	IOBL0[3]	IOBL0[2]	IOBL0[1]	IOBL0[0]

IOBL0[7:0] — Low order byte of I/O base for Function 0.

IOBL1: PCMCIA Function 1 I/O Low Base Register **Address: 0x42A**

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
IOBL1[7]	IOBL1[6]	IOBL1[5]	IOBL1[4]	IOBL1[3]	IOBL1[2]	IOBL1[1]	IOBL1[0]

IOBL1[7:0] — Low order byte of I/O base for Function 1.

RNGIA Host PC Interrupt from RING Pin Acknowledge. In ISA mode, RING Pin initiated interrupts to the host PC are cleared by writes to this bit. Each time a "1" is written to this bit, the RNGI (Host PC interrupt request from RING Pin) bit in the PC I/O mapped register PCS is cleared to "0." Writing a "0" to this bit has no effect on RNGI.

DSPIE Host PC Interrupt from DSP Enable. Used only in ISA mode. This bit determines if a pending host interrupt request from the DSP, indicated by the DSPI bit in the PCS register being set to "1," can cause a host interrupt. The state of this bit does not however effect the ability to set and clear the DSPI bit itself.
0 = IRQ to Host when DSPI Equals "1" Disabled (default)
1 = IRQ to Host when DSPI Equals "1" Enabled

RNGIE Host PC Interrupt from RING Pin Enable. Used only in ISA mode. This bit determines if a pending host interrupt from the RING Pin, indicated by the RNGI bit in the PCS register being set to "1," can cause a host interrupt. The state of this bit does not, however, effect the ability to set and clear the RNGI bit itself.
0 = IRQ to Host when RNGI Equals "1" Disabled (default)
1 = IRQ to Host when RNGI Equals "1" Enabled

INT DSP Interrupt. The DSP is sent an interrupt pulse via IRQ2 each time a "1" is written to this bit. Note: IRQ2 must be configured in the DSP to be edge-sensitive.

RST DSP Reset. Each time this bit is set to "1," the DSP is sent a reset pulse. Setting this bit to "1" also causes:
1) The DSP Reset source indicator bits (see DRST[1:0] in the DSP I/O mapped register IP) to be set to "11"; and
2) The codec channel enable bits (see MEN, HEN and MSEN in the DSP I/O mapped register CC) to be reset to "0."

PD AD1801 Power-Down. Writing a "1" to this bit initiates the process of powering down the AD1801. Writing a "0" to this bit has no effect. A read of this bit will always return a "0." See the Power Consumption section of this document for important additional details.

Default state after reset: 0000 0000 0000 0000 (0x0000).

PC Status **Mnemonic: PCS** **Access: Read Only** **Address Offset: 0x0**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
DSPI	RNGI	res	res	res	res	res	res
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
res	res	res	res	res	res	res	res

DSPI2 Host PC Interrupt Request from DSP. This bit is set to "1" whenever the DSP writes a "1" to the PCIRQ (Host PC interrupt request) bit in the DC (DSP Control) register. This bit is cleared each time the host PC writes a "1" to the DSPIA (Host PC interrupt from DSP acknowledge) bit in the PCC (PC Control) register. When set to "1," a host PC interrupt will be generated by driving the selected IRQ pin LO provided: 1) the AD1801 is in ISA mode; 2) host PC interrupts from the DSP are enabled (see the DSPIE bit in the PCC register); and 3) an interrupt from the RING Pin is not already active, i.e., the IRQ pin is not already driven LO. If a RING Pin interrupt is already active, the DSP interrupt will be postponed until 500 to 600 ns after the RING Pin interrupt is cleared, provided ALL conditions necessary to generate a DSP interrupt are still active. Although this bit is not used in PCMCIA mode to generate host interrupts, it may still be monitored to aid in distinguishing between DSP and RING Pin interrupts provided it is cleared at the appropriate times.

RNGI Host PC Interrupt Request from RING Pin. This bit is set to "1" whenever the RING Pin is driven from HI to LO. This bit is cleared each time the host PC writes a "1" to the RNGIA (Host PC interrupt from RING Pin acknowledge) bit in the PCC (PC Control) register. When set to "1," a host PC interrupt will be generated by driving the selected IRQ pin LO provided: 1) the AD1801 is in ISA mode; 2) host PC interrupts from the RING Pin are enabled (see the RNGIE bit in the PCC register); and 3) an interrupt from the DSP is not already active, i.e., the IRQ pin is not already being driven LO. If a DSP interrupt is already active, the RING Pin interrupt will be postponed until 500 to 600 ns after the DSP interrupt is cleared, providing ALL conditions necessary to generate a RING Pin interrupt are still active. Although this bit is not used in PCMCIA mode to generate host interrupts, it may still be monitored to aid in distinguishing between DSP and RING Pin interrupts, provided it is cleared at the appropriate times.

Default state after reset: 0000 0000 0000 0000 (0x0000).

Internal DMA Control **Mnemonic: IDMAC** **Access: Write Only** **Address Offset: 0x2**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
RWS	TYPE	MA13	MA12	MA11	MA10	MA9	MA8
Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

Note: After writing this register, the MDI register must NOT be read for at least 250 ns (assuming a 16.9344 MHz clock input on the XTALI pin). Performing a dummy read of the PCS register immediately after writing this register would be one way of satisfying this required delay.

RWS Read or Write Select. Specifies which DMA access is enabled.
0 = Read Access via Register MDI Enabled (Write Access via MDO Register Ignored)
1 = Write Access via Register MDO Enabled (Read Access via MDI Yield Data)

TYPE Memory Type Select. Specifies the memory type accessed by reads of the MDI register or writes to the MDO register.
0 = Program Memory Accessed
1 = Data Memory Accessed

MA[13:0] Memory Address. Specifies an initial memory address to be read via reads of the MDI register, or written via writes to the MDO register. After either a read or a write, this address is auto-incremented.

Default state after system reset: 0000 0000 0000 0000 (0x0000).

Memory Data Inputs **Mnemonic: MDI** **Access: Read Only** **Address Offset: 0x4**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
MDI15	MDI14	MDI13	MDI12	MDI11	MDI10	MDI9	MDI8
Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
MDI7	MDI6	MDI5	MDI4	MDI3	MDI2	MDI1	MDI0

MDI[15:0] Memory Data Input. Reading this register returns stale data if IDMA read access is not enabled. See the RWS bit in register IDMAC.

When reading program memory: the upper 16 bits of the 24-bit program memory word are read by a first read of this register. The lowest eight bits of the program memory word are read on bits 7:0 of this register by the next read of this register. During the second read, bits 15:8 are always read as zeros.

Memory Data Output **Mnemonic: MDO** **Access: Write Only** **Address Offset: 0x4**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
MDO15	MDO14	MDO13	MDO12	MDO11	MDO10	MDO9	MDO8
Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
MDO7	MDO6	MDO5	MDO4	MDO3	MDO2	MDO1	MDO0

MDO[15:0] Memory Data Output. Writes to this register are ignored if IDMA write access is not enabled. See the RWS bit in register IDMAC.

When writing program memory: the upper 16 bits of the 24-bit program memory word are written by a first write to this register. The lowest eight bits of the program memory word are written via bits 7:0 of this register by the next write to this register. During the second write, bits 15:8 are ignored.

Test Modes **Mnemonic: TM** **Access: Write Only** **Address Offset: 0x6**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0

TM[15:0] TBD Test Mode Control Bits.

Default state after system reset: 0000 0000 0000 0000 (0x0000).

DSP I/O Memory Map

The AD1801 uses the DSP's $\overline{\text{IOMS}}$ control and a 10-bit address A(9:0) to qualify DSP accesses to the internal CIS RAM, registers and I/O port pins addressed according to the table below. The host PC will not access the CIS RAM until it detects the deactivation of the $\overline{\text{IREQ}}$ bus signal after a system reset. The DSP has control over the deactivation of this pin after a reset has occurred via the RDY bit in the DSP Control register. Under normal operations, the DSP will initialize the CIS RAM, then set the RDY bit; it will not access the CIS memory again until after the next reset. An additional qualifying control, the DC register OVRIDE bit, is used to determine whether the DSP can access the PnP function registers listed in the table or not. (The DSP must set this bit to a logical "1" to temporarily take the PnP function "off-line" from the host PC in order to initialize or configure the PnP function itself. The DSP clears this bit to return the PnP function back "on-line" for host PC use.)

Note: I/O memory space must be set for at least one wait state for proper AD1801 functionality.

Table X. DSP I/O Memory Map

DSP Address Bits A[13:0]	Resource Accessed		
	Reads	Writes	Function
0x000–0x1FF	reserved	CIS RAM	PCMCIA or PnP Attribute Configuration
0x200	DC	DC	DSP Control
0x201	reserved	IPC	I/O Port Control
0x202	IP	OP	I/O Port Data
0x203	reserved	BA	Base Address
0x204	reserved	IS	Interrupt Select
0x205	CC	CC	Codec Configuration
0x206	MSR	MSR	Modem Sample Rate
0x207	HSR	HSR	Handset Sample Rate
0x208	ML	ML	Modem Levels
0x209	HL	HL	Handset Levels
0x20A	reserved	MSD	Monitor Speaker Data

Program Memory Organization

Program Memory Organization is controlled by the value of the PMOVLAY register. For the AD1801, valid settings of this register are 0 and 4. When set to 0, all 16K of internal program memory RAM may be addressed. When set to 4, the upper 8K is swapped out and replaced with the 4080 word ROM. After a DSP reset, PMOVLAY defaults to 4 and code execution commences at the first ROM address, which is 0x2000.

Table XI. Program Memory Organization

PMOVLAY = 4 (Default after DSP Reset)	
Address	**Program Memory**
0x0000–0x1FFF	Lower 8K of Internal RAM
0x2000–0x2FEF	4080 Words of Internal ROM
0x2FF0–0x2FFF	16 Words Reserved for Analog Devices
0x3000–0x3FFF	Reserved (Invalid Addresses)
PMOVLAY = 0	
Address	**Program Memory**
0x0000–0x1FFF	Lower 8K of Internal RAM
0x2000–0x3FFF	Upper 8K of Internal RAM

CIS RAM **Access: Write Only** **Address 0x000 to 0x1FF**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
ignored	ignored	ignored	ignored	ignored	ignored	ignored	ignored

DATA[7:0] Only one byte of data may be written to the CIS RAM per cycle, and it must be MSB justified on the 16-bit DSP data bus. Each CIS RAM address points to a single byte.

If in PnP Mode: The PnP Identifier must be written into the first nine bytes of the CIS RAM, i.e., addresses 0x000 to 0x008. Immediately after the PnP Identifier, the PnP Resource Data must be loaded. Resource Data may use any number of the remaining 503 CIS RAM bytes. The first PnP Identifier byte must be written into the CIS RAM within 1 ms after system reset ($\overline{\text{RESET}}$ pin) is deasserted. The remaining eight PnP Identifier bytes must be loaded at a rate of one every 2 ms or faster. Resource Data may be written into the CIS RAM at any rate. All bytes, whether PnP Identifier or Resource Data, must be written into CIS RAM consecutively, and in a single pass.

If In PCMCIA Mode: Writes of tuples may be at any rate and in any order. Once the CIS RAM is configured, the RDY bit in register DC must be set to "1" to indicate CIS RAM load completion. After setting the RDY bit to "1," further writes to CIS RAM must not occur.

DSP Control **Mnemonic: DC** **Access: Read/Write** **Address: 0x200**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
DSPIX	RNGIX	PCIRQ	res	BYPAS	RDY	FP1DBW	FP2DBW
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
PMODE	PSPORT	SPCHAN	IO01A	SBWAIT	PDRM	PDRN	PD

DSPIX Alternate DSP access for PC I/O mapped register bits. Reading this bit returns the state of the DSPI bit in the PC I/O memory mapped register PCS. Writing this bit is identical to writing the DSPIA bit in the PC I/O memory mapped register PCC.

RNGIX Alternate DSP access for PC I/O mapped register bits. Reading this bit returns the state of the RNGI bit in the PC I/O memory mapped register PCS. Writing this bit is identical to writing the RNGIA bit in the PC I/O memory mapped register PCC.

PCIRQ PC Interrupt Request. If in ISA or PCMCIA mode, writing a "1" to this bit sets the DSPI (host PC interrupt request from DSP) bit in the PC mapped I/O register PCS. In ISA mode, an interrupt to the host PC is asserted if DSPI is set to "1," provided DSP interrupts to the host are enabled (see bit DSPIE in PC I/O mapped register PCC). In PCMCIA mode, DSPI itself does not cause a host interrupt, but can be monitored to distinguish between DSP and RING Pin interrupts to the host PC. When in PCMCIA mode, writing a "1" to PCIRQ sets CSR0 Bit 0 to a "1," in addition to setting DSPI. If CSR0 Bit 0 is set to "1," an interrupt to the host PC is asserted, provided DSP interrupts to the host are enabled (see COR0 bit 2) and the function is enabled (see COR0).

BYPAS PnP Bypass. Used in ISA mode only and ignored in PCMCIA mode. When this bit is set to "0," the PNP_$\overline{\text{STD}}$ pin determines whether the AD1801 is in PnP or non-PnP mode. When set to "1," the PNP_$\overline{\text{STD}}$ pin is ignored, and the AD1801 is always in non-PnP mode. When in non-PnP mode, the BA and IRQ registers must be written to select base address and IRQ.
0 = PNP_$\overline{\text{STD}}$ Pin Selects Mode
1 = PNP_$\overline{\text{STD}}$ Pin Ignored, Non-PnP Mode Forced

RDY CIS Memory Initialized Indicator. Used in PCMCIA mode only and ignored in ISA mode. This bit should be changed from its reset default of "0" to "1" by the DSP once the DSP has completely initialized the CIS RAM. When set to "1," the $\overline{\text{IREQ}}$ pin, which serves as the PCMCIA READY pin at startup, is released from its reset default of LO and driven HI. This indicates to the PCMCIA host bus adapter that the AD1801 has completed self-initialization and is ready to be accessed.

FP1DBW PCMCIA Function Port 1 Data Bus Width Identifier. Used in PCMCIA mode only and ignored in ISA mode. This bit must be written by the DSP before the AD1801 indicates it is ready to proceed with configuration at startup, i.e., before or coincident with the RDY bit in this register being written to a "1." It is used to define the behavior of the $\overline{\text{IOCS16}}$ pin when function port 1 is read.
0 = PCMCIA Function Port 1 is 8 bits
1 = PCMCIA Function Port 1 is 16 bits

FP2DBW PCMCIA Function Port 2 Data Bus Width Identifier. Used in PCMCIA mode only and ignored in ISA mode. This bit must be written by the DSP before the AD1801 indicates it is ready to proceed with configuration at startup, i.e., before or coincident with the RDY bit in this register being written to a "1." It is used to define the behavior of the $\overline{\text{IOCS16}}$ pin when function port 2 is read.
0 = PCMCIA Function Port 2 is 8 bits
1 = PCMCIA Function Port 2 is 16 bits

PMODE — Port Mode Select. Selects which feature is supported by Pins 53 to 56, either the secondary PCMCIA function port or a DSP serial port. When the DSP serial port is selected, data I/O to either the modem or the handset codec channels is sacrificed since both serial ports are nominally used within the AD1801 for codec communication. See the PSPORT and SPCHAN bits for further details on which codec channels are lost.
0 = PCMCIA Function Port 2 Activated (default)
1 = DSP Serial Port Activated (Modem or Handset DSP Data I/O is Sacrificed)

PSPORT — Port Serial Port Select. When PMODE is reset to "0," this bit is ignored. When PMODE is set to "1," this bit selects which of the two DSP serial ports is connected to Pins 53 to 56. Note that this bit, together with the SPCHAN bit, determine whether the modem or the handset codec channels are sacrificed when a DSP serial port is assigned to Pins 53 to 56.
0 = DSP Port 0 Assigned to Pins 53 to 56 when PMODE = 1 (default)
1 = DSP Port 1 Assigned to Pins 53 to 56 when PMODE = 1

SPCHAN — DSP Serial Port Channel Assignment. This bit selects which codec channel uses which DSP serial port for data communication.
0 = Modem ADC and DAC Data Sent on SPORT 0, Handset ADC and DAC Data Sent on SPORT 1 (default)
1 = Modem ADC and DAC Data Sent on SPORT 1, Handset ADC and DAC Data Sent on SPORT 0

IO0IA — IO0 Pin Interrupt Acknowledge. Writing a "1" to this bit acknowledges and deasserts the DSP's IRQL1 level interrupt. This interrupt is asserted any time the logical input level on the IO0 pin changes state, either from HI to LO or LO to HI.

SBWAIT — System Bus Wait. This bit is used by the DSP when servicing a power-down interrupt to support entering and exiting AD1801 power-down mode. Once this bit is set to "1," any future PC read/write cycles to the AD1801 will be extended through the assertion of the IOCHRDY/$\overline{\text{WAIT}}$ pin. When reset to "0," IOCHRDY/$\overline{\text{WAIT}}$ will be deasserted (if asserted) to allow completion of an extended bus cycle. Resetting this bit to "0" is also the mechanism of clearing a power-down interrupt initiated by the PC (see PD bit in the PC I/O mapped register PCC), so this bit should be reset to "0" before exiting a power-down interrupt service routine, even if it was not set to "1." See the Power-Down section of this document for important additional details.

PDRM — Power-Down Request from PCMCIA. This bit reflects the state of the PWRDN bit in the PCMCIA register CSR0. While set to "1," level interrupt IRQL0 is asserted to the DSP. This bit may be used by the DSP to determine the source of the IRQL0 interrupt, as the PDRN bit below also asserts IRQL0. Writing to this bit has no effect. See the Power-Down section of this document for important additional details.

PDRN — Power-Down Request from $\overline{\text{PDN}}$ pin. This bit reflects the state of the $\overline{\text{PWD}}$ pin. While the $\overline{\text{PWD}}$ pin is held LO, level interrupt IRQL0 is asserted to the DSP. This bit may be used by the DSP to determine the source of the IRQL0 interrupt, as the PDRM bit above also asserts IRQL0. Writing to this bit has no effect. See the Power-Down section of this document for important additional details.

PD — AD1801 Power-Down. Writing a "1" to this bit initiates the process of powering down the AD1801. Writing a "0" to this bit has no effect. When read as a "1," this bit indicates that there is no active nonextended system bus access to the AD1801. See the Power-Down section of this document for further clarification and important additional details.

Default state after reset: 0000 0000 0000 0000 (0x0000).

I/O Port Control **Mnemonic: IPC** **Access: Read/Write** **Address 0x201**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
res	res	res	res	res	SCKIE	SENIE	SDIE
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0

SDIE — Serial Memory Port Data Direction. Determines directionality of the SDATA pin.
0 = SDATA is an Output Pin with Logic Level Set by SDO Bit (see OP register).
1 = SDATA is an Input Pin (default).

SENIE — Serial Data Enable Control Direction. Determines directionality of the SEN pin.
0 = SEN is an Output Pin with Logic Level Set by SEN Bit (see OP register) (default).
1 = SEN is an Input Pin.

SCKIE — Serial Data Clock Direction. Determines directionality of the SCK pin.
0 = SCK is an Output Pin with Logic Level Set by SCK Bit (see OP register) (default).
1 = SCK is an Input Pin.

IPC[7:0] — I/O Port Control. Defines directionality of associated I/O port Pins IO7 through IO0.
0 = Output
1 = Input (default)

Default state after system reset: 0000 0001 1111 1111 (0x01FF).

Input Port/Status **Mnemonic: IP** **Access: Read Only** **Address 0x202**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
DRST1	DRST0	RING	PNP_STDZ	PCM_ISAZ	SCK	SEN	SDI
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0

DRST[1:0] DSP Reset Indicator. These bits identify the source of the most recent DSP reset.
00 = Last DSP Reset was Hard and from $\overline{\text{RESET}}$ Pin (Power-Up Reset)
01 = Last DSP Reset was Hard and from RESET Pin (ISA Reset)
10 = Last DSP Reset was Soft and from PnP or PCMCIA
11 = Last DSP Reset was Soft and from RST Bit in PC I/O Memory Mapped Register PCC

RING RING Pin Status. Reflects the logic level on the RING pin.

PNP_STDZ ISA Mode Configuration Status. Reflects the logic level on the PNP_$\overline{\text{STD}}$ pin.
0 = Standard Mode (PnP Disabled: Base Address Set by BA Register, IRQ Set by IS Register)
1 = PnP Mode

When the AD1801 is configured in PCMCIA mode (i.e., when the PCM_$\overline{\text{ISA}}$ pin is HI), then the PNP_$\overline{\text{STD}}$ pin can be used as a general purpose input. The PNP_STDZ register bit can be used to monitor the state of this general purpose input under those conditions.

PCM_ISAZ AD1801 Operating Mode Status. Reflects the logic level on the PCM_$\overline{\text{ISA}}$ pin.
0 = ISA Mode
1 = PCMCIA Mode

SCK Serial Data Clock Status. Reflects the logic level on the SCK pin.

SEN Serial Data Enable Control Status. Reflects the logic level on the SEN pin.

SDI Serial Data In Pin Status. Reflects the logic level on the SDATA pin.

IP[7:0] I/O Port Input State. Reflects the logic levels on associated I/O port pins IO7 through IO0. I/O port pins not connected externally are evaluated as logic "1" due to internal pull-up resistors. Will drive a weak HI level externally.

Default state after system reset: 0000 X0XX XXXX XXXX (0x0XXX).

Output Port **Mnemonic: OP** **Access: Write Only** **Address 0x202**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
res	res	res	res	res	SCK	SEN	SDO
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0

SCK Serial Memory Port Clock Output. The state of this bit is reflected on the SCK pin.

SEN Serial Memory Port Chip Enable Output. The state of this bit is reflected on the SEN pin.

SDO Serial Memory Port Data Output. The state of this bit is reflected on the SDATA pin provided bit SDIE (register IPC) is reset to "0."

OP[7:0] I/O Port Output State. Defines the logic levels to be driven out on I/O port pins IO7 through IO0 provided the associated I/O port control bit in the IPC register is reset to "0."

Default state after system reset: 0000 0000 1111 1111 (0x00FF).

Default Base Address **Mnemonic: BA** **Access: Write Only** **Address 0x203**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
BA12	BA11	BA10	BA9	BA8	BA7	BA6	BA5
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
BA4	BA3	BA2	BA1	BA0	res	res	res

BA[12:0] Default Base Address. These bits are used to qualify host PC I/O access to the AD1801 if either in non-PnP ISA mode (PCM_$\overline{ISA}$ pin tied LO and PNP_$\overline{STD}$ pin tied LO), or if the BYPAS bit in the DSP Control (DC) register is set to "1."

NOTE: This register always qualifies host PC I/O access, but the DSP must initialize it when the AD1801 is configured in non-PnP ISA mode, since PnP/PCMCIA hardware/software does not. Note that independent of mode, the DSP can always write the Base Address register, but under the obvious risk of interfering with PnP ISA or PCMCIA transactions.

Default state after system reset: 0000 0000 0000 0000 (0x0000).

Default Interrupt Select **Mnemonic: IS** **Access: Write Only** **Address 0x204**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
INTP2	INTP1	SMODE	res	res	res	res	res
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
res	res	res	res	IS3	IS2	IS1	IS0

INTP2 Interrupt Edge Polarity for PCMCIA Function 2. This bit is ignored unless in PCMCIA mode. It defines the edge necessary on the INT2 pin to cause a Function 2 interrupt.
0 = Falling Edge Interrupt (default).
1 = Rising Edge Interrupt.

INTP1 Interrupt Edge Polarity for PCMCIA Function 1. This bit is ignored unless in PCMCIA mode. It defines the edge necessary on the INT1 pin to cause a Function 1 interrupt.
0 = Falling Edge Interrupt (default).
1 = Rising Edge Interrupt.

SMODE Strobe Mode. This bit selects the functionality of Pins 82 and 94 when the AD1801 is in PCMCIA mode.
0 = Pins 82 and 94 function as VCTL2 and VCTL1, respectively (default)
1 = Pins 82 and 94 function as $\overline{EXTWR}$ and $\overline{EXTRD}$, respectively.

IS[3:0] Default Interrupt Request. These bits are ignored unless in ISA mode (PCM_$\overline{ISA}$ pin tied LO). When in ISA mode, these bits select the AD1801 IRQ if either in non-PnP mode (PNP_$\overline{STD}$ pin tied LO), or if the DC register BYPAS bit is set to "1." Valid settings for IS[3:0] are: 3, 4, 5, 7, 9, 10, 11, 12 and 15. Other settings are ignored and result in no IRQ selection.

NOTE: This register always selects the AD1801 IRQ when in ISA mode, but the DSP must initialize it when the AD1801 is configured in non-PnP ISA mode, since PnP/PCMCIA hardware/software does not. Note that independent of mode, the DSP can always write to the Interrupt Select register, but under the obvious risk of interfering with PnP ISA transactions.

Default state after system reset: 0000 0000 0000 0000 (0x0000).

Codec Configuration **Mnemonic: CC** **Access: Read/Write** **Address 0x205**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
res	MDFS	MLCT	MSM1	MSM0	MSSR	MSSD0	MSSDR2
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
MSSDR1	MSSDR0	MSAEN	MEN	HEN	MSEN	SBEN	CEN

MDFS Modem Digital Filter Select. This bit is used to select which of two digital filters is applied to the modem ADC and DAC channels. The first choice has been optimized for filter performance, while the second choice has been optimized for a reduced linear group delay.

	Passband			Stopband		
MDFS	**Ripple[1]**	**Edge**	**-3 dB Point**	**Ripple[2]**	**Edge**	**Linear Group Delay**
0	–017 dB	0.445 × MSR	0.490 × MSR	<–78.0 dB	0.555 × MSR	<19/MSR
1	–0.24 dB	0.400 × MSR	0.453 × MSR	<–52.8 dB	0.555 × MSR	<10/MSR

MSR is the modem sample rate set by MSR[15:0] in the MSR register.

NOTES
[1]Passband ripple listed above does not include the following fixed (sample rate independent) roll-off which appears on the ADC channels. DAC channels do not have this roll-off. Consult the filter plots at the end of this document for further details.
[2]Stopband ripple listed does not include two filter peaks near 3.5 × MSR and 4.5 × MSR. When using modem filter 0 (MDFS = 0), the tallest of these two peaks is –55.2 dB. When using modem filter 1 (MDFS = 1), the tallest of these two peaks is –58.6 dB. While these peaks will be further attenuated by the analog continuous-time filters within the AD1801, the corner frequency of this analog filter is too high to have a substantial effect when low sample rates are used. Consult the filter plots at the end of this document for further details.

Frequency Range	Roll-Off
0 kHz to 4 kHz	<0.0016 dB
4 kHz to 9 kHz	<0.01 dB
9 kHz to 16 kHz	<0.05 dB
16 kHz to 20 kHz	<0.10

MLCT — Modem DAC Level Change Timing. This bit controls when changes to the modem DAC level (see MDAM and MDAL[4:0] bits in the ML register) take effect. When reset to "0," changes take effect immediately. When set to "1," changes are delayed until either the output level crosses zero (midscale), or until a 10 ms to 12 ms timeout period is reached. Delaying level changes until zero crossings reduces instantaneous output voltage changes, that reduces audible "clicks."
0 = Level Changes Applied Immediately (default)
1 = Level Changes Applied on Signal Zero (Midscale) Crossing or After 10 ms–12 ms Timeout

MSM[1:0] — Modem Sample Rate Modifier. These bits are used to select the LSB weighting of the MSR[15:0] (Modem Sample Rate) bits in the MSR register.
00 = MSR[15:0] LSB Weight is 1 Hertz (default)
01 = MSR[15:0] LSB Weight is 8/7 Hertz
10 = MSR[15:0] LSB Weight is 10/7 Hertz
11 = Reserved

MSSR — Monitor Speaker Sample Rate Select.
0 = Monitor Speaker Sample Rate Locked to Modem Sample Rate (See MSR Register)
1 = Monitor Speaker Sample Rate Locked to Handset Sample Rate (See HSR Register)

MSSDO — Monitor Speaker Sigma-Delta Order and Bitstream Density Select. Available in PCMCIA mode or in ISA mode. Setting this bit to a "1" will double the nominal output volume from a speaker connected to the $\overline{\text{SPKR}}$ pin or the MSPKR pin, but will also significantly increase output noise. The state of the MSSDO bit should only be changed when the monitor speaker is powered down (i.e., MSEN = 0).
0 = Third Order Modulator with 75%/25% Bitstream Positive/Negative Full-Scale Mapping
1 = First Order Modulator with 100%/0% Bitstream Positive/Negative Full-Scale Mapping

MSSDR[2:0] — Monitor Speaker Sigma-Delta Bitstream Rate Select. Used in PCMCIA mode only and ignored in ISA mode. These bits may be used to decrease the nominal output bitstream rate sent to the $\overline{\text{SPKR}}$ pin. A decreased bitstream rate will allow more time for a piezoelectric speaker to properly discharge before being redriven, but will also decrease the oversampling rate, resulting in more output noise. The state of the MSSDR[2:0] bits should only be changed when the monitor speaker is powered down (i.e., MSEN = 0).
0xx = 1411.2 kHz Bitstream Rate (default)
100 = 705.6 kHz Bitstream Rate
101 = 352.8 kHz Bitstream Rate
110 = 176.4 kHz Bitstream Rate
111 = 88.2 kHz Bitstream Rate

MSAEN — Monitor Speaker Analog Output Enable. Used in PCMCIA mode only and ignored in ISA mode.
0 = Analog Monitor Speaker Output (pin MSPKR) Always Powered Down
1 = Analog Monitor Speaker Output (pin MSPKR) Powered Up when MSEN is Set to "1"

MEN — Modem Enable. Up to 100 µs are required to enable (power-up) the modem codec channels once the codec is enabled (see Bit CEN). Approximately 30 µs are required to power down these channels if MLCT (Modem DAC Level Change Timing) is reset to "0." Both power-up and power-down are internally sequenced to minimize instantaneous output voltage changes; however, the power-down sequence for this channel may be quieter if MLCT is set to "1."
0 = Modem ADC and DAC Power-Down (default)
1 = Modem ADC and DAC Enabled Provided CEN (Codec Enable Bit) is Set to "1"

HEN — Handset Enable. Up to 100 µs are required to enable (power-up) the handset codec channels once the codec is enabled (see Bit CEN). Approximately 30 µs are required to power down these channels. Both power-up and power-
down are internally sequenced to minimize instantaneous output voltage changes (i.e., pops and clicks).
0 = Handset ADC and DAC Powered-Down (default)
1 = Handset ADC and DAC Enabled Provided CEN (Codec Enable Bit) is Set to "1"

MSEN — Monitor Speaker Enable. Up to 100 µs are required to enable (power up) the monitor speaker DAC channel once the DAC is enabled (see Bit CEN). Approximately 30 µs are required to power down this channel. Both power-up and power-down are internally sequenced to minimize instantaneous output voltage changes (i.e., pops and clicks).
0 = Monitor Speaker DAC Powered Down (default)
1 = Monitor Speaker DAC Enabled Provided CEN (Codec Enable Bit) = "1"

SBEN Codec Standby Enable. If either this bit or the CEN (Codec Enable) bit is set to "1," the process of powering up the AD1801's codec voltage reference is initiated. If both this bit and the CEN bit are reset to "0," the process of powering down the AD1801's codec voltage reference is initiated. Approximately 700 ms are required to power up the codec voltage reference while only 30 ns are required to power it down. This bit may be used to keep the codec voltage reference powered up when the rest of the codec is powered down, which results in a much quicker power-up sequence. See the CEN bit for further details.
0 = Codec Powered Down (Provided CEN = 0) (default)
1 = Codec in Standby (Provided CEN = 0)

CEN Codec Enable. When a "1" is written to this bit, the process of powering up the AD1801 codecs is initiated. When a "0" is written to this bit, the process of powering down the AD1801 codecs is initiated. When read as a "0," the codecs are either powered down or in the process of powering up. When read as a "1," the codecs are either powered up or in the process of powering down. Therefore, completion of the process of powering up or down can be detected by writing the appropriate value to this bit and reading this bit until the written value is echoed. Power-up normally requires no more than 700 ms, but up to 840 ms will be required the first time the codecs are powered up after an AD1801 reset, since this is when the codecs perform an autocalibration. Note that if the codecs are first put in standby using the SBEN bit (and given 700 ms time to complete the transition into standby), only 30 ns will be required after setting the CEN bit to "1" to complete the power-up process. Powering down the codecs never requires more than 150 ns. See Table XII for a complete summary.

Default state after system reset: 0000 0000 0000 0000 (0x0000).

Modem Sample Rate **Mnemonic: MSR** **Access: Read/Write** **Address: 0x206**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
MSR15	MSR14	MSR13	MSR12	MSR11	MSR10	MSR9	MSR8
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
MSR7	MSR6	MSR5	MSR4	MSR3	MSR2	MSR1	MSR0

MSR[15:0] Modem Sample Rate. Together with MSM[15:0] (Modem Sample Rate Modifier) in the CC register, these bits define the conversion rate for the modem ADC and DAC channels. If the MSSR bit (Monitor Speaker Sample Rate Select) in register CC is reset to "0" (default), these bits also define the conversion rate for the monitor speaker DAC. With a 16.9344 MHz clock input on the XTALI pin, one LSB represents: exactly 1 Hertz when MSM[1:0] = 00; exactly 8/7 Hertz when MSM[1:0] = 01; and exactly 10/7 Hertz when MSM[1:0] = 10. Permitted settings of MSR[15:0] range from: 5400 to 48000 when MSM[1:0] = 00; 4725 to 42000 when MSM[1:0] = 01; and 3780 to 33600 when MSM[1:0] = 10. Resultant sample rate, regardless of MSM[1:0] setting, always ranges from 5400 Hz to 48000 Hz.

Default state after system reset: 0001 1100 0010 0000 (0x1C20) which is 7200 Hz with MSM[1:0] = 00.

Handset Sample Rate **Mnemonic: HSR** **Access: Read/Write** **Address: 0x207**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
HSR15	HSR14	HSR13	HSR12	HSR11	HSR10	HSR9	HSR8
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
HSR7	HSR6	HSR5	HSR4	HSR3	HSR2	HSR1	HSR0

HSR[15:0] Handset Sample Rate. Defines the conversion rate for the Handset ADC and DAC channels. If the MSSR (Monitor Speaker Sample Rate select) bit in register CC is set to "1," these bits also define the conversion rate for the monitor speaker DAC. One LSB represents exactly 1 Hertz, assuming a 16.9344 MHz clock input on the XTALI pin. Usable range is 5400 Hz (0x1518) to 48000 Hz (0xBB80).

Default state after system reset: 0001 1111 0100 0000 (0x1F40) which is 8 kHz.

Modem Levels **Mnemonic: ML** **Access: Read/Write** **Address: 0x208**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
res	res	res	res	res	res	MADL1	MADL0
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
MDAM	MDAL4	MDAL3	MDAL2	MDAL1	MDAL0	SDAL1	SDAL0

MADL[1:0] Modem ADC Gain Level Select. Least significant bit represents +6.0 dB.
00 = 0.0 dB Gain (default)
01 = +6.0 dB Gain
10 = +12.0 dB Gain
11 = Reserved

MDAM Modem DAC Mute.
0 = Enabled
1 = Muted (default)

MDAL[4:0] Modem DAC Attenuation Level Select. Least significant bit represents –1.0 dB.
00000 = 0 dB Attenuation (default)
11111 = –31 dB Attenuation

SDAL[1:0] Monitor Speaker Attenuation Level.
00 = 0.0 dB Attenuation
01 = –6.0 dB Attenuation
10 = –12.0 dB Attenuation
11 = Muted (default)

Default state after system reset: 0000 0000 1000 0011 (0x0083).

Handset Levels **Mnemonic: HL** **Access: Read/Write** **Address: 0x209**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
HADS	HMGE	res	res	HADL3	HADL2	HADL1	HADL0
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
HDASM	HDALM	res	HDAL4	HDAL3	HDAL2	HDAL1	HDAL0

HADS Handset ADC Input Select.
0 = Mic (default)
1 = Line

HMGE Handset Mic Gain Enable.
0 = 0 dB Gain (default)
1 = +20 dB Gain

HADL[3:0] Handset ADC Gain Level Select. Least significant bit represents +1.5 dB.
0000 = 0.0 dB Gain (default)
1111 = +22.5 dB Gain

HDASM Handset DAC Speaker Mute.
0 = Enabled
1 = Muted (default)

HDALM Handset DAC Line Mute.
0 = Enabled
1 = Muted (default). Midscale voltage output on HSPKRP and HSPKRN

HDAL[4:0] Handset DAC Attenuation Level Select. Least significant bit represents –1.5 dB.
00000 = +12.0 dB Gain
01000 = 0.0 dB Attenuation (default)
11111 = –34.5 dB Attenuation

Default state after system reset: 0000 0000 1100 1000 (0x00C8).

Modem Speaker Data **Mnemonic: MSD** **Access: Write** **Address: 0x20A**

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
MSD15	MSD14	MSD13	MSD12	MSD11	MSD10	MSD9	MSD8
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
MSD7	MSD6	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0

MSD[15:0] Monitor Speaker Data. Writes to this register fill a 16 deep FIFO. If this FIFO underruns, the last sample will be repeated to the monitor speaker DAC for up to 16 consecutive underruns; thereafter, midscale sample data is used for all additional underruns. This avoids clicks due to momentary FIFO underruns (easing playback startup) and avoids sustained dc output levels. Data written to this FIFO that would cause FIFO overrun is ignored. No status bits are needed for this FIFO since it is locked to either the modem or handset sample rate (see the MSSR bit in register CC).

POWER CONSUMPTION

The AD1801 power consumption is dependent on many factors, including codec resources used, ADSP-2181 core resources used and instruction mix. Table XII provides some estimates of the maximum current consumption of the AD1801 as a function of device resources used.

Table XII. AD1801 Current Consumption Estimates

Power States	DSP	Codec	System Bus Interface	Estimated Max Current
1MHS*	Active	Up: Mod & Hnd & Spk Enabled	Responsive	252 mA
1MH*	Active	Up: Mod & Hnd Enabled	Responsive	157 mA
1S*	Active	Up: Spk Enabled	Responsive	220 mA
1H*	Active	Up: Hnd Enabled	Responsive	142 mA
1M*	Active	Up: Mod Enabled	Responsive	140 mA
1	Active	Up: All Channels Disabled	Responsive	125 mA
2C	Active	Standby	Responsive	94 mA
2	Active	Down	Responsive	92 mA
R	NOP	Down	Nonresponsive	40 mA
3C	Idle	Standby	Responsive	19 mA
3	Idle	Down	Responsive	17 mA
4C	Standby	Standby	Slow Responsive	≈5 mA
4	Standby	Down	Slow Responsive	≈3 mA
5C	Down	Standby	Nonresponsive	2.5 mA
5	Down	Down	Nonresponsive	0.5 mA

*When in Power State 1, any combination of the Modem (Mod), Handset (Hnd), and Speaker (Spk) channels may be enabled through the use of independent channel enable bits (see the DSP I/O mapped CC register). Only the combinations thought most likely to be used have been listed.

Current numbers assume:

1. 50% of instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle.
2. Device is operating with no ISA/PCMCIA pin loads.

WARNING: For proper operation of the AD1801, DSP code must never:

1. Use the IDLE(n) instruction (critical internal clocks will be slowed).
2. Write the PDFORCE (power-down interrupt force) bit in the SPORT1 Autobuffer Control Register to "1" (this would power down the AD1801 with no means of powering back up other than a pin reset).

Power-Down States

Power State R

DSP: Running NOP
Codec: Powered Down
Interface: Nonresponsive
Crystal: Enabled

The AD1801 is forced into this Power State any time one or both of the reset pins (RESET and $\overline{\text{RESET}}$) is asserted. The AD1801 will remain in this Power State until both of the reset pins are deasserted. Immediately after both reset pins are deasserted, the AD1801 will enter Power State 2 and commence instruction execution at location 0x2000 ROM.

When power is first applied, the AD1801 must be kept in this Power State (by the continuous assertion of at least one of the reset pins) until the clock input on the XTALI pin stabilizes, plus another 1000 XTALI cycles to allow the AD1801's phase locked loop to lock. With a crystal connected between the XTALI and XTALO pins, the time required for the clock input to stabilize is dependent upon the type of crystal used and the capacitance of the external crystal circuit; typically 2000 XTALI cycles is adequate.

If the AD1801 was in Power State 5 prior to the assertion of a pin reset, the procedure listed above for initial power-up must be followed since the clocks were stopped while in Power State 5.

If the AD1801 was in Power State 1, 2, 3 or 4 prior to the assertion of a reset pin, the AD1801 must be kept in this Power State (by the continuous assertion of at least one of the reset pins) for at least five XTALI cycles. Note that asserting a reset while in Power State 1 is not recommended due to the "noisy" abrupt shutdown of the codec.

Power State 2

DSP: Active
Codec: Powered Down or in Standby
Interface: Responsive
Crystal: Enabled

If the codec is in standby (see the SBEN bit in DSP I/O mapped register CC), its voltage reference circuitry is not powered down which results in greater power consumption; however, the time required to transition from Power State 2 to Power State 1 is decreased from approximately 500 ms to approximately 15 ms.

If the CEN (Codec Enable) bit is set to "1" (see DSP I/O mapped register CC), the process of entering Power State 1 will be initiated. The DSP may poll the codec (by reading the CEN bit and waiting for an echo of "1") to determine when Power State 1 is actually entered.

Power State 3 will be entered if an IDLE instruction is executed by the DSP, provided the DSP is not currently servicing a power-down interrupt. Note that the IDLE(n) DSP instruction must not be used since the internal clock slow down caused by this instruction will interfere with the AD1801 bus interface logic.

Power State 1 (Any Form)

DSP: Active
Codec: Powered up. Any combination of Modem, Handset and Speaker Codec Channels Enabled.
Interface: Responsive
Crystal: Enabled

Although the codec is powered up in this Power State, the amount of power actually consumed is still dependent on the number of codec channels actually enabled. The modem (ADC and DAC), handset (ADC and DAC) and speaker (DAC) channels can be independently enabled and disabled using the MEN, HEN and MSEN bits in DSP I/O mapped register CC.

Before enabling either the modem of handset codec channels, the DSP serial port used to communicate with the codec channels must first be properly configured in the DSP. If serial port 0 is used, the "SPORT 0 Control" register at 0x3FF6 must be set to 0x3C0F. If serial port 1 is used, the "SPORT 1 Control" register at 0x3FF2 must be set to 0x3C0F. Also, the used serial ports must be enabled by setting the appropriate bits in the

"System Control" register at 0x3FFF. Finally, note that the PMODE, PSPORT and SPCHAN bits in the DSP I/O mapped register DC, which specify DSP serial port usage, must also be defined before enabling related codec channels.

If the CEN (Codec Enable) bit is reset to "0" (see DSP I/O mapped register CC), the process of entering Power State 2 will be initiated. The DSP may poll the codec (by reading the CEN bit and waiting for an echo of "0") to determine when Power State 2 is actually entered.

Power State 3

DSP:	Idle
Codec:	Powered Down or in Standby
Interface:	Responsive
Crystal:	Enabled

Power State 3 will be entered if an IDLE instruction is executed by the DSP, provided the DSP is not currently servicing a power-down interrupt. Note that the IDLE(n) DSP instruction must not be used since the internal clock slow down caused by this instruction will interfere with the AD1801 bus interface logic.

In this Power State, the DSP is idle and the codec is powered down.

When an unmasked interrupt occurs, the AD1801 will return to Power State 2 immediately and service the interrupt.

Power State 4

DSP:	Powered Down
Codec:	Powered Down or in Standby
Interface:	Slow responsive
Crystal:	Enabled

Entering and exiting this Power State requires DSP code support. This code is outlined below. While in this Power State, the AD1801 will not be immediately responsive to system bus accesses, but will extend bus cycles through the assertion of the IOCHRDY/$\overline{\text{WAIT}}$ pin until able to respond. Any system bus access to the AD1801, read or write, will wake the AD1801 from this Power State and return it to Power State 2 where the AD1801 can respond to bus cycles. The system bus will be stalled for no more than 7 µs, which is acceptable for both ISA and PCMCIA buses. The ISA bus specifies a maximum stall of 15.6 µs, and the PCMCIA bus specifies a maximum stall of 12 µs.

Entering Power State 4:

1. The transition to Power State 4 is initiated by the assertion of a nonmaskable power-down interrupt. The source of this power-down interrupt may be: 1) the PC writing to the PD bit in the PC I/O memory mapped register PCC; 2) the DSP writing the PD bit in DSP I/O memory mapped register DC. This interrupt will cause the DSP to vector to address 0x002C. The transition to this Power State may be indirectly initiated by asserting the PWD (power-down pin) or the PCMCIA power-down bit (bit PWRDN of register CSR0). Either of these actions will cause an IRQL0 interrupt to the DSP, causing it to vector to address 0x000C. In this interrupt handler, the DSP may in turn write the PD bit. Note that the DSP has access to two flag bits (PDRN and PDRM in DSP I/O mapped register DC) that indicate the source of an IRQL0 interrupt.
2. Beginning at 0x002C, any number of housekeeping instructions can be executed prior to the DSP entering actual power-down. These instructions must ensure that the codec is powered down before continuing with this procedure. See the CEN (Codec Enable) bit located in the DSP I/O mapped register CC (Codec Configuration) for detailed information on how to power-down the codec and check its power-up/-down status. These instructions must also program the "SPORT1 Autobuffer/Power-Down Control Register" memory mapped at location 0x3FEF to 0x0XXX unless these settings are made in advance. This sets:

   XTALDIS = 0, which causes the crystal oscillator to stay enabled during DSP power-down.

   XTALDELAY = 0, which causes the DSP startup delay to be less than 100 cycles.

   PDFORCE = 0, which should never be set to "1" in the AD1801.

   PUCR = 0, which avoids a DSP power-up reset so instruction execution continues in the power-down handler after power-up.
3. The DSP must write a "1" to the SBWAIT (System Bus Wait) bit in DSP I/O mapped register DC. Any bus transactions to the AD1801 started AFTER this point will be extended (through the assertion of the IOCHRDY/$\overline{\text{WAIT}}$ pin) until the DSP wakes up again after being powered down by the steps below. Any currently active bus access to the AD1801 will be completed without bus cycle extension to insure that the AD1801 doesn't assert IOCHRDY/$\overline{\text{WAIT}}$ too close to the end of a bus access.
4. The DSP must poll the PD bit in the DSP I/O mapped DC register until it is read as a "1." In most systems, this will require no more than 1 µs. When read as a "1," this indicates that there is either no active system bus access to the AD1801, or that a bus access to the AD1801 has been stalled through the assertion of the IOCHRDY/$\overline{\text{WAIT}}$ pin. Once read as a "1," it is safe to power down the DSP and stop the AD1801 internal clocks.
5. The DSP powers itself down with the execution of an IDLE instruction. This completes the transition into Power State 4. While the AD1801 is now mostly powered down, it continues decoding bus traffic waiting for any AD1801 access, read or write, which will initiate AD1801 wakeup. Note that accesses to PCMCIA external devices will occur without waking up the AD1801.

   The process of entering Power State 4 may be aborted up until step 4 where SBWAIT is set to "1." Once set to "1," Steps 4 and 5 must also be executed for proper future AD1801 operation. If SBWAIT was not set to "1," Power State 4 can be aborted by first resetting SBWAIT to a "0," that signals an early exit to the AD1801, and then executing an RTI instruction which will exit the power-down handler.

Exiting Power State 4:

6. There are two conditions under which the DSP will be powered up, and Power State 4 exited. The first is the host PC initiating a read or write access to the AD1801. The second is a logic transition (either LO to HI or HI to LO) on any of the following input signals: RING, INT1, and INT2.
7. When the host initiates the read or write access, the AD1801 asserts the IOCHRDY/$\overline{\text{WAIT}}$ pin to extend the bus cycle until it can respond, and begins the process of powering up the DSP. When the wake is caused by a transition on RING, INT1, or INT2, the IOCHRDY/$\overline{\text{WAIT}}$ signal is not asserted. Powering up the DSP requires about 6 µs.
8. When the DSP wakes up, it continues executing code where it left off in the power-down handler. The first instruction should reset the SBWAIT bit to "0" to allow the completion of the extended bus cycle.
9. Any number of housekeeping instructions can now be executed before the power-down interrupt handler is exited by an RTI instruction.

   Power State 4 may also be exited with the assertion of a pin reset, RESET or $\overline{\text{RESET}}$.

Power State 5

DSP:	Powered Down
Codec:	Powered Down or in Standby
Interface:	Nonresponsive
Crystal:	Disabled

WARNING: When in this Power State, bus accesses to the AD1801 are not possible. This Power State must not be used if ISA PnP or PCMCIA configuration register access must be maintained.

Entering and exiting this Power State requires DSP code support. This code is outlined below. While in this Power State, the AD1801 will not be responsive to system bus accesses. Any system bus access to the AD1801, read or write, will, however, wake the AD1801 from this Power State into Power State 2. On the order of 280 µs plus a crystal settle time will be necessary to wake the AD1801. Unlike waking from Power State 4, bus cycles will not be extended when waking from this Power State.

Entering Power State 5:

1. The transition to Power State 5 is initiated by the assertion of a nonmaskable power-down interrupt. The source of this power-down interrupt may be: 1) the PC writing to the PD bit in the PC I/O memory mapped register PCC; 2) the DSP writing the PD bit in DSP I/O memory mapped register DC. This interrupt will cause the DSP to vector to address 0x002C. The transition to this Power State may be indirectly initiated by asserting the PWD (power-down pin) or the PCMCIA power-down bit (bit PWRDN of register CSR0). Either of these actions will cause an IRQL0 interrupt to the DSP, causing it to vector to address 0x000C. In this interrupt handler, the DSP may in turn write the PD bit. Note that the DSP has access to two flag bits (PDRN and PDRM in DSP I/O mapped register DC), which indicate the source of an IRQL0 interrupt.
2. Beginning at 0x002C, any number of housekeeping instructions can be executed prior to the DSP entering actual power-down. These instructions must insure that the codec is powered down before continuing with this procedure. See the CEN (Codec Enable) bit located in the DSP I/O mapped register CC (Codec Configuration) for detailed information on how to power down the codec and check its power up/down status. These instructions must also program the "SPORT1 Autobuffer/Power-Down Control Register" memory mapped at location 0x3FEF to 0x0XXX unless these settings are made in advance. This sets:

   XTALDIS = 1, which causes the crystal oscillator to power down during DSP power-down.

   XTALDELAY = 1, which causes the DSP startup delay to be 4096 clock cycles.

   PDFORCE = 0, which should never be set to "1" in AD1801.

   PUCR = 0, which avoids a DSP power up reset so instruction execution continues in the power-down handler after power-up.
3. The DSP powers itself down with the execution of an IDLE instruction. This completes the transition into Power State 5. While the AD1801 is now mostly powered down, it continues decoding bus traffic waiting for any AD1801 access, read or write, that will initiate AD1801 wakeup. Note that accesses to PCMCIA external devices will occur without waking up the AD1801.

   The process of entering Power State 5 may be aborted up until Step 3 where the IDLE instruction is executed. Power State 5 can be aborted by first resetting SBWAIT to a "0," which signals an early exit to the AD1801, and then executing an RTI instruction which will exit the power-down handler.

Exiting Power State 5:

4. There are two conditions under which the DSP will be powered up, and Power State 5 exited. The first is the host PC initiating a dummy read access to the AD1801. This bus access to the AD1801, and all others until the AD1801 is awake, is lost. The second is a logic state transition (either LO to HI or HI to LO) on any of the following input signals: RING, INT1, and INT2.
5. When the DSP wakes up, it continues executing code where it left off in the power-down handler. The first instruction should reset the SBWAIT bit to "0" to clear the power-down logic.
6. Any number of housekeeping instructions can now be executed before the power-down interrupt handler is exited by an RTI instruction. It may be desirable to send an interrupt to the host PC to signal AD1801 wakeup.

   Power State 5 may also be exited with the assertion of a pin reset, RESET or $\overline{\text{RESET}}$.

Table XIII. Power State Transitions

Initial State	Final State	Transition Trigger (Bits in CC Register)	Time Required for Transition	Indicator to DSP of Transition Completion
2	1[M, H, S]	CEN Set to 1, [MEN, HEN, MSEN] Set to 1	< 700 ms*	CEN Read Back as 1
1[M, H, S]	2	CEN Reset to 0, SBEN Set to 1	< 100 µs*	CEN Read Back as 0
2C	1[M, H, S]	CEN Set to 1, [MEN, HEN, MSEN] Set to 1	< 100 µs*	CEN Read Back as 1
1[M, H, S]	2C	CEN Reset to 0, SBEN Reset to 0	< 100 µs*	CEN Read Back as 0
1	1S	MSEN Set to 1	< 100 µs	None
1S	1	MSEN Reset to 0	< 100 µs	None
1	1H	HEN Set to 1	< 100 µs	DSP SPORT Activity
1H	1	HEN Reset to 0	< 100 µs	SPORT Activity Stops
1	1M	MEN Set to 1	< 100 µs	DSP SPORT Activity
1M	1	MEN Reset to 0	< 100 µs	SPORT Activity Stops
2	1	CEN Set to 1, SBEN Don't Care	< 700 ms*	CEN Read Back as 1
1	2	CEN Reset to 0, SBEN Reset to 0	< 150 ns*	CEN Read Back as 0
2C	1	CEN Set to 1, SBEN Don't Care	< 30 ns*	CEN Read Back as 1
1	2C	CEN Reset to 0, SBEN Set to 1	< 120 ns*	CEN Read Back as 0
2	2C	CEN Reset to 0, SBEN Reset to 0	< 700 ms*	None
2C	2	CEN Reset to 0, SBEN Set to 1	< 30 ns*	None
2[C]**	3[C]**	DSP Executes IDLE Instruction	None	None
3[C]**	2[C]**	DSP Stops Executing IDLE	None	None
2[C]**	4[C]**	See Power State 4 Paragraph	See PS4 Par.	PWDACK Pin HI
4[C]**	2[C]**	See Power State 4 Paragraph	< 7 µs	PWDACK Pin LO
2[C]**	5[C]**	See Power State 5 Paragraph	See PS5 Par.	PWDACK Pin HI
5[C]**	2[C]**	See Power State 5 Paragraph	> 280 µs	PWDACK Pin LO

*Delay will be increased by 140 ms if the AD1801 has not yet autocalibrated itself. Autocalibration is executed the first time the AD1801 transitions to Power State 1 after a hard reset, i.e., a reset initiated by either the RESET pin or $\overline{\text{RESET}}$ pin. If the transition to Power State 1 is aborted before it is completed (by resetting CEN to 0), autocalibration is postponed until the next transition to Power State 1. However, once autocalibration is actually begun, which occurs at the end of the nominal transition to Power State 1, it cannot be interrupted and attempts to abort the transition will be ignored until autocalibration has been completed.

**Power States 3, 4 and 5 can be entered only from Power State 2. Power States 3C, 4C and 5C can be entered only from Power State 2C.

START-UP SEQUENCE

The following paragraphs describe a typical, generic start-up sequence for the purpose of helping hardware, systems and software driver engineers understand some of the considerations involved in bringing up a system that includes the AD1801. Note that it does not exhaustively outline all of the flexible configurations and features available in the AD1801.

1. System power supplies stabilize.
2. Assert the RESET and/or $\overline{\text{RESET}}$ signals.
3. Deassert the RESET and/or $\overline{\text{RESET}}$ signals.
4. Power up the codecs. Write "1" to the CEN (Codec Enable) bit in the Codec Configuration register. This will initiate the process of powering up the AD1801 codecs (DAA codec, handset codec and monitor speaker DAC). Poll this bit until the readback value is "1," which indicates that the codec power-up process is complete.

   The time required to power up the codec from the powered down state (not from cold start) depends on the state of the SBEN (Standby Enable) bit in the Codec Configuration register. Codec power-up will take either 500 ms (SBEN = 0) or 15 ms (SBEN = 1). When SBEN is set to "1," the analog voltage reference is not powered down, so power-up is faster at the expense of higher power consumption in the powered down state.
5. Power up the individual codec channels.
   Write "1" to the MEN (Modem Enable) bit in the Codec Configuration register to power up the modem (DAA) codec channel (ADC and DAC). Power-up of the modem channel takes approximately 10 µs.

   Write "1" to the HEN (Handset Enable) bit in the Codec Configuration register to power-up the handset codec channel (ADC and DAC). Power up of the handset codec channel takes approximately 10 µs.

   Write "1" to the MSEN (Monitor Speaker Enable) bit in the Codec Configuration register to power up the monitor speaker DAC. Power-up of the monitor speaker DAC takes approximately 10 µs.

BOOT-UP SEQUENCE

The AD1801 boot process is a combination of software and hardware operations. Because much of the boot process is driven by software, it can be performed in a number of ways. The following steps provide a rough guideline.

1. Once the power supplies have stabilized, the RESET interrupt vectors the DSP program counter to DSP program memory address 0x2000, which is the first ROM address when PMOVLAY = 4, and is the default after DSP reset. It then starts to execute the instructions which the OEM has programmed into on-chip ROM. These instructions would typically include DSP I/O writes to configure DSP resources (such as the SPORTS) and the IDMA registers (such as the DAGs).

2. The DSP core looks for the presence of an external serial EEPROM. Using software, it looks to see whether the EEPROM data and clock signals are tied together; if so, this identifies an ADI test mode configuration. If the EEPROM data and clock signals are independent, the DSP will typically attempt to read the EEPROM contents as slowly as possible, in order to minimize power.

   In PCMCIA mode, the DSP core reads the entire EEPROM contents into the CIS RAM and/or DSP data memory, unless some of the EEPROM data is program memory patch code. In PCMCIA mode, the DSP must write "1" to the RDY bit in the DSP Control register in order to notify the host that the CIS memory is initialized. In ISA PnP mode, the DSP core reads the first 64 bytes and writes to 0x000 through 0x03F in its I/O space, which is the start of the 512 byte CIS memory. (The first byte, the first PnP Identifier, must be written to the CIS RAM within 1 ms after system reset. The remaining eight PnP Identifiers must be written to the CIS RAM at a rate of one every 2 ms, or faster.) After writing the first 64 bytes of the CIS memory, the DSP core typically computes a checksum or executes some other error detection algorithm. It then resumes reading the remaining contents of the EEPROM into DSP data memory, unless some of the EEPROM data is program memory patch code.

   If some of the EEPROM data is program memory patch code, these instructions are written to the DSP core program memory, typically to address 0x1000. The end of the program memory ROM (from which the DSP is still executing instructions) then jumps to 0x1000 and starts to execute the instructions that were just loaded. The instructions starting at 0x1000 can include writes to various AD1801 specific control bits in the DSP I/O map, including the FP1DBW and FP2DBW bits in the DSP Control register which configure the PCMCIA Function Port data bus widths, as well as the INTP1 and INTP2 bits in the Default Interrupt Select register which configures the PCMCIA Function 1 and 2 interrupt polarities. Actions are taken to put the AD1801 into a state that consumes as little power as possible, including full codec power-down. The code then generally settles into a loop, awaiting action from the host CPU. The DSP may enter an intermittent idle state and the EEPROM will go into sleep mode.

3. By this time, the host system is coming alive. If the AD1801 is being used in an ISA PnP application, the AD1801 will be configured (IRQ channels and ISA base address) by the PnP BIOS routines. If the AD1801 is being used in a PCMCIA application, it will be configured (IRQ channels and ISA base address) by the PCMCIA Card and Socket Services driver. Either the PnP BIOS or the PCMCIA Card and Socket Services also writes to the AD1801 logical device bit to enable the AD1801.

4. The AD1801 host driver software then writes to the AD1801 PC I/O mapped registers to set up the DSP core IDMA controller to download the modem data pump software to the DSP core program memory. The host writes RWS = 1 (in the Internal DMA Control register) to enable write access. It also writes TYPE = 0 (in the Internal DMA Control register) to select program memory accesses. It then programs the start address in DSP core program memory for the download (the code to be downloaded must have been linked to this absolute address) by writing this address to the MA[13:0] bit field in the Internal DMA Control register. The host then writes the actual data (ADSP-2181 instructions) to the Memory Data Output register. For program memory downloads, two 16-bit writes are required for each 24-bit program memory word. Note that the IDMA controller auto-
   increments the DSP program memory address following each 24-bit transfer during program memory downloads.

5. The DSP core is still awaiting action from the host CPU. There are two ways the host can notify the DSP that program memory download has been completed. Either the DSP can poll a semaphore bit in its data memory (which the host can write using the same download procedure as described in 4, above, but using TYPE = 1 to reach DSP data memory) or the host can interrupt the DSP. Whether through polling a semaphore bit or through an interrupt, the DSP then jumps to the first valid instruction in the newly downloaded program memory and starts to function as a modem. Note that along the way, the DSP must manage its program memory address space, i.e., it must swap out the boot ROM and replace it with program memory RAM. This is accomplished by resetting PMOVLAY to 0.

AD1801 INTERFACE TO SMC91C94

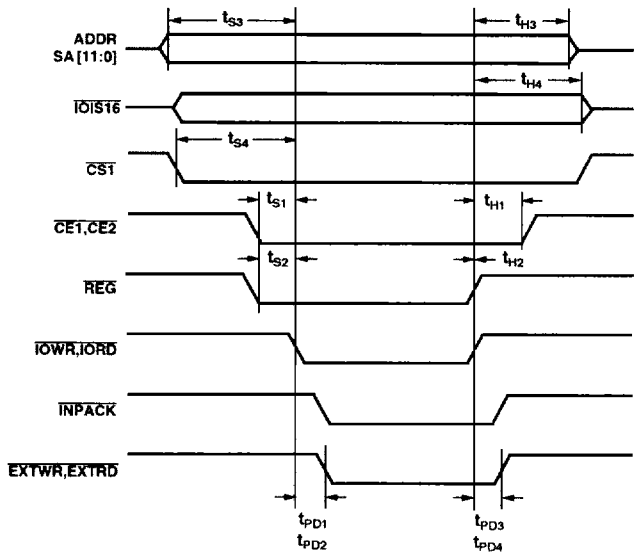


Figure 13. AD1801 Interface to the SMC91C94

Table XIV. Timing Parameters

	Min	Typ	Max	Units
$\overline{CE1}/\overline{CE2}$ from $\overline{IOR}/\overline{IOW}$ Rising (t_{H1})	20			ns
$\overline{CE1}/\overline{CE2}$ before $\overline{IOR}/\overline{IOW}$ Falling (t_{S1})		5		ns
$\overline{REG}$ from $\overline{IOR}/\overline{IOW}$ Rising (t_{H2})		0		ns
$\overline{REG}$ before $\overline{IOR}/\overline{IOW}$ Falling (t_{S2})		5		ns
SA[11:0] from $\overline{IOR}/\overline{IOW}$ Rising (t_{H3})		20		ns
SA[11:0] before $\overline{IOR}/\overline{IOW}$ Falling (t_{S3})		70		ns
$\overline{CS1}$ from $\overline{IOR}/\overline{IOW}$ Rising (t_{H4})		22		ns
$\overline{CS1}$ before $\overline{IOR}/\overline{IOW}$ Falling (t_{S4})		45		ns
$\overline{EXTWR}$ Falling from $\overline{IOW}$ Falling (t_{PD1})		2	15	ns
$\overline{EXTRD}$ Falling from $\overline{IOR}$ Falling (t_{PD2})		2	15	ns
$\overline{EXTWR}$ Rising from $\overline{IOW}$ Falling (t_{PD3})		2	15	ns
$\overline{EXTRD}$ Rising from $\overline{IOR}$ Rising (t_{PD4})		2	15	ns

AD1801 Generated Signal Explanation:

$\overline{CS1}$ and $\overline{CS2}$ are combinational decodes of the address lines only; they do not include $\overline{REG}$, $\overline{CE1}$ or $\overline{CE2}$.

$\overline{EXTWR}$ and $\overline{EXTRD}$, when enabled in "STROBE MODE," are the following functions:

$\overline{EXTWR} = \overline{IOW} + \overline{REG} + \overline{CE1}$

$\overline{EXTRD} = \overline{IOR} + \overline{REG} + \overline{CE1}$

$\overline{IOIS16}$ is a combinational decode of the SA[11:0] wires without $\overline{CS1}$, $\overline{CS2}$, or $\overline{REG}$.

$\overline{INPACK}$ is asserted during reads only, and depends on $\overline{IOR}$, SA[11:0], $\overline{CS1}$, and $\overline{REG}$. It does not depend on $\overline{CS2}$.

To access the external PCMCIA functions, the AD1801 must operate in PCMCIA mode. The SMC chip may operate in either PCMCIA or ISA mode; ISA mode is desired because the SMC's COR and CSR registers do not need to be programmed in ISA mode. ISA mode connections:

1. Connect SA[3:0] to the SMC's A[3:0]. This provides the register indexing.
2. The SMC must have a hard coded base address (from either pins or EEPROM). Wire the remaining A[15:4] bits to GND and V_{DD} to match the hardcoded base address.
3. Connect the AD1801 $\overline{CS1}$ output to the SMC's AEN input. $\overline{REG}$ is the corresponding PCMCIA signal; however, the timing for $\overline{REG}$ will violate the requirements of the SMC's AEN input. Therefore $\overline{REG}$ is included in the $\overline{EXTWR}$ and $\overline{EXTRD}$ signals instead.
4. Connect the SMC's $\overline{SBHE}$ pin to the bus $\overline{CE2}$ pin.
5. Connect the SMC's $\overline{IOW}$ pin to the AD1801's $\overline{EXTWR}$ pin (Pin 82, called "IRQ15/VTCL2/$\overline{EXTWR}$").
6. Connect the SMC's $\overline{IOR}$ pin to the AD1801's $\overline{EXTRD}$ pin (Pin 94, called "IRQ3/VTCL1/$\overline{EXTRD}$").

Before the AD1801's COR1 or COR2 is programmed, set the AD1801 into "STROBE MODE" by writing to the Interrupt Select register (DSP location 0x204). Writing bit 13 turns on STROBE MODE, enabling $\overline{EXTRD}$ and $\overline{EXTWR}$ to replace VCTL1 and VCTL2. Setting "STROBE MODE" in ISA mode has no effect.

Following this setup, the timing is as follows:

t_{SETUP} [$\overline{CS1}$ before $\overline{EXTRD}$/$\overline{EXTWR}$ falling] = 45 ns + 2 ns = 47 ns

t_{HOLD} [$\overline{CS1}$ from $\overline{EXTRD}$/$\overline{EXTWR}$ rising] = 22 ns – 15 ns = 7 ns

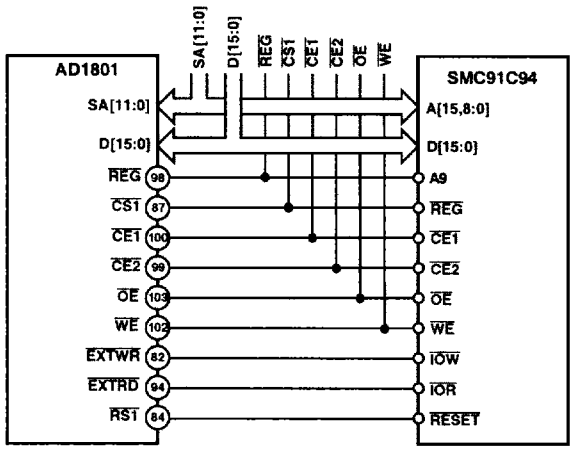


Figure 14. SMC91C94 Interface to AD1801 PCMCIA Mode

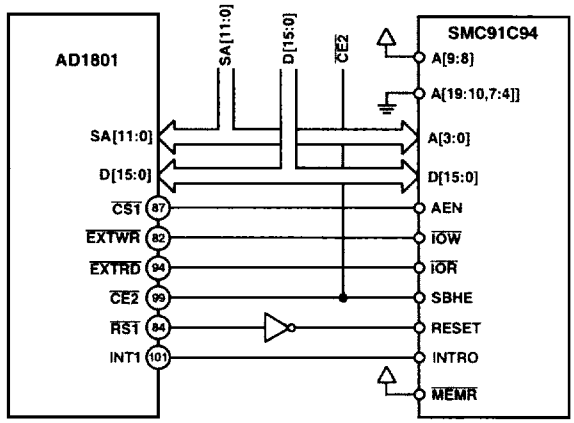


Figure 15. SMC91C94 Interface to AD1801 ISA Mode

APPLICATION CIRCUITS

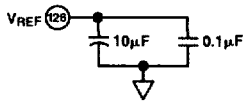


Figure 16. V_{REF} Bypassing

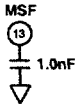


Figure 17. Monitor Speaker Filter

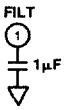


Figure 18. Antialias Filter Connection

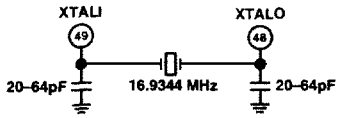


Figure 19. Crystal Circuit

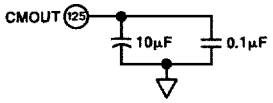


Figure 20. CMOUT Bypassing

If the target application requires any current from the CMOUT Pin (i.e., more than a few microamps), the circuit in Figure 20 (or its equivalent) must be used. The CMOUT output on the AD1801 cannot source/sink current directly without compromising analog performance.

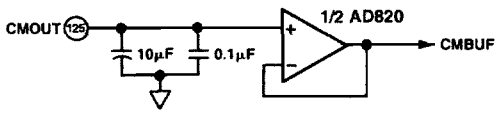


Figure 21. Buffered Reference Circuit

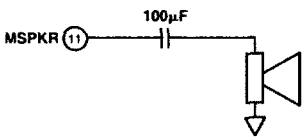


Figure 22. Monitor Speaker Connection

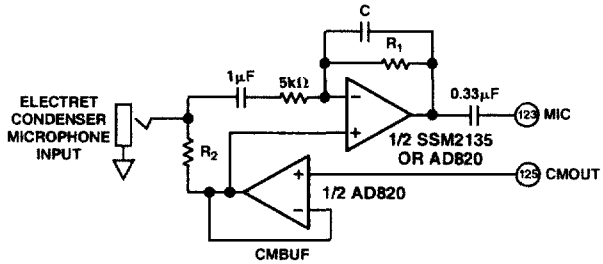


Figure 23. Phantom Power Mic Circuit

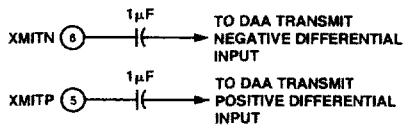


Figure 24. DAA Transmit Circuit

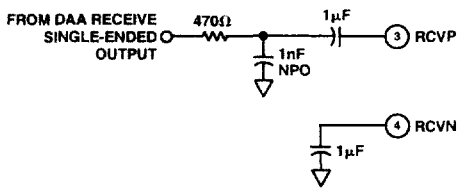


Figure 25. DAA Single-Ended Receive Circuit

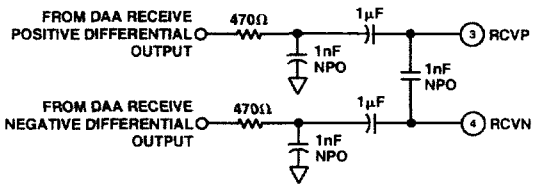


Figure 26. DAA Differential Receive Circuit

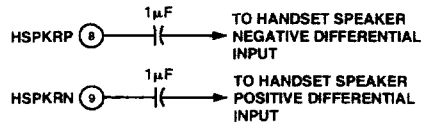


Figure 27. Handset Speaker Circuit

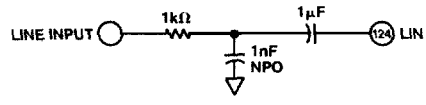


Figure 28. Line Input Circuitry

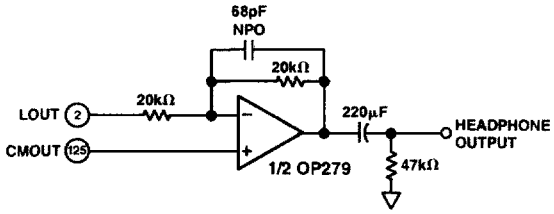


Figure 29. Headphone Output Circuitry

Note: Due to the nature of the SRAM process used to fabricate the AD1801, the digital and analog supplies for the device MUST be derived from the same source.

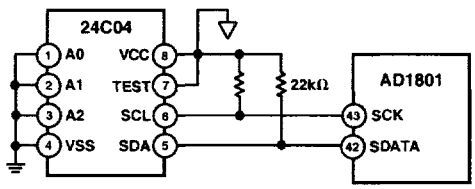


Figure 30. Serial EEPROM (Two Wire) Circuit

DESIGN GUIDELINES

The analog and digital power pins on the AD1801 have to be powered by the same supply to make sure that the analog power pins are at the same dc potential as the digital power pins. Otherwise substrate currents inside the AD1801 could exceed safe limits and the device could be permanently damaged. In view of this, it is recommended that the AD1801 be located over one and the same power plane and each AD1801 power pin (DV_{DD} and AV_{DD}) be connected to that power plane. Other digital devices on the PCB (at least ones driving AD1801 digital inputs) would typically be connected to this same power plane. It is important that a low impedance, well bypassed power source drive this power plane to reduce the chance of any DSP code dependent noise appearing on the AD1801 analog signals. The ISA/PCMCIA bus +5 V supply should suffice for this purpose. In addition to bypassing each AD1801 supply pin, it is recommended that an array of 0.001 μF, 1 μF ceramic and 10 μF tantalum capacitors be connected between the power plane and ground where power enters the PCB.

To minimize the digital ground currents flowing through the analog area, it is recommended that two ground planes be used for the AD1801, one for the digital half of the AD1801 plus other digital circuitry (digital ground plane), and the other for the analog half of the AD1801 plus any other analog circuitry (analog ground plane). This is shown in Figure 31. The analog and digital ground planes should only be tied together (mecca), at the point where the supply enters the PCB. Instead of connecting the two ground planes directly (with a trace) on prototype PCBs, it is recommended that this connection be made with a wire. This provides the flexibility to connect the two ground planes through a ferrite bead (which increases the isolation between the analog and digital circuitry), which may be desirable in some systems.

Care should be taken to provide as clean supplies as possible to the AD1801. At a minimum, an array of 10 μF, 0.1 μF and 0.01 μF capacitors should be used to filter the supply used to power the AD1801 where it enters the PCB. A combination of ferrite beads and capacitors can also be used to filter the supply, but care should be observed when doing this, since a particular combination of values, along with the power line supplying the PCB, may form a high Q circuit that could produce undesirable ringing of the supplies. As a general rule, regulating the +12 V available on the ISA bus may provide the cleanest supplies for the analog circuitry. If a regulator is used, it should be located close to where the unregulated voltage enters the PCB, at mecca ground.

In addition to having the amplifiers that perform signal conditioning on the DAA input also perform antialias filtering, it is recommended that the user build their first system with additional RC antialias circuitry between the DAA amplifiers and the DAA ADC input as shown in Figures 25 and 26. In addition to providing residual antialias filtering, the resistors isolate the DAA amplifiers from the switched capacitor DAA ADC inputs. These components may be removed if performance testing yields satisfactory results with the components not installed. The audio inputs (MIC and LIN) should not need an antialias filter in addition to what is provided by the amplifiers that drive those inputs. Installing such RC filters on the audio inputs, however, will only help improve the performance of the audio channels, especially in a noisy environment.

To ensure the best performance, the AD1801 bypass capacitors should be located as close to the AD1801 as possible. The following capacitors should be located as close to the AD1801 as possible. Note that the positive side (preferably also the ground side) of the supply bypass capacitors should be connected directly to the pin they are bypassing (i.e., not connected through the power plane). This list is in the order of importance with the capacitors that should be located closest listed first:

1. 0.1 μF ceramic capacitors bypassing V_{REF} and CMOUT.
2. 0.1 μF ceramic capacitors on the voltage supply pins and the 22 pF capacitors on the crystal I/O pins.
3. Any antialias filter capacitors and ac coupling capacitors that may be needed on the ADC inputs and the 1 nF ceramic capacitor on the MSF pin.
4. 10 μF tantalum capacitors bypassing V_{REF} and CMOUT and the 1 μF tantalum capacitor connected to the FILT Pin.
5. Input and output ac coupling capacitors not mentioned above do not need to be located close to the AD1801.

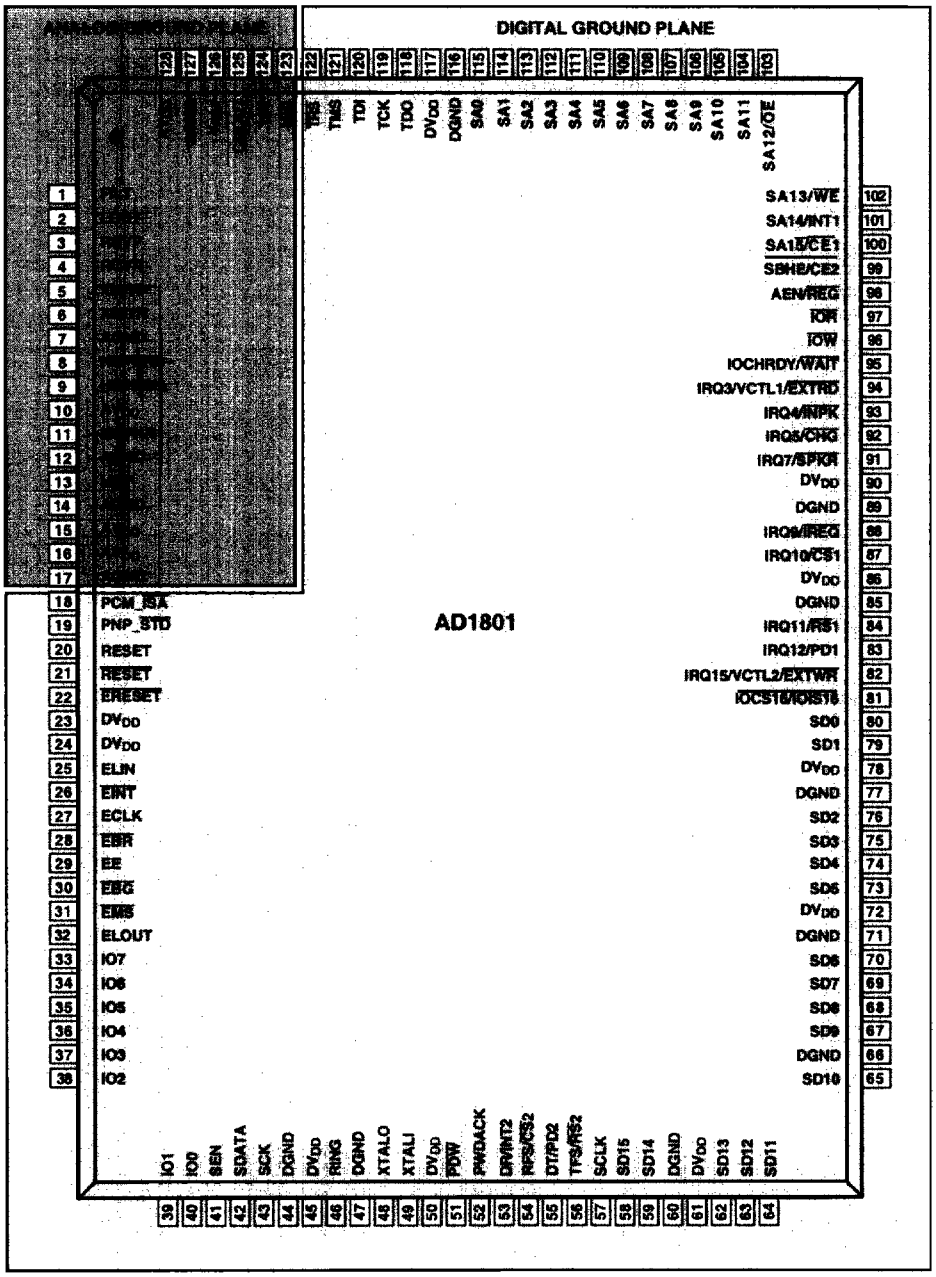
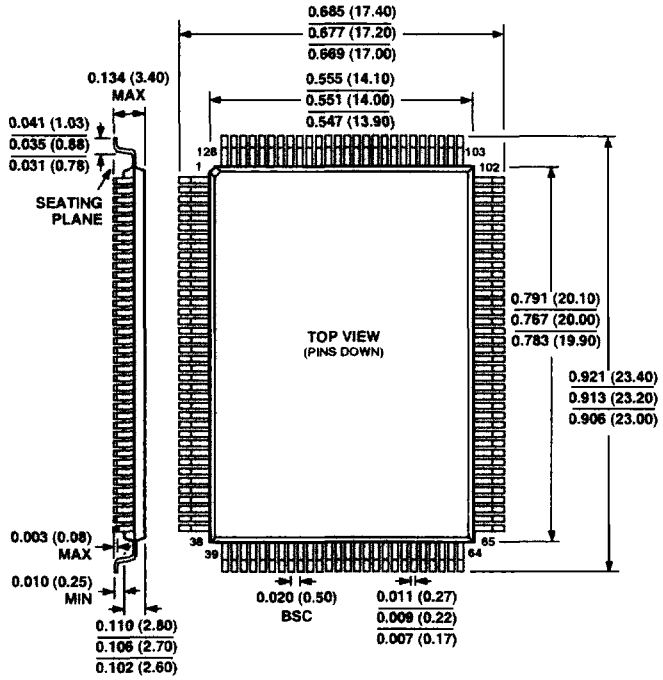


Figure 31. AD1801 Ground Planes

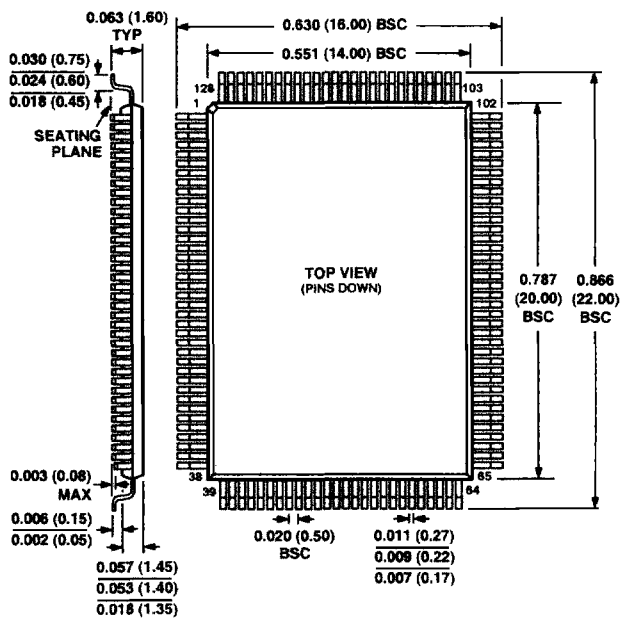
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

128-Lead PQFP
(S-128A)



128-Lead TQFP
(ST-128)



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