AMENDMENT

80L186/80L188

Low-Voltage CMOS High-Integration 16-Bit Microprocessors

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Operation Modes Include**
  - —Enhanced mode with
    - DRAM Refresh Control Unit
    - Power-save mode
  - —Compatible Mode
    - NMOS 80186/80188 pin-for-pin replacement for non-numerics applications
- **Integrated Feature Set**
  - —Enhanced 80C86/C88 CPU
  - —Clock generator
  - —Two independent DMA channels
  - —Programmable interrupt controller
  - —Three programmable 16-bit timers
  - —Dynamic RAM Refresh Control Unit
    - Programmable memory and peripheral chip select logic
  - —Programmable wait-state generator
  - —Local bus controller
  - —Power-save mode
  - —System-level testing support (high-impedance test mode)
- **Available in 16-MHz, 12.5-MHz, and 10-MHz versions**
- **Direct addressing capability to 1-Mbyte of memory and 64-Kbyte I/O**
- **Fully static CMOS design**
- **Completely object code compatible with all existing 8086/8088 software. Has ten additional instructions over 8086/8088.**
- **Complete system development**
  - —There are many vendors making support tools for the 80L186/L188. Software tools for the NMOS 80186/80188 can be used for the 80L186/L188 as can the NMOS emulators
- **Available in**
  - —68-Pin Plastic Leaded Chip Carrier (PLCC)
  - —80-Pin Thin Quad Flat Pack (TQFP)
  - —80-Pin Plastic Quad Flat Pack (PQFP)
    - In Trimmed/Formed Configuration

GENERAL DESCRIPTION

The 80L186 and 80L188 are low-voltage versions of the 80C186/80C188 CMOS high-integration microprocessors. With the operating range of 3 V to 5.5 V, the 80L186 and 80L188 are ideal for portable/battery operated system designs where battery life and/or system weight are concerns. Lowering the operating voltage from 5 V to 3.3 V effectively halves the power consumption of the device. The 80L186 and 80L188 are pin and function compatible with the industry standard 80C186 and 80C188 and operate at speeds of 10, 12, and 16 MHz. The 80L186 and 80L188 are upward compatible with 8086 and 8088 software and fully compatible with 80186 and 80188 software.

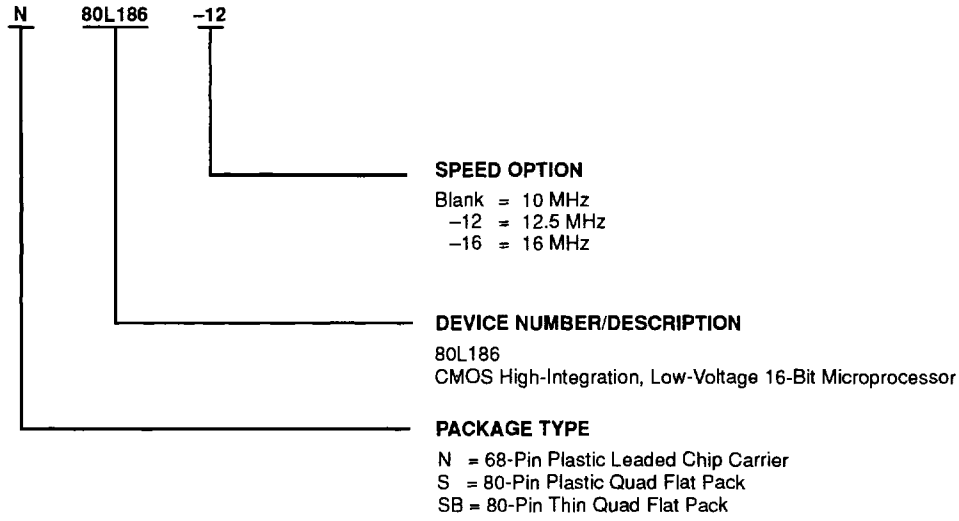
The 80L186 and 80L188 are packaged in the industry standard 68-pin PLCC and 80-pin PQFP packages. The PQFP version is only offered in Trim and Form.

Publication #: 17907 Rev. A Amendment /1
Issue Date: September 1993

80L186 ORDERING INFORMATION

Commodity Products

AMD® commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
PLCC	N80L186
	N80L186–12
	N80L186–16

PQFP Trimmed and Formed	S80L186
	S80L186–12
	S80L186–16

TQFP	SB80L186
	SB80L186–12
	SB80L186–16

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

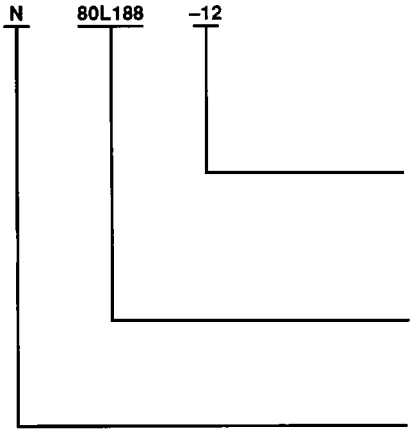
Note:

Trimmed and formed configuration has AMD doing the trim and form function to a JEDEC standard standoff and lead length. The product is shipped in trays.

80L188 ORDERING INFORMATION

Commodity Products

AMD® commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



SPEED OPTION

Blank = 10 MHz
–12 = 12.5 MHz
–16 = 16 MHz

DEVICE NUMBER/DESCRIPTION

80L188
CMOS High-Integration Low-Voltage 16-Bit Microprocessor

PACKAGE TYPE

N = 68-Pin Plastic Leaded Chip Carrier
S = 80-Pin Plastic Quad Flat Pack
SB = 80-Pin Thin Quad Flat Pack

Valid Combinations	
PLCC	N80L188
	N80L188–12
	N80L188–16

PQFP Trimmed and Formed	S80L188
	S80L188–12
	S80L188–16

TQFP	SB80L188
	SB80L188–12
	SB80L188–16

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note:

Trimmed and formed configuration has AMD doing the trim and form function to a JEDEC standard standoff and lead length. The product is shipped in trays.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias
- Commercial(T_A) ..... 0°C to +70°C
- Industrial(T_{A-IND}) ..... –40°C to +85°C

Storage temperature ..... –65°C to +150°C

Voltage on any pin with respect to ground ..... –1.0 V to +7.0 V

Package power dissipation ..... 1 W

Not to exceed the maximum allowable die temperature based on thermal resistance of the package.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

80L186/80L188 DC CHARACTERISTICS over operating ranges (Low Voltage)

T_A = 0°C to +70°C, V_{CC} = 3.3 V ±10%

Symbol	Parameter Description	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	–0.5	0.3 V_{CC}	V	
V_{IL1}	Clock Input Low Voltage (X1)	–0.5	0.6	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Clock Input High Voltage (X1)	2.7	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	V_{CC}–0.5	V_{CC}	V	I_{OH} = –1.0 mA
I_{CC}	Power Supply Current				
			40	mA	@ 16 MHz, 85°C V_{CC} = 3.6 V (Note 3)
			32	mA	@ 12.5 MHz, 85°C V_{CC} = 3.6 V (Note 3)
			25	mA	@ 10 MHz, 85°C V_{CC} = 3.6 V (Note 3)
			100	µA	@ DC, 85°C V_{CC} = 3.6 V
I_{LI}	Input Leakage Current (All others)		±10	µA	@ 0.5 MHz, 0.45 V < V_{IN} < V_{CC}
I_{LI2}	Input Leakage Current ($\overline{RD}$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$, $\overline{TEST}$)		–700	µA	V_{IN} = 0 V (Note 4)
I_{LO}	Output Leakage Current		±10	µA	@ 0.5 MHz, 0.45 V < V_{OUT} < V_{CC} (Note 1)
C_{IN}	Input Capacitance		15	pF	@ 1 MHz (Note 2)
C_{IO}	Output or I/O Capacitance		20	pF	@ 1 MHz (Note 2)

Notes:
1. *Pins being floated during HOLD or by invoking the ONCE Mode. Characterization conditions are: a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} @ +3.3 V or 0.45 V.*
2. *This parameter is not tested.*
3. *Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.*
4. *$\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$,and $\overline{TEST}$ pins have internal pull-up devices. Loading some of these pins above I_{OH} = –700 µA can cause the 80L186/L188 to go into alternative modes of operation.*

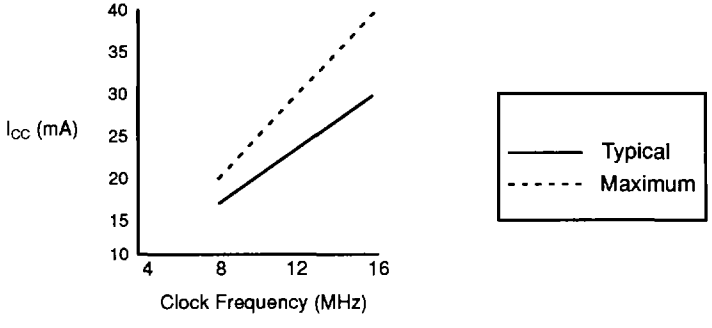
Maximum current is given by I_{CC} (Max) = 2.5 mA x freq. (MHz)
Typical current is given by I_{CC} (typ)= 1.75 mA x freq. (MHz) + 1 mA

Power Supply Current

Current is linearly proportional to clock frequency and is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.

Maximum current is given by I_{CC} = 2.5 mA x freq. (MHz).

Typical current is given by I_{CC} (typical) = 1.75 mA x freq. + 1 mA (MHz). "Typicals" are based on a limited number of samples taken from early manufacturing lots measured at V_{CC} = 3.6 V and room temperature. "Typicals" are not guaranteed.



13087D–045

Figure 1. I_{CC} versus Frequency

80L186/80L188 SWITCHING CHARACTERISTICS over COMMERCIAL operating range

T_A = 0°C to +70°C, V_{CC} = 3.0 V to 5.5 V

Parameter			Preliminary					
			10 MHz		12 MHz		16 MHz	
#	Sym	Description	Min	Max	Min	Max	Min	Max
General Timing Requirements								
1	t_{DVCL}	Data in Setup (A/D)	15		15		15	
2	t_{CLDX}	Data in Hold (A/D)	3		3		3	
General Timing Responses								
3	t_{CHSV}	Status Active Delay	3	45	3	35	3	33
4	t_{CLSH}	Status Inactive Delay	3	46	3	37	3	35
5	t_{CLAV}	Address Valid Delay	3	44	3	36	3	33
6	t_{CLAX}	Address Hold	0		0		0	
7	t_{CLDV}	Data Valid Delay	3	40	3	36	3	33
8	t_{CHDX}	Status Hold Time	10		10		10	
9	t_{CHLH}	ALE Active Delay		30		27		25
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 85		t_{CLCL}–15 = 65		t_{CLCL}–15 = 47.5	
11	t_{CHLL}	ALE Inactive Delay		30		25		20
12	t_{AVLL}	Address Valid to ALE Low*	t_{CLCH}–18= 26		t_{CLCH}–15 = 20		t_{CLCH}–15 = 11.25	
13	t_{LLAX}	Address Hold from ALE Inactive*	t_{CHCL}–15= 29		t_{CHCL}–15 = 20		t_{CHCL}–15 = 11.25	
14	t_{AVCH}	Address Valid to Clock High	0		0		0	
15	t_{CLAZ}	Address Float Delay	t_{CLAX} = 0	30	t_{CLAX} = 0	25	t_{CLAX} = 0	20
16	t_{CLCSV}	Chip-Select Active Delay	3	42	3	33	3	30
17	t_{CXCSX}	Chip-Select Hold from Command Inactive*	t_{CLCH}–10= 34		t_{CLCH}–10= 25		t_{CLCH}–10= 16.25	
18	t_{CHCSX}	Chip-Select Inactive Delay	3	35	3	30	3	25
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low*	0		0		0	
20	t_{CVCTV}	Control Active Delay 1						
		$\overline{DEN}$	3	44	3	37	3	31
		$\overline{INTA}$	3	44	3	37	3	31
		$\overline{WR}$	3	44	3	37	3	31
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	44	3	37	3	35
22	t_{CHCTV}	Control Active Delay 2						
		$\overline{DEN}$	3	44	3	37	3	33
		$\overline{INTA}$	3	44	3	37	3	33
		$\overline{WR}$	3	44	3	37	3	33
23	t_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	3	35
Timing Responses–Read Cycle								
24	t_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		0	
25	t_{CLRL}	$\overline{RD}$ Active Delay	3	44	3	37	3	35
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}$–30= 170		$2t_{CLCL}$–25= 135		$2t_{CLCL}$–25= 100	
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	3	44	3	37	3	31
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High*	t_{CLCH}–14= 30		t_{CLCH}–14= 21		t_{CLCH}–14= 12.25	
29	t_{RHAV}	$\overline{RD}$ Inactive to Address Active*	t_{CLCL}–15= 85		t_{CLCL}–15= 65		t_{CLCL}–15= 47.5	

Notes:
**Equal Loading*
*** $\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$*
All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All ouput test conditions are with C_L = 50–100 pF (10–25 MHz).
For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V.

80L186/80L188 SWITCHING CHARACTERISTICS over COMMERCIAL operating range (continued)

T_A = 0°C to +70°C, V_{CC} = 3.0 V to 5.5 V

Parameter			Preliminary					
			10 MHz		12 MHz		16 MHz	
#	Sym	Description	Min	Max	Min	Max	Min	Max
Timing Responses Write Cycle								
30	t_{CLDOX}	Data Hold Time	3		3		3	
31	t_{CVCTX}	Control Inactive Delay						
		$\overline{DEN}$	3	44	3	37	3	31
		$\overline{INTA}$	3	44	3	37	3	31
		$\overline{WR}$	3	44	3	37	3	31
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-30$ = 170		$2t_{CLCL}-25$ = 135		$2t_{CLCL}-25$ = 100	
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High*	$t_{CLCH}-14$ = 30		$t_{CLCH}-14$ = 21		$t_{CLCH}-14$ = 12.25	
34	t_{WHDX}	Data Hold after $\overline{WR}$*	$t_{CLCL}-34$ = 66		$t_{CLCL}-20$ = 60		$t_{CLCL}-20$ = 42.5	
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive*	$t_{CLCH}-10$ = 34		$t_{CLCH}-10$ = 25		$t_{CLCH}-10$ = 16.25	
CLKIN Requirements **Measurements taken with external clock input to X1 and X2 not connected (Float).**								
36	t_{CKIN}	CLKIN Period	50		40		31.25	
37	t_{CLCK}	CLKIN Low Time 1.5 V (Note 2)	20		16		13	
38	t_{CHCK}	CLKIN High Time 1.5 V (Note 2)	20		16		13	
39	t_{CKHL}	CLKIN Fall Time 3.5 to 1.0 V		5		5		5
40	t_{CKLH}	CLKIN Rise Time 1.0 to 3.5 V		5		5		5
CLKOUT Timing								
41	t_{CICO}	CLKIN to CLKOUT Skew		25		21		17
42	t_{CLCL}	CLKOUT Period	100		80		62.5	
43	t_{CLCH}	CLKOUT Low Time C_L = 100 pF (Note 2)	$0.5\,t_{CLCL}-8$ = 42		$0.5\,t_{CLCL}-7$ = 33		$0.5\,t_{CLCL}-7$ = 24.25	
		C_L = 50 pF (Note 3)	$0.5\,t_{CLCL}-6$ = 44		$0.5\,t_{CLCL}-5$ = 35		$0.5\,t_{CLCL}-5$ = 26.25	
44	t_{CHCL}	CLKOUT High Time C_L = 100 pF (Note 4)	$0.5\,t_{CLCL}-8$ = 42		$0.5\,t_{CLCL}-7$ = 33		$0.5\,t_{CLCL}-7$ = 24.25	
		C_L = 50 pF (Note 3)	$0.5\,t_{CLCL}-6$ = 44		$0.5\,t_{CLCL}-5$ = 35		$0.5\,t_{CLCL}-5$ = 26.25	
45	t_{CH1CH2}	CLKOUT Rise Time 1.0 to 3.5 V		10		10		10
46	t_{CL2CL1}	CLKOUT Fall Time 3.5 to 1.0 V		10		10		10
Ready and Peripheral Timing Requirements								
47	t_{SRYCL}	SRDY Transition Setup Time (Note 5)	15		15		15	
48	t_{CLSRY}	SRDY Transition Hold Time (Note 5)	15		15		15	
49	t_{ARYCH}	ARDY Res. Transition Setup Time (Note 6)	15		15		15	
50	t_{CLARX}	ARDY Active Hold Time (Note 5)	15		15		15	
51	t_{ARYCHL}	ARDY Inactive Holding Time	15		15		15	
52	t_{ARYLCL}	ARDY Setup Time (Note 5)	25		25		25	

80L186/80L188 SWITCHING CHARACTERISTICS over COMMERCIAL operating range (continued)

T_A = 0°C to +70°C, V_{CC} = 3.0 V to 5.5 V

Parameter			Preliminary					
			10 MHz		12 MHz		16 MHz	
#	Sym	Description	Min	Max	Min	Max	Min	Max
Ready and Peripheral Timing Requirements (continued)								
53	t_{INVCH}	Peripheral Setup (Note 6)						
		INTx	15		15		15	
		NMI	15		15		151	
		TMR IN	15		15		15	
		TEST/BUSY	15		15		15	
54	t_{INVCL}	DRQ0, DRQ1 Setup Time (Note 6)	15		15		15	
Peripheral and Queue Status Timing Responses								
55	t_{CLTMV}	Timer Output Delay		40		33		27
56	t_{CHQSV}	Queue Status Delay		37		32		30
RESET and HOLD/HLDA Timing Requirements								
57	t_{RESIN}	RES Setup	15		15		15	
58	t_{HVCL}	HOLD Setup (Note 7)	15		15		15	
15	t_{CLAZ}	Address Float Delay	0	30	0	25	0	20
5	t_{CLAV}	Address Valid Delay	3	44	3	36	3	33
RESET and HOLD/HLDA Timing Responses								
61	t_{CLRO}	Reset Delay		40		33		27
62	t_{CLHAV}	HLDA Valid Delay	3	40	3	33	3	25
63	t_{CHCZ}	Command Lines Float Delay		40		33		28
64	t_{CHCV}	Command Lines Valid Delay (after Float)		44		36		32

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 – 100 pF.
For AC tests, input V_{IL} = 0 V and V_{IH} = V_{CC}.

Notes:

1. *t_{CLCK} and t_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of t_{CKIN}.*
2. *Tested under worst case conditions: V_{CC} = 5.5 V, Ta = 70°C.*
3. *Not tested.*
4. *Tested under worst case conditions: V_{CC} = 4.5 V, Ta = 0°C.*
5. *To guarantee proper operation.*
6. *To guarantee recognition at clock edge.*
7. *To guarantee recognition at next clock.*

LOW-VOLTAGE OPERATION OVERVIEW

The low-voltage operation of the 80L186 and 80L188 microprocessors is an enabling technology for the design of portable systems with long battery life. This capability, combined with CPU clock management and SMM features, allows the design of very low power computing systems.

Low-Voltage Standard

Industry standards for low-voltage operation are emerging to facilitate the design of components which will make up a complete low-voltage system. As a guideline, the 80L186 and 80L188 processor specifications follow the first article or regulated version of the JEDEC 8.0 low-voltage proposal. This standard proposal calls for a V_{CC} range of 3.3 V ± 10%. To ease the design of a mixed voltage system, the standard also supports CMOS and TTL outputs.

Power Savings

CMOS Dynamic power consumption is proportional to the square of the operating voltage multiplied by capacitance and operating frequency. Static CPU operation can reduce power consumption by enabling the system designer to reduce operating frequency when possible. However, operating voltage is always the dominant factor in power consumption. By reducing the operating voltage from 5 V to 3.3 V for any device, the power consumed is reduced by 56% (see Figure 2).

The reduction of CPU and core logic operating voltage dramatically reduces overall system power consumption. Additional power savings can be realized as low-voltage mass storage and peripheral devices become available.

Two basic strategies exist in designing systems containing the 80L186 and 80L188 microprocessors. The first strategy is to design a homogenous system in which all logic components operate at 3.3 V. This provides the best overall power consumption. However, system designers may need to include devices for which 3.3-V versions are not available. In the second strategy, the system designer must then design a mixed 5-V/3.3-V system. This compromise allows the system designer to minimize the core logic power consumption while still including the functionality of the 5-V features. The choice of a mixed voltage system design also involves balancing design complexity with the need for the additional features.

PIN LEVEL INTERFACE

Ideally, 80L186 and 80L188 microprocessors are used in homogenous low-voltage systems. However, in some cases not all system logic devices are available in low-voltage versions. In this case, mixed voltage systems must be examined. There are two cases to consider when designing mixed voltage systems.

First consider a 3.3-V device driving a 5-V input (see Figure 3a). In this case, the 3.3-V signal is subject to lower noise immunity than a 5-V signal. If the buffer has a pure CMOS input, the 3.3-V signal does not drive the input buffer completely out of the transition region, thereby allowing excessive current to be consumed. The second case, a 5-V device driving a 3.3-V input (see Figure 3b), poses a more serious problem. In this case, the 5-V signal will over drive and possibly breakdown the 3.3-V input. This breakdown can lead to potentially damaging latch up of the 3.3-V device.

These interface problems can be avoided in two ways. The first consideration is the use of voltage translation buffers (see Figure 4). These dual voltage devices provide a seamless interface between different voltage devices.

A second solution addresses the 5-V driving a 3.3-V input case and uses discrete components to provide the 5-V to 3.3-V interface (see Figure 5). Here the use of a diode and pull-up simply and effectively translates a 5-V input signal to a 3.3-V input signal.

The operation of the discrete translator is diagramed in Figure 6. When the 5-V signal is Low, the diode is forward biased and the pull-up current is shunted through the 5-V driver (see Figure 6a). Thus, a low voltage is presented to the 3.3-V input. When the 5-V signal is High, the diode is reverse biased with respect to the 3.3-V pull-up and is thus blocked from the 3.3-V input (see Figure 6b); therefore, the 3.3-V pull-up is presented to the input as a valid High. The choice of the pull-up value must balance the AC timing requirements of the signal with the desire for low current consumption.

Optionally, the use of discrete components can be eliminated by understanding the type of devices needed to interface to 3.3-V and 5-V logic and including the translation into the system core logic. Signals requiring a 5-V interface can be driven by circuitry with 5-V supplies. Any 3.3-V devices can be driven by circuitry with 3.3-V supplies. In this solution the core logic isolates different parts of the interface logic to drive the appropriate levels.

3.3 V

$P_3 = V^2CFK$
$P_3 = K(3.3)^2CFK$
$P_3 = 10.89CFK$

5 V

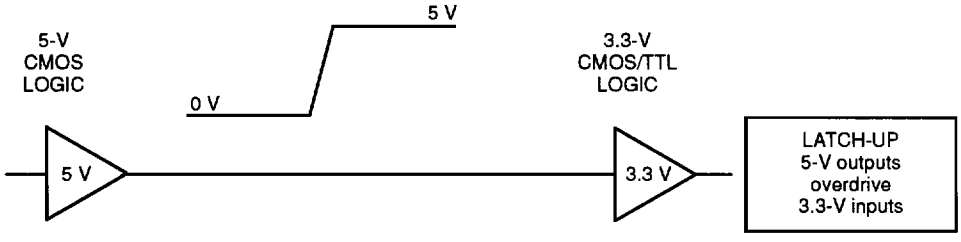
$P_5 = V^2CFK$
$P_5 = (5)^2CFK$
$P_5 = 25CFK$

Reduction = $1 - P_3/P_5$
= $1 - 0.44$
= 56%

where V = Voltage
C = Capacitance
F = Frequency
K = Constant

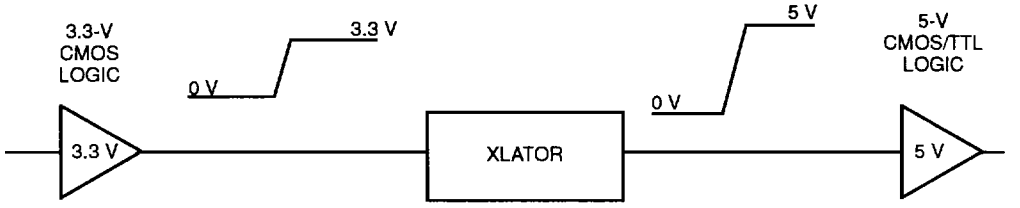
Figure 2. 3-V and 5-V System Dynamic Power Consumption

a. 3.3-V Driver to 5-V Input

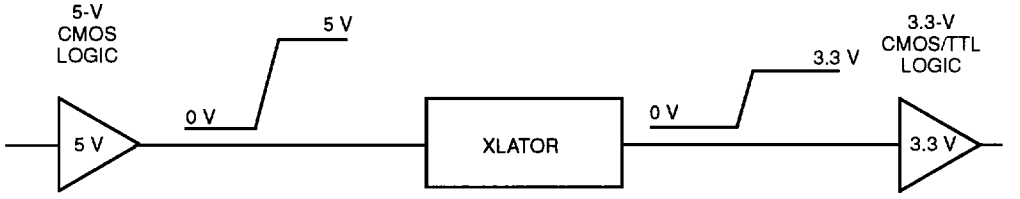


b. 5-V Driver to 3.3-V Input

Figure 3. Mixed 5-V/3-V Considerations



a. 3.3-V to 5-V Translation



b. 5-V to 3.3-V Translation

Figure 4. Mixed System with Voltage Translators

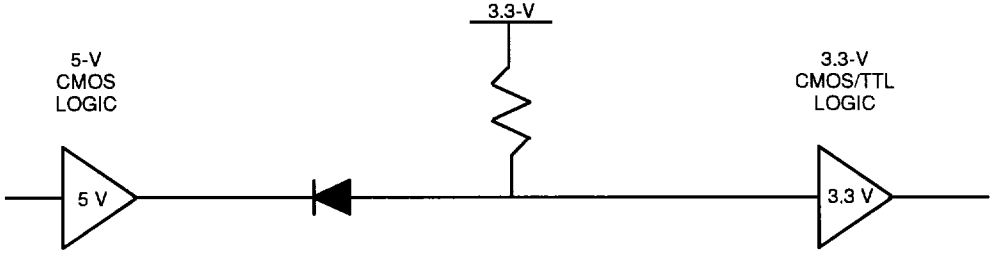
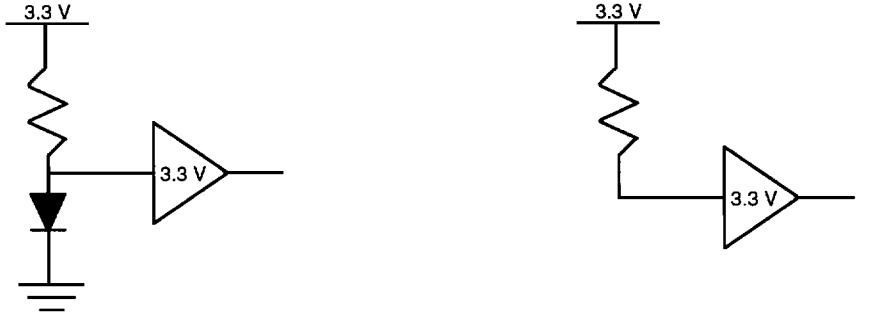


Figure 5. Mixed System with Discrete Translators



a. 5-V Output at Logic 0

b. 5-V Output at Logic 1

Figure 6. Discrete Translator Function

The operation of this discrete translator is diagramed in Figure 6. When the 5-V signal is Low, the diode is forward biased and the pull-up current is shunted through the 5-V driver (see Figure 6a). Thus, a low voltage is presented to the 3.3-V input. when the 5-V signal is High, the diode is reverse biased with respect to the 3.3-V pull up and is thus blocked from the 3.3-V input (see Figure 6b); therefore, the 3.3-V pull-up is presented to the input as a valid High. The choice of the pull-up value must balance the AC timing requirements of the signal with the desire for low current consumption.

Optionally, the use of discrete components can be eliminated by understanding the type of devices needed to interface to 3.3-V and 5-V logic and including the translation into the system core logic. Signals requiring a 5-V interface can be driven by circuity with 5-V supplies. Any 3.3-V devices can be driven by circuitry with 3.3-V supplies. In this solution the core logic isolates different parts of the interface logic to drive the appropriate levels.