NEC

MOS INTEGRATED CIRCUIT

μPD30550A

VR5500A, VR5532A

64-/32-BIT MICROPROCESSOR

DESCRIPTION

★ The μPD30550AF2-300-NN1 and μPD30550AF2-400-NN1 (VR5500A), and μPD30550AGD-300-WML and
★ μPD30550AGD-350-WML (VR5532A) are members of the VR™ Series of RISC (Reduced Instruction Set Computer) microprocessors. They are high-performance 64-/32-bit microprocessors that employ the RISC architecture developed by MIPS™. The VR5500A uses a BGA package and provides a 300 MHz product and a 400 MHz product. The VR5532A uses a QFP package and provides a 300 MHz product and a 350 MHz product (please refer to **ORDERING INFORMATION** for details).

The VR5500A allows selection of a 64-bit or 32-bit bus width for the system interface, and can operate using protocols compatible with the VR5000 Series and VR5432. The VR5532A does not include a system interface bus width selection function (the bus is fixed to 32 bits).

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

- **VR5500A, VR5532A User's Manual (U16677E/U16677J)**

FEATURES

- MIPS 64-bit RISC architecture
- High-speed operation processing
  - Two-way superscalar super pipeline
  - [VR5500A]
    300 MHz product: 603 MIPS
    400 MHz product: 804 MIPS
    [VR5532A]
    300 MHz product: 603 MIPS
★ 350 MHz product: 703 MIPS
★ • High-speed translation lookaside buffer (TLB)(48 entries)
- Address space
  - Physical: 36 bits (64-bit bus selected)[Note]
    32 bits (32-bit bus selected)
  - Virtual: 40 bits (in 64-bit mode)
    31 bits (in 32-bit mode)
- On-chip floating-point unit (FPU)
  - Supports sum-of-products instructions
- On-chip primary cache memory
  (instruction/data: 32 KB each)
  - 2-way set associative
  - Supports line lock feature
- 64-/32-bit address/data multiplexed bus
  - Bus width selectable during reset[Note]
  - Bus protocol compatibility with existing products retained
- Maximum operating frequency
  - [VR5500A]
    300 MHz product: Internal 300 MHz, external 133 MHz
    400 MHz product: Internal 400 MHz, external 133 MHz
    [VR5532A]
    300 MHz product: Internal 300 MHz, external 100 MHz
    350 MHz product: Internal 350 MHz, external 100 MHz
  - External/internal multiplication factor selectable from ×2 to ×5.5 by increments of 0.5
- Conforms to MIPS I, II, III, and IV instruction sets. Also supports product-sum operation instruction, rotate instruction, register scan instruction, and instruction for low power mode.
- Supports hardware debug function (N-Wire)
- Supply voltage
  Core block: 1.5 V ±5% (300 MHz product)
  1.5 V ±5% (350 MHz product, VR5532A)
  1.6 to 1.7 V (400 MHz product, VR5500A)
  I/O block: 3.3 V ±5%, 2.5 V ±5%

Note VR5500A only.

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The mark ★ shows major revised points.

APPLICATIONS

- Set-top boxes
- MFP/LBP
- RAID
- High-end embedded devices, etc.

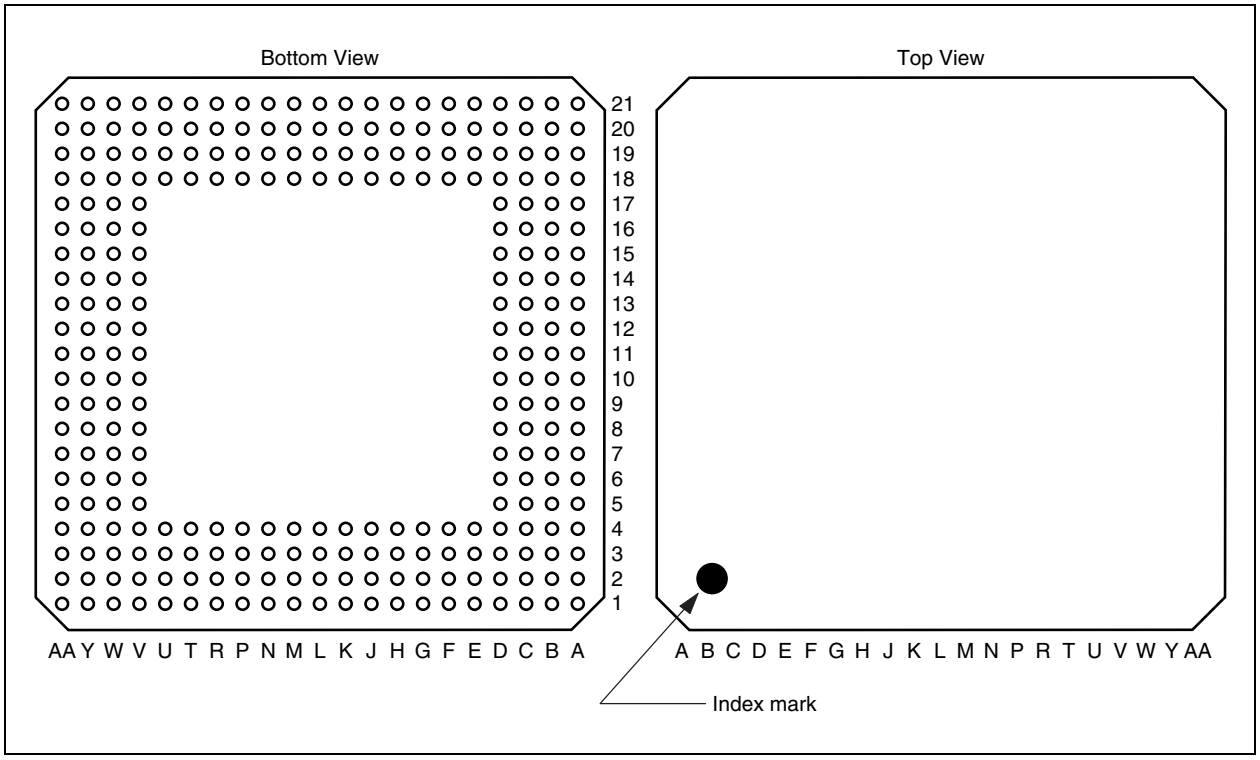
ORDERING INFORMATION

Part Number	Package	Maximum Operating Frequency
μPD30550AF2-300-NN1	272-pin plastic BGA (C/D advanced type) (29 × 29)	300 MHz
μPD30550AF2-300-NN1-A[Note]	272-pin plastic BGA (C/D advanced type) (29 × 29)	300 MHz
μPD30550AF2-400-NN1	272-pin plastic BGA (C/D advanced type) (29 × 29)	400 MHz
μPD30550AF2-400-NN1-A[Note]	272-pin plastic BGA (C/D advanced type) (29 × 29)	400 MHz
★ μPD30550AGD-300-WML	208-pin plastic QFP (fine pitch) (28 × 28)	300 MHz
★ μPD30550AGD-300-WML-A[Note]	208-pin plastic QFP (fine pitch) (28 × 28)	300 MHz
★ μPD30550AGD-350-WML	208-pin plastic QFP (fine pitch) (28 × 28)	350 MHz
★ μPD30550AGD-350-WML-A[Note]	208-pin plastic QFP (fine pitch) (28 × 28)	350 MHz

Note Lead-free product

PIN CONFIGURATION

- 272-pin plastic BGA (C/D advanced type) (29 × 29)
  μPD30550AF2-300-NN1, μPD30550AF2-300-NN1-A, μPD30550AF2-400-NN1, μPD30550AF2-400-NN1-A



(1/2)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
A1	V_{SS}	B17	SysAD27	D12	V_{SS}	H4	V_{DD}
A2	V_{SS}	B18	V_{DD}IO	D13	SysAD31	H18	V_{SS}
A3	V_{DD}IO	B19	V_{DD}IO	D14	V_{DD}	H19	V_{SS}
A4	V_{DD}IO	B20	V_{SS}	D15	SysAD60	H20	V_{SS}
A5	Reset#	B21	V_{SS}	D16	V_{SS}	H21	SysAD21
A6	PReq#	C1	V_{DD}IO	D17	SysAD26	J1	SysCmd7
A7	ValidIn#	C2	V_{DD}IO	D18	V_{SS}	J2	SysCmd8
A8	ValidOut#	C3	V_{SS}	D19	V_{SS}	J3	TIntSel
A9	V_{SS}	C4	V_{SS}	D20	V_{DD}IO	J4	Int0#
A10	SysADC7	C5	V_{SS}	D21	V_{DD}IO	J18	SysAD52
A11	SysADC3	C6	V_{DD}	E1	SysCmd0	J19	SysAD20
A12	SysADC1	C7	WrRdy#	E2	DisDValidO#	J20	SysAD51
A13	SysADC4	C8	V_{SS}	E3	DWBTrans#	J21	SysAD19
A14	SysAD62	C9	SysID1	E4	O3Return#	K1	Int1#
A15	SysAD30	C10	V_{DD}	E18	SysAD57	K2	V_{SS}
A16	SysAD28	C11	SysADC2	E19	SysAD25	K3	V_{SS}
A17	SysAD59	C12	V_{SS}	E20	SysAD56	K4	V_{SS}
A18	V_{DD}IO	C13	SysAD63	E21	SysAD24	K18	V_{DD}
A19	V_{DD}IO	C14	V_{DD}	F1	SysCmd1	K19	V_{DD}
A20	V_{SS}	C15	SysAD29	F2	V_{SS}	K20	V_{DD}
A21	V_{SS}	C16	V_{SS}	F3	V_{SS}	K21	V_{DD}
B1	V_{SS}	C17	SysAD58	F4	V_{SS}	L1	Int2#
B2	V_{SS}	C18	V_{DD}IO	F18	V_{DD}	L2	Int3#
B3	V_{DD}IO	C19	V_{SS}	F19	V_{DD}	L3	Int4#
B4	V_{DD}IO	C20	V_{DD}IO	F20	V_{DD}	L4	Int5#
B5	ColdReset#	C21	V_{DD}IO	F21	SysAD55	L18	SysAD17
B6	Release#	D1	V_{DD}IO	G1	SysCmd2	L19	SysAD49
B7	ExtRqst#	D2	V_{DD}IO	G2	SysCmd3	L20	SysAD18
B8	BusMode	D3	V_{SS}	G3	SysCmd4	L21	SysAD50
B9	SysID2	D4	V_{SS}	G4	SysCmd5	M1	RMode#/BKTGIO#
B10	V_{DD}	D5	IC	G18	SysAD23	M2	V_{DD}
B11	SysADC6	D6	V_{DD}	G19	SysAD54	M3	V_{DD}
B12	V_{SS}	D7	RdRdy#	G20	SysAD22	M4	V_{DD}
B13	SysADC0	D8	V_{SS}	G21	SysAD53	M18	V_{SS}
B14	V_{DD}	D9	SysID0	H1	SysCmd6	M19	V_{SS}
B15	SysAD61	D10	V_{DD}	H2	V_{DD}	M20	V_{SS}
B16	V_{SS}	D11	SysADC5	H3	V_{DD}	M21	V_{SS}

Caution Leave the IC pin open.

Remark # indicates active low.

(2/2)

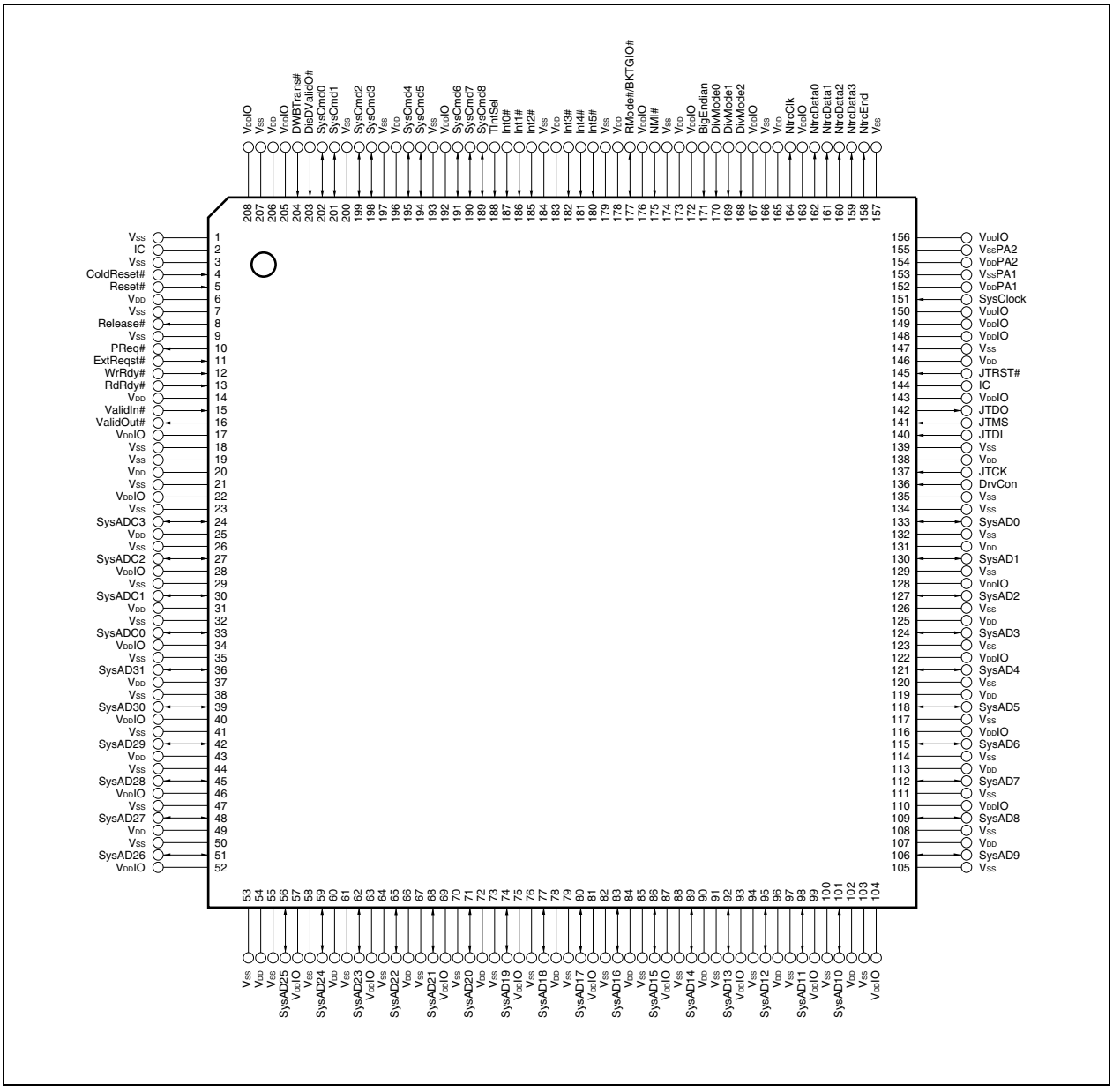
No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
N1	V_{DD}IO	T21	SysAD12	W2	V_{DD}IO	Y12	V_{DD}
N2	NMI#	U1	NTrcClk	W3	V_{SS}	Y13	SysAD3
N3	V_{DD}IO	U2	NTrcData0	W4	V_{SS}	Y14	V_{SS}
N4	BigEndian	U3	NTrcData1	W5	V_{DD}PA2	Y15	SysAD37
N18	SysAD15	U4	NTrcData3	W6	V_{SS}	Y16	SysAD39
N19	SysAD47	U18	SysAD10	W7	V_{DD}IO	Y17	SysAD40
N20	SysAD16	U19	SysAD42	W8	V_{DD}	Y18	V_{DD}IO
N21	SysAD48	U20	SysAD11	W9	JTDI	Y19	V_{DD}IO
P1	V_{SS}	U21	SysAD43	W10	V_{SS}	Y20	V_{SS}
P2	V_{SS}	V1	NTrcData2	W11	SysAD1	Y21	V_{SS}
P3	V_{SS}	V2	NTrcEnd	W12	V_{DD}	AA1	V_{SS}
P4	V_{SS}	V3	V_{SS}	W13	SysAD35	AA2	V_{SS}
P18	V_{DD}	V4	V_{SS}	W14	V_{SS}	AA3	V_{DD}IO
P19	V_{DD}	V5	V_{SS}PA2	W15	SysAD38	AA4	V_{DD}IO
P20	V_{DD}	V6	V_{SS}	W16	V_{DD}	AA5	V_{DD}PA1
P21	SysAD46	V7	V_{DD}IO	W17	SysAD9	AA6	V_{DD}IO
R1	DivMode0	V8	V_{DD}	W18	V_{SS}	AA7	IC
R2	DivMode1	V9	JTMS	W19	V_{SS}	AA8	JTDO
R3	DivMode2	V10	V_{SS}	W20	V_{DD}IO	AA9	DrvCon
R4	V_{DD}IO	V11	SysAD33	W21	V_{DD}IO	AA10	V_{SS}
R18	SysAD44	V12	V_{DD}	Y1	V_{SS}	AA11	SysAD0
R19	SysAD13	V13	SysAD4	Y2	V_{SS}	AA12	SysAD2
R20	SysAD45	V14	V_{SS}	Y3	V_{DD}IO	AA13	SysAD34
R21	SysAD14	V15	SysAD7	Y4	V_{DD}IO	AA14	SysAD36
T1	V_{DD}	V16	V_{DD}	Y5	V_{SS}PA1	AA15	SysAD5
T2	V_{DD}	V17	SysAD41	Y6	SysClock	AA16	SysAD6
T3	V_{DD}	V18	V_{SS}	Y7	JTRST#	AA17	SysAD8
T4	V_{DD}	V19	V_{SS}	Y8	V_{DD}	AA18	V_{DD}IO
T18	V_{SS}	V20	V_{DD}IO	Y9	JTCK	AA19	V_{DD}IO
T19	V_{SS}	V21	V_{DD}IO	Y10	V_{SS}	AA20	V_{SS}
T20	V_{SS}	W1	V_{DD}IO	Y11	SysAD32	AA21	V_{SS}

Caution Leave the IC pin open.

Remark # indicates active low.

- 208-pin plastic QFP (fine pitch) (28 × 28)

★ μPD30550AGD-300-WML, μPD30550AGD-300-WML-A, μPD30550AGD-350-WML, μPD30550AGD-350-WML-A



PIN NAMES

BigEndian:	Big endian	PReq#:	Processor request
BKTGIO#:	Break/trigger input/output	RdRdy#:	Read ready
BusMode[Note 1]:	Bus mode	Release#:	Release
ColdReset#:	Cold reset	Reset#:	Reset
DisDValidO#:	Disable delay ValidOut#	RMode#:	Reset mode
DivMode(2:0):	Divide mode	SysAD(63:0)[Note 2]:	System address/data bus
DrvCon:	Driver control	SysADC(7:0)[Note 3]:	System address/data check bus
DWBTrans#:	Doubleword block transfer		
ExtRqst#:	External request	SysClock:	System clock
IC	Internally connected	SysCmd(8:0):	System command/data identifier bus
Int(5:0)#:	Interrupt		
JTCK:	JTAG clock	SysID(2:0)[Note 1]:	System bus identifier
JTDI:	JTAG data input	TIntSel:	Timer interrupt selection
JTDO:	JTAG data output	ValidIn#:	Valid input
JTMS:	JTAG mode select	ValidOut#:	Valid output
JTRST#:	JTAG reset	V_{DD}:	Power supply for CPU core
NMI#:	Non-maskable interrupt	V_{DD}IO:	Power supply for I/O
NTrcClk:	N-Trace clock	V_{DD}PA1, V_{DD}PA2:	Quiet V_{DD} for PLL
NTrcData(3:0) :	N-Trace data output	V_{SS}:	Ground
NTrcEnd:	N-Trace end	V_{SS}PA1, V_{SS}PA2:	Quiet V_{SS} for PLL
O3Return#[Note 1]:	Out-of-Order Return mode	WrRdy#:	Write ready

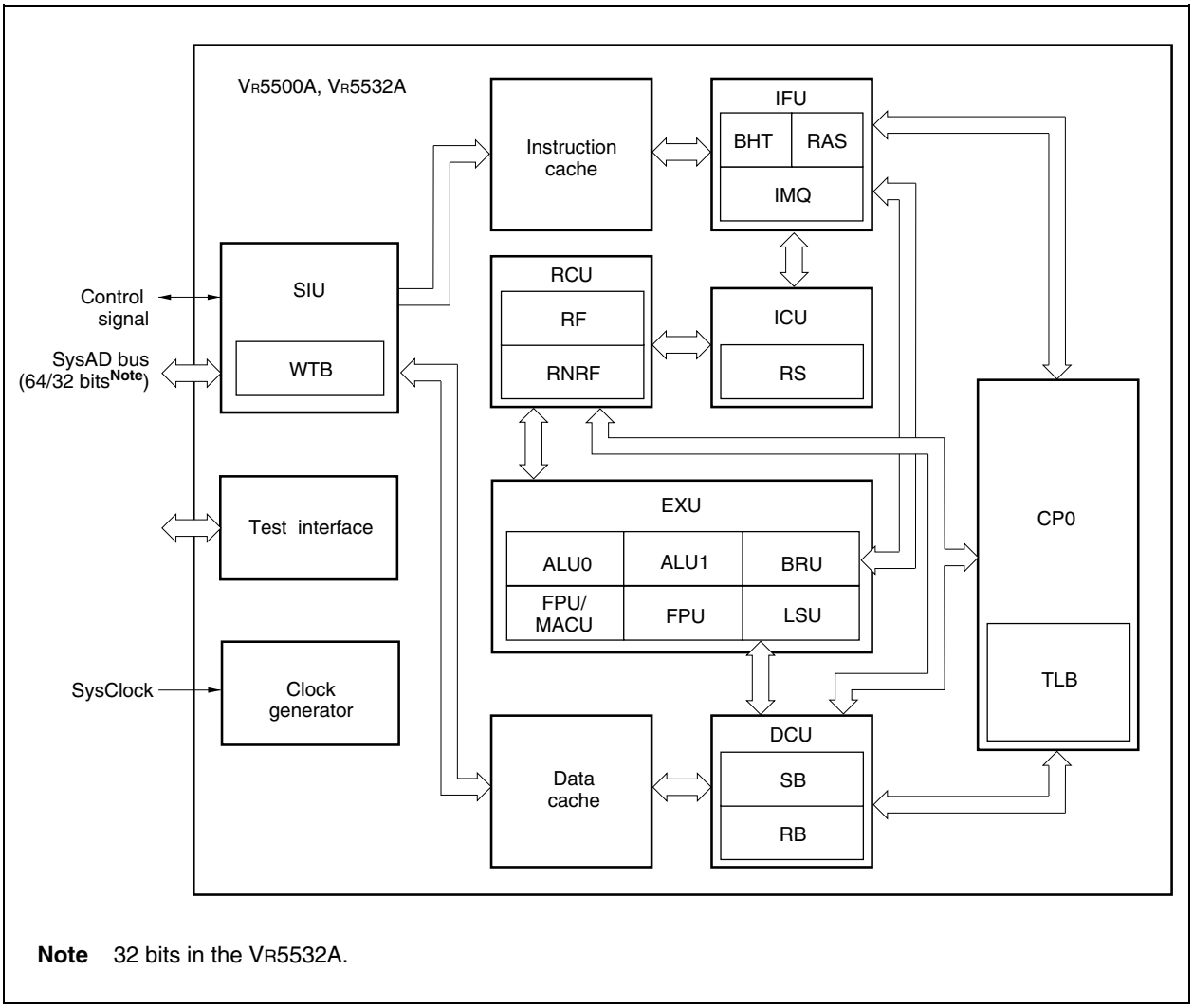
Notes 1. VR5500A only.

2. In the VR5500A. SysAD(31:0) in the VR5532A.

3. In the VR5500A. SysADC(3:0) in the VR5532A.

Remark # indicates active low.

INTERNAL BLOCK DIAGRAM



Note 32 bits in the VR5532A.

CONTENTS

1. PIN FUNCTIONS

Remark # indicates active low.

1.1 List of Pin Functions

Caution Unless otherwise specified, the VR5500A is treated as the representative model throughout this chapter.

(1) System interface signals

Pin Name	I/O	Function
SysAD(63:0)[Note1]	I/O	System address/data bus A 64-bit bus for communication between the processor and external agent. The lower 32 bits (SysAD(31:0)) are used in 32-bit bus mode.
SysADC(7:0)[Note1]	I/O	System address/data check bus A bus for SysAD bus parity. Valid only during a data cycle. The lower 4 bits (SysADC(3:0)) are used in 32-bit bus mode.
SysCmd(8:0)	I/O	System command/data ID bus A 9-bit bus that transfers command and data identifiers between the processor and external agent
SysID(2:0)[Note 2]	I/O	System bus protocol ID These signals transfer request identifiers in the out-of-order return mode. The processor drives a valid identifier in synchronization with the activation of the ValidOut# signal. The external agent must drive valid identifiers in synchronization with the activation of the ValidIn# signal.
ValidIn#	Input	Valid In A signal indicating that the external agent is driving a valid address or data onto the SysAD bus, a valid command or data identifier onto the SysCmd bus, or a valid request identifier onto the SysID bus in the out-of-order return mode.
ValidOut#	Output	Valid out A signal indicating that the processor is driving a valid address or data onto the SysAD bus, a valid command or data identifier onto the SysCmd bus, or a valid request identifier onto the SysID bus in the out-of-order return mode.
RdRdy#	Input	Read ready A signal indicating that the external agent is ready to accept a processor read request
WrRdy#	Input	Write ready A signal indicating that the external agent is ready to accept a processor write request
ExtRqst#	Input	External request A signal indicating that the external agent is requesting the right to use the system interface
Release#	Output	Releases interface A signal indicating that the processor is releasing the system interface to a slave state
PReq#	Output	Processor request A signal indicating that the processor has a request that is pending

Notes 1. In the VR5500A. SysAD(31:0), SysADC(3:0) in the VR5532A.

2. VR5500A only.

(2) Initialization interface signals (1/2)

Pin Name	I/O	Function
DivMode(2:0)	Input	Division mode These signals set the division ratio of PClock and SysClock as follows: 111: 5.5 110: 5 101: 4.5 100: 4 011: 3.5 010: 3 001: 2.5 000: 2 Set the input levels of these signals before a power-on reset. Make sure that the levels of these signals do not change while the VR5500A is operating.
BigEndian	Input	Endian mode This signal sets the byte ordering for addressing. 1: Big endian 0: Little endian Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change while the VR5500A is operating.
BusMode[Note]	Input	Bus mode This signal sets the bus width of the system interface. 1: 64 bits 0: 32 bits Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change while the VR5500A is operating.
TIntSel	Input	Interrupt source select This signal sets the interrupt source to be assigned to the IP7 bit of the Cause register. 1: Timer interrupt 0: Int5# input and external write request (SysAD5) Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change while the VR5500A is operating.
DisDValidO#	Input	ValidOut# delay enable 1: ValidOut# is active even while the address cycle is stalled 0: ValidOut# is active during the address issuance cycle only Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change while the VR5500A is operating.
DWBTrans#	Input	Doubleword block transfer enable (valid in 32-bit bus mode only) 1: Disabled 0: Enabled Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change while the VR5500A is operating.

Note VR5500A only.

Remark 1: High level, 0: Low level

(2/2)

Pin Name	I/O	Function
O3Return#[Note]	Input	Out-of-Order Return mode This signal sets the protocol of the system interface. 1: Normal mode 0: Out-of-order return mode Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change while the VR5500A is operating.
ColdReset#	Input	Cold reset This signal completely initializes the internal status of the processor. Deassert it in synchronization with SysClock.
Reset#	Input	Reset This signal logically initializes the internal status of the processor. Deassert it in synchronization with SysClock.
DrvCon	Input	Drive control This signal sets the impedance of the external output driver. 1: Low 0: Normal (recommended) Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change while the VR5500A is operating.

Note VR5500A only.

Remark 1: High level, 0: Low level

The O3Return#[Note], DWBTrans#, DisDValidO#, and BusMode[Note] signals are used for determining the protocol of the system interface. The protocol is selected as follows in accordance with the setting of these signals.

Note VR5500A only.

[VR5500A bus protocol]

Protocol	O3Return#	DWBTrans#	DisDValidO#	BusMode
VR5000 compatible	1	1	1	1
RM523x compatible	1	1	1	0
VR5432 native mode compatible	1	0	0	0
Out-of-order return mode	0	Arbitrary	Arbitrary	Arbitrary

[VR5532A bus protocol]

Protocol	DWBTrans#	DisDValidO#
RM523x compatible	1	1
VR5432 native mode compatible	0	0

Remark 1: High level, 0:Low level
RM523x is a product of PMC-Sierra, Inc.

(3) Interrupt interface signals

Pin Name	I/O	Function
Int(5:0)#	Input	Interrupt These are general-purpose processor interrupt requests. The input states can be checked by the Cause register. Whether Int5# is acknowledged or not depends on the status of the TIntSel signal during reset.
NMI#	Input	Non-maskable interrupt This is the non-maskable interrupt request.

(4) Clock interface signals

Pin Name	I/O	Function
SysClock	Input	System clock Clock input to the processor
V_{DD}PA1 V_{DD}PA2	–	V_{DD} for PLL Power supply for the internal PLL
V_{SS}PA1 V_{SS}PA2	–	V_{SS} for PLL Ground for the internal PLL

(5) Power supply

Pin Name	I/O	Function
V_{DD}	–	Power supply pin for core
V_{DD}IO	–	Power supply pin for I/O
V_{SS}	–	Ground potential pin

Caution The V_R5500A uses two power supply pins. These power supply pins can be applied in any sequence. However, power must not be applied to one pin for 100 ms or longer while it is not applied to the other.

(6) Test interface signals

Pin Name	I/O	Function
NTrcData(3:0)	Output	Trace data Trace data output
NTrcEnd	Output	Trace end A signal that indicates the end of a trace data packet.
NTrcClk	Output	Trace clock Clock for the test interface. The same clock as SysClock is output.
RMode#/ BKTGIO#	I/O	Reset mode/break trigger I/O A debug reset mode input signal while the JTRST# signal is active. It serves as a break or trigger I/O signal during normal operation.
JTDI	Input	JTAG data input Serial data input for JTAG
JTDO	Output	JTAG data output Serial data output for JTAG. Output is performed in synchronization with the fall of JTCK.
JTMS	Input	JTAG mode select This signal selects the JTAG test mode.
JTCK	Input	JTAG clock input Serial clock input for JTAG. The maximum frequency is 33 MHz. There is no need for it to be synchronized with SysClock.
JTRST#	Input	JTAG reset input A signal for initializing the JTAG test module.

1.2 Recommended Connection of Unused Pins

(1) System interface pins

(a) Unused pins in 32-bit bus mode (VR5500A only)

The VR5500A allows selection of a SysAD bus width from 64 bits or 32 bits. When the 32-bit bus mode is selected, the VR5500A operates using only the required system interface pins. Therefore, set the unused pins as follows when operating the VR5500A in the 32-bit bus mode.

Pin Name	Recommended Connection of Unused Pins
SysAD(63:32)	Leave open
SysADC(7:4)	Leave open

(b) Unused pins in normal mode (VR5500A only)

The VR5500A can process read/write transactions regardless of the order in which requests are issued in the out-of-order return mode. The SysID(2:0) signals are used to identify each request during this processing. Set these signals, which are not used in the normal mode, as follows.

Pin Name	Recommended Connection of Unused Pins
SysID(2:0)	Leave open

(c) Parity bus

The VR5500A and VR5532A allow selection of whether the data is protected using parity. When parity is used, the parity data is output from the processor or external agent to the SysADC bus.

However, whether the parity is used or not is selected by software, so unless the program is started, the VR5500A and VR5532A cannot determine the operation of the SysADC bus. Therefore, care must be taken to prevent the SysADC bus from being left open or in a high-impedance state.

When parity is not used, it is recommended to connect each pin of the SysADC bus to VDDIO via a resistor with a high resistance value.

(2) Test interface pins

The VR5500A and VR5532A can be used to perform testing and debugging with the device mounted on the board. The test interface pins are used for connection with the external debug tool during such debugging. Therefore set the test interface pins as follows when the debug function is not used and in the normal operation mode.

Pin Name	Recommended Connection of Unused Pins
JTCK	Pull up
JTDI	Pull up
JTMS	Pull up
JTRST#	Pull down
JTDO	Leave open
NTrcClk	Leave open
NTrcData(3:0)	Leave open
NTrcEnd	Leave open
RMode#/BKTGIO#	Pull up

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}IO$		−0.5 to +4.6	V
	V_{DD}		−0.5 to +2.0	V
	$V_{DD}P$		−0.5 to +2.0	V
Input voltage[Note]	V_I		−0.5 to $V_{DD}IO$ + 0.3	V
		Pulse of less than 7 ns	−1.5 to $V_{DD}IO$ + 1.0	V
Operating case temperature	T_C		−10 to +85	°C
Storage temperature	T_{stg}		−40 to +125	°C

Note The upper limit of the input voltage ($V_{DD}IO$ + 0.3) is +4.6 V.

Cautions 1. Do not short-circuit two or more outputs at the same time.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics sections are the ranges within which the product can normally operate and the quality can be guaranteed.

Operating Conditions

(1) 300 MHz product (V_R5500A, V_R5532A), 350 MHz product (V_R5532A only)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Supply voltage	$V_{DD}IO$		2.375	2.625	V
			3.135	3.465	V
	V_{DD}		1.425	1.575	V
	$V_{DD}P$		1.425	1.575	V

Caution In the V_R5500A, V_{DD} can also be used in the voltage range of the 400 MHz product (1.6 to 1.7 V). In this case, internal operation at 300 MHz is guaranteed. The supply current of the core block in this case is the specified value of the 400 MHz product (MAX. 1.68 A).

(2) 400 MHz product (V_R5500A only)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Supply voltage	V_{DD}IO		2.375	2.625	V
			3.135	3.465	V
	V_{DD}		1.6	1.7	V
	V_{DD}P		1.6	1.7	V

Caution V_{DD} can also be used with the voltage range of the 300 MHz product (1.425 to 1.575 V). In this case, internal operation at 300 MHz is guaranteed. The supply current of the core block in this case is the specified value of the 300 MHz product (MAX. 1.25 A).

Supply Current

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Supply current of core block	I_{DD}	V_R5500A	300 MHz product, during normal operation, V_{DD} = V_{DD}P = 1.575 V		1.25	A
			400 MHz product, during normal operation, V_{DD} = V_{DD}P = 1.7 V		1.68	A
		V_R5532A	300 MHz product, during normal operation, V_{DD} = V_{DD}P = 1.575 V		1.25	A
			350 MHz product, during normal operation, V_{DD} = V_{DD}P = 1.575 V		1.40	A
	I_{DD}_sb	V_R5500A	300 MHz product, in standby mode, V_{DD} = V_{DD}P = 1.575 V		0.25	A
			400 MHz product, in standby mode, V_{DD} = V_{DD}P = 1.7 V		0.31	A
		V_R5532A	300 MHz product, in standby mode, V_{DD} = V_{DD}P = 1.575 V		0.25	A
			350 MHz product, in standby mode, V_{DD} = V_{DD}P = 1.575 V		0.28	A

Remark The supply current in the I/O block varies depending on the application used. It is normally 20% I_{DD} or lower.

DC Characteristics

(1) When $V_{DD}IO$ = 2.5 V ±5%

(300 MHz product: T_C = −10 to +85°C, $V_{DD}IO$ = 2.5 V ±5%, V_{DD} = $V_{DD}P$ = 1.5 V ±5%) (V_R5500A, V_R5532A)

(350 MHz product: T_C = −10 to +85°C, $V_{DD}IO$ = 2.5 V ±5%, V_{DD} = $V_{DD}P$ = 1.5 V ±5%) (V_R5532A only)

(400 MHz product: T_C = −10 to +85°C, $V_{DD}IO$ = 2.5 V ±5%, V_{DD} = $V_{DD}P$ = 1.6 to 1.7 V) (V_R5500A only)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V_{OH}	$V_{DD}IO$ = MIN., I_{OH} = −4 mA	0.8 × $V_{DD}IO$		V
Output voltage, low	V_{OL}	$V_{DD}IO$ = MIN., I_{OL} = 4 mA		0.4	V
Input voltage, high[Note 1]	V_{IH}		2.0	$V_{DD}IO$ + 0.3	V
		Pulse of less than 7 ns	2.0	$V_{DD}IO$ + 1.0	V
Input voltage, low[Note 1]	V_{IL}		−0.5	0.2 × $V_{DD}IO$	V
		Pulse of less than 7 ns	−1.5	0.2 × $V_{DD}IO$	V
Input voltage, high[Note 2]	V_{IHC}		0.8 × $V_{DD}IO$	$V_{DD}IO$ + 0.3	V
		Pulse of less than 7 ns	0.8 × $V_{DD}IO$	$V_{DD}IO$ + 1.0	V
Input voltage, low[Note 2]	V_{ILC}		−0.5	0.2 × $V_{DD}IO$	V
		Pulse of less than 7 ns	−1.5	0.2 × $V_{DD}IO$	V
Input current leakage, high	I_{LIH}	V_I = $V_{DD}IO$		5.0	μA
Input current leakage, low	I_{LIL}	V_I = 0 V		−5.0	μA
Output current leakage, high	I_{LOH}	V_O = $V_{DD}IO$		5.0	μA
Output current leakage, low	I_{LOL}	V_O = 0 V		−5.0	μA

Notes 1. Does not apply to the SysClock pin.

2. Only applies to the SysClock pin.

(2) When $V_{DD}IO$ = 3.3 V ±5%

(300 MHz product: T_C = −10 to +85°C, $V_{DD}IO$ = 3.3 V ±5%, V_{DD} = $V_{DD}P$ = 1.5 V ±5%) (V_R5500A, V_R5532A)

(350 MHz product: T_C = −10 to +85°C, $V_{DD}IO$ = 3.3 V ±5%, V_{DD} = $V_{DD}P$ = 1.5 V ±5%) (V_R5532A only)

(400 MHz product: T_C = −10 to +85°C, $V_{DD}IO$ = 3.3 V ±5%, V_{DD} = $V_{DD}P$ = 1.6 to 1.7 V) (V_R5500A only)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V_{OH}	$V_{DD}IO$ = MIN., I_{OH} = −4 mA	2.4		V
Output voltage, low	V_{OL}	$V_{DD}IO$ = MIN., I_{OL} = 4 mA		0.4	V
Input voltage, high[Note 1]	V_{IH}		2.0	$V_{DD}IO$ + 0.3	V
		Pulse of less than 7 ns	2.0	$V_{DD}IO$ + 1.0	V
Input voltage, low[Note 1]	V_{IL}		−0.5	0.8	V
		Pulse of less than 7 ns	−1.5	0.8	V
Input voltage, high[Note 2]	V_{IHC}		0.8 × $V_{DD}IO$	$V_{DD}IO$ + 0.3	V
		Pulse of less than 7 ns	0.8 × $V_{DD}IO$	$V_{DD}IO$ + 1.0	V
Input voltage, low[Note 2]	V_{ILC}		−0.5	0.2 × $V_{DD}IO$	V
		Pulse of less than 7 ns	−1.5	0.2 × $V_{DD}IO$	V
Input current leakage, high	I_{LIH}	V_I = $V_{DD}IO$		5.0	μA
Input current leakage, low	I_{LIL}	V_I = 0 V		−5.0	μA
Output current leakage, high	I_{LOH}	V_O = $V_{DD}IO$		5.0	μA
Output current leakage, low	I_{LOL}	V_O = 0 V		−5.0	μA

Notes 1. Does not apply to the SysClock pin.

2. Only applies to the SysClock pin.

Power-on Sequence

The V_R5500A and V_R5532A use two power supply pins. These power supply pins can be applied in any sequence. However, power must not be applied to one pin for 100 ms or longer while it is not applied to the other.

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Power-on delay	t_{DF}		0	100	ms

Capacitance (T_A = 25°C, $V_{DD}IO$ = V_{DD} = $V_{DD}P$ = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{IN}	f_C = 1 MHz		5.0	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V		7.0	pF

AC Characteristics

(300 MHz product: T_C = –10 to +85°C, $V_{DD}IO$ = 2.5 V ±5%, 3.3 V ±5%, V_{DD} = $V_{DD}P$ = 1.5 V ±5%) (V_R5500A, V_R5532A)
(350 MHz product: T_C = –10 to +85°C, $V_{DD}IO$ = 2.5 V ±5%, 3.3 V ±5%, V_{DD} = $V_{DD}P$ = 1.5 V ±5%) (V_R5532A only)
(400 MHz product: T_C = –10 to +85°C, $V_{DD}IO$ = 2.5 V ±5%, 3.3 V ±5%, V_{DD} = $V_{DD}P$ = 1.6 to 1.7 V) (V_R5500A only)

Clock parameters (1/2)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
System clock high-level width	t_{CH}			1.8		ns
System clock low-level width	t_{CL}			1.8		ns
Pipeline clock frequency		300 MHz product (V_R5500A, V_R5532A)		200	300	MHz
		350 MHz product (V_R5532A only)		200	350	MHz
		400 MHz product (V_R5500A only)		200	400	MHz
System clock frequency[Note]		300 MHz product (V_R5500A)	DivMode = 2:1	100	133	MHz
			DivMode = 2.5:1	80	120	MHz
			DivMode = 3:1	66.7	100	MHz
			DivMode = 3.5:1	57.2	85.7	MHz
			DivMode = 4:1	50	75	MHz
			DivMode = 4.5:1	44.5	66.6	MHz
			DivMode = 5:1	40	60	MHz
			DivMode = 5.5:1	36.4	54.5	MHz
★		300 MHz product (V_R5532A)	DivMode = 2:1	100	100	MHz
			DivMode = 2.5:1	80	100	MHz
			DivMode = 3:1	66.7	100	MHz
			DivMode = 3.5:1	57.2	85.7	MHz
			DivMode = 4:1	50	75	MHz
			DivMode = 4.5:1	44.5	66.6	MHz
			DivMode = 5:1	40	60	MHz
			DivMode = 5.5:1	36.4	54.5	MHz
★		350 MHz product (V_R5532A only)	DivMode = 2:1	100	100	MHz
★			DivMode = 2.5:1	80	100	MHz
★			DivMode = 3:1	66.7	100	MHz
			DivMode = 3.5:1	57.2	100	MHz
			DivMode = 4:1	50	87.5	MHz
			DivMode = 4.5:1	44.5	77.7	MHz
			DivMode = 5:1	40	70	MHz
			DivMode = 5.5:1	36.4	63.6	MHz
		400 MHz product (V_R5500A only)	DivMode = 2:1	100	133	MHz
			DivMode = 2.5:1	80	133	MHz
			DivMode = 3:1	66.7	133	MHz
			DivMode = 3.5:1	57.2	114	MHz
			DivMode = 4:1	50	100	MHz
			DivMode = 4.5:1	44.5	88.8	MHz
			DivMode = 5:1	40	80	MHz
			DivMode = 5.5:1	36.4	72.7	MHz

Note This is the frequency at which the operation of the internal PLL is guaranteed.

Clock parameters (2/2)

	Parameter	Symbol	Conditions		MIN.	MAX.	Unit
	System clock cycle	t_{CP}	300 MHz product (VR5500A)	DivMode = 2:1	7.5	10	ns
				DivMode = 2.5:1	8.3	12.5	ns
				DivMode = 3:1	10	15	ns
				DivMode = 3.5:1	11.7	17.5	ns
				DivMode = 4:1	13.3	20	ns
				DivMode = 4.5:1	15	22.5	ns
				DivMode = 5:1	16.7	25	ns
				DivMode = 5.5:1	18.3	27.5	ns
★			300 MHz product (VR5532A)	DivMode = 2:1	10	10	ns
				DivMode = 2.5:1	10	12.5	ns
				DivMode = 3:1	10	15	ns
				DivMode = 3.5:1	11.7	17.5	ns
				DivMode = 4:1	13.3	20	ns
				DivMode = 4.5:1	15	22.5	ns
				DivMode = 5:1	16.7	25	ns
				DivMode = 5.5:1	18.3	27.5	ns
★			350 MHz product (VR5532A only)	DivMode = 2:1	10	10	ns
★				DivMode = 2.5:1	10	12.5	ns
★				DivMode = 3:1	10	15	ns
				DivMode = 3.5:1	10	17.5	ns
				DivMode = 4:1	11.4	20	ns
				DivMode = 4.5:1	12.8	22.5	ns
				DivMode = 5:1	14.2	25	ns
				DivMode = 5.5:1	15.7	27.5	ns
			400 MHz product (VR5500A only)	DivMode = 2:1	7.5	10	ns
				DivMode = 2.5:1	7.5	12.5	ns
				DivMode = 3:1	7.5	15	ns
				DivMode = 3.5:1	8.8	17.5	ns
				DivMode = 4:1	10	20	ns
				DivMode = 4.5:1	11.3	22.5	ns
				DivMode = 5:1	12.5	25	ns
				DivMode = 5.5:1	13.8	27.5	ns
	System clock jitter	t_J				±5	%
	System clock rise time	t_{CR}				1.2	ns
	System clock fall time	t_{CF}				1.2	ns
	JTAG clock frequency					33	MHz

Remarks 1. The system clock jitter is a cycle-to-cycle jitter.

2. The JTAG clock runs asynchronously to the system clock.

System interface parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data output hold time[Note 1]	t_{DM}		1.0		ns
Data output delay time[Note 1]	t_{DO}			5.0	ns
Data input setup time[Note 2]	t_{DS}		1.5		ns
Data input hold time[Note 2]	t_{DH}	300 MHz product (VR5500A, VR5532A)	1.0		ns
		350 MHz product (VR5532A only)	0.5		ns
		400 MHz product (VR5500A only)	0.5		ns

Notes 1. Applies to the Release#, ValidOut#, PReq#, SysAD(63:0), SysADC(7:0), SysCmd(8:0), and SysID(2:0) pins in the VR5500A.

Applies to the Release#, ValidOut#, PReq#, SysAD(31:0), SysADC(3:0), and SysCmd(8:0) pins in the VR5532A.

2. Applies to the ColdReset#, Reset#, Int(5:0)#, NMI#, ExtRqst#, RdRdy#, WrRdy#, ValidIn#, SysAD(63:0), SysADC(7:0), SysCmd(8:0), and SysID(2:0) pins in the VR5500A.

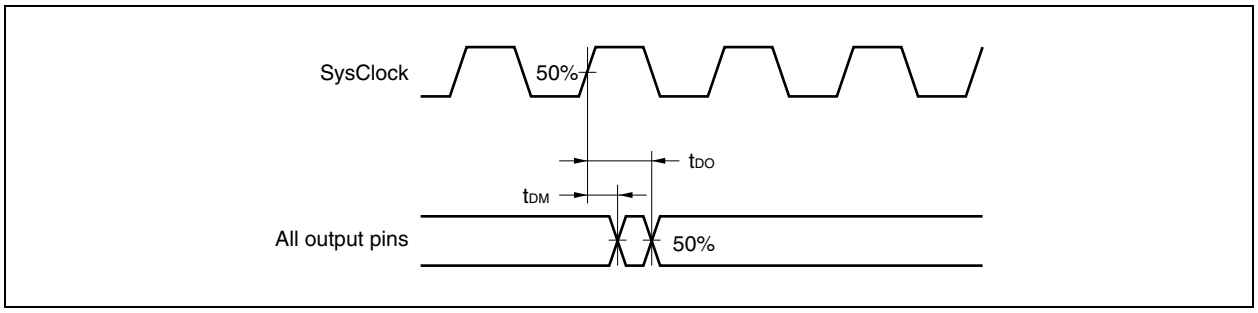
Applies to the ColdReset#, Reset#, Int(5:0)#, NMI#, ExtRqst#, RdRdy#, WrRdy#, ValidIn#, SysAD(31:0), SysADC(3:0), and SysCmd(8:0) pins in the VR5532A.

Load coefficient

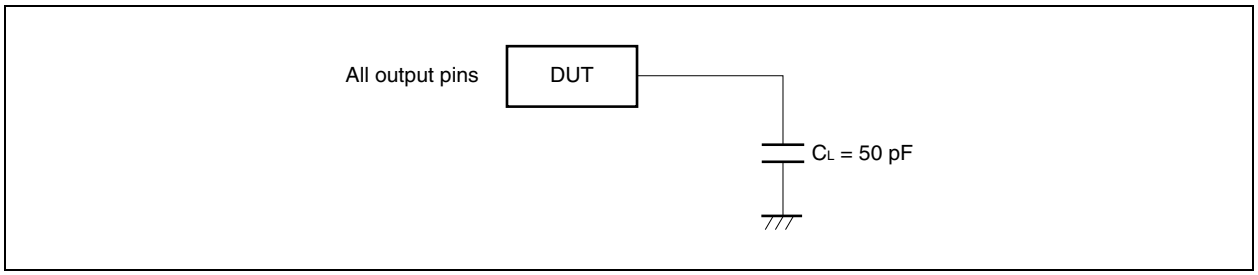
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Load coefficient	CLD			1.0	ns/25 pF

Measurement Conditions

Measurement points

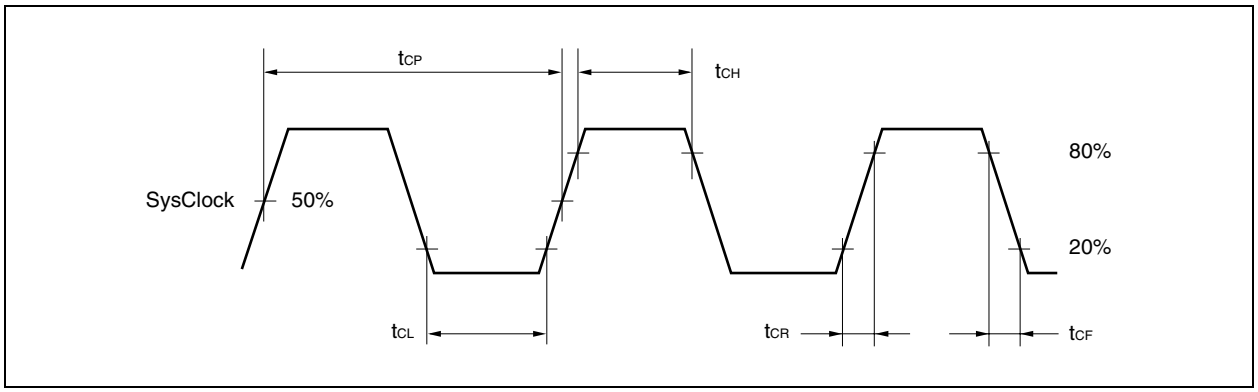


Load conditions

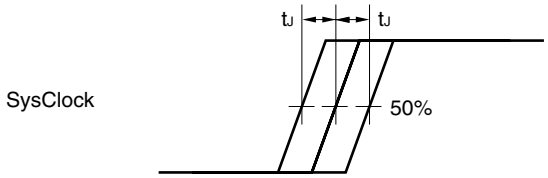


Timing Charts

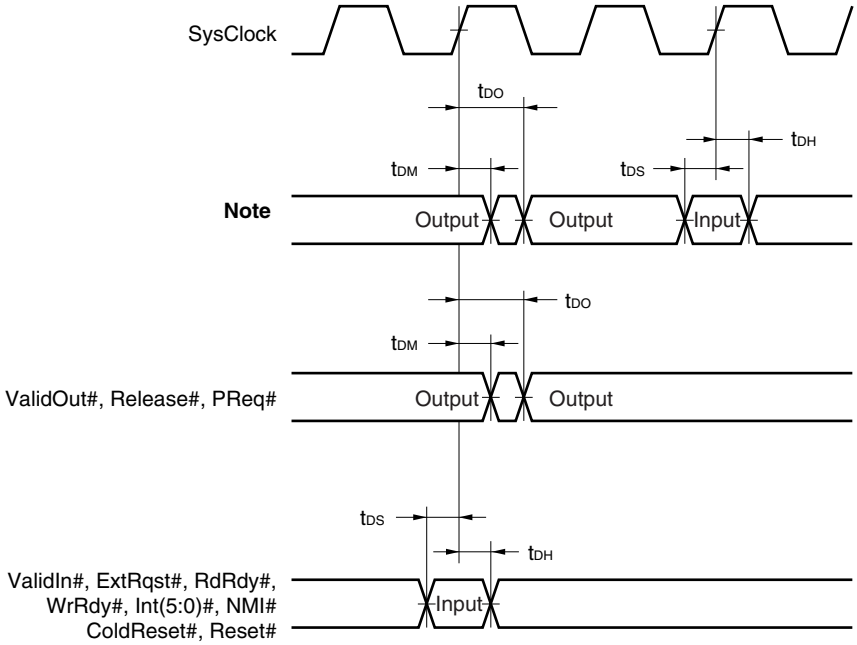
Clock timing



Clock jitter

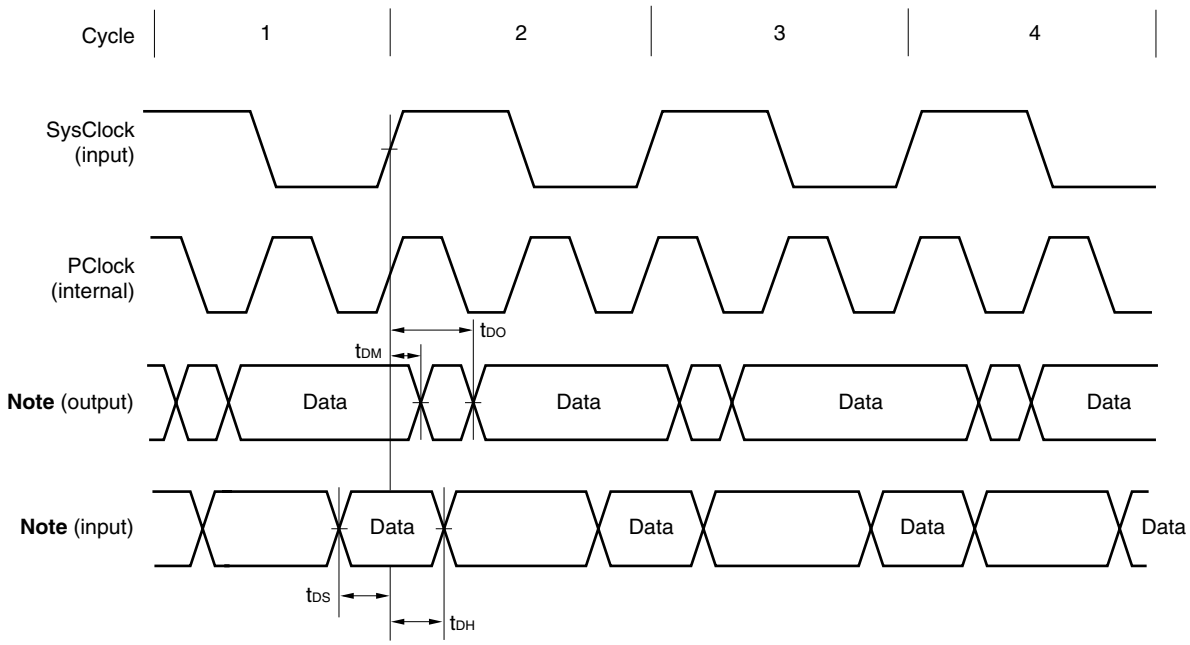


System interface edge timing



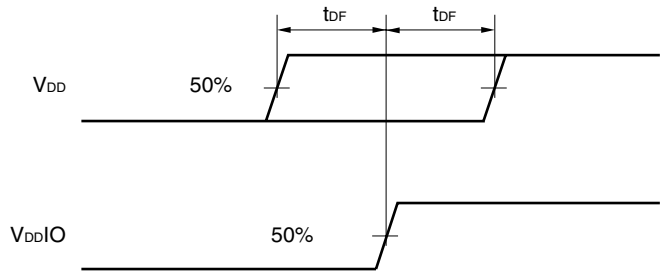
Note VR5500A: SysAD(63:0), SysADC(7:0), SysCmd(8:0), SysID(2:0)
VR5532A: SysAD(31:0), SysADC(3:0), SysCmd(8:0)

Clock relationships (DivMode = 2:1)



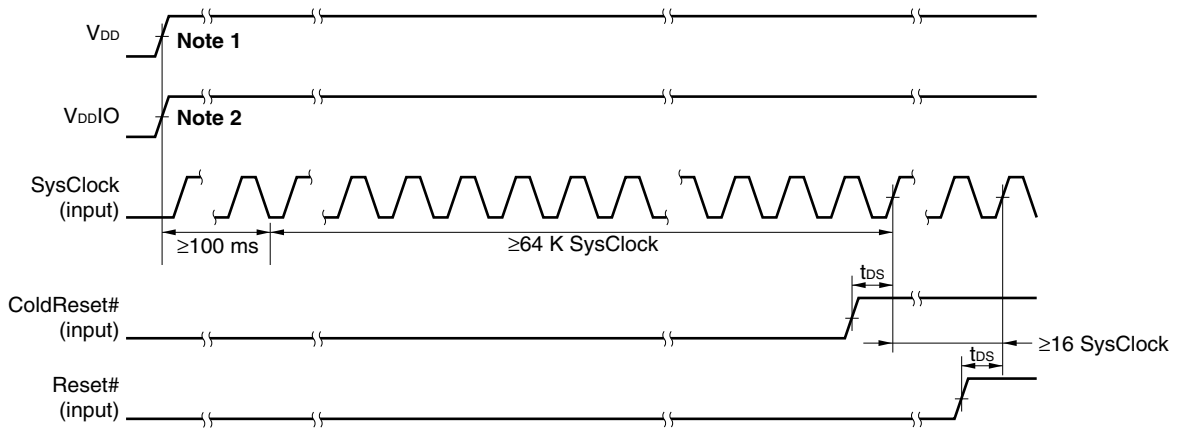
Note VR5500A: SysAD(63:0), SysADC(7:0), SysCmd(8:0), SysID(2:0)
VR5532A: SysAD(31:0), SysADC(3:0), SysCmd(8:0)

Power-on sequence



Reset timing

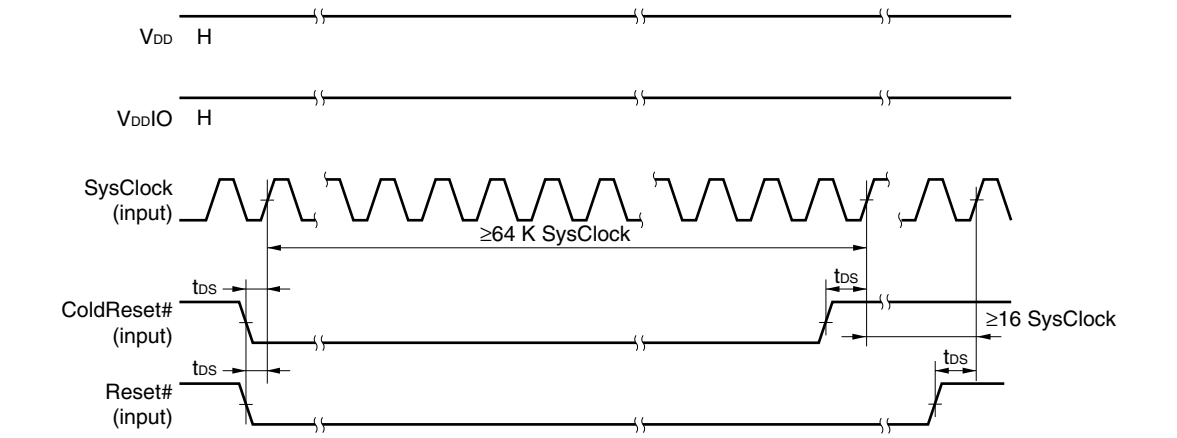
Power-on reset timing



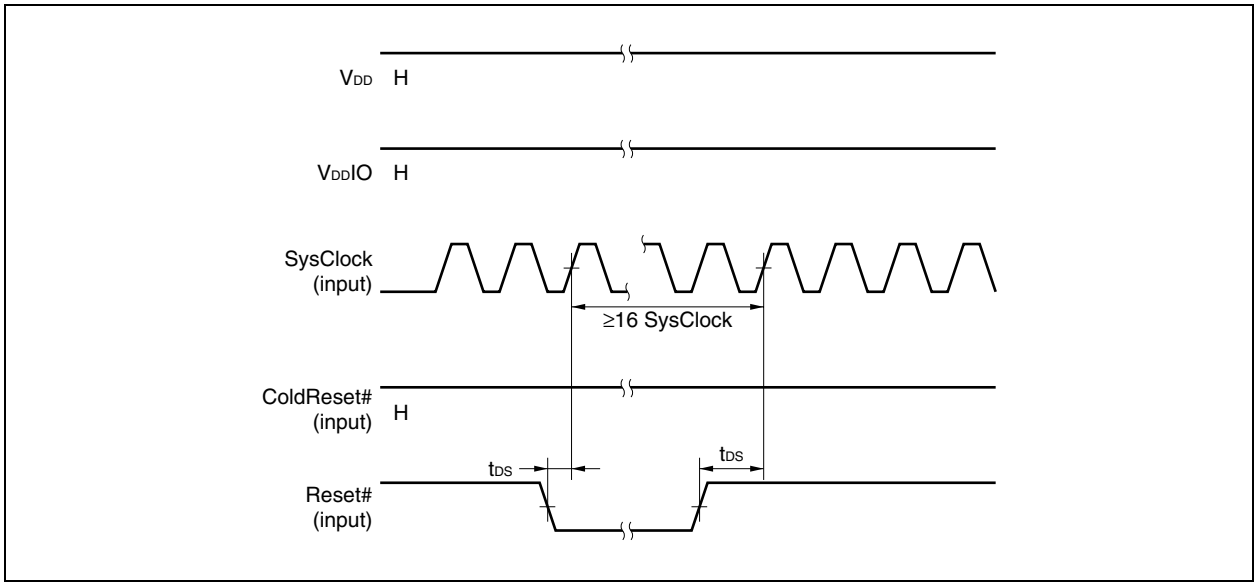
Notes 1. 1.425 V (300 MHz, 350 MHz product), 1.6 V (400 MHz product)

2. 2.375 V at 2.5 V operation or 3.135 V at 3.3 V operation

Cold reset timing

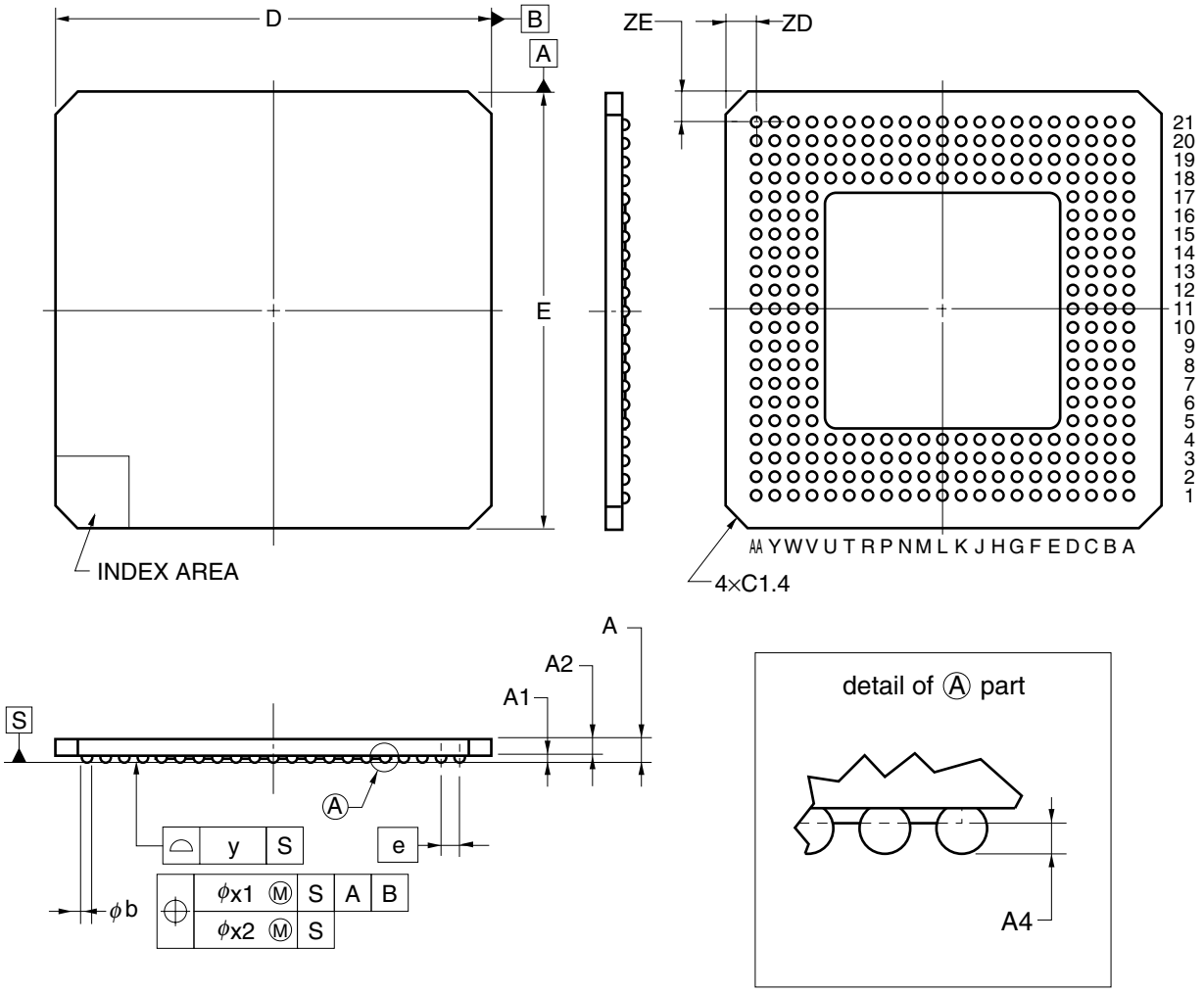


Warm reset timing



3. PACKAGE DRAWING

272-PIN PLASTIC BGA (CAVITY DOWN ADVANCED TYPE) (29x29)

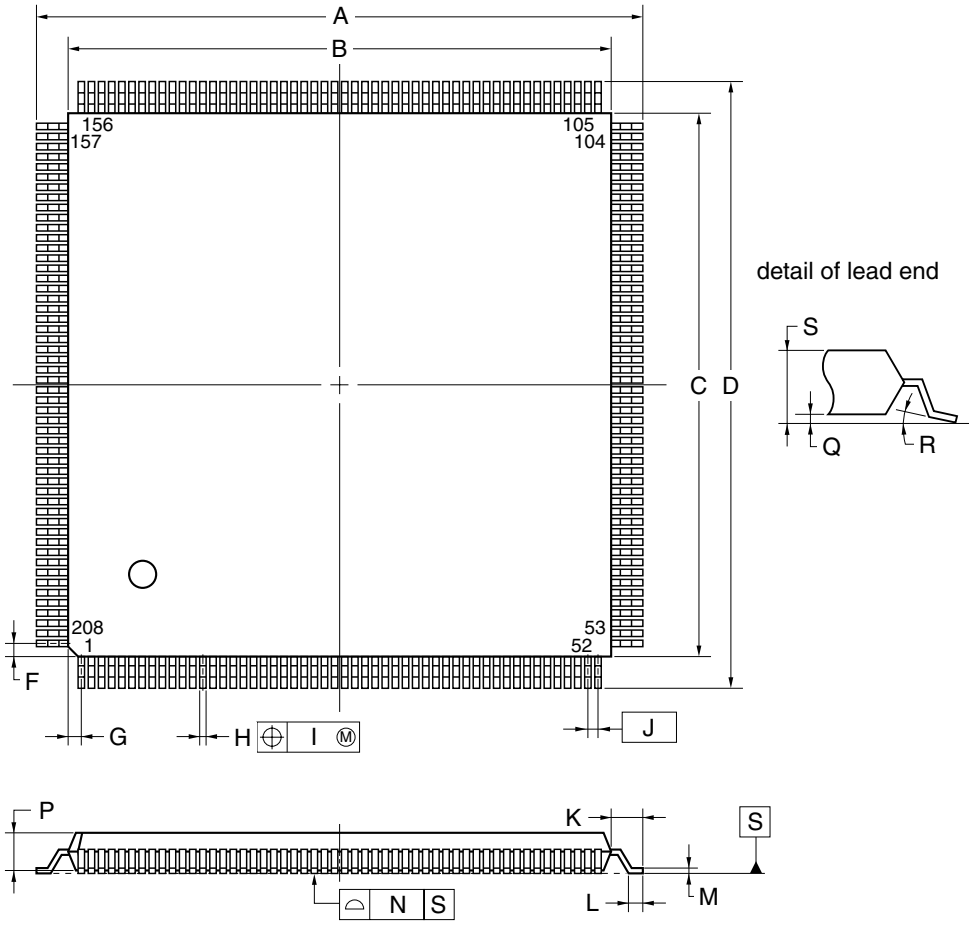


(unit:mm)

ITEM	DIMENSIONS
D	29.00±0.20
E	29.00±0.20
e	1.27
A	1.75±0.30
A1	0.60±0.10
A2	1.15
A4	0.25 MIN.
b	φ0.75±0.15
x1	0.30
x2	0.15
y	0.20
ZD	1.80
ZE	1.80

P272F2-127-NN1

208-PIN PLASTIC QFP (FINE PITCH) (28x28)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	30.6±0.2
B	28.0±0.2
C	28.0±0.2
D	30.6±0.2
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.3±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	3.2±0.1
Q	0.4±0.1
R	5°±5°
S	3.8 MAX.

P208GD-50-LML,MML,SML,WML-7

4. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 4-1. Surface mounting Type Soldering Conditions

(1) μPD30550AF2-300-NN1 : 272-pin plastic BGA (C/D advanced type) (29 × 29)
μPD30550AF2-300-NN1-A[Note 1] : 272-pin plastic BGA (C/D advanced type) (29 × 29)
μPD30550AF2-400-NN1 : 272-pin plastic BGA (C/D advanced type) (29 × 29)
μPD30550AF2-400-NN1-A[Note 1] : 272-pin plastic BGA (C/D advanced type) (29 × 29)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 250°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 3 days[Note 2] (after that, prebake at 125°C for 20 to 72 hours)	IR50-203-3[Note 3]

Notes 1. Lead-free product

2. After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

3. The IR50-203-3 conditions include the IR35-203-3 conditions, so the μPD30550AF2-300-NN1 and μPD30550AF2-400-NN1 can be soldered and mounted under the conventional IR35-203-3 conditions. For details of the IR35-203-3 conditions, contact an NEC Electronics sales representative.

★ **(2) μPD30550AGD-300-WML : 208-pin plastic QFP (fine pitch) (28 × 28)**
μPD30550AGD-300-WML-A[Note 1] : 208-pin plastic QFP (fine pitch) (28 × 28)
μPD30550AGD-350-WML : 208-pin plastic QFP (fine pitch) (28 × 28)
μPD30550AGD-350-WML-A[Note 1] : 208-pin plastic QFP (fine pitch) (28 × 28)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days[Note 2] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3

Notes 1. Lead-free product

2. After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

Reference document Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of Japanese version.

The related documents indicated in the publication may include preliminary versions. However, preliminary versions are not marked as such.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC Electronics product in your application, please contact the NEC Electronics office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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http://www.necel.com/en/support/support.html

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