



Regarding the usage of our schematics and alike documentation for Trenz module TE0712.

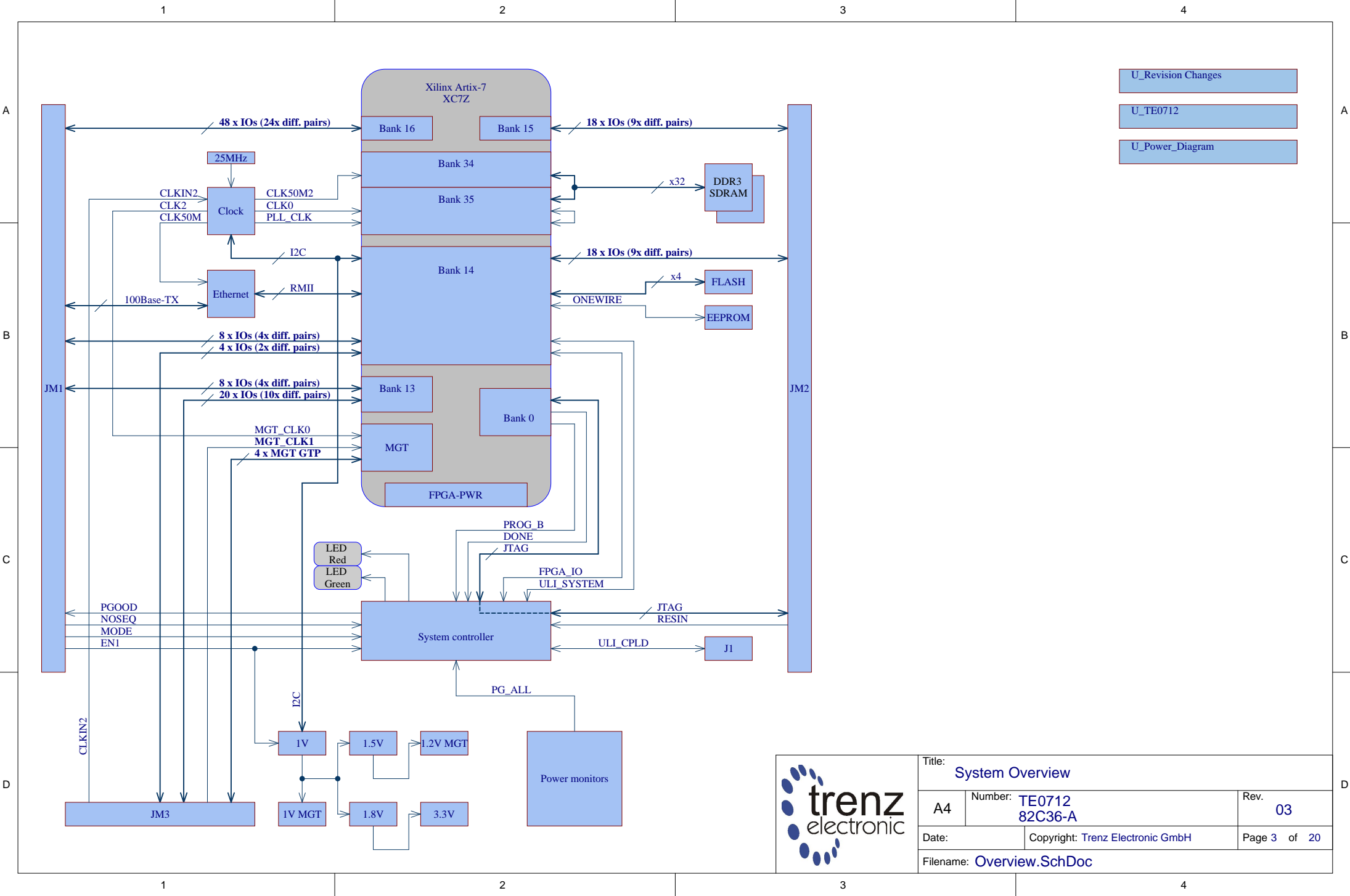
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Schematics and other handouts serve for informational purposes only!

	Title:		
	A4	Number: <b>TE0712</b> <b>82C36-A</b>	Rev. <b>03</b>
	Date: *	Copyright: Trenz Electronic GmbH / TT	Page 1 of 20
	Filename: <b>Legal Notices Modules.SchDoc</b>		

REV	Description	
-01	Initial revision	
-02		
-03	<p>1. Added Legal notices, project overview and revision changes. Updated page count and page order.</p> <p>2. Added a <a href="#">D3</a> diode between the <a href="#">INIT</a> and <a href="#">PROG_B</a> signals to keep the FPGA in the reset state while <a href="#">PROG_B</a> is low during the initial power-up.</p> <p>3. Resistors <a href="#">R2</a> , <a href="#">R68</a> replaced by 2K2 (were 4K87) to improve I2C stability at higher baud rates.</p> <p>4. Replaced obsolete ferrite beads BKP0603HS121-T to MPZ0603S121HT000.</p> <p>5. Revised power supply circuit. Replaced obsolete components:  - EN63A0QI - MPM869SGL-Z ( <a href="#">U14</a> );  - EP53F8QI - MPM3834CGPA ( <a href="#">U6</a> , <a href="#">U16</a> ).</p> <p>6. Replaced <a href="#">Q1</a> power switch TPS27082LDDCR by MP5077GG-Z.</p> <p>7. Added power monitors <a href="#">U10</a> , <a href="#">U11</a> STM6710LWB6F. U3.25 <a href="#">3.3V</a> signal replaced by <a href="#">PG_ALL</a>, generated by <a href="#">U10</a> , <a href="#">U11</a> power</p> <p>8. <a href="#">U14</a> I2C interface connected to bus <a href="#">PLL_SDA</a> / <a href="#">PLL_SCL</a> <a href="#">U1B</a> . Added table with device addresses on the I2C bus. A new device will be detected during a bus scan</p> <p>9. Capacitors <a href="#">C177</a> ,</p>	VY

	Title: <b>Revision History</b>		
	A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>
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	Drawn by: <b>VY</b>	Filename: <b>Revision Changes.SchDoc</b>	



U\_Revision Changes

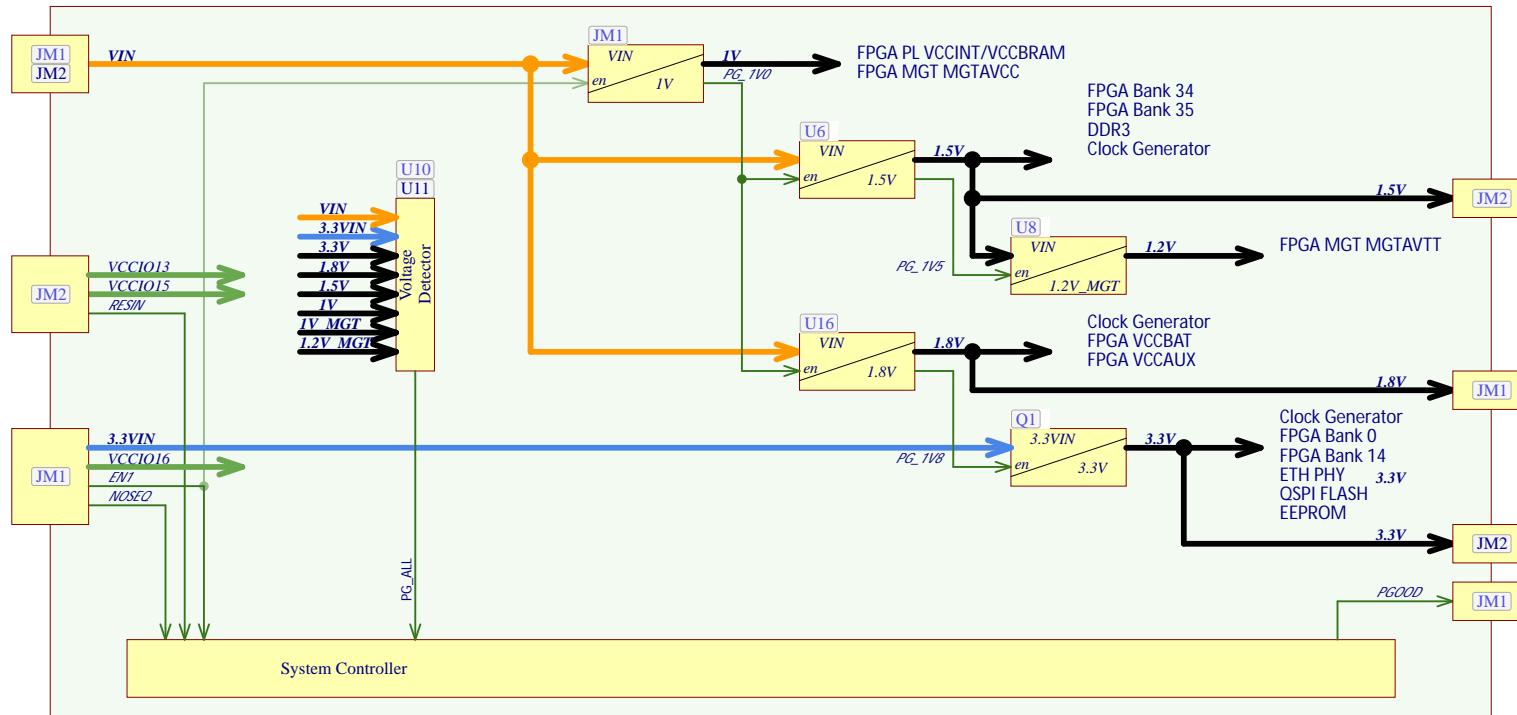
U\_TE0712

U\_Power\_Diagram



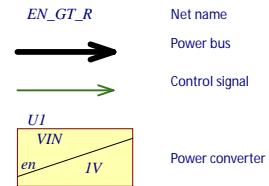
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A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>
Date:	Copyright: Trenz Electronic GmbH	Page 3 of 20
Filename: <b>Overview.SchDoc</b>		

## Power-on sequencing:



## Recommended Operating Conditions

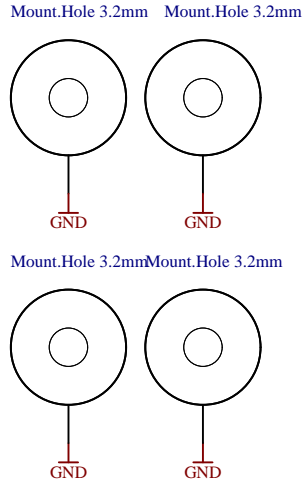
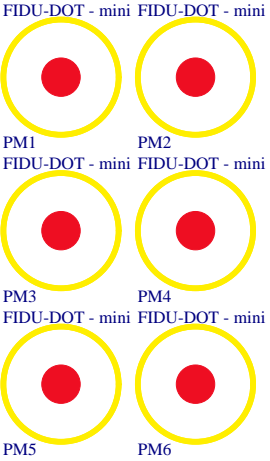
Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-5%	HR IO Bank13	-
VCCIO14	IN	3.3V	+/-5%	HR IO Bank14	Fixed
VCCIO15	IN	1.2 - 3.3V	+/-5%	HR IO Bank15	-
VCCIO16	IN	1.2 - 3.3V	+/-5%	HR IO Bank16	-
1.5V	OUT	1.5V	+/-5%	For Carrier card Periphery	-
1.8V	OUT	1.8V	+/-5%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-5%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-5%	For Carrier card Periphery	Connected to 3.3V



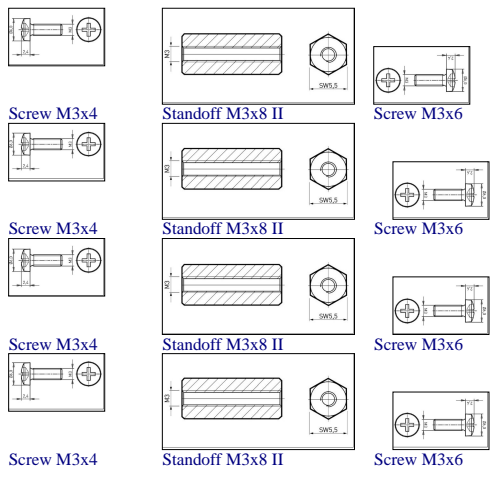
Title:		
A4	Number: 82C36-A	Rev. 03
Date: 27.10.2022	Copyright:	Page of
Filename: Power_Diagram.SchDoc		

Special notes:

- .
- .



Top of Board



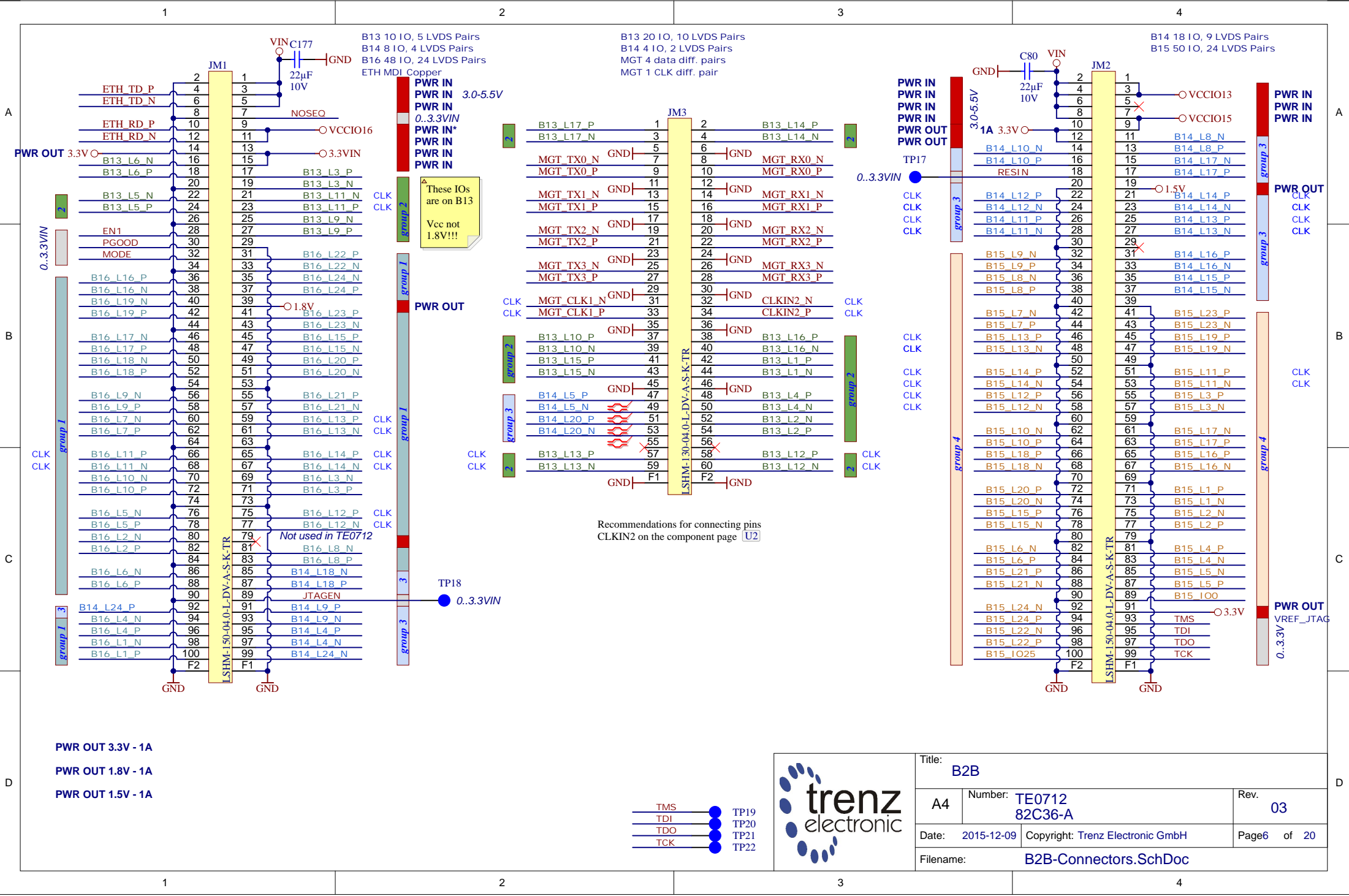
Serial  
 Serialnumber 6,3 x 6.3mm

Serial1  
 TE Address Overlay  
 LOGO ADDRESS

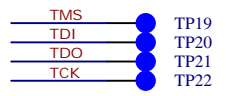
Assembly variant	82C36-A
Created by	MR
Modified by	MR
Modified at	2021-02-16
SVN Revision	14001



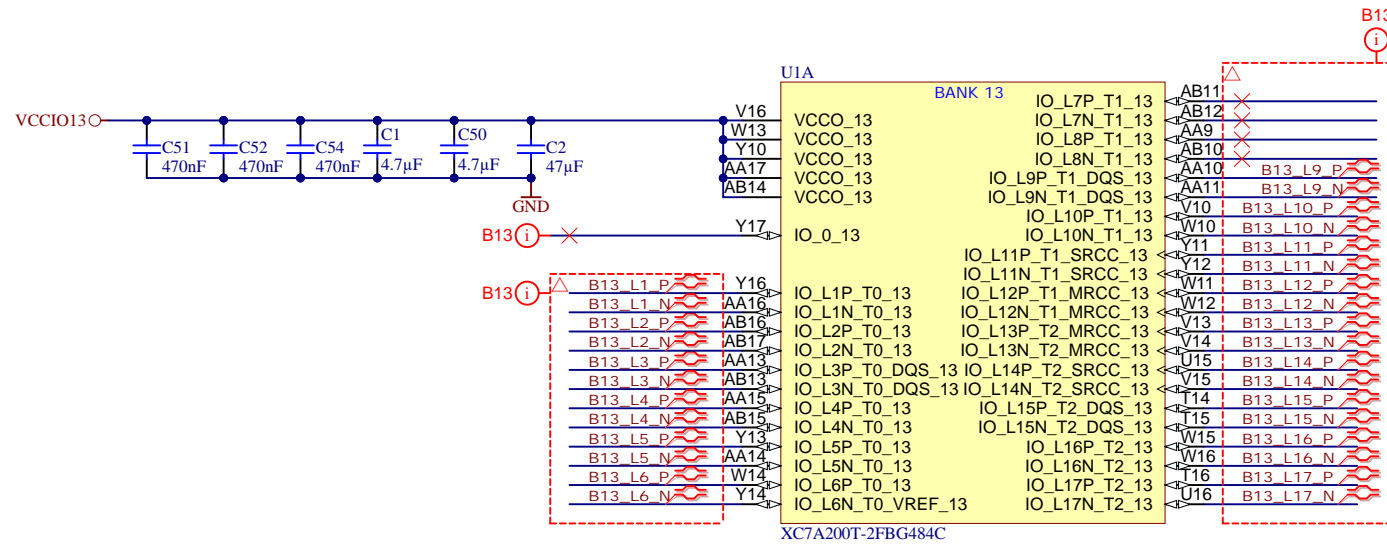
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A4	Number: TE0712 82C36-A	Rev. 03
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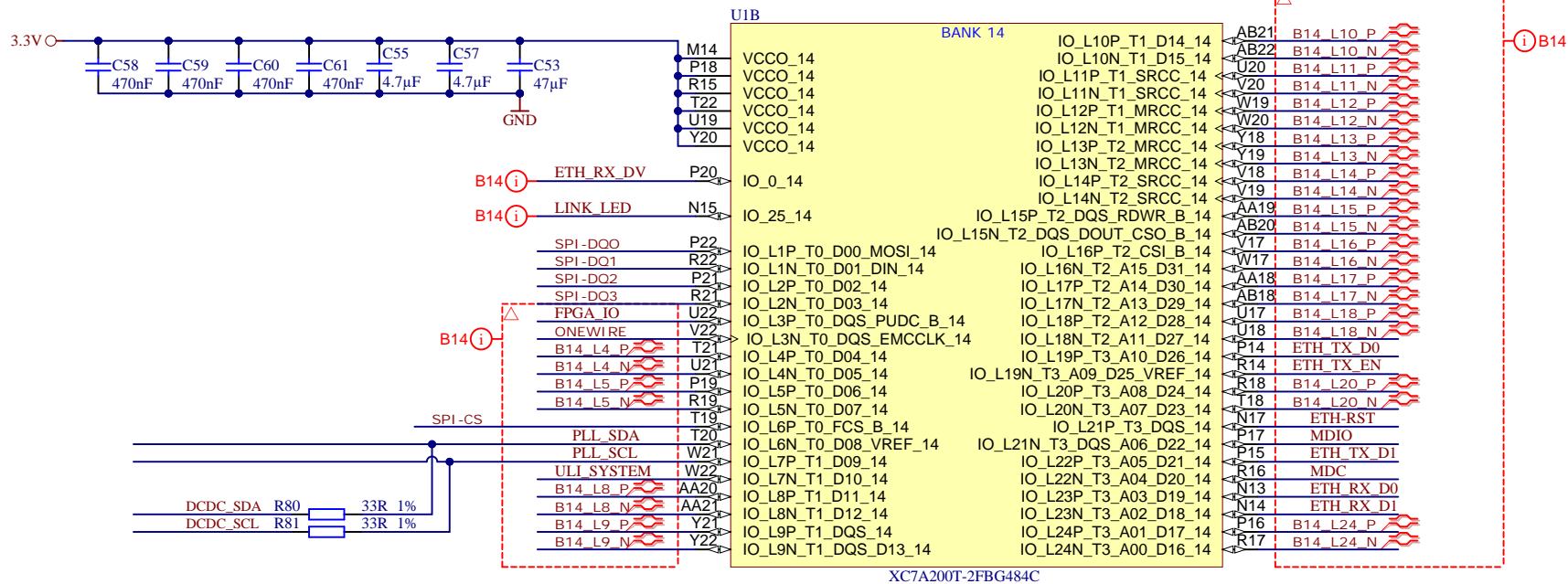
PWR OUT 3.3V - 1A  
PWR OUT 1.8V - 1A  
PWR OUT 1.5V - 1A



Title: B2B		
A4	Number: TE0712 82C36-A	Rev. 03
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Title: <b>B13</b>		
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Filename: <b>B13.SchDoc</b>		

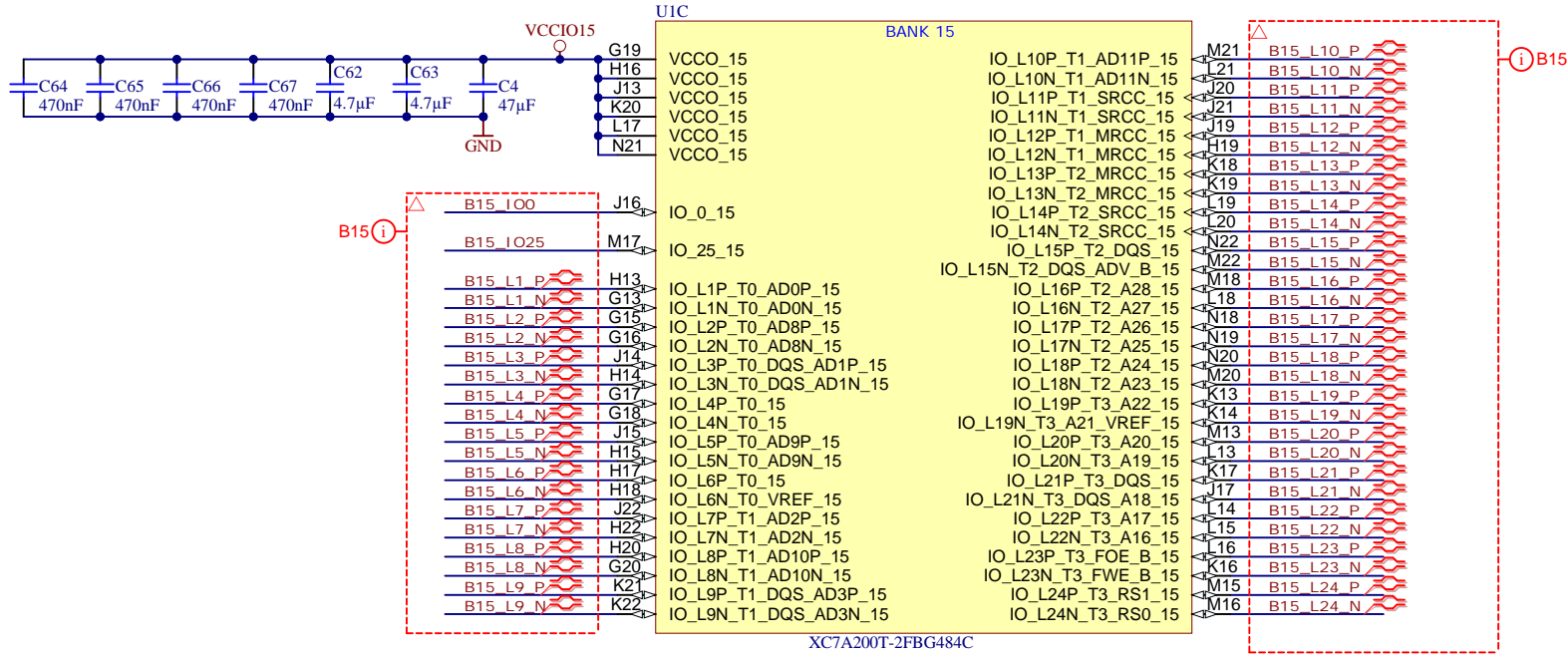


I2C bus addresses		
U1B	FPGA B14	h**
U2	Clock generator	h70
U14	DCDC VCCINT	h61



Title: <b>B14</b>		
A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>
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Filename: <b>B14.SchDoc</b>		

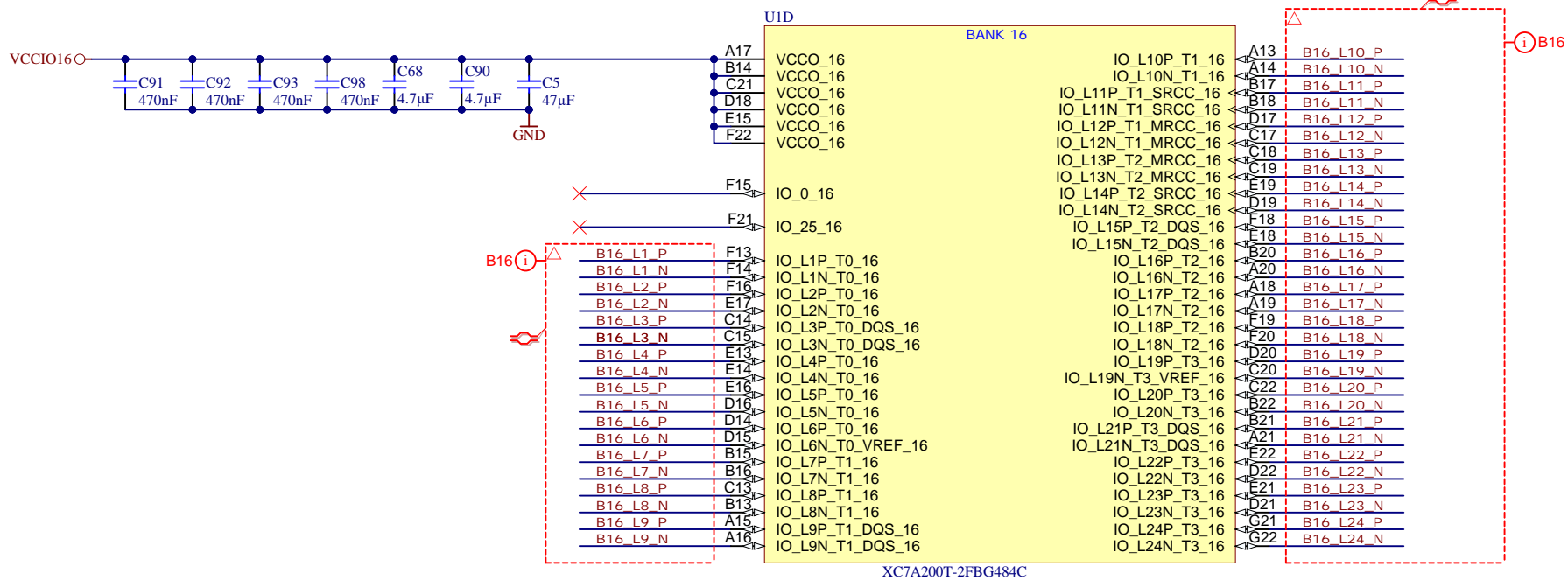





XC7A200T-2FBG484C



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A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>
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XC7A200T-2FBG484C

	Title: <b>B16</b>		
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	Filename: <b>B16.SchDoc</b>		

1

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3

4

A

A

B

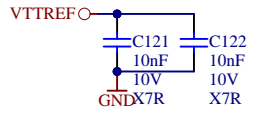
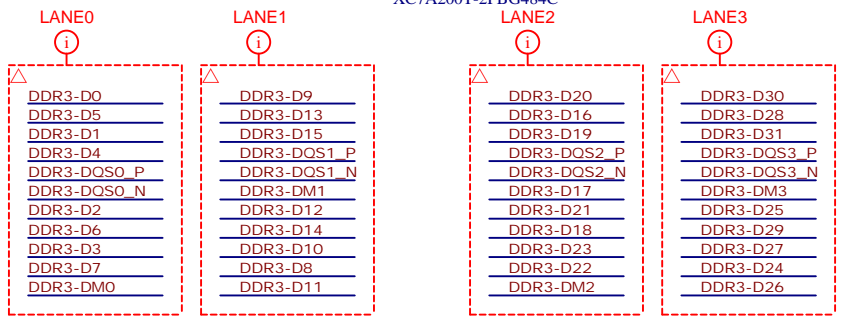
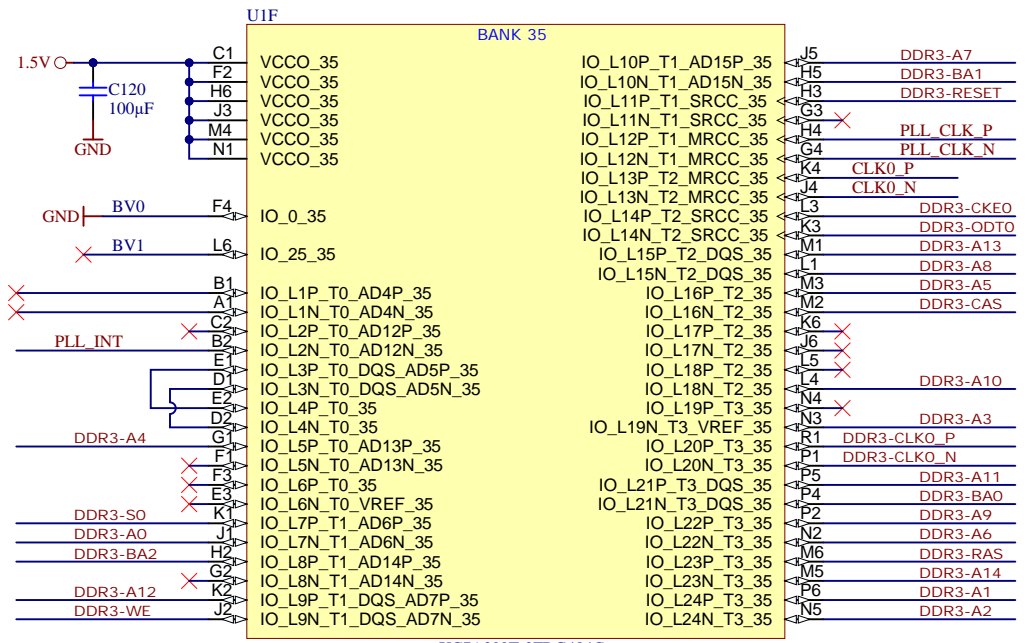
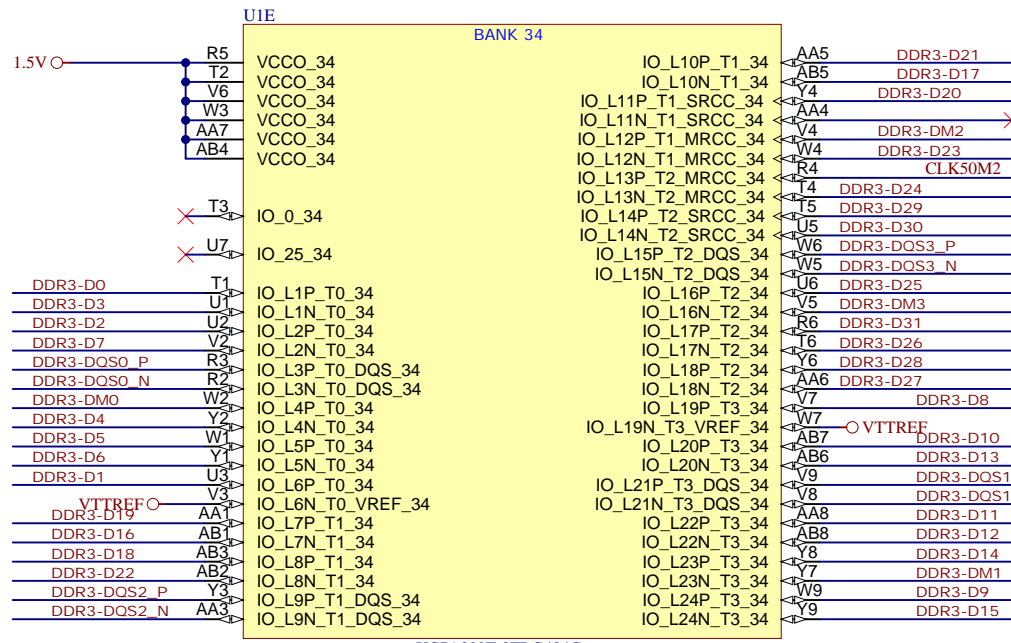
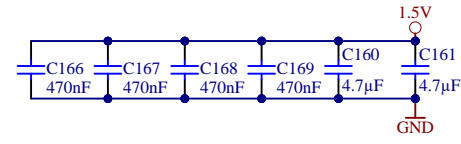
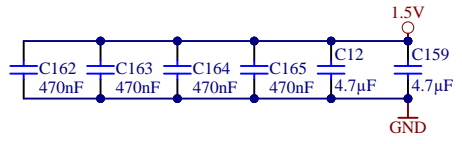
B

C

C

D

D



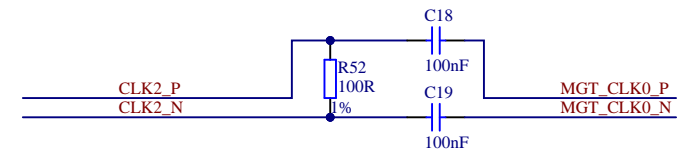
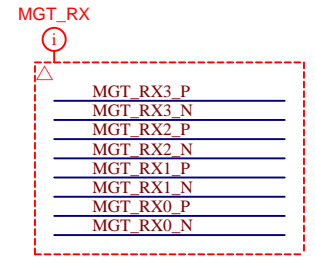
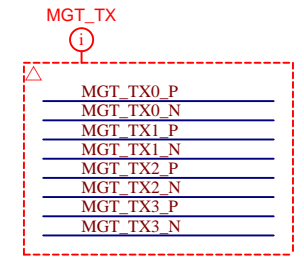
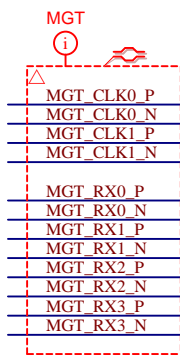
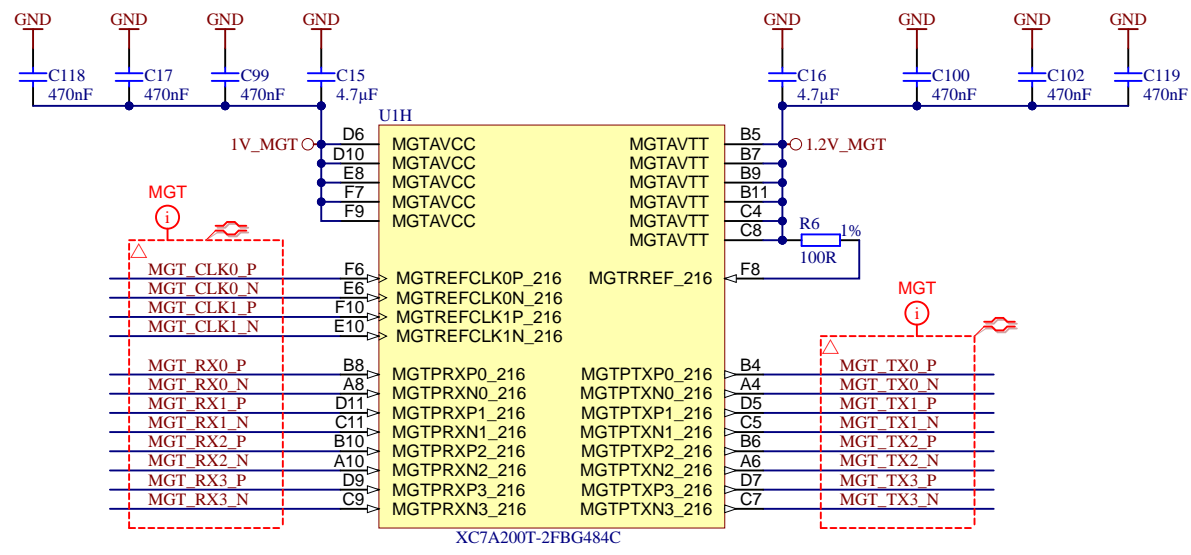
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A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>	
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Filename: <b>B34.SchDoc</b>			

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3

4

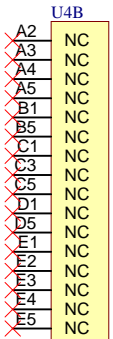
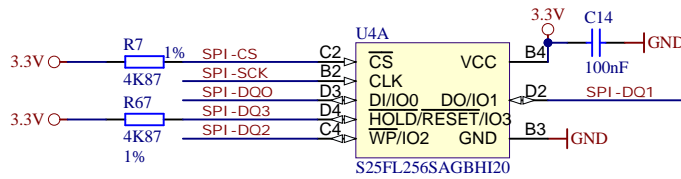
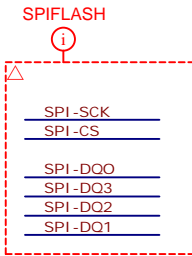
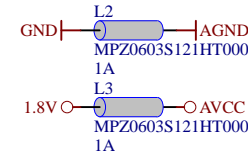
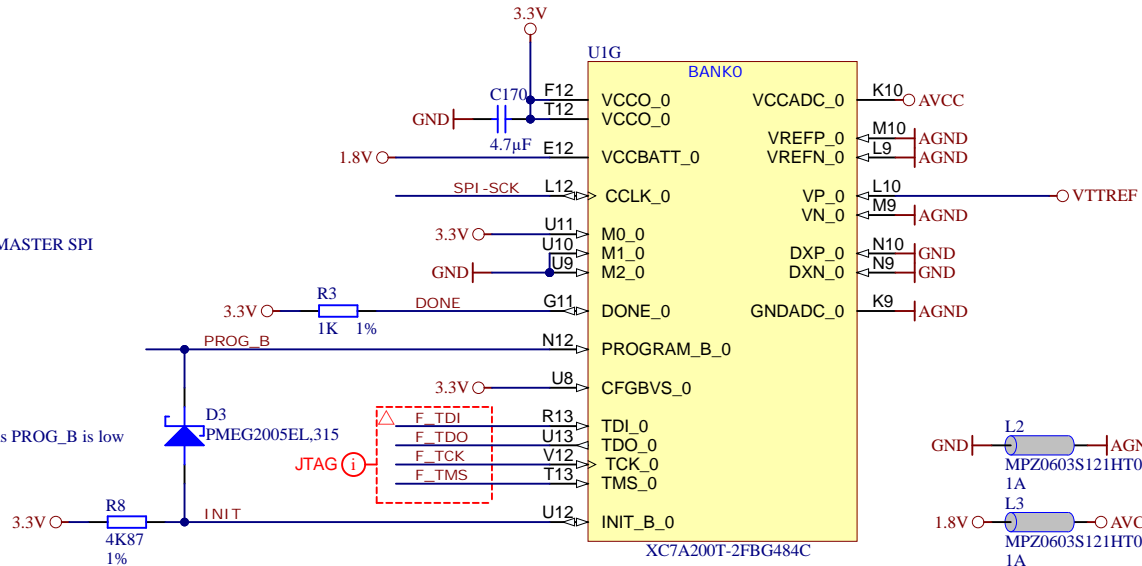


	Title: <b>MGT</b>		
	A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>
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BOOTMODE = MASTER SPI

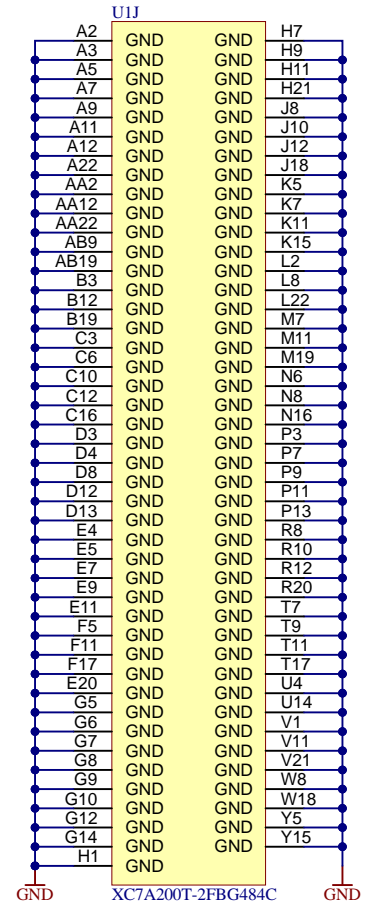
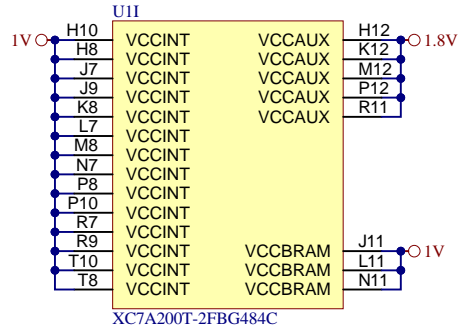
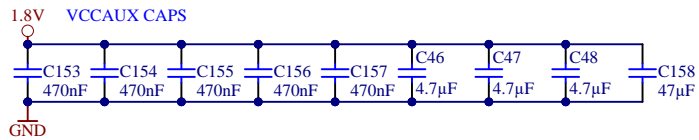
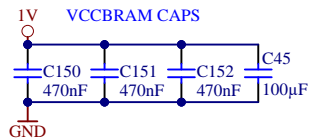
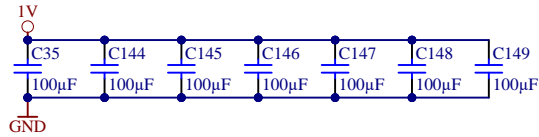
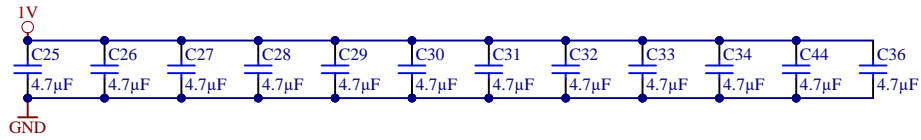
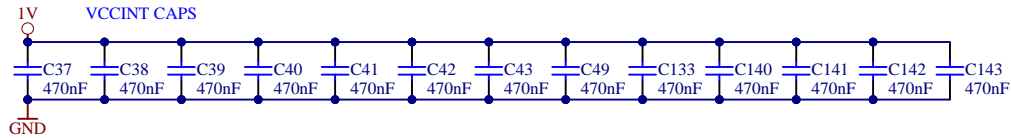
D3 keeps INIT low as long as PROG\_B is low



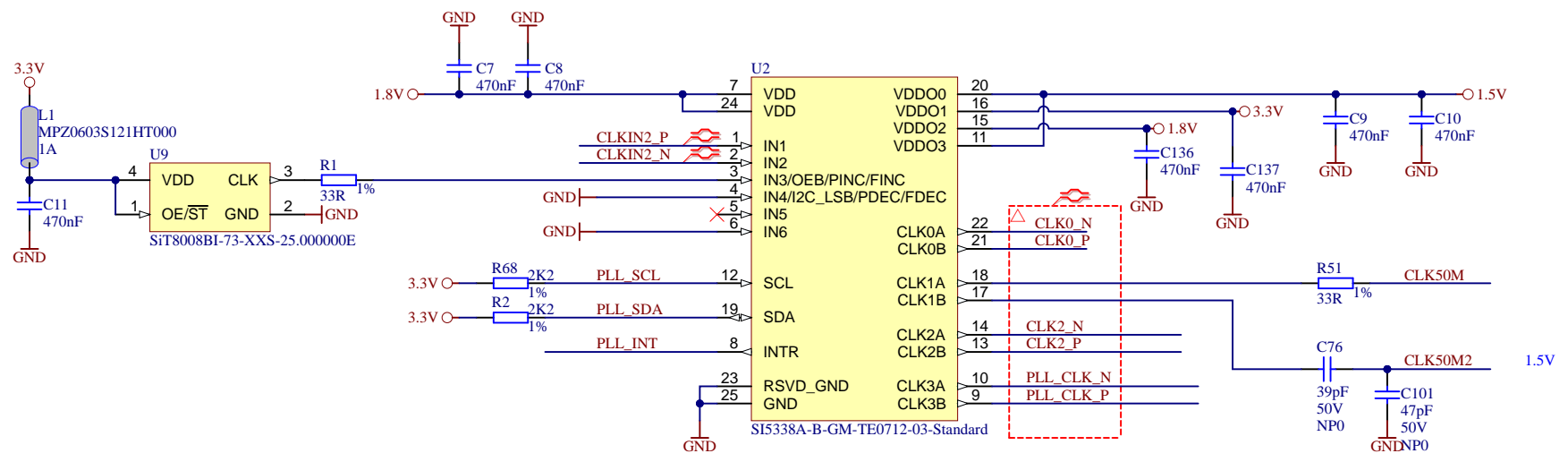
S25FL256SAGBH120



Title: CFG		
A4	Number: TE0712 82C36-A	Rev. 03
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Title: PWR		
A4	Number: TE0712 82C36-A	Rev. 03
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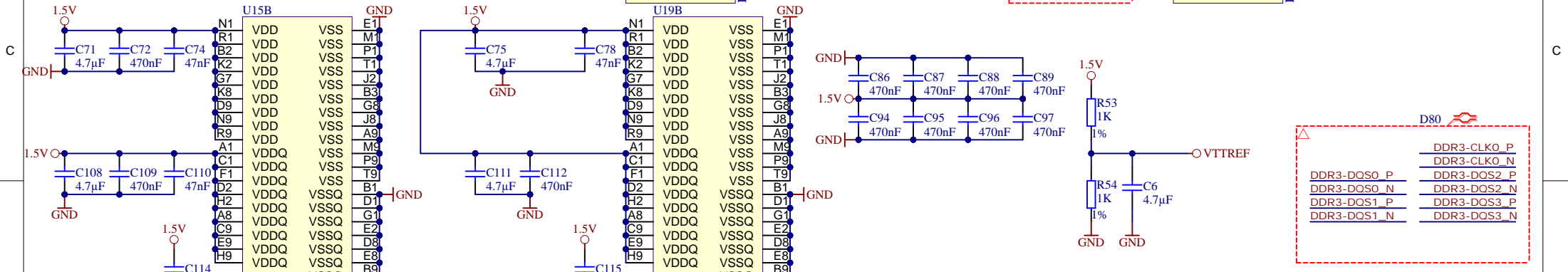
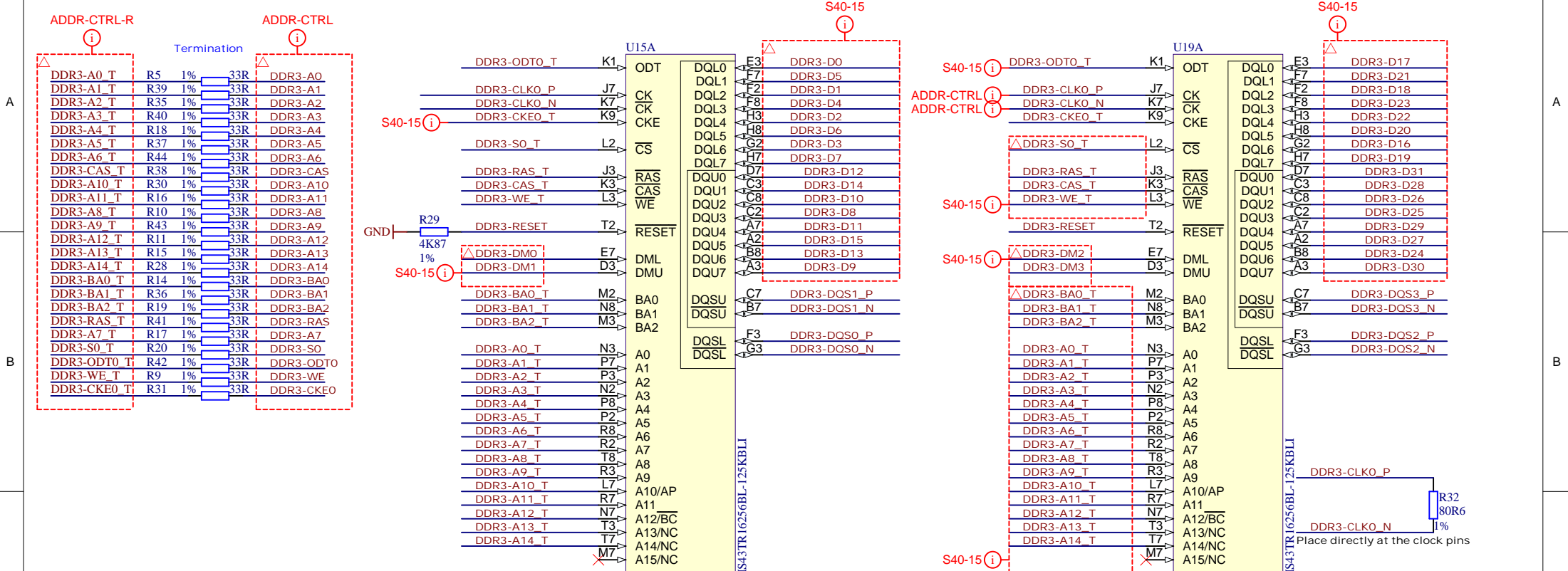
Datasheet SI5338:

IN1/IN2

These pins are used as the main differential clock input or as the XTAL input. See "3.2. Input Stage" on page 19, Figure 3 and Figure 4, for connection details. Clock inputs to these pins must be ac-coupled. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal.

When not in use, leave IN1 unconnected and IN2 connected to GND.

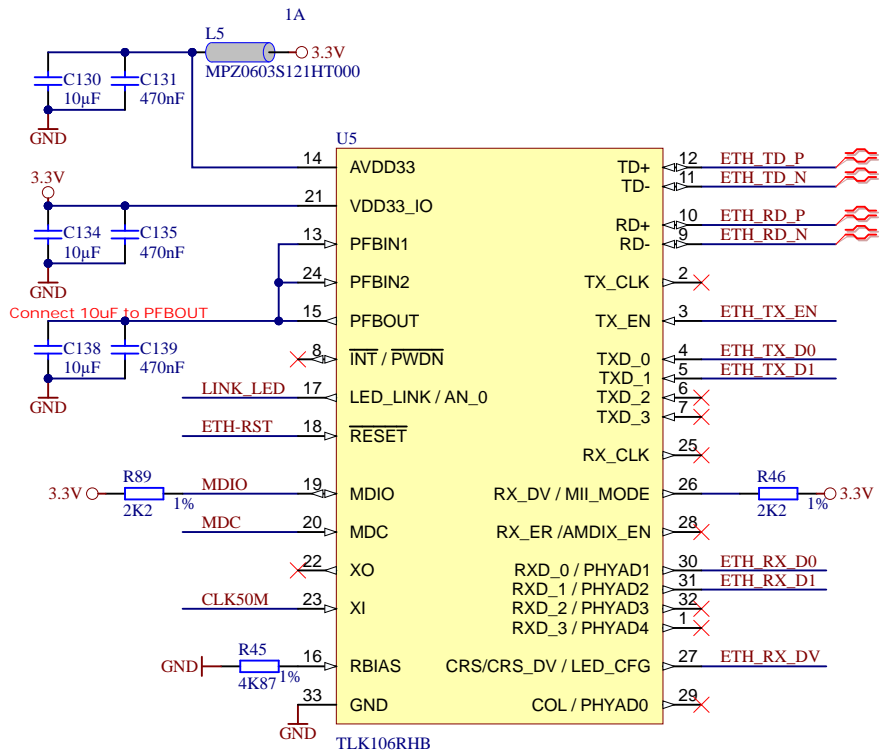
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	A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>
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	Filename: <b>Clock.SchDoc</b>		



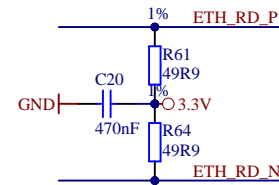
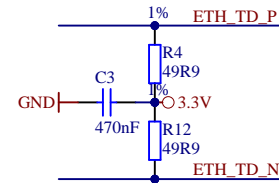
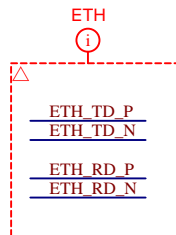
**Title: DDR3**

A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>
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Filename: <b>DDR3-RAM.SchDoc</b>		Page 16 of 20

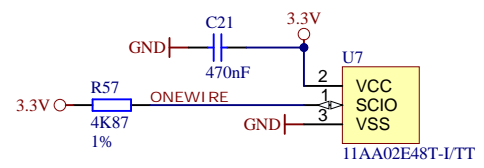
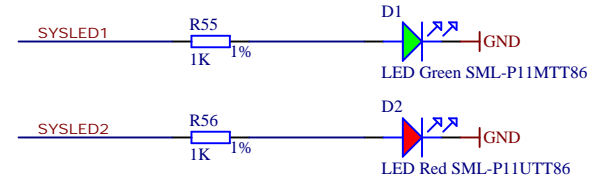
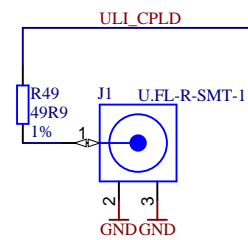
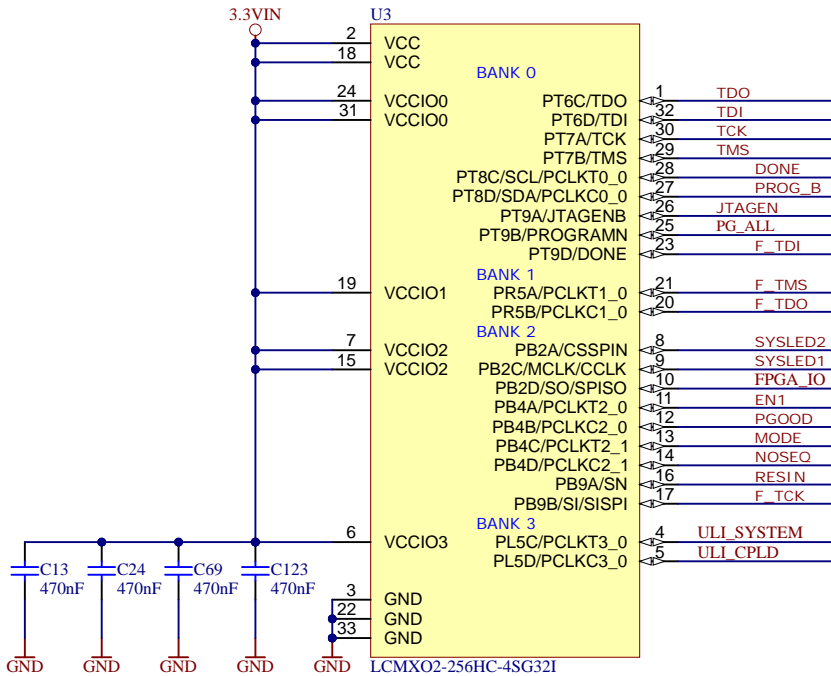




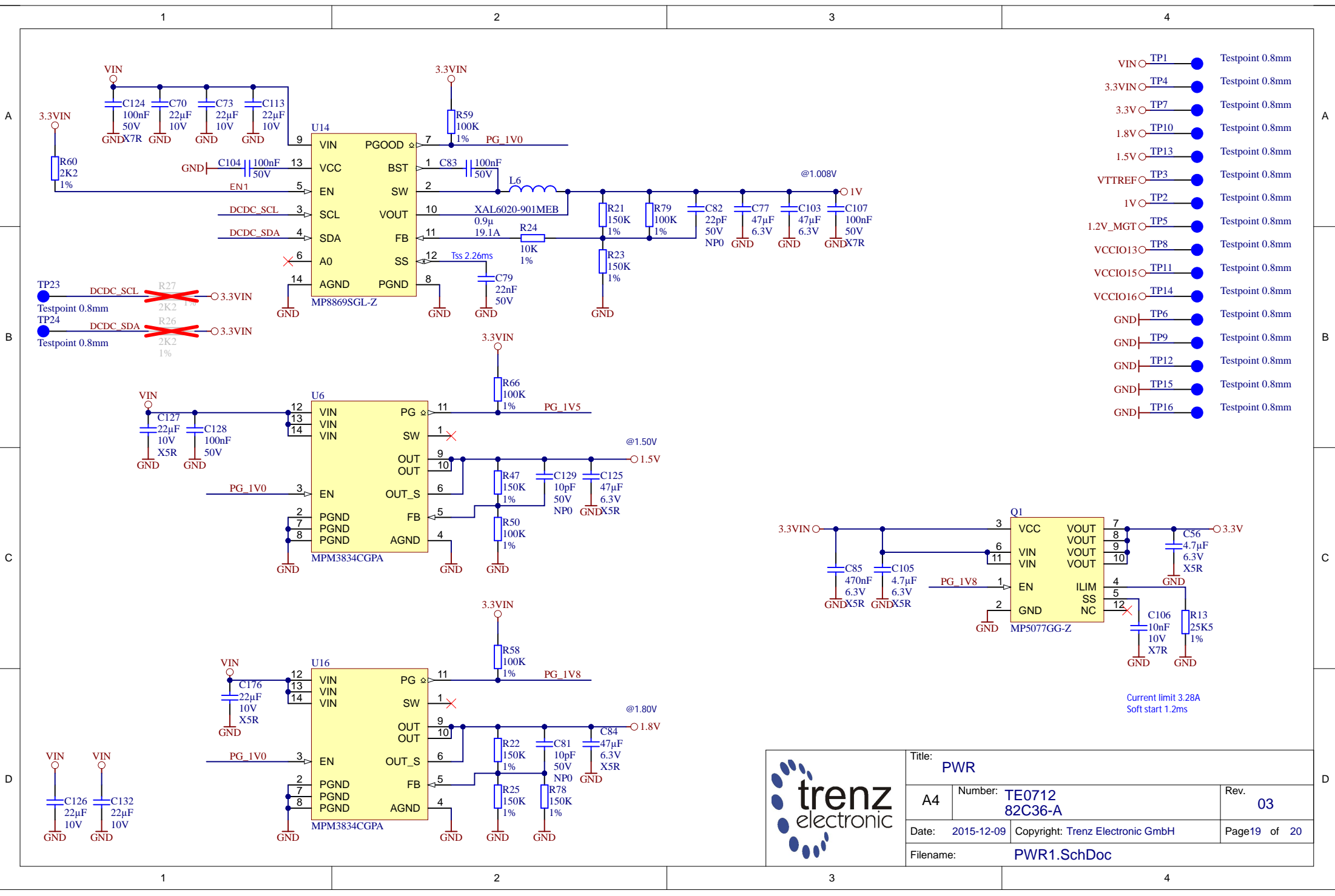
TLK106 is pin compatible with DP83822



Title: <b>ETH</b>		
A4	Number: <b>TE0712 82C36-A</b>	Rev. <b>03</b>
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Filename: <b>ETHERNET.SchDoc</b>		



	Title: <b>CPLD</b>		
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	Filename: <b>CPLD.SchDoc</b>		



Title: PWR		
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Current limit 3.28A  
Soft start 1.2ms

1

2

3

4

A

A

B

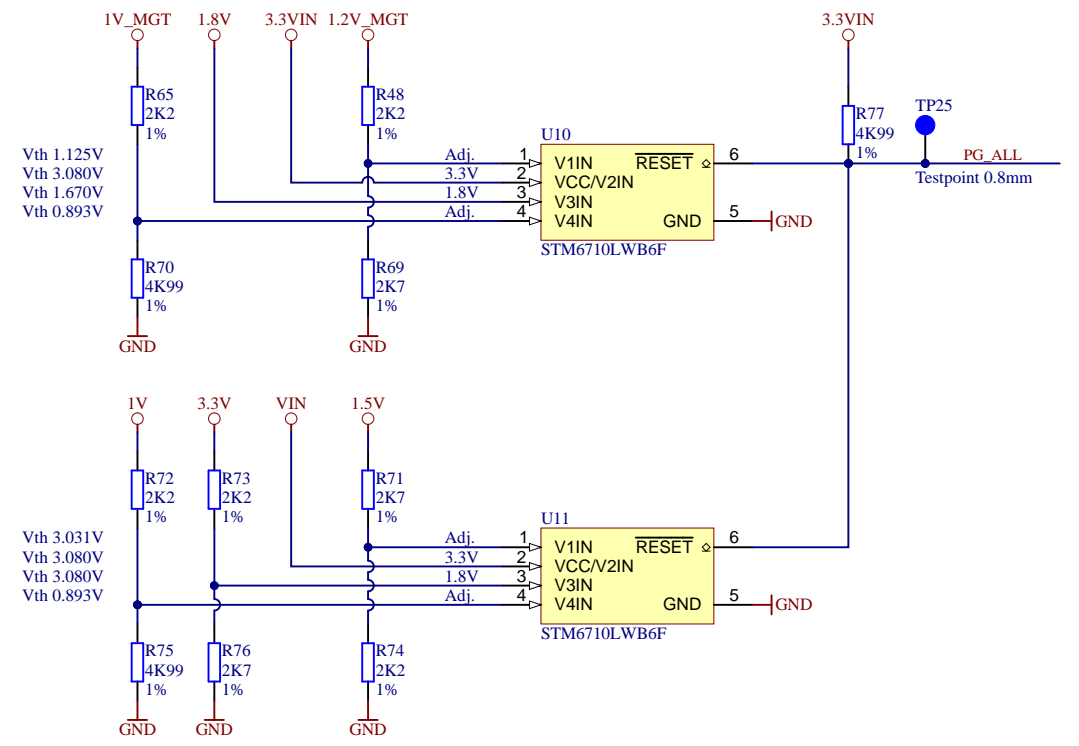
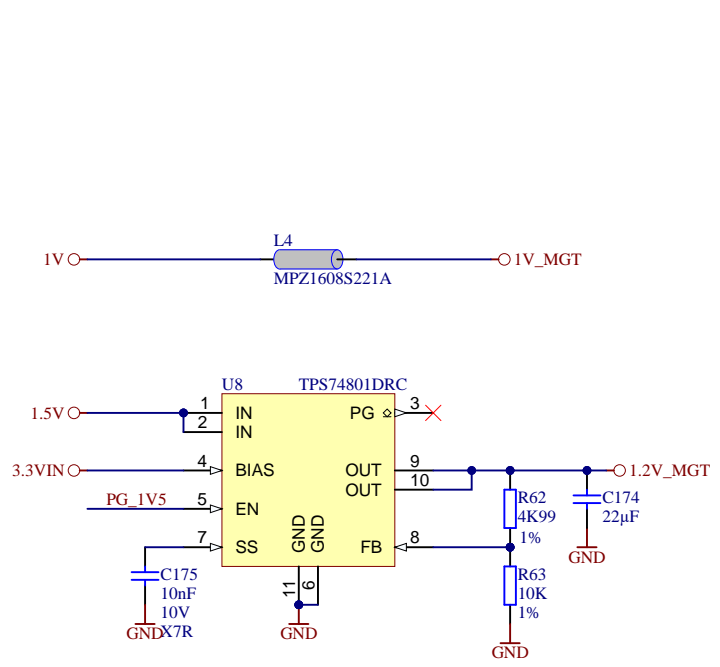
B


C

C

D

D



		Title: PWR	
		A4	Number: TE0712 82C36-A
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1

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