Am29C668

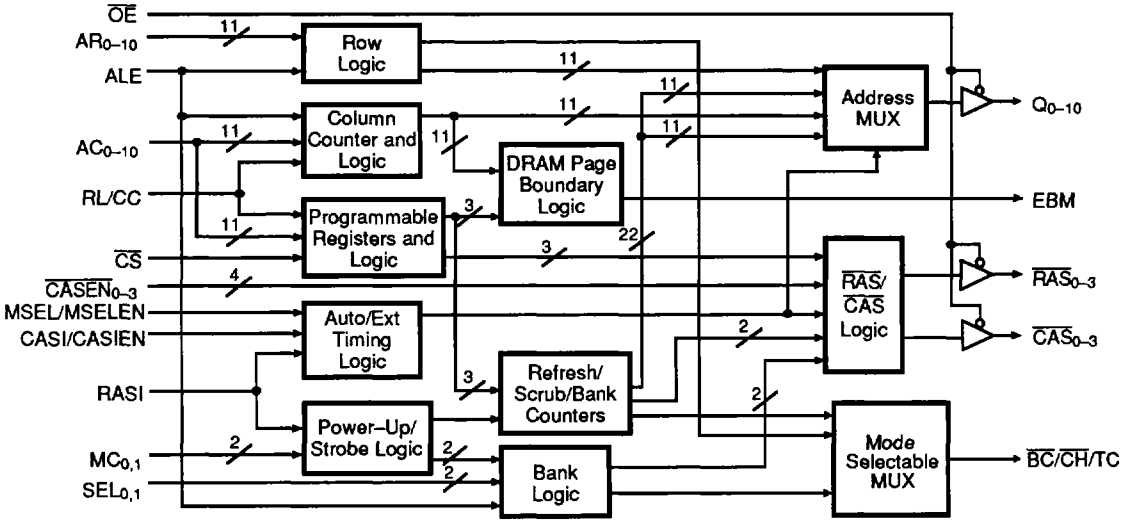
4M Configurable Dynamic Memory Controller/Driver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Provides control for 4M, 1M, 256K, 64K dynamic RAMs
- Programmable Burst/Block Access support for Am29000,68000 family, iAPX family
- Proprietary "Cache" Mode supports Page Mode accessing
- Single-chip Bank Interleaving saves precharge time
- Nibble mode support (for Page Mode or Nibble Mode DRAMs)
- Selectable Address and Strobe autotiming or external timing
- Supports "Scrubbing" with refresh when used in an EDC system
- Supports CAS before RAS refresh
- Byte and Bank CAS Decoding
- Selectable 2 or 4 bank drive
- Outputs directly drive up to 88 DRAMs, with a guaranteed worst-case limit on the undershoot and overshoot
- Low-power advanced sub-micron CMOS process
- User configurable to replace Am2968A and Am29368 DMCs

BLOCK DIAGRAM



11068–001B

Publication # 11068 Rev. B Amendment /0
Issue Date: March 1990

GENERAL DESCRIPTION

The Am29C668 4M Configurable Dynamic Memory Controller/Driver (CDMC) is designed for high performance memory systems. The CDMC acts as the address controller between the processor and the dynamic memory array. It uses its 11-bit row latch and 11-bit-column latch and counter to hold the row and column addresses, respectively, for multiplexing these to any DRAM size up to 4M. These latches and counter and the row/column refresh counter are used to directly drive the address lines of the DRAM array. The output of the 2-bit bank latch is decoded to select the bank to be accessed.

The Am29C668 has two basic modes of operation, read/write and refresh. In the read/write mode, the Am29C668 latches the row, column, and bank addresses and multiplexes them to the DRAM array. This multiplexing occurs under the control of the internally-generated timing strobes in the Auto Timing Mode, or the externally-generated MSEL in External Timing Mode. The read/write mode of the Am29C668 may be optimized for the shortest memory access time, through burst/block access, "cache" mode access, nibble mode access, or bank interleaving.

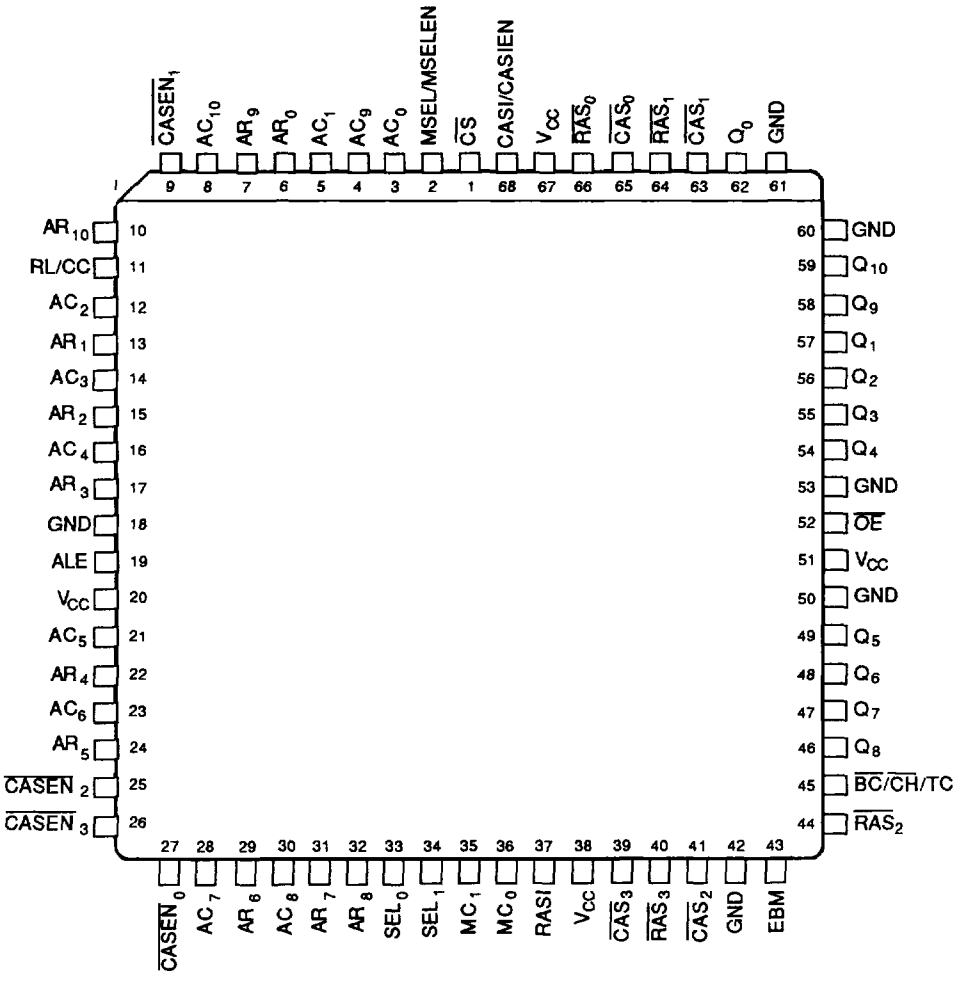
In the refresh mode, the refresh address is generated by the Am29C668 refresh counter. This counter is automatically adjusted for different DRAM sizes. If memory scrubbing is not being implemented, only the row counter is used to generate the row address for refresh. When memory scrubbing is being performed in EDC systems, both the row and column address counters are used.

RELATED AMD PRODUCTS

Part No.	Description
Am29368	1M Dynamic Memory Controller/Driver
Am29C60A	High Speed CMOS Cascadable 16-Bit EDC
Am29C660D	12 ns CMOS Cascadable 32-Bit EDC
Am2968A	256K Dynamic Memory Controller/Driver
Am2976	11-Bit Dynamic RAM Driver
Am29C983	9-Bit x 4-Port Multiple Bus Exchange
Am2965/6	8-Bit Dynamic RAM Driver Inverting/Non-Inverting
Am29C983A	9-Bit x 4-Port Multiple Bus Exchange, High Speed
Am29C985	9-Bit x 4-Port MBE with Parity
Am29C827A	10-Bit 48 mA Bus Buffer

CONNECTION DIAGRAMS
Top View

PLCC



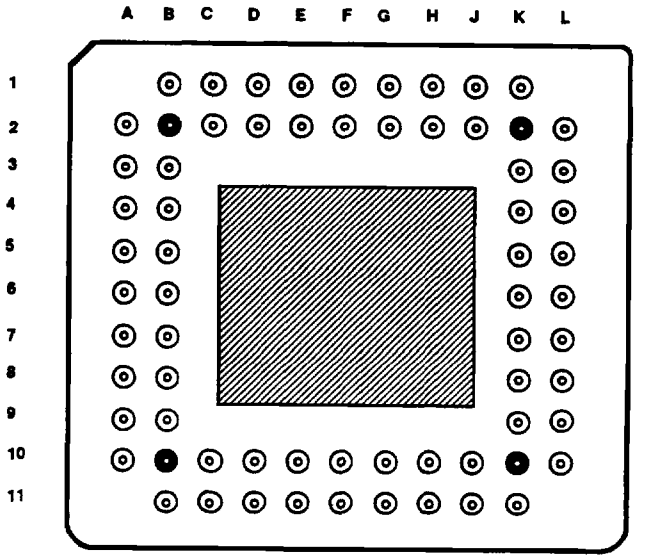
11068-002A

Note: Pin1 is marked for orientation (PLCC only).

CONNECTION DIAGRAM

Top View (Pins Pointing **Down**)

PGA*



11068–003A

*Pinout matches socketed PLCC pinout and footprint.

PGA PIN DESIGNATIONS

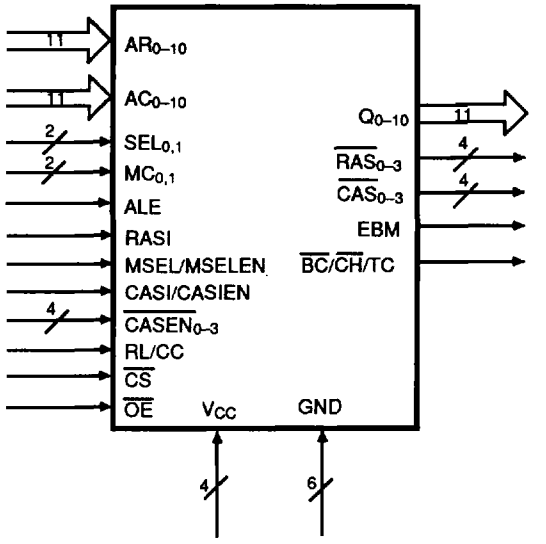
(Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A-2	AR_{10}	**B-9**	$\overline{CASEN_2}$	**F-10**	MC_0	**K-4**	Q_1
A-3	AC_2	**B-10**	AC_7	**F-11**	MC_1	**K-5**	Q_3
A-4	AC_3	**B-11**	$\overline{CASEN_0}$	**G-1**	V_{CC}	**K-6**	GND
A-5	AC_4	**C-1**	AR_9	**G-2**	CASI/CASIEN	**K-7**	V_{CC}
A-6	GND	**C-2**	AC_{10}	**G-10**	V_{CC}	**K-8**	Q_5
A-7	V_{CC}	**C-10**	AC_8	**G-11**	RASI	**K-9**	Q_7
A-8	AR_4	**C-11**	AR_6	**H-1**	$\overline{CAS_0}$	**K-10**	$\overline{BC/CH}$/TC
A-9	AR_5	**D-1**	AC_1	**H-2**	$\overline{RAS_0}$	**K-11**	EBM
A-10	$\overline{CASEN_3}$	**D-2**	AR_0	**H-10**	$\overline{RAS_3}$	**L-2**	GND
B-1	$\overline{CASEN_1}$	**D-10**	AR_8	**H-11**	$\overline{CAS_3}$	**L-3**	Q_9
B-2	RL/CC	**D-11**	AR_7	**J-1**	$\overline{CAS_1}$	**L-4**	Q_2
B-3	AR_1	**E-1**	AC_0	**J-2**	$\overline{RAS_1}$	**L-5**	Q_4
B-4	AR_2	**E-2**	AC_9	**J-10**	GND	**L-6**	$\overline{OE}$
B-5	AR_3	**E-10**	SEL_1	**J-11**	$\overline{CAS_2}$	**L-7**	GND
B-6	ALE	**E-11**	SEL_0	**K-1**	GND	**L-8**	Q_6
B-7	AC_5	**F-1**	$\overline{CS}$	**K-2**	Q_0	**L-9**	Q_8
B-8	AC_6	**F-2**	MSEL/MSELEN	**K-3**	Q_{10}	**L-10**	$\overline{RAS_2}$

(Sorted by Pin Name)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
E-1	**AC_0**	C-11	**AR_6**	K-11	**EBM**	L-8	**Q_6**
D-1	**AC_1**	D-11	**AR_7**	A-6	**GND**	K-9	**Q_7**
A-3	**AC_2**	D-10	**AR_8**	J-10	**GND**	L-9	**Q_8**
A-4	**AC_3**	C-1	**AR_9**	K-1	**GND**	L-3	**Q_9**
A-5	**AC_4**	A-2	**AR_{10}**	K-6	**GND**	K-3	**Q_{10}**
B-7	**AC_5**	B-6	**ALE**	L-2	**GND**	H-2	**$\overline{RAS_0}$**
B-8	**AC_6**	K-10	**$\overline{BC/CH}$/TC**	L-7	**GND**	J-2	**$\overline{RAS_1}$**
B-10	**AC_7**	H-1	**$\overline{CAS_0}$**	F-10	**MC_0**	L-10	**$\overline{RAS_2}$**
C-10	**AC_8**	J-1	**$\overline{CAS_1}$**	F-11	**MC_1**	H-10	**$\overline{RAS_3}$**
E-2	**AC_9**	J-11	**$\overline{CAS_2}$**	F-2	**MSEL/MSELEN**	G-11	**RASI**
C-2	**AC_{10}**	H-11	**$\overline{CAS_3}$**	L-6	**$\overline{OE}$**	B-2	**RL/CC**
D-2	**AR_0**	B-11	**$\overline{CASEN_0}$**	K-2	**Q_0**	E-11	**SEL_0**
B-3	**AR_1**	B-1	**$\overline{CASEN_1}$**	K-4	**Q_1**	E-10	**SEL_1**
B-4	**AR_2**	B-9	**$\overline{CASEN_2}$**	L-4	**Q_2**	A-7	**V_{CC}**
B-5	**AR_3**	A-10	**$\overline{CASEN_3}$**	K-5	**Q_3**	G-1	**V_{CC}**
A-8	**AR_4**	G-2	**CASI/CASIEN**	L-5	**Q_4**	G-10	**V_{CC}**
A-9	**AR_5**	F-1	**$\overline{CS}$**	K-8	**Q_5**	K-7	**V_{CC}**

LOGIC SYMBOL



Die Size: 0.233" x 0.165" Gate Count: 3600 11068–004A

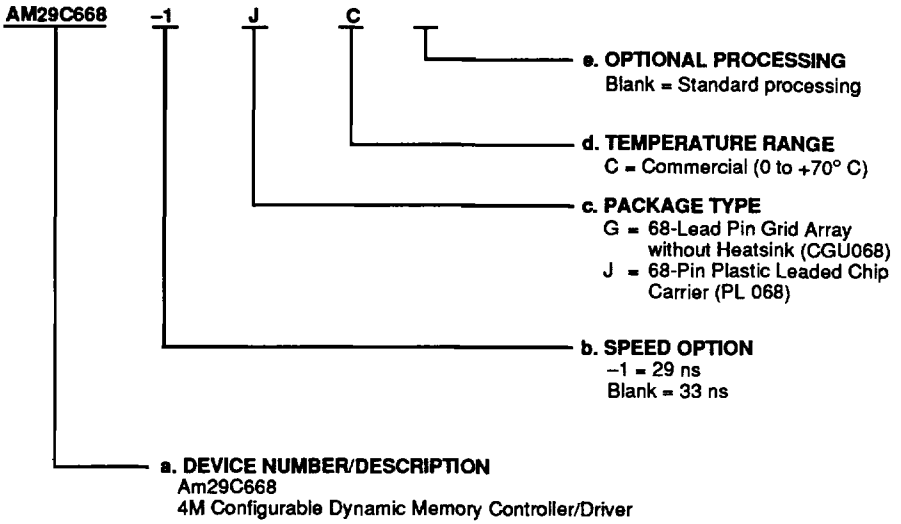
Package Information

Parameter	PGA	PLCC	Units
θ_{JA}	34	35	°C/W
θ_{JC}	–	N/A	

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C668	JC, GC
AM29C668-1	

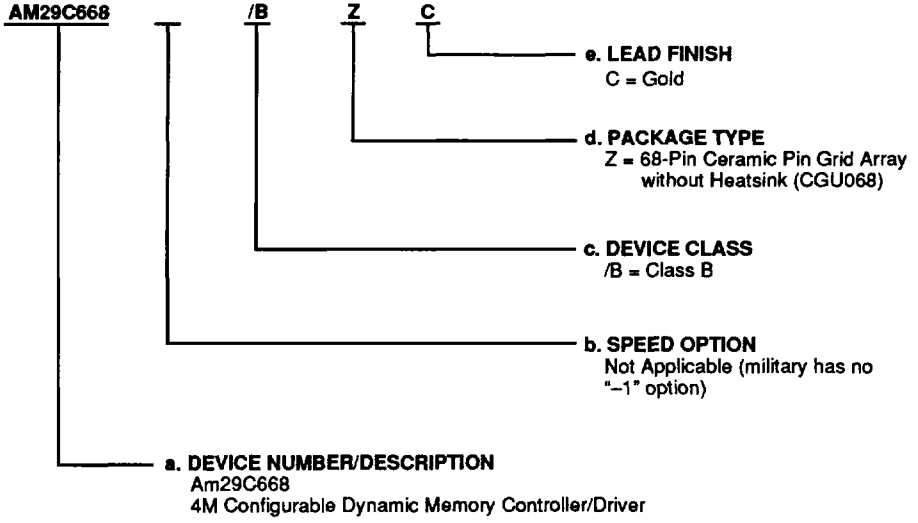
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION
APL Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C668	/BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11

PIN DESCRIPTION

AC_{0-10} and AR_{0-10}

Column and Row Address Inputs (Inputs(22))

The address on these lines is latched by the LOW going edge of the Address Latch Enable (ALE) signal. AC_{0-10} are connected to the lower side of the system address bus and are driven on the output address lines Q_{0-10} when the MSEL (Multiplexer Select) signal is HIGH. AR_{0-10} are connected to the upper side of the system address bus and are driven on the output address lines Q_{0-10} when the MSEL signal is LOW.

AC_{0-7} and AR_{0-7} are used for 64K DRAMs.
AC_{0-8} and AR_{0-8} are used for 256K DRAMs.
AC_{0-9} and AR_{0-9} are used for 1M DRAMs.
AC_{0-10} and AR_{0-10} are used for 4M DRAMs.

ALE

Address Latch Enable (Input; Active HIGH)

This input causes the Row Latch, Column Latch and Counter, and the Bank Latch to become transparent allowing the latches to accept new input data. A LOW input on ALE latches the input data, assuming it meets specified set-up and hold requirements.

$\overline{BC}/\overline{CH}/TC$

Bank Compare/Cache Hit/Terminal Count (Outputs; Active LOW/LOW/HIGH)

This is a triple function output, dependent upon the Mode Control inputs and the Bank Interleave (BI) Bit in the Configuration Register. If the Mode Control inputs are 1,0 ($MC_{0,1}$ = 10) the Am29C668 is in the Refresh-With-Scrubbing or Initialize mode and this output acts as the Terminal Count (TC).

As **Terminal Count**, this output goes active (HIGH) when the Refresh Counter has gone through an entire count. The Refresh Counter is user configured for DRAM size (64K, 256K, 1M, 4M) and number of banks (2 or 4), which are programmable via the Memory Size Bits and the $\overline{RAS}/\overline{CAS}$ configuration Bit, respectively, in the Configuration Register (Reference Figure 6). The TC signal is used to indicate the end of initialization in an Error Detection and Correction (EDC) system.

In the read/write mode ($MC_{0,1}$ = 01), this output acts as either the Bank Compare ($\overline{BC}$) signal if BI = 0, or as the Cache Hit ($\overline{CH}$) signal if BI = 1. As **$\overline{BC}$**, this output goes active (LOW) when the current memory access is to the same bank as the previous memory access and remains active until a memory access to a different bank is requested. This signal is used by the external timing generator during bank interleaving to either immediately activate the RASI input if two consecutive accesses are to two different banks (saving RAS precharge time) or delay the RASI input if two consecutive accesses are to the same bank (allowing the current $\overline{RAS}_n$ output to go through a precharge cycle before it is reactivated).

As **$\overline{Cache\ Hit}$**, this output goes active (LOW) when the current memory access is to the same row and the same bank as the previous access. The $\overline{CH}$ signal is used to facilitate Fast Page Mode or Static Column accesses.

$\overline{CAS}_{0-3}$

Column Address Strobe (Outputs (4); Active LOW; Three State)

Each $\overline{CAS}_n$ output will go active when selected by $SEL_{0,1}$ in a bank-wise $\overline{CAS}$ decoding method (CDM = 0, reference Figure 6) or when selected by $\overline{CASEN}_{0-3}$ in a byte-wise $\overline{CAS}$ decoding implementation. This will occur only when CASI goes active in the External Timing Mode or when CASIEN and the internally generated $\overline{CAS}$ go active in the Auto Timing Mode.

Each output provides a $\overline{CAS}_n$ signal to one of four banks of the dynamic memory, if four banks are used. If two banks are used, each bank can use 2 $\overline{CAS}_n$ signals to reduce the capacitive load on each. The number of banks (2 or 4) is programmable via the $\overline{RAS}/\overline{CAS}$ Configuration Bit in the Configuration Register (reference Table 4).

The $\overline{CAS}_n$ outputs contain pull-up resistors which ensure a logical HIGH (inactive) when in the high impedence state.

$\overline{CASEN}_{0-3}$

Column Address Strobe Enable (Inputs (4); Active LOW)

When a byte-wise method is used for $\overline{CAS}$ decoding these four inputs are decoded externally to handle byte operations. The timing generation may be Auto or External. Only those $\overline{CAS}_n$ outputs will be activated whose corresponding $\overline{CASEN}_n$ inputs are selected by the external byte decode circuit.

When a bank-wise method is used for $\overline{CAS}$ decoding these inputs are not used.

CASI/CASIEN

Column Addess Strobe Input/Column Address Strobe Input Enable (Input; Active HIGH)

This is a dual function input. In the External Timing mode this input is used as **CASI**. With a bank-wise $\overline{CAS}$ decoding method, the internally decoded $\overline{CAS}_n$ output is forced LOW after CASI goes active. When used as CASI with a byte-wise decoding method, the selected $\overline{CAS}_n$ output is forced LOW depending upon the externally decoded $\overline{CASEN}_n$ inputs after CASI goes active.

In Auto Timing Mode this input is used as **CASIEN**. With a bank-wise $\overline{CAS}$ decoding method, the decoded $\overline{CAS}_n$ output is forced LOW, if both the internally generated $\overline{CAS}$ and the CASIEN signals are active. This input is used to delay the $\overline{CAS}_{0-3}$ outputs from going active if de-

sired, resulting in a longer auto timing access sequence. This input is generally not used as CASIEN with a byte-wise $\overline{CAS}$ decoding implementation.

$\overline{CS}$

Chip Select (Input; Active LOW)

This input is used to enable the Am29C668. When active, the Am29C668 operates normally in all four modes. When $\overline{CS}$ goes inactive (HIGH), the device will not enter the Read/Write mode.

EBM

End Burst/Block Mode (Output Active HIGH)

This output is only used in the burst/block mode of data transfer. It indicates to the processor that the Am29C668 cannot perform any more data transfers in the burst/block mode for one of two reasons. Either the DRAM page boundary is reached (in which case a new row address is required from the processor), or a programmed allowable number of transfers has been completed.

GND (6) 0-V Power Supply

These pins are the 0-V power supply for the Am29C668. All grounds must be connected for proper device operation.

$MC_{0,1}$ Mode Control (Inputs (2))

These inputs specify one of four modes of operation of the Am29C668. Operating modes are described in Table 1.

MSEL/MSELEN

Multiplexer Select/Multiplexer Select Enable (Input; Active HIGH)

This is a dual function input. In the External Timing mode this input is used as **MSEL**. When MSEL is HIGH the column address is selected. When MSEL is LOW the row address is selected.

In the Auto Timing Mode this input acts as **MSELEN**. When MSELEN is HIGH and the internally generated MSEL is active the column address is selected. When MSELEN is LOW or the internally generated MSEL is inactive the row address is selected. MSELEN is used to delay the address change from row to column, if desired, resulting in a longer auto timing access sequence.

The address may come form either the address latches and counter or the refresh address counter depending upon $MC_{0,1}$. The MSEL/MSELEN input is only applicable in the Read/Write or Refresh with Scrubbing Modes.

$\overline{OE}$

Output Enable (Input; Active LOW)

This input enables/disables the output signals. When $\overline{OE}$ is inactive (HIGH), all address outputs of the Am29C668 enter a high impedence state and the $\overline{RAS}_n$ and $\overline{CAS}_n$ outputs are pulled inactive (HIGH).

$Q_{0\text{-}10}$

Address Outputs (Outputs(11);Three State)

These edge rate controlled outputs drive the dynamic memory address inputs. The drivers on these lines are able to drive high capacitive loads, which are specified at 350pF. Greater capacitive loads may also be driven, however. See section labeled "Typical Change in Propagation Delay vs Loading Capacitance" following the AC Characteristics.

$\overline{RAS}_{0\text{-}3}$

Row Address Strobe (Outputs (4); Active LOW; Three State)

Each Row Address Strobe output provides a $\overline{RAS}_n$ signal to one of four memory banks. Each will go low when selected by $SEL_{0,1}$ and only when RASI goes HIGH. All four go LOW in response to RASI in the refresh modes.

When a 2 bank $\overline{RAS}/\overline{CAS}$ configuration is selected (RCC = 1), RAS_0 and RAS_1 are tied together internally, as are RAS_2 and RAS_3. This reduces the capacitive loading on the $\overline{RAS}_n$ outputs in a two bank system (reference Table 4).

In four bank mode, the $\overline{RAS}_n$ outputs are decoded with $SEL_{0,1}$. In two bank mode these outputs are decoded with SEL_0. In this case SEL_1, should be tied LOW.

The RAS_n outputs contain pull-up resistors which ensure a logical HIGH (inactive) when in the high impedence state.

RASI

Row Address Strobe Input (Input; Active HIGH)

During normal memory cycles, the decoded $\overline{RAS}_n$ outputs ($\overline{RAS}_0$,$\overline{RAS}_1$,$\overline{RAS}_2$,$\overline{RAS}_3$) as determined by $SEL_{0,1}$ and the RCC bit in the Configuration Register are forced LOW after RASI goes active HIGH. During refresh, all four RAS_n outputs go LOW after RASI goes active HIGH. If auto timing is enabled, the HIGH going edge of RASI also initiates the internal timing cycle and its LOW going edge terminates the internal timing cycle.

RL/CC

Register Load/Column Clock (Input)

This is a dual function pin which depends upon the Mode Control inputs ($MC_{0,1}$). If $MC_{0,1}$ =11, the Am29C668 is in the Reset Mode and this pin acts as the Register Load signal. If $MC_{0,1}$ = 01 the Am29C668 is in the Read/Write Mode and this input acts as the Column Clock signal.

When used as **Register Load**, the LOW-to-HIGH edge of the signal loads either the Burst Count Register, the Mask Register, or the Configuration Register via the $AC_{0\text{-}10}$ Address Inputs. (Reference Figure 5).

When used as **Column Clock**, the HIGH-to-LOW edge of the signal increments the Column Counter during burst and nibble mode accessing.

$SEL_{0,1}$
Bank Select (Inputs (2))

These two inputs are the highest-order address bits when the Am29C668 is used in the normal access mode or in the burst/block access mode. They are the two lowest-order address bits when the Am29C668 is used in the bank interleave mode. In both cases $SEL_{0,1}$ are used in the Read/Write Mode to select which bank of memory will receive the $\overline{RAS}_n$ and $\overline{CAS}_n$ signals when RASI and CASI (or the internally generated CAS in the auto-timing mode) go active HIGH. The $\overline{CAS}_n$ signals will not be decoded from $SEL_{0,1}$ if a byte-wise $\overline{CAS}$ decoding scheme is selected. In two bank mode, only SEL_0 is used. SEL_1 should be tied LOW.

V_{CC} (4) + 5-V
Positive Power Supply Voltage

These inputs provide the power necessary to operate the Am29C668. All power supply inputs must be connected for proper device operation.

Table 1. Mode Control Function

MC_0	MC_1	Operating Mode
0	0	**Refresh Without Scrubbing (a more detailed description can be found in the section entitled "Refresh Modes")** a) $\overline{RAS}$–Only Refresh: Refresh cycles are performed with only the row refresh counter being used to increment addresses. In this mode, all four $\overline{RAS}_n$ outputs are active while the four $\overline{CAS}_n$ outputs are held inactive. b) $\overline{CAS}$ Before $\overline{RAS}$ Refresh: Refresh addresses are generated internally by the DRAMs. In this mode, all four $\overline{CAS}_n$ outputs are active followed by all four $\overline{RAS}_n$ outputs going active. This new type of refresh is selected via the CBR-bit in the Configuration Register. In this mode, RASI controls the $\overline{CAS}_n$ outputs and CASI controls the $\overline{RAS}_n$ outputs.
1	0	**Refresh With Scrubbing/Initialize (EDC Systems)** This mode may be used only in systems with Error Detection and Correction (EDC) capability. In this mode, refresh cycles are performed with both the row and column refresh counters generating the addresses. MSEL is used to select between the row and column addresses. All four $\overline{RAS}_n$ signals go active in response to RASI and one $\overline{CAS}_n$ output goes active in response to CASI. The CAS_n output is decoded from the bank refresh counter. The remaining three $\overline{CAS}_n$ outputs are left inactive, while their respective banks undergo normal refresh. This mode is also used to initialize the memory array by writing a known data pattern and corresponding check bits.
0	1	**Read/Write** This mode is used to perform read/write operations. The row address is taken from the row latch and the column address is taken from the column latch and counter. $SEL_{0,1}$ are decoded to determine which $\overline{RAS}_n$ and $\overline{CAS}_n$ will be active.
1	1	**Reset/Configuration** This mode is used to clear the refresh counters and the Register Logic. These operations are performed on the HIGH-to-LOW transition of RASI. This mode is used to load the configuration, burst count, and mask registers.

Table 2. Address Output Function

$\overline{CS}$	MC_1	MC_0	Internal MSEL	Mode	Address Multiplexer Output
0	0	0	X	Refresh W/O Scrubbing	Row Counter
	0	1	1	Refresh with Scrubbing	Column Counter
			0		Row Counter
	1	0	1	Read/Write	Column Latch
			0		Row Latch
	1	1	X	Reset	All Zero
1	0	0	X	Refresh W/O Scrubbing	Row Counter
	0	1	1	Refresh with Scrubbing	Column Counter
			0		Row Counter
	1	0	X	Read/Write	All Zero
	1	1	X	Reset	All Zero

X = Don't care

Table 3. $\overline{RAS}$ Output Function

Inputs						Outputs			
Internal RASI	$\overline{CS}$	MC	SEL*	RCC**	MODE	$\overline{RAS}_n$			
		1 0	1 0			3	2	1	0
0	X	X X	X X	X	No operation	1	1	1	1
1	0	0 0	X X	X	Refresh W/O Scrubbing	0	0	0	0
		0 1	X X	X	Refresh with Scrubbing	0	0	0	0
		1 0	0 0	0	Read/Write	1	1	1	0
			X 0	1		1	1	0	0
			0 1	0		1	1	0	1
			X 1	1		0	0	1	1
			1 0	0		1	0	1	1
			X 0	1		1	1	0	0
			1 1	0		0	1	1	1
			X 1	1		0	0	1	1
		1 1	X X	X	Reset	0	0	0	0
	1	0 0	X X	X	Refresh W/O Scrubbing	0	0	0	0
		0 1			Refresh with Scrubbing	0	0	0	0
		1 0			Read/Write	1	1	1	1
		1 1			Reset	0	0	0	0

* After Internal RASI is asserted, changing $SEL_{0,1}$ will not effect the $\overline{RAS}_n$ decoding until Internal RASI is deasserted.
** Reference Figure 6.

Table 4. $\overline{RAS}/\overline{CAS}$ Configuration Decode*

RCC	Mode	$\overline{RAS}/\overline{CAS}$ CONFIGURATION		
0	4-Bank	RAS_0	CAS_0	BANK 0
		RAS_1	CAS_1	BANK 1
		RAS_2	CAS_2	BANK 2
		RAS_3	CAS_3	BANK 3
1	2-Bank	RAS_0	CAS_0	BANK 0
		RAS_1	CAS_1	
		RAS_2	CAS_2	BANK 1
		RAS_3	CAS_3	

*CDM = 0

Table 5. $\overline{CAS}$ Output Function

Inputs								Outputs			
CDM**	Internal CASI†	$\overline{CS}$	CBR**	MC	SEL*	Internal Counter	RCC**	$\overline{CAS}_n$			
				1 0	1 0	1 0		3	2	1	0
0	1	0	1	0 0	X X	X X	X	0	0	0	0
			0					1	1	1	1
			1	0 1	X X	X X	X	1	1	1	1
			0			0 0		0	1	1	1	0
								1	1	1	0	0
						0 1		0	1	1	0	1
								1	0	0	1	1
						1 0		0	1	0	1	1
								1	1	1	0	0
						1 1		0	0	1	1	1
								1	0	0	1	1
			X	1 0	0 0	X X		0	1	1	1	0
								1	1	1	0	0
					0 1			0	1	1	0	1
								1	0	0	1	1
					1 0			0	1	0	1	1
								1	1	1	0	0
					1 1			0	0	1	1	1
								1	0	0	1	1
				1 1	X X	X X	X	1	1	1	1	1
		1	1	0 0	X X	X X	X	0	0	0	0	0
			0					1	1	1	1	1
			1	0 1	X X	X X	X	1	1	1	1	1
			0			0 0		0	1	1	1	0
								1	1	1	0	0
						0 1		0	1	1	0	1
								1	0	0	1	1
						1 0		0	1	0	1	1
								1	1	1	0	0
						1 1		0	0	1	1	1
								1	0	0	1	1
			X	1 0 1 1	X X	X X	X	1	1	1	1	1
	0	X	X	X X	X X	X X	X	1	1	1	1	1
1	1	X	1	0 0	X X	X X	X	0	0	0	0	0
			0					1	1	1	1	1
			X	0 1	X X	X X	X	1	1	1	1	1
				1 X	X X	X X	X	1	1	1	1	1
			X	X X	X X	X X	X	1	1	1	1	1
	0		X	X X	X X	X X	X	1	1	1	1	1

† In the external timing mode, Internal CASI follows the CASI input. In Autotiming Mode, this signal is generated internally and is enabled by the CASIEN inputs.

* After Internal RASI is asserted, changing $SEL_{0,1}$ will not effect the $\overline{CAS}_n$ decoding until Internal RASI is deasserted.

** Reference Figure 6.

FUNCTIONAL DESCRIPTION*

General Description

The Am29C668 4M Configurable Dynamic Memory Controller/Driver provides the controls required to operate dynamic RAMs up to 4Mbit x n. Manufactured in submicron CMOS technology, the Am29C668 performs the address control and generation function and strobe control and generation for 64K, 256K, 1M or 4M DRAMs. The Am29C668 controls the address to the DRAMs from the processor in the read/write mode and it generates and controls the address to the DRAMs in the refresh mode. The Am29C668 also generates the row and column address strobe signals in the read/write and refresh modes.

The Am29C668 has on-chip series damping resistors on its driver outputs to restrict the output signals to +0.8-V overshoot and -1.0V undershoot maximum (See Switching Waveforms).

Logic Overview

The functional blocks of the Am29C668 can be summarized as follows (reference block diagram):

Row Logic
Column Counter and Logic
Bank Logic
Programmable Registers and Logic
Auto/External Timing Logic
Power-Up/Strobe Logic
DRAM Page Boundary Logic
Refresh/Scrubbing/Bank Counters
Address Multiplexer
$\overline{RAS}/\overline{CAS}$ Logic

Row Logic

This block (Figure 1) consists of a Row Latch, a Register, and a Comparator. The 11-bit Row Latch holds the DRAM row address. It is transparent when the Address Latch Enable signal is HIGH, and the address is latched on the LOW-going edge of ALE.

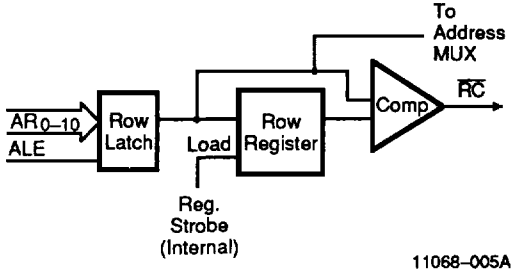


Figure 1. Row Logic

The 11-bit Row Register holds the row address of the previous DRAM access. The register is clocked at the beginning of every access where $MC_{0,1} = 01$ by the HIGH - going edge of the RASI input.

The 11-bit Row Comparator compares the row address of the current access (contents of the Row Latch) with the row address of the previous access (contents of the Row Register) and generates the Row Compare ($\overline{RC}$) signal. The $\overline{RC}$ and $\overline{BC}$ signals are ORed to generate a $\overline{CH}$ signal (Figure 2). $\overline{CH}$ is LOW if the current row and bank addresses are the same as the previous row and bank addresses, respectively. $\overline{CH}$ is high if they are not. This indicator is used by the external timing generator during Cache Mode accesses. The RASI input is held active (HIGH) if consecutive accesses are to the same row in the same bank, saving precharge time and access time on the current $\overline{RAS}_n$. The RASI input is deactivated if consecutive accesses are to different rows or banks, thereby ending the "cache" access.

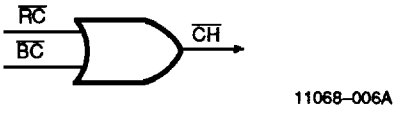


Figure 2. $\overline{Cache\ Hit}$ Generation

Column Counter and Logic

The block (Figure 3) consists of the Column Latch and Counter. The 11-bit loadable counter holds the DRAM column address. The counter is transparent when ALE is HIGH and the address is loaded on the LOW-going edge of ALE. The HIGH-to-LOW edge of the signal increments the Column Counter. ALE must be LOW in order to increment the counter.

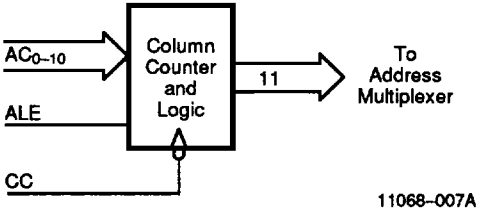


Figure 3. Column Counter and Logic

If the Nibble Count bit of the Configuration Register is enabled (NIBCNT = 1), then only the two LSBs of the Column Latch are clocked, generating a modulo four nibble count (Reference Nibble Mode section).

* Modes of operation are described beginning on page 22.

Bank Logic

This block (Figure 4) contains the Bank Latch, Bank Register, and Bank Comparator. The 2-bit Bank Latch holds the DRAM bank address. The latch is transparent when ALE is HIGH and latches the address on the LOW-going edge of ALE.

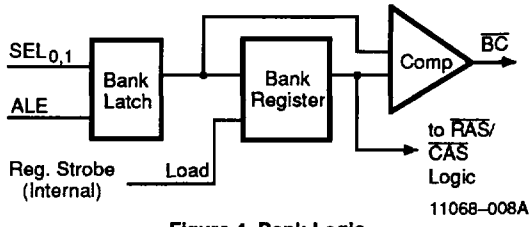


Figure 4. Bank Logic

The 2-bit Bank Register holds the bank address of the previous DRAM access. The register is clocked at the beginning of every access by the HIGH-going edge of RASI in Read/Write mode only.

The 2-bit Bank Comparator compares the bank address of the current access (contents of the Bank Latch) and the bank address of the previous access (contents of the Bank Register) and generates the $\overline{BC}$ signal. $\overline{BC}$ is LOW if the current bank address is the same as the previous bank address. $\overline{BC}$ is used by the external timing generator during bank interleaving to either activate the RASI input if two consecutive accesses are to two different banks (saving $\overline{RAS}$ precharge time on the current $\overline{RAS}_n$) or to delay the RASI input if two consecutive accesses are to the same bank (so that the current $\overline{RAS}_n$ output can go through precharge before it is reactivated).

Programmable Registers and Logic

This block (Figure 5) consists of the Configuration Register, Burst Count Register, Mask Register, Column Comparator Logic, Register Load Logic, and DRAM Size Decoder.

In order to load the 11-bit Configuration Register, a device reset ($MC_{0,1}$=11 with RASI ↓) must occur followed by switching MC_0, or MC_1 to 0 (to end reset operation). Then the Configuration Register is loaded via the column address bus (AC_{0-10}) by the High-going edge of RL/CC signal (↓) with $MC_{0,1}$=11. The Configuration Register is programmed to select the options shown in Figure 6 (reference Figure 15).

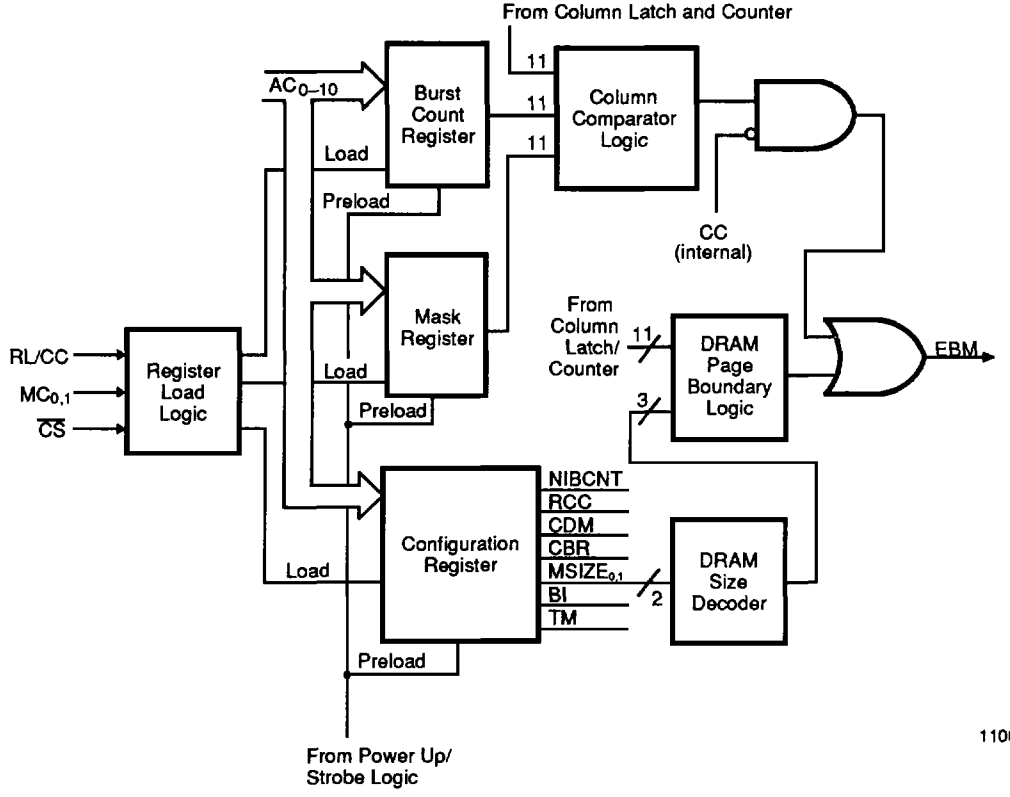


Figure 5. Programmable Registers and Logic

The 11-bit Burst Count Register is loaded via AC_{0-10} by the HIGH-going edge of RL through the Register Load Logic. This register is preloaded with all 1's (for a maximum burst count) in the Reset mode after power-up, and is only used in the Burst/Block mode of access, if a programmed number of accesses is required. This register is loaded with the maximum number of transfers to occur during any burst/block access. This number is dependent on the specifics of the system (i.e... page size or processor type).

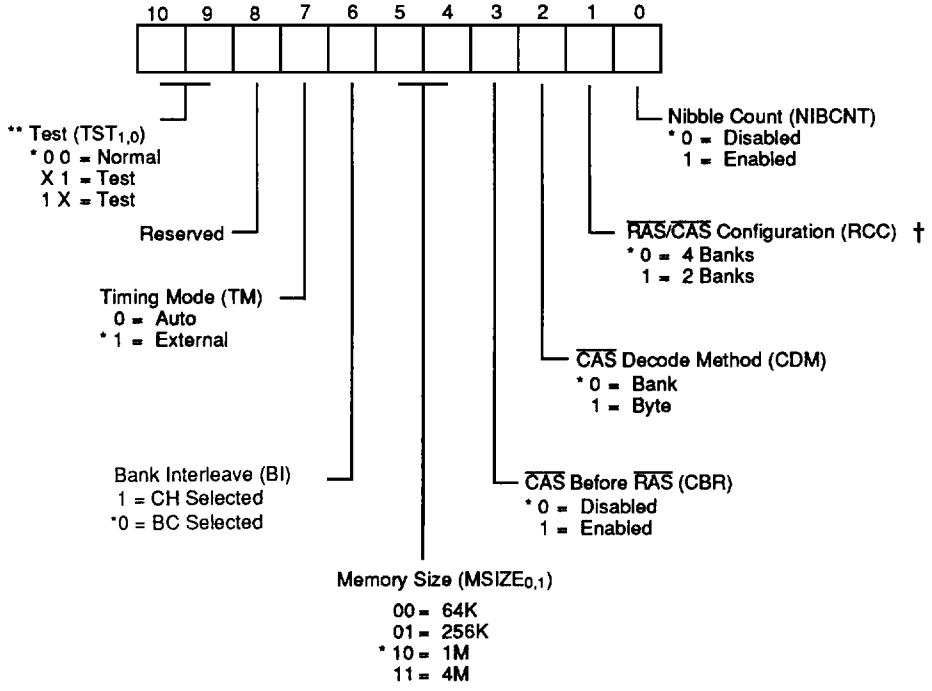
The 11-bit Mask Register is loaded via AC_{0-10} by the HIGH-going edge of the RL signal through the Register Load Logic. This register is preloaded with all 1's (for all bits to be compared) in the Reset Mode after power-up, and is only used in the Burst/Block mode of access, if a programmed number of accesses is required.

This register allows a burst to be made which is shorter than the page size of the memory. When the Mask Register is loaded with a "1" in a bit location, the corresponding bit in the Column Latch and the Burst Count Register is compared. This register also aligns the Column Latch and Counter for succeeding bursts of full length if they occur immediately after termination of the prior burst. The Mask Register is loaded with 00000001111 for a 16-bit maximum burst.

The Column Comparator Logic compares the contents of the Column Latch and Counter with that of the Burst Count Register (which contains the end of burst count value). The HIGH bits in the Mask Register determine which of the 11-bits of the Column Latch and Counter and the Burst Count Register are compared. This logic is used only in the Burst/Block mode of access. Reference Figure 6a.

The Register Load Logic loads the Burst Count, Mask and Configuration Registers via the address bus (AC_{0-10}) dependent upon the state of the Register Loading diagram in Figure 7. RL/CC Decoder and Register Load Logic are shown in Figure 8.

The DRAM Size Decoder determines the DRAM size being used. The $MSIZE_{1,0}$ bits in the Configuration Register are used to decode the size of the DRAMs being used as shown in Figure 6.



* Default. The Am29C668 will power up in Am29368 mode if the user does not reprogram the configuration register.

† Reference Table 4.

** These bits are used during factory testing only.

11068–010A

Figure 6. Configuration Register Options

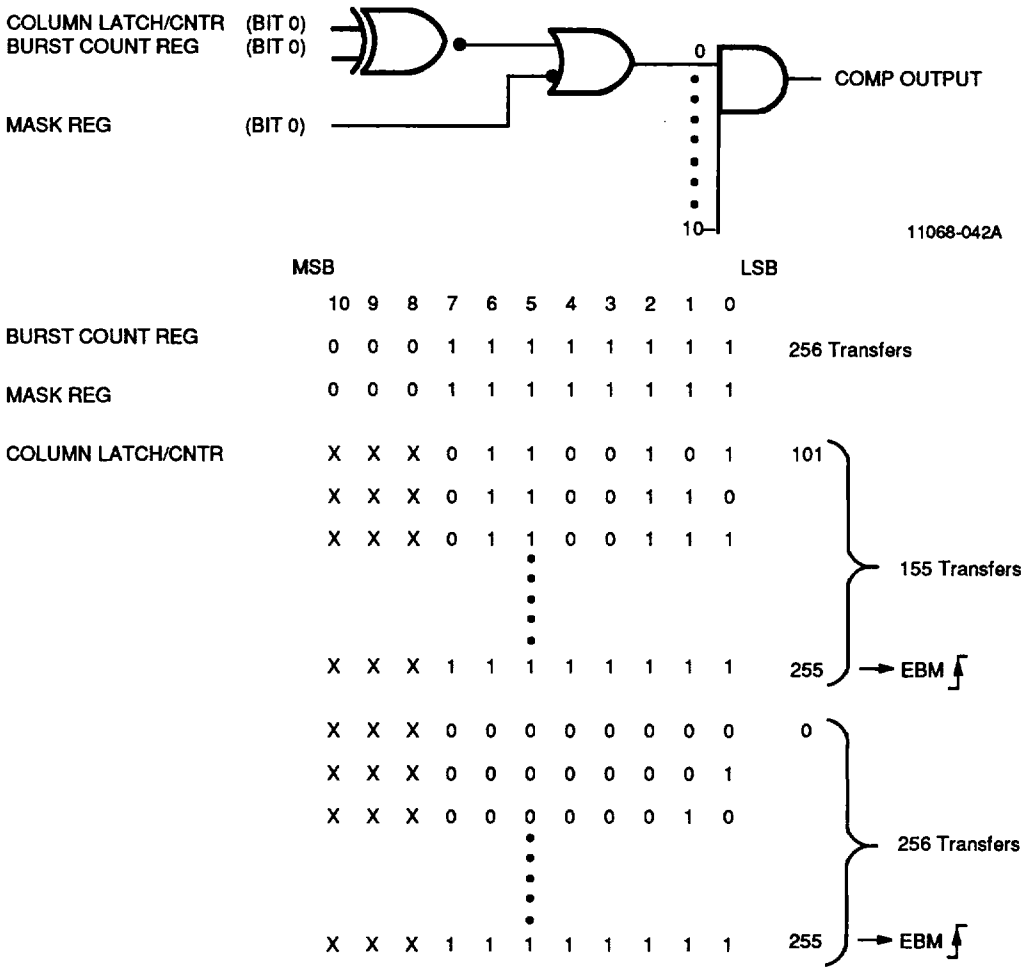


Figure 6a. Programmable Burst Logic with 256-word Burst Length Example

In this example, the self alignment feature of the Am29C668 is shown. The first burst is terminated on the DRAM page boundary by the EBM output. All subsequent bursts are then set at 256 transfers, which has been programmed via the Burst Count and Mask registers.

Auto/External Timing Logic

When Auto Timing mode is selected via the Timing Mode (TM) bit in the Configuration Register (TM = 0), this circuit generates internal timing delays between RASI-MSEL and MSEL-CASI. These delays are optimized for use with 100ns DRAMs.

In the Auto Timing mode the CASI/CASIEN input acts as CASIEN. In this mode internal $\overline{CAS}$ is generated from the active (HIGH) edge of RASI and is deactivated when RASI goes inactive by the Auto Timing Circuit. This internally generated $\overline{CAS}$ is gated with the CASIEN input to generate the $\overline{CAS}_n$ outputs. This gating circuit allows the Auto-Timing to be externally overridden (Figure 9). It is used for specialty DRAM accesses.

In the External Timing mode (TM = 1), the internal $\overline{CAS}$ signal follows the externally generated CASI input.

In the Auto Timing Mode the MSEL/MSELEN input acts as MSELEN. In this mode, internal MSEL is generated from the active (HIGH) edge of RASI, and is deactivated when RASI goes inactive, by the Auto Timing Circuit. This internally generated MSEL is gated with the MSELEN input to generate the internal MSEL signal. This feature is used to extend row address hold time via external control (overriding the Auto Timing feature).

In the External Timing mode (TM = 1), the internal MSEL signal follows the externally generated MSEL input.

The Auto Timing mode allows 4 banks of 16-bit data plus 6 EDC check bits or 2 banks of 32-bit data plus 7 EDC check bits comprised of 100ns DRAMs to be operated without external drivers.

Power-up/Strobe Logic

This block automatically presets the Am29C668 to the default condition upon power-up (Figure 6). This circuit also generates all the internal control signals for the Refresh Counter, Configuration, Burst Count, and Mask Registers, the Register Load Logic, and the Bank Register.

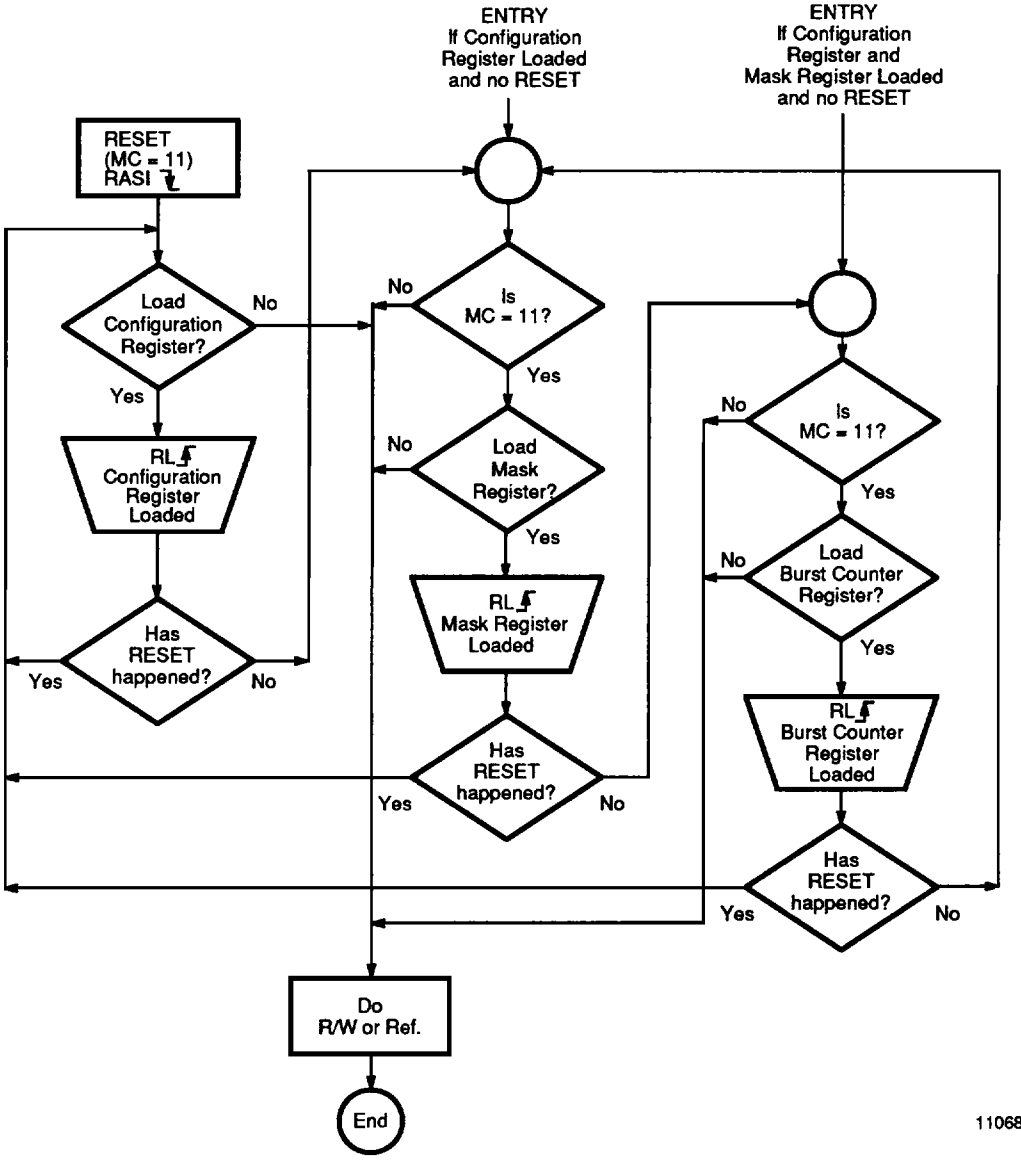


Figure 7. Register Loading (See paragraph on page 20)

Figure 7. Register Loading. The Configuration Register must be loaded before the Mask and Burst Count Registers may be loaded. Once the Configuration Register is loaded, the Register Load Logic will toggle between loading the Mask Register and Burst Count Register. The Configuration Register may only be loaded immediately after a reset. The Mask Register and Burst Count Register are only used in the Burst/Block access mode, in other modes only the Configuration Register need be loaded if the user wishes to alter its default mode indicated in Figure 6.

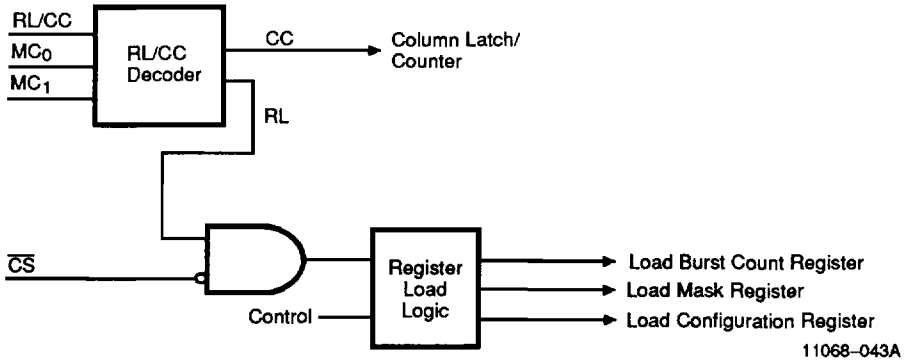


Figure 8. Register Load Logic and RL/CC Decoder (Register Logic)

DRAM Page Boundary Logic

This logic block indicates to the processor when a page boundary on the DRAM is reached. It monitors the contents of the Column Latch/Counter and, depending upon the outputs of the DRAM Size Decoder, signals an End of Burst/Block Mode (EBM) when a page boundary is reached. A page boundary condition is reached when the contents of the Column Latch/Counter equals the DRAM page boundary address.

This logic is used only in the Burst/Block mode of access.

Refresh/Scrubbing/Bank Counters

This block (Figure 10) contains the 11-bit Row Refresh Counter, 11-bit Column Refresh Counter, and 2-bit Bank Refresh Counter. All three counters are synchronous and are reset when $MC_{0,1}$ = 11 and RASI transitions from LOW to HIGH. These counters are clocked when $MC_{0,1}$ = 00 or 10 and RASI transitions from HIGH to LOW.

The size of the Row and Column Refresh Counters are automatically adjusted for the DRAM size being used. This is done by selecting the proper Row Counter output to go to the low order Column Counter input and similarly selecting the proper Column Counter output to go to the low order Bank Counter input. This selection is determined by the outputs of the DRAM Size Decoder with the help of a multiplexer.

The $\overline{RAS}/\overline{CAS}$ Configuration Bit of the Configuration Register selects which bit of the Bank Counter is used for the Terminal Count (TC) output, depending upon whether 2 or 4 banks of DRAM are used.

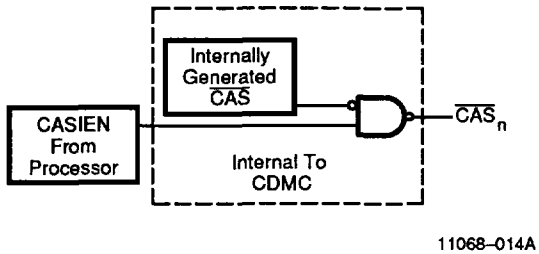


Figure 9. Auto Timing With External Override

Address Multiplexer

This block is an 11-bit, four input multiplexer which selects the address to the DRAMs. Its four address inputs are the row latch output, column latch/counter output, row refresh counter output, and column refresh counter output. The $MC_{0,1}$, internal MSEL, and $\overline{CS}$ input signals are decoded to select one of the four addresses.

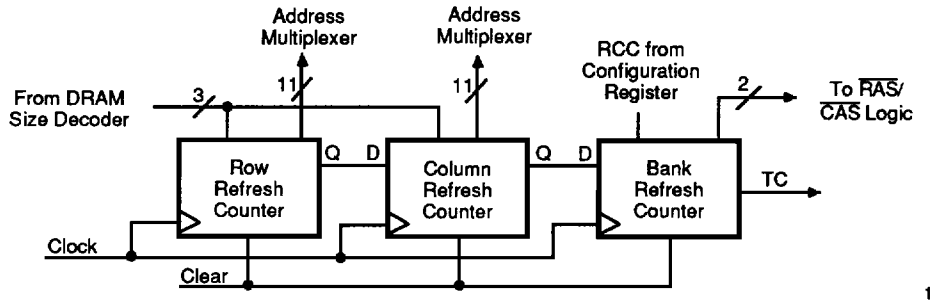


Figure 10. Refresh/Scrubbing/Bank Counters

RAS/CAS Logic

This block (Figure 11) contains the CAS Before RAS Logic, RAS and CAS Decode Logic, CAS Enable Logic, and CAS Multiplexer.

The CAS Before RAS Logic switches the RAS and CAS lines to the RAS and CAS Decode Logic if the CBR selection bit in the Configuration Register is set (1). This allows a CAS Before RAS refresh to be accomplished without altering the order of the RASI and CASI input strobes. Refresh With Scrubbing ($MC_{0,1}$ = 10) is not allowed when the CBR bit is set (1).

The RAS and CAS Decode Logic decodes the internal RAS and CAS timing signals to generate the four $\overline{RAS}_n$ and four $\overline{CAS}_n$ output signals.

The CAS Enable Logic is used if a byte-wise CAS decoding method is selected. Byte enables are decoded externally and are connected to the $\overline{CASEN}_{0-3}$ inputs. In the CAS Enable Logic all the $\overline{CASEN}_{0-3}$ signals are individually gated with the internal CAS signal to generate the $\overline{CAS}_n$ proper outputs.

The CAS Multiplexer is a 4-bit, two input multiplexer. It selects one set of $\overline{CAS}_n$ signals to the output depending upon the CAS decode method being used (selected by the CDM bit in the Configuration Register) and the operating mode (selected by $MC_{0,1}$).

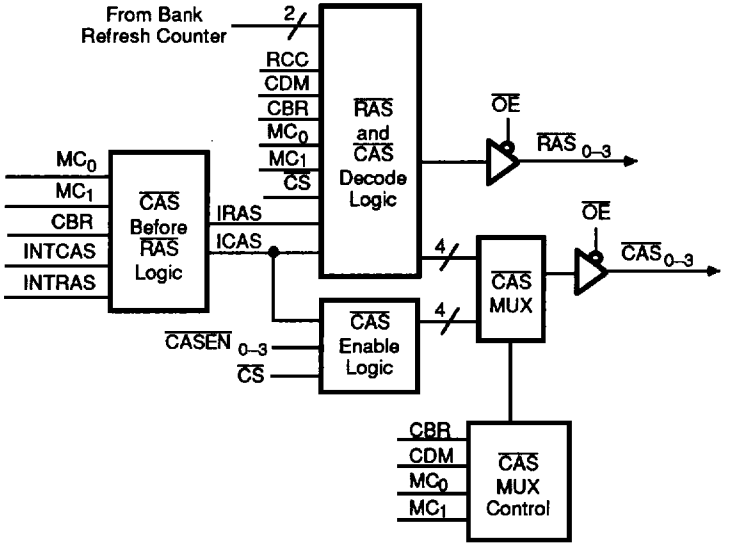


Figure 11. RAS/CAS Logic

MODES OF OPERATION

The Am29C668 has two basic modes of operation, read/write and refresh.

Read/Write Modes

In the read/write mode the Am29C668 latches the row, column and bank addresses and multiplexes them to the DRAM array under the control of the internally generated timing strobes in the Auto Timing Mode or the externally generated MSEL in the External Timing Mode. The timing option is selected via the Timing Mode (TM) bit in the Configuration Register (Figure 6).

The row address is latched in the DRAMs by the active (LOW-going) edge of the $\overline{RAS}_n$ output, which follows the active (HIGH-going) edge of the RASI input. The address lines are then switched to column address by either an internally generated signal in the Auto Timing Mode or by pulling MSEL active HIGH in the External Timing Mode. The column address is latched in the DRAMs on the active (LOW-going) edge of the $\overline{CAS}_n$ output, which follows either an internally generated signal in the Auto Timing Mode or the active (HIGH-going) edge of the CASI input in the External Timing Mode.

The read/write mode of the Am29C668 may be optimized for the shortest memory cycle time, through burst/block accesses, nibble mode accesses, "cache" mode accesses, or bank interleaving.

Burst/Block Mode

When a burst/block access is requested by the processor, the Am29C668 latches the initial row, column, and bank addresses. Subsequent column addresses are generated internally by the Am29C668, allowing consecutive memory locations to be accessed at high speed without the processor actually generating each memory location address. This type of transfer can be used by high performance processors to fill their on-chip or external cache when a cache miss is encountered.

During a burst access the CC input of the Am29C668 is toggled after the initial row, column, and bank addresses have been latched. While the RASI input is held high by the processor, each high-to-low transition of CC increments the column address for the next memory access.

The burst access will continue until a programmed number of accesses (which is stored in the Burst Count Register) has been completed or a page boundary is reached. Both conditions are indicated to the processor by the EBM output.

Nibble Mode

For Nibble mode accesses the Nibble Count bit (NIBCNT) in the Configuration Register is set to "1". This bit enables only the two least significant bits of the Column Latch and Counter to be clocked, allowing the Column Latch and Counter to perform a modulo four count when making a nibble burst access (as in the case of the 68030 processor) using non-nibble DRAMs.

When "nibble" DRAMs are used nibble accesses are accomplished by toggling CASI (Reference Figure 25).

Cache Mode

This mode allows the efficient use of page mode and fast page mode DRAMs by comparing back-to-back row and bank addresses from the processor.

In the "cache" mode of access of the Am29C668 the $\overline{RAS}_n$ output is held active (LOW) and any location in that row is accessed by only changing the column address. This makes the entire row look like a cache, since any access in that row can be made at high speed. To select the cache access mode, the Bank Interleave (BI) bit in the Configuration Register is set to "1". The row and bank addresses of consecutive accesses are compared by the Am29C668. If the row and bank addresses of consecutive accesses match, $\overline{CH}$ goes active (LOW) and signals the timing generator not to deactivate the RASI input but only to toggle the CASI/CASIEN input. If the row and bank addresses of consecutive accesses do not match, the $\overline{CH}$ signal goes inactive (HIGH) and informs the timing generator to deactivate the RASI input and start a new RASI cycle after the current cycle has gone through a $\overline{RAS}$ precharge cycle. When the RASI input is activated, its HIGH-going edge loads the row and bank registers with the contents of the row and bank latches, respectively, saving the current values for the next comparison.

Bank Interleave Mode

The Am29C668 can be configured to support on-chip bank interleaving by connecting the two LSBs of the processor address to $SEL_{0,1}$ and resetting the Bank Interleave (BI) bit in the Configuration Register to "0". Accesses being made to consecutive locations will be in adjacent banks, allowing the $\overline{RAS}_n$ strobe for the new bank to be activated as soon as the $\overline{RAS}_n$ strobe for the previous bank is deactivated and is precharging. This reduces the memory cycle time and improves memory throughput. The Bank Compare ($\overline{BC}$) signal indicates to the external timing generator whether the current access is to a different bank than the previous access and therefore whether bank interleaving is possible. The $\overline{BC}$ signal goes active (LOW) when the present access is to the same bank as the previous access.

The Bank Interleave Mode may not be used in conjunction with the Burst/Block, Nibble, or Cache Modes. The number of memory banks is set with the RCC bit in the Configuration Register.

Refresh Modes

Normal Refresh

In the normal refresh mode, the refresh address is generated by the Am29C668 refresh counter. The row refresh counter is used to generate the row address. All corresponding rows in all four banks are refreshed simultaneously by generating all four $\overline{RAS}_n$ outputs in response to the RASI input. Hence, the entire memory may be refreshed by stepping through the row refresh counter once. The row refresh counter is incremented to the next refresh address by the inactive (LOW going) edge of the RASI input.

Refresh With Scrubbing

When memory scrubbing is performed in systems employing error detection and correction (EDC), the row, column, and bank refresh counters are used. In this case, all four corresponding rows are refreshed and one location of one row is "scrubbed", ie...a read/modify/write cycle is performed. An entire memory array can be scrubbed by stepping through the row, column, and bank address counters once. The Am29C668 has four independent $\overline{CAS}_n$ outputs allowing a single bit to be accessed during refresh cycles.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This is a feature of some dynamic RAMs. The DRAM on-chip refresh counter is updated and a refresh cycle performed by generating a $\overline{CAS}$ strobe before the $\overline{RAS}$ strobe. This refresh support is selected by enabling (setting to "1") the $\overline{CAS}$ Before $\overline{RAS}$ bit in the Configuration Register. Refresh with scrubbing ($MC_{0,1}$ = 10) is not allowed when the CBR bit is set (1).

In this mode, RASI controls the $\overline{CAS}_n$ outputs and CASI controls the $\overline{RAS}_n$ outputs. This allows a $\overline{CAS}$ before $\overline{RAS}$ refresh to be accomplished without altering the order of the RASI and CASI input strobes. When this mode is set, memory "scrubbing" ($MC_{0,1}$ = 10) is prohibited.

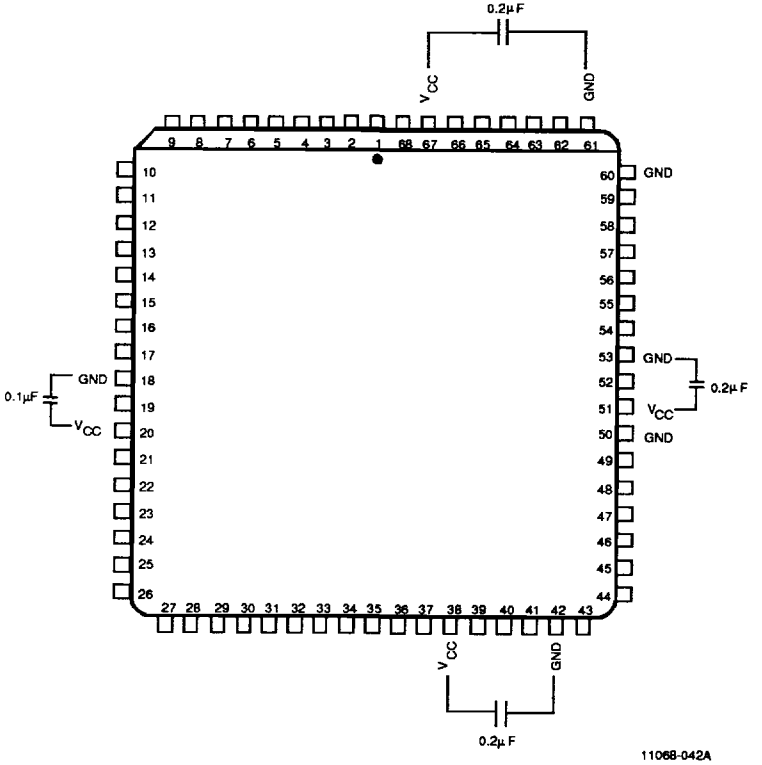


Figure 12. Device Decoupling – V_{CC} and Ground Pin Connections

Note:

Due to the high switching speeds and high drive capability of the Am29C668, it is necessary to decouple the device for proper operation. Multilayer ceramic capacitors are recommended. It is important to mount the capacitors as close as possible to the power pins (V_{CC}, GND) to minimize lead inductance and noise. A ground plane is strongly recommended. A wire wrapped board without power and ground planes is not recommended.

It is strongly recommended that this part be directly surface mounted whenever possible. Should a PLCC, or PGA socket be required, a one-time-insertion-only socket with minimal lead length is necessary for proper device function. The socket lead inductance should be 8nH maximum per pin.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Operating Temperature	-55 to +125°C
Maximum V_{CC}	-0.5 to +7.0 V
DC Voltage Applied to Any Pin	-0.5 to V_{CC} +0.3 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.50 to +5.50 V

Military (M)

Case Temperature (T_C)	-55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified (for APL Products, Group A, Subgroups 1,2,3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND			–5.0	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = –10 mA		2.7		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 10 mA			0.5	V
V_{ON}	Output Undershoot ↓ Voltage (Note 4)	CL = 50pF			–1.0	V
V_{OP}	Output Overshoot ↑ Voltage (Note 4)	CL = 50pF			0.8	V
V_{OP}	Output Overshoot ↑ Voltage (Note 4)	CL = 50pF			0.8	V
I_{OZ}	Off–State (High Impedence) Output Current; Q Outputs	V_{CC} = Max.	V_O = 0V		–10	µA
			V_O = V_{CC} (Max)		10	
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. 4.3V ≤ V_{IN} V_{IN} ≤ 0.2V f_{OP} = 0			5.0	mA
I_{CCT}	Quiescent Input Power Supply Current (@ TTL HIGH)	V_{CC} = Max. V_{IN} = 2.4 f_{OP} = 0			25	mA
I_{CCD}	Dynamic Power Supply Current (Note 5)	V_{CC} = Max. 4.3 V ≤ V_{IN} , V_{IN} ≤ 0.2V C_L = 150pF $\overline{OE}$ = LOW	MIL		7	mA/ MHz
			COM'L		7	
I_{CC}	Total Power Supply Current (Notes 3 and 5)	V_{CC} = Max., f_{OP} = 10 MHz $\overline{OE}$ = LOW 50% Duty cycle, C_L = 150pF 4.3 V ≤ V_{IN} , V_{IN} ≤ 0.2V	MIL		100	mA
			COM'L		100	
		V_{CC} = Max., f_{OP} = 10 MHz $\overline{OE}$ = LOW 50% Duty cycle, C_L = 150pF V_{IN} = 3.4, V_{IL} = 0.4 V	MIL		100	
			COM'L		100	

Notes:

1. For conditions shown as Min. or Max., use appropriate value specified under Operating Range for the applicable device type.
2. Tested with limited test pattern.
3. Total Power Supply Current is the sum of the Quiescent Current and the dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Power Supply Current can be calculated by using the following equation:

   $I_{CC} = I_{CCQ} + I_{CCD}(f_{op})$ (CMOS Inputs), $I_{CC} = I_{CCT} + I_{CCD}(f_{op})$ (TTL Inputs), f_{op} = Operating Frequency in Megahertz

   During device characterization, two addresses, one $\overline{RAS}_n$ and one $\overline{CAS}_n$ output were toggled at f_{OP} = 10 MHz during I_{CC} measurement.
4. V_{ON} and V_{OP} are not production tested but are guaranteed by characterization data for surface mounted devices with proper capacitive decoupling. Limits specified are for all outputs switching simultaneously with minimum specified loading. As loading increases, V_{ON} and V_{OP} will approach zero. Reference Switching Waveforms.
5. Not tested in production. Guaranteed by characterization data.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Capacitive Loading = 350pF for all Q_n, $\overline{RAS}_n$, and $\overline{CAS}_n$; 100pF for all other parameters (minimum tester load)

No.	Parameter Symbol	Parameter Description	Test Conditions	Commercial				Military		Units
				29C668		29C668-1		29C668		
				Min	Max	Min	Max	Min	Max	
COMMON PARAMETERS										
1	t_{PD}	AC_n/AR_n to Q_n	ALE = 1	4	33	4	29			ns
2	t_{PD}	MC_n to Q_n		6	37	6	34			ns
3	t_{PD}	ALE to Q_n		5	34	5	29			ns
4	t_{PD}	$\overline{CS}$ to Q_n		4	34	4	34			ns
5	t_S	AC_n/AR_n to ALE ↓ Set Up Time		4		4				ns
6	t_H	AC_n/AR_n to ALE ↓ Hold Time		4		4				ns
7	t_S	SEL_n to ALE ↓ Set Up Time		4		4				ns
8	t_H	SEL_n to ALE ↓ Hold Time		4		4				ns
9	t_S	MC_n to RASI ↓ Set Up Time		0		0				ns
10	t_H	MC_n to RASI ↓ Hold Time		4		4				ns
11	t_{PD}	$\overline{CS}$ ↓ to RASI ↓		4		4				ns
12	t_{PD}	$\overline{CS}$ ↓ to RASI ↓		4		4				ns
13	t_S	SEL_n to RASI ↓ Set Up Time	ALE = 1	4		4				ns
14	t_H	SEL_n to RASI ↓ Hold Time	ALE = 1	4		4				ns
15	t_{PWL}	RASI, CASI, CASIEN Pulse Width LOW	Note 2	10		10				ns
16	t_{PWH}	RASI, CASI, CASIEN PulseWidth HIGH	Note 2	10		10				ns
EXTERNAL TIMING MODE										
17	t_{PD}	RASI to $\overline{RAS}_n$		2	30	2	26			ns
18	t_{PD}	CASI to $\overline{CAS}_n$		3	30	3	26			ns
19	t_{PD}	MSEL to Q_n		4	30	4	26			ns
AUTO TIMING MODE										
20	t_{PD}	RASI to $\overline{RAS}_n$			30		26			ns
21	t_{PD}	$\overline{RAS}_n$ to Q_n (row address)	MSELEN = 1	15		15				ns
22	t_{PD}	RASI to $\overline{CAS}_n$	CASIEN = 1		88		88			ns
23	t_{PD}	$\overline{RAS}_n$ to $\overline{CAS}_n$	CASIEN = 1	25	66	25	66			ns
24	t_{PD}	Q_n to $\overline{CAS}_n$ (column address)	MSELEN = 1 CASIEN = 1	4		4				ns
25	t_{PD}	MSELEN to Q_n (column address)			33		31			ns
26	t_{PD}	CASIEN to $\overline{CAS}_n$			30		26			ns

SWITCHING CHARACTERISTICS (Continued)

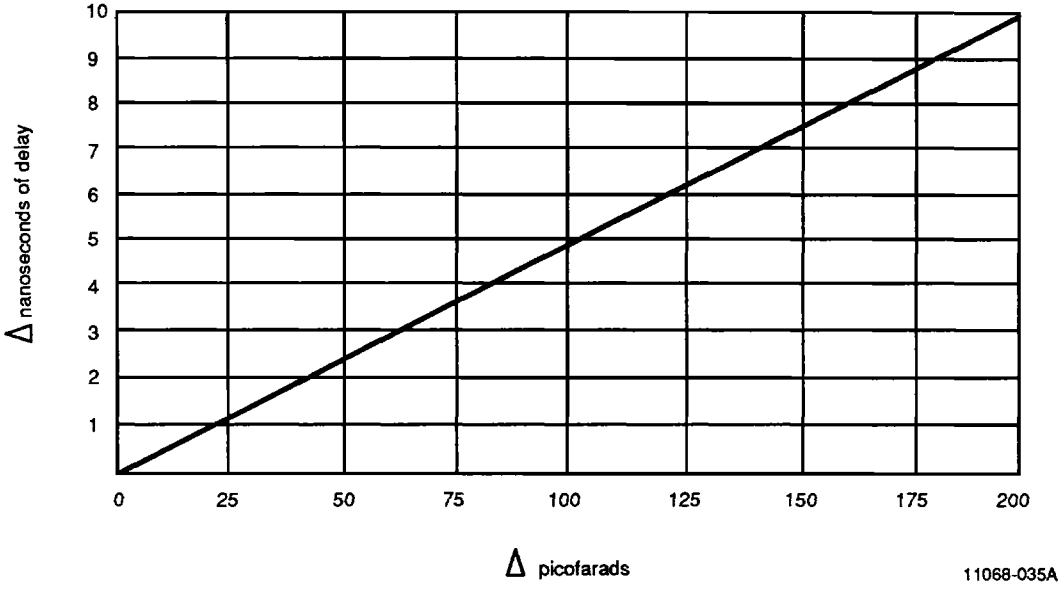
Capacitive Loading = 350pF for all Q_n, $\overline{RAS}_n$, and $\overline{CAS}_n$; 100pF for all other parameters (minimum tester load)

No.	Parameter Symbol	Parameter Description	Test Conditions	Commercial				Military		Units
				29C668		29C668-1		29C668		
				Min	Max	Min	Max	Min	Max	
SPECIALTY MODES										
27	t_{PD}	CC ↓ to Q_n			33		30			ns
28	t_{PD}	CC ↓ to EBM			18		17			ns
29	t_{PW}	CC Pulse Width LOW or HIGH	Note 2	10		10				ns
30	t_{PD}	SEL_n to $\overline{BC}$	ALE = 1		14		12			ns
31	t_{PD}	ALE to $\overline{BC}$			14		13			ns
32	t_{PD}	AR_n to $\overline{CH}$	ALE = 1		17		16			ns
33	t_{PD}	SEL_n to $\overline{CH}$	ALE = 1		14		13			ns
34	t_{PD}	ALE to $\overline{CH}$			18		16			ns
35	t_{PD}	RASI ↓ to TC			19		19			ns
36	t_S	AC_n/AR_n to RL ↑ Set Up Time		0		0				ns
37	t_H	AC_n/AR_n to RL ↑ Hold Time		10		10				ns
38	t_S	MC_n to RL ↑ Set Up Time		5		5				ns
39	t_H	MC_n to RL ↓ Hold Time		2		2				ns
40	t_{PW}	RL Pulse Width LOW or HIGH	Note 2	10		10				ns
41	t_{PD}	$\overline{CASEN}_n$ to $\overline{CAS}_n$			35		31			ns
OUTPUT SKEWS										
42	t_{SKEW}	$\{t_{PD}(AC_n/AR_n$ to $Q_n) - t_{PD}(RASI$ to $\overline{RAS}_n)\}$	MC_n = 01		23		20			ns
43	t_{SKEW}	$\{t_{PD}(MC_n$ to $Q_n) - t_{PD}(RASI$ to $\overline{RAS}_n)\}$	MC_n = 00,01		23		21			ns
44	t_{SKEW}	$\{t_{PD}(MSEL$ to $Q_n - t_{PD}(RASI$ to $\overline{RAS}_n)\}$	Note 3		18		16			ns
45	t_{SKEW}	$\{t_{PD}(MSEL$ to $Q_n - t_{PD}(CASI$ to $\overline{CAS}_n)\}$			16		16			ns
THREE STATE OUTPUTS										
46	t_{PLZ}	Output Disable Time from LOW	Note 2		20		20			ns
47	t_{PHZ}	Output Disable Time from HIGH			25		25			ns
48	t_{PZL}	Output Enable Time from LOW			27		27			ns
49	t_{PZH}	Output Enable Time from HIGH			26		26			ns

Notes:

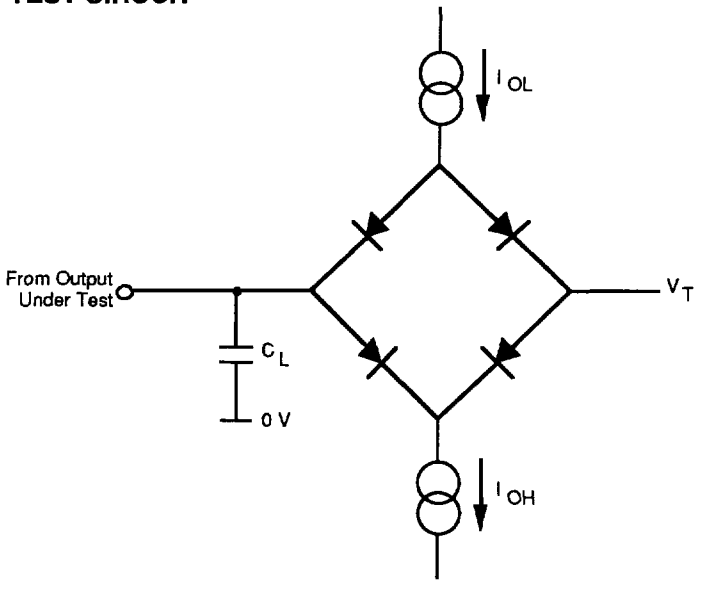
1. For additional loading information or to calculate t_{PD} between specified loads see section labeled "TYPICAL Change in Propagation Delay vs. Loading Capacitance" following the Switching Waveforms.
2. Not included in Group A testing. Not production tested. Guaranteed by characterization data.
3. Worst case for any given device.

TYPICAL Change in Propagation Delay vs Loading Capacitance



11068-035A

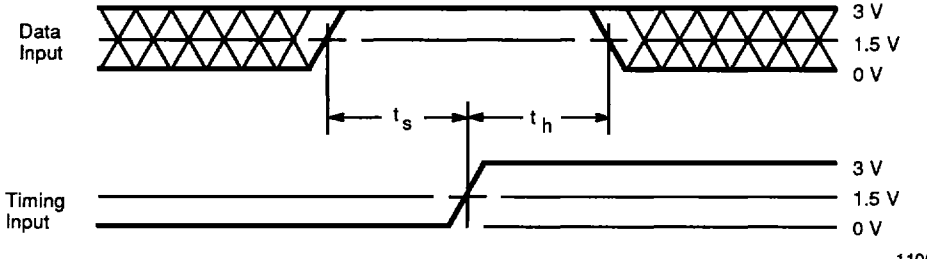
SWITCHING TEST CIRCUIT



11068–036A

Notes: 1. C_L is specified in Switching Characteristics Table.
2. V_T = 1.5V.

SWITCHING TEST WAVEFORMS



11068–037A

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross–hatched area is don't care condition.

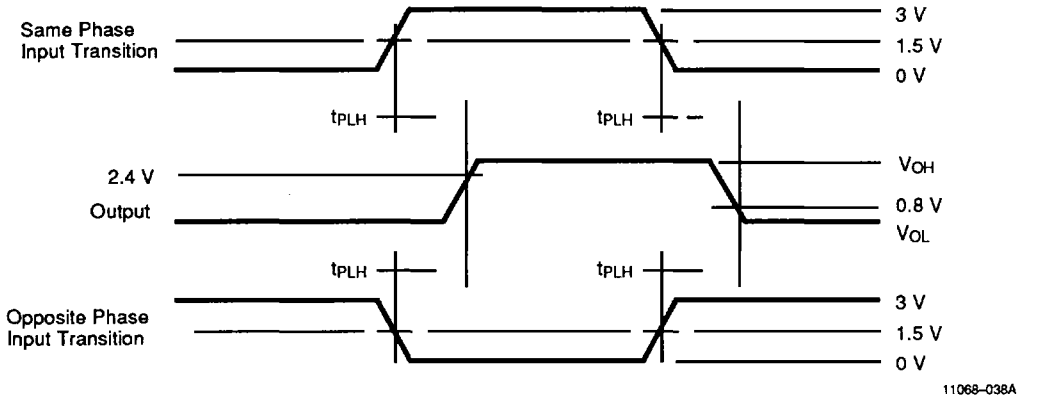
Setup and Hold Times

Notes on Testing

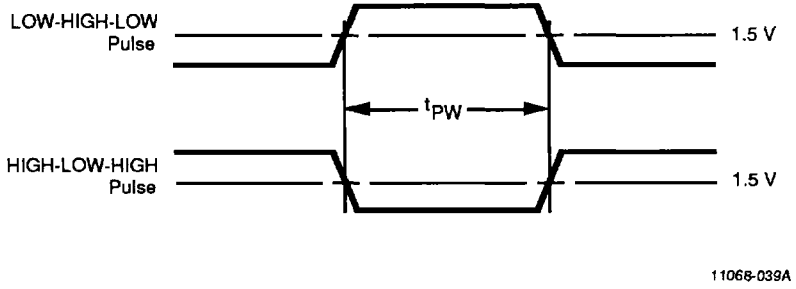
Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Proper device grounding is critical when device testing. Multi-layer performance boards with radial decoupling between power and ground planes is recommended. Wiring unused interconnect pins to the ground plane is recommended. The ground plane must be sustained from the performance board to the device under test interface board. To minimize inductance, heavy-gauge stranded wire with twisted pairs should be used for power wiring.

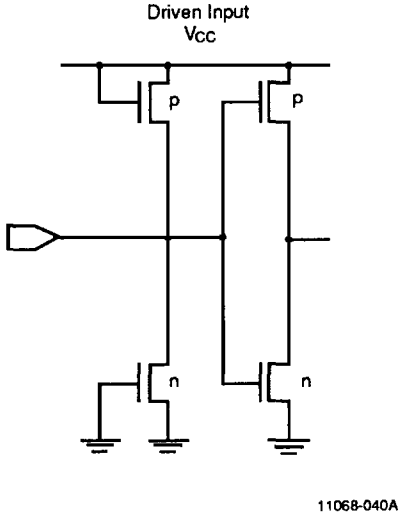
SWITCHING WAVEFORMS (Continued)



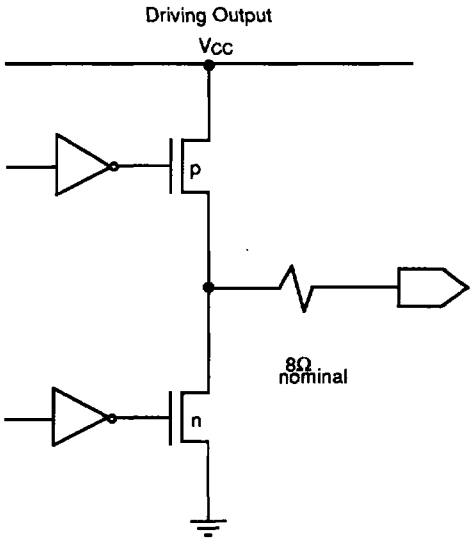
Propagation Delay



Input Pulse Width

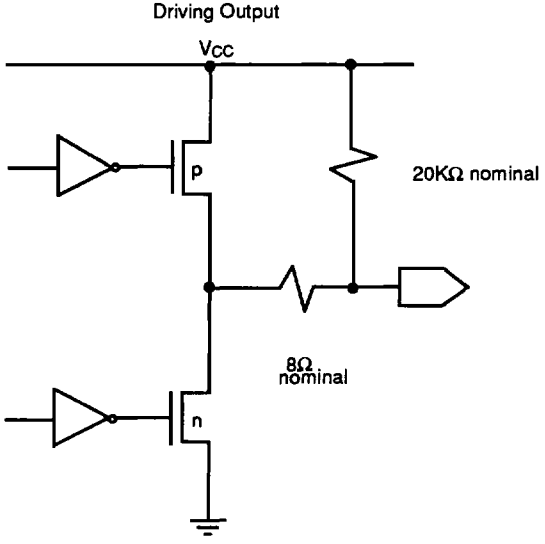


Equivalent Input Circuit



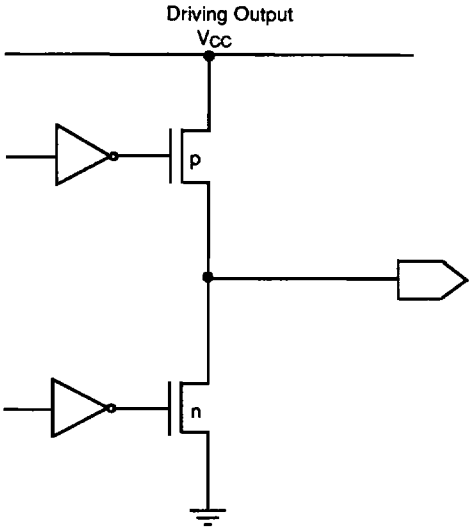
11068-044A

Equivalent Output Circuit (Q_n Outputs)



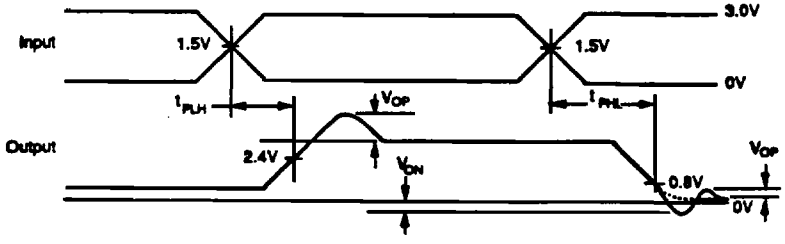
11068-045A

Equivalent Output Circuit ($\overline{RAS}_n$, $\overline{CAS}_n$ Outputs)



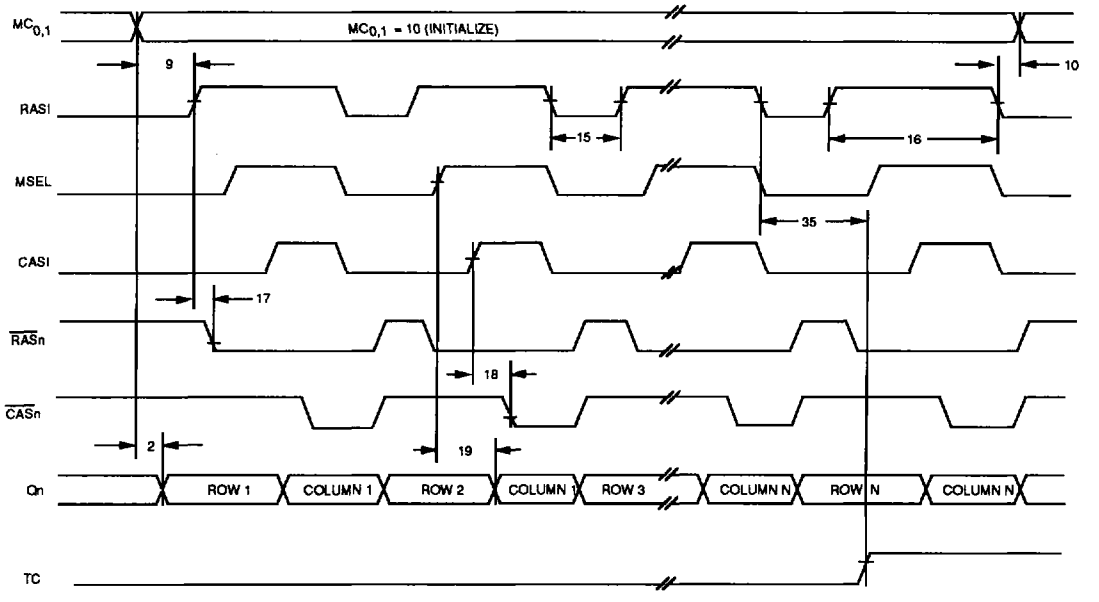
11068-046A

Equivalent Output Circuit
(All outputs except Q_n, $\overline{RAS}_n$, $\overline{CAS}_n$)



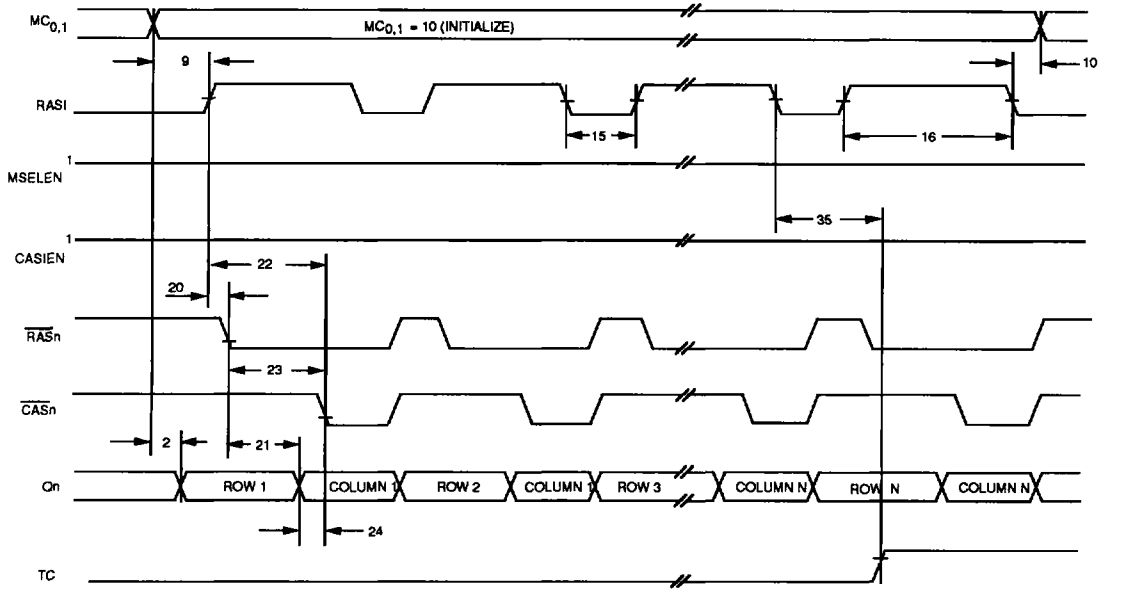
11068–041A

Output Drivers Level



11068-017A

Figure 13. EDC Initialization with External Timing



11068-018A

Figure 14. EDC Initialization with Auto-Timing

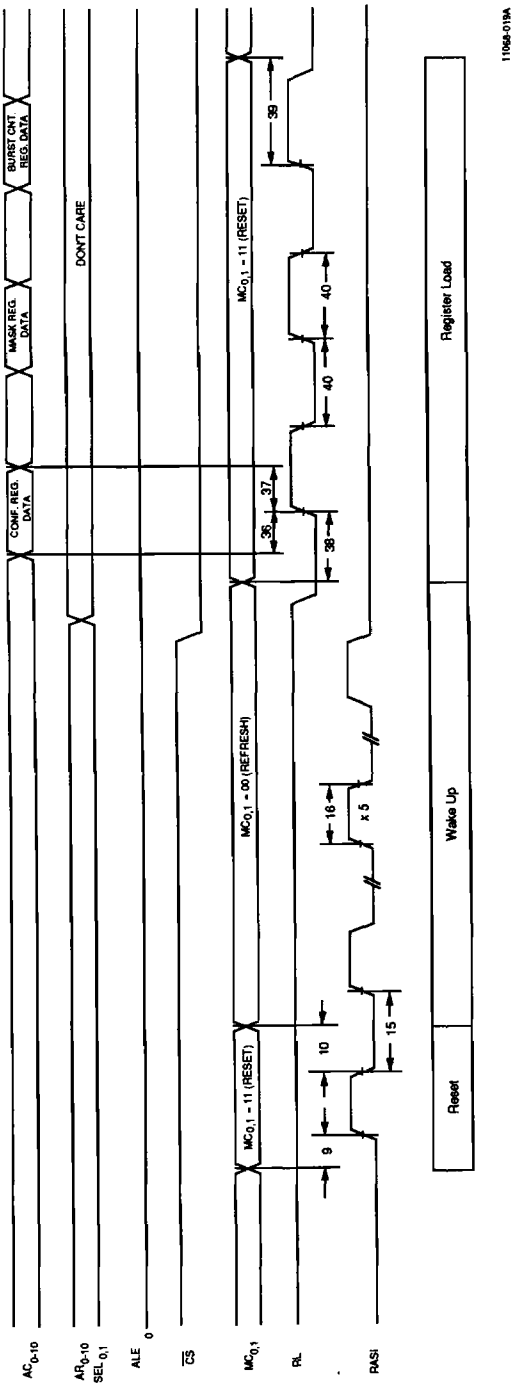
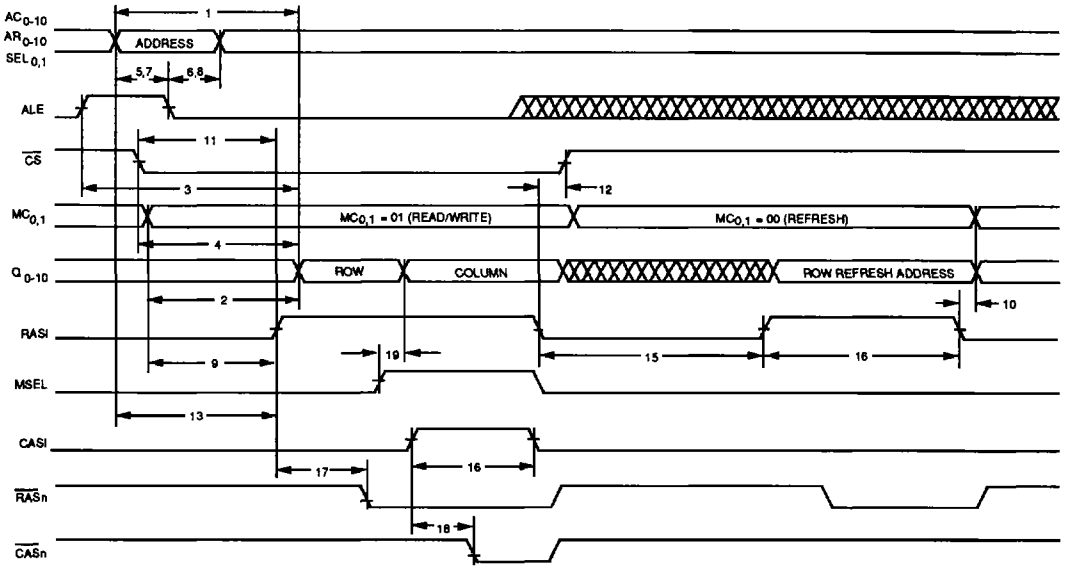
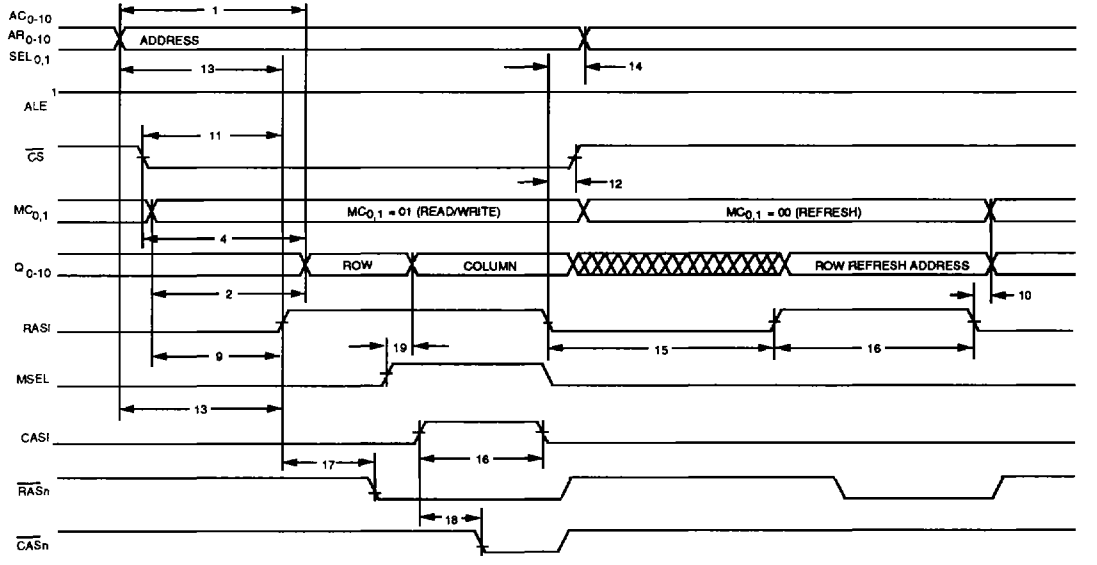


Figure 15. Reset, Wake Up, and Register Load Operation



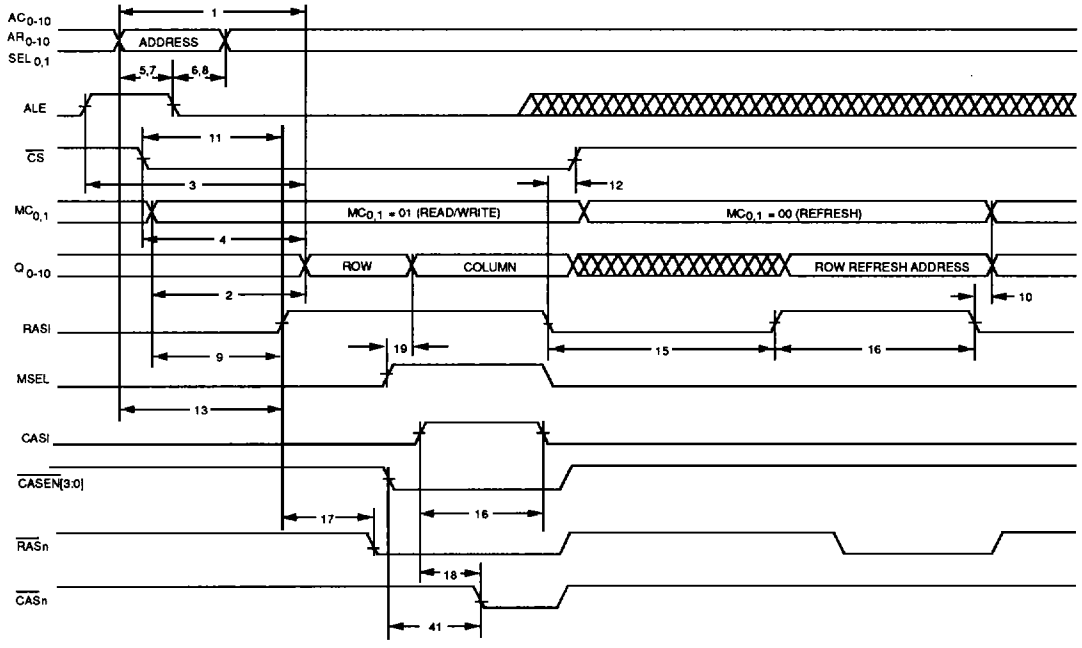
11068-020A

Figure 16. Standard Read/Write, Refresh Accesses with External Timing



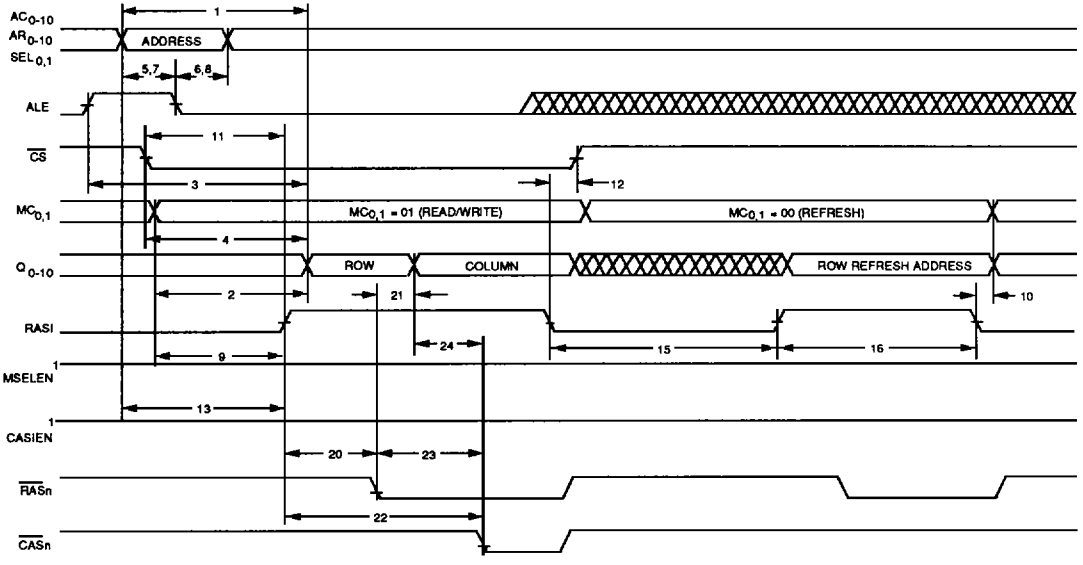
11068-021A

Figure 17. Standard Read/Write, Refresh Accesses with ALE = 1



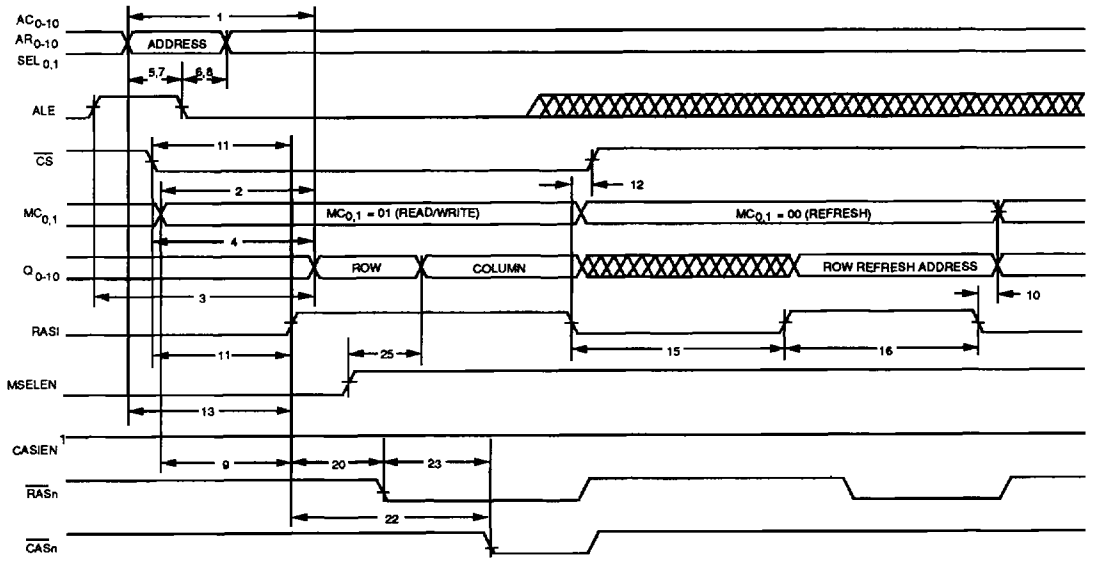
11068-022A

Figure 18. Standard Read/Write, Byte Access; Refresh (External Timing)



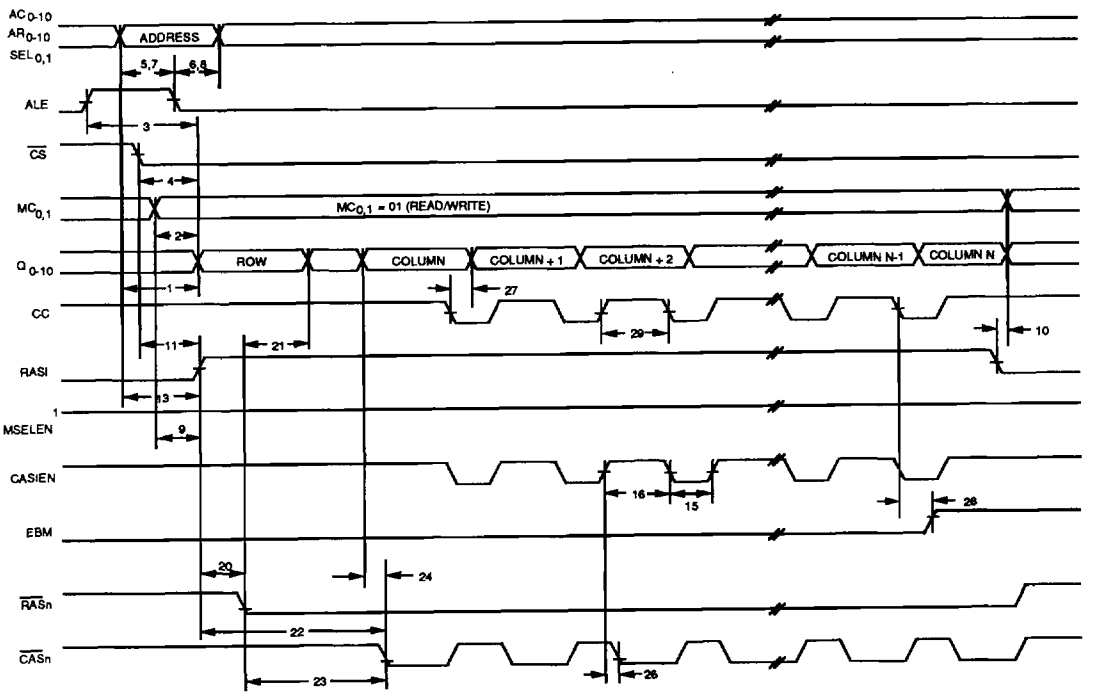
11068-023A

Figure 19. Standard Read/Write, Refresh Accesses with Auto-Timing



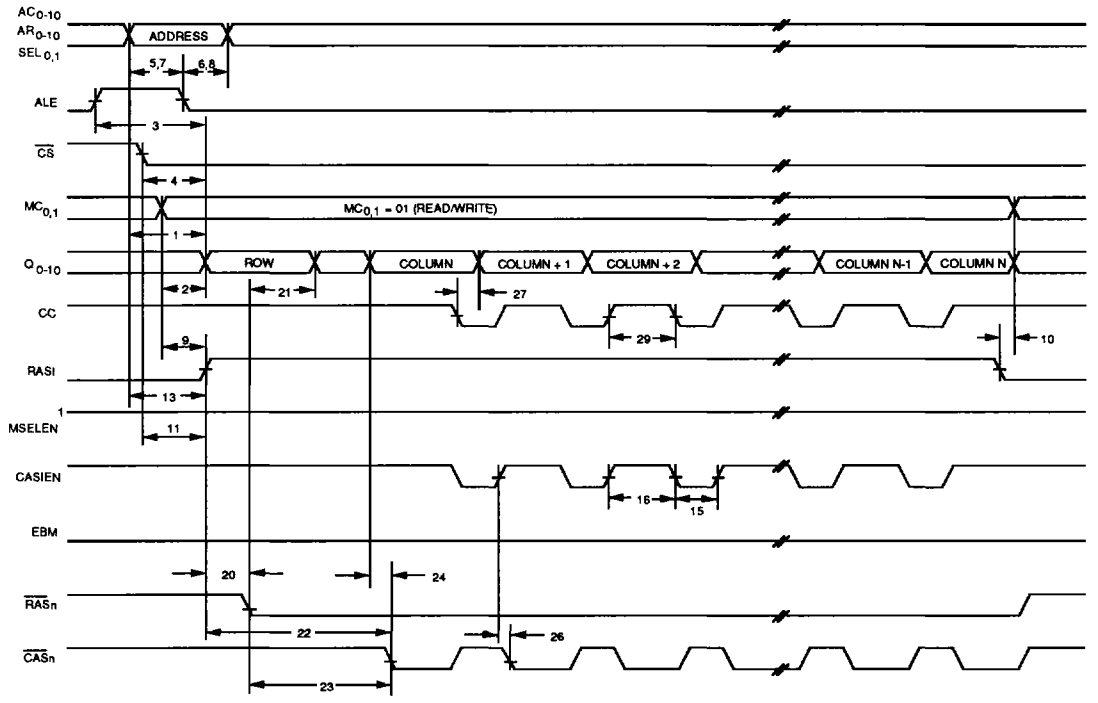
11068-024A

Figure 20. Read/Write, with Auto-Timing with External Override on MSELEN



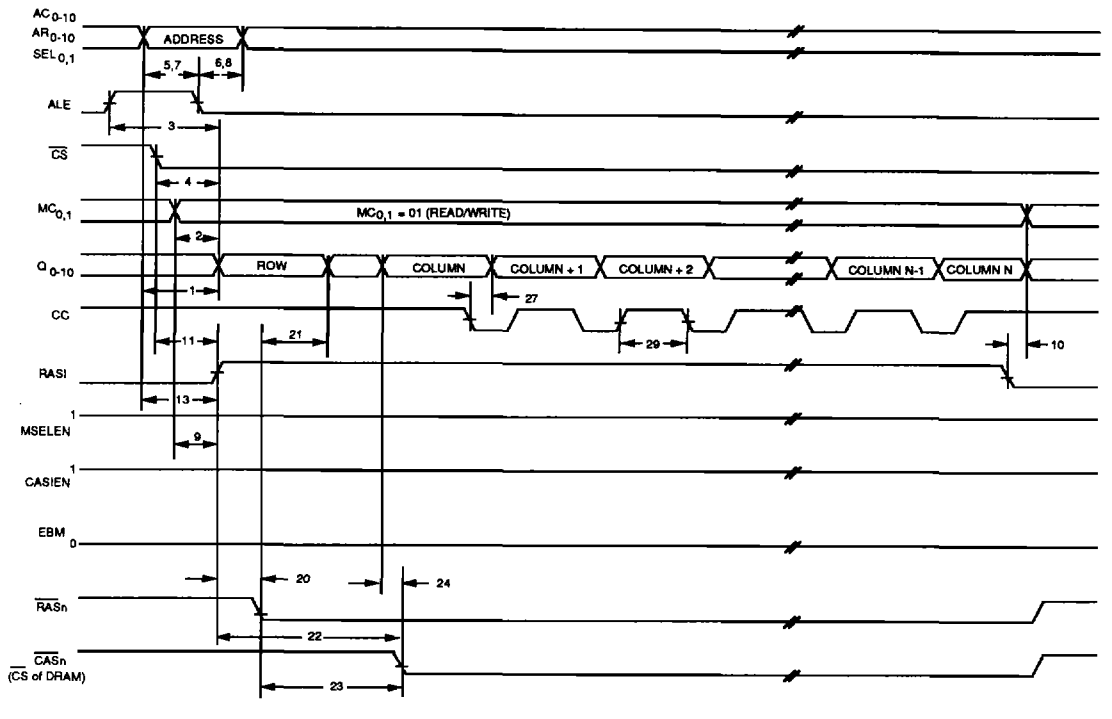
11068-025A

Figure 21. Burst Mode Access Ended by the Am29C668 (Auto-Timing with External Override)



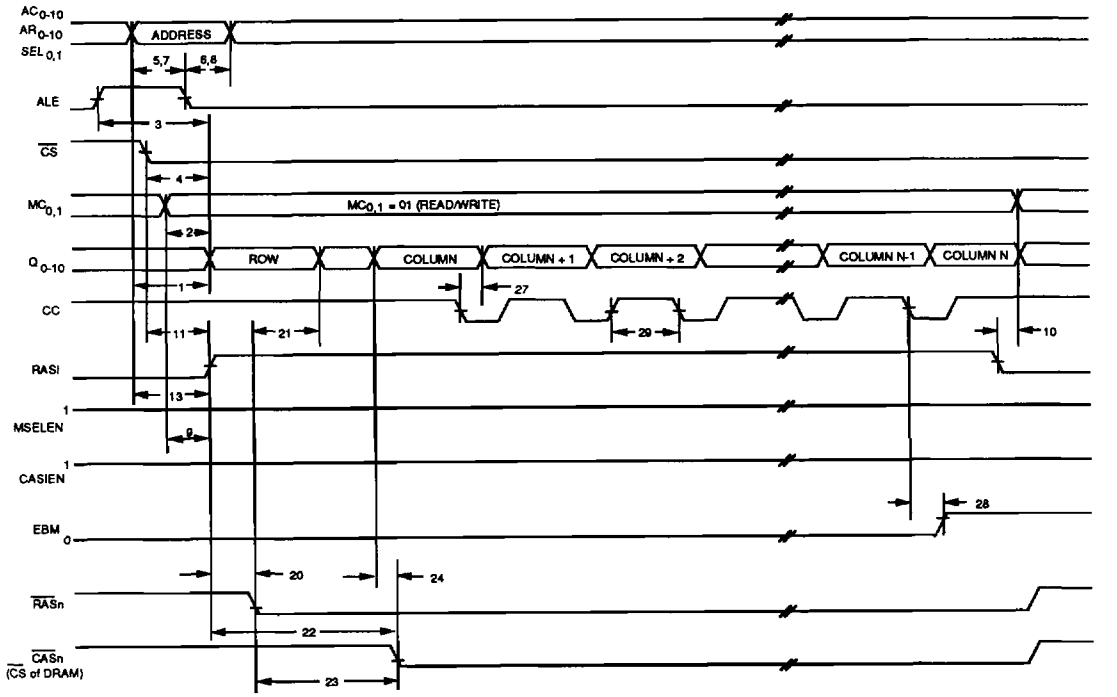
11068-026A

Figure 22. Burst Mode Access with Static Column DRAMs Ended by the Microprocessor (Auto-Timing)



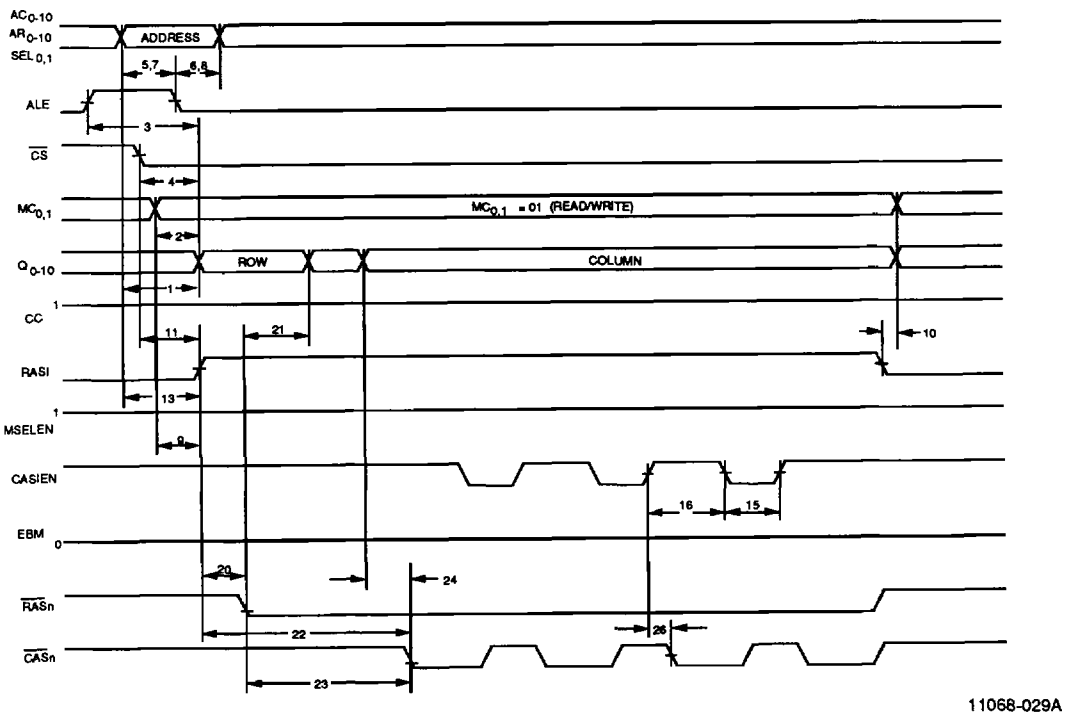
11068-027A

Figure 23. Burst Mode Access Ended by the Microprocessor (Auto-Timing with External Override)



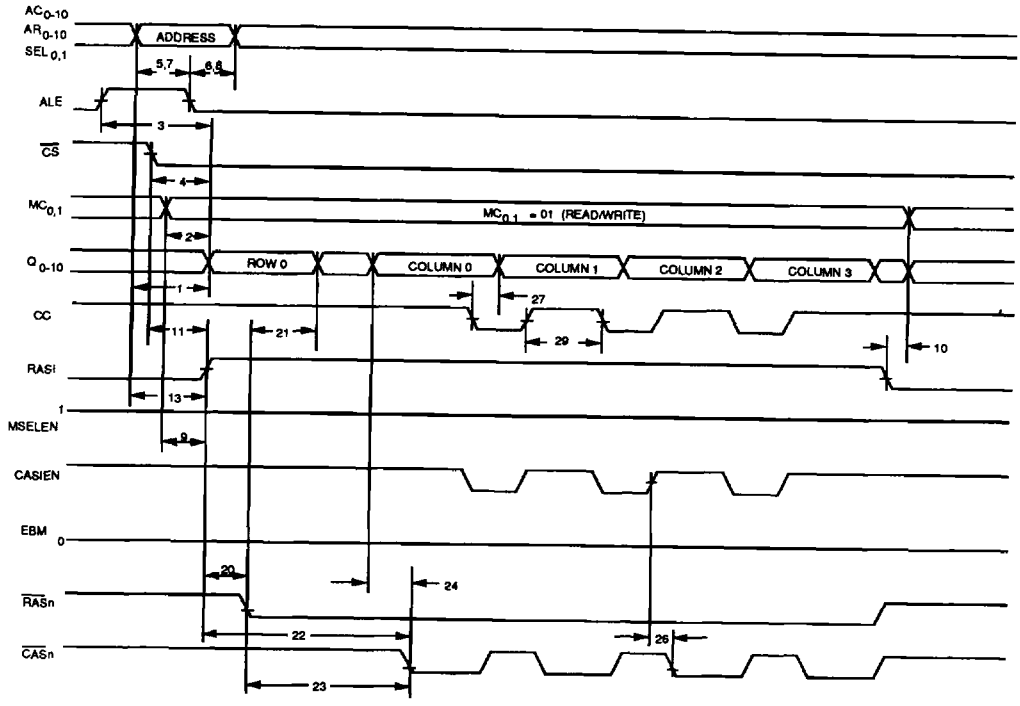
11068-028A

Figure 24. Burst Mode Access with Static Column DRAMs Ended by the Am29C668 (Auto-Timing)



11068-029A

Figure 25. Burst Mode Access with Nibble Mode DRAMs (Auto-Timing with External Override)



11068-030A

Figure 26. Nibble Mode Access with Page Mode DRAMs (Auto-Timing with External Override)

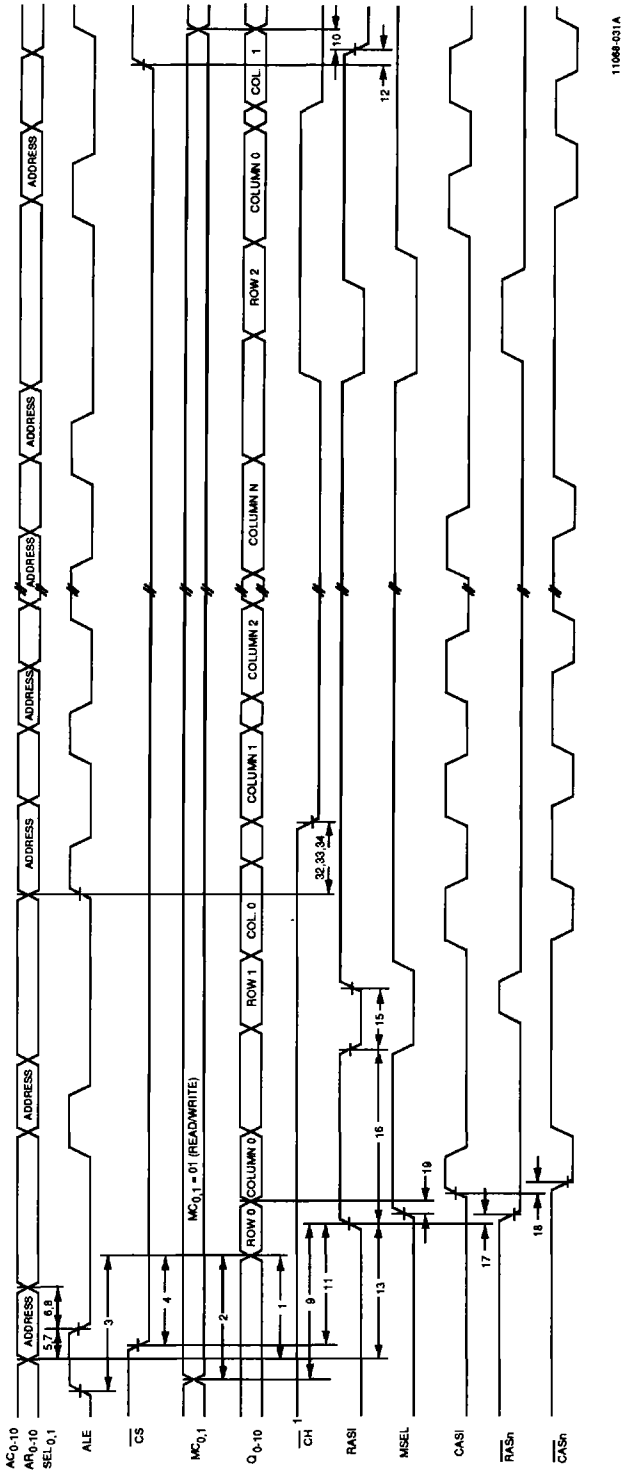


Figure 27. "Cache" Mode Access with Page Mode DRAMs (External Timing)

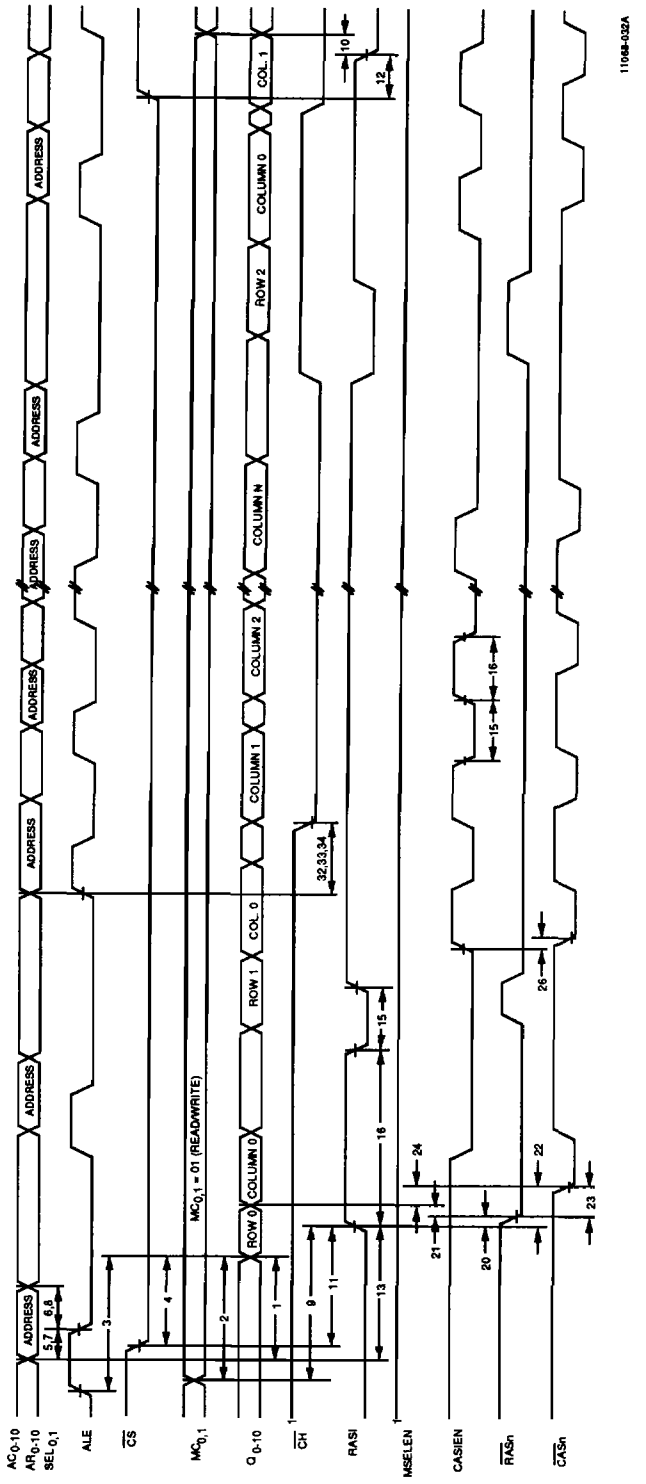


Figure 28. "Cache" Mode Access with Page Mode DRAMs (Auto-Timing with External Override)

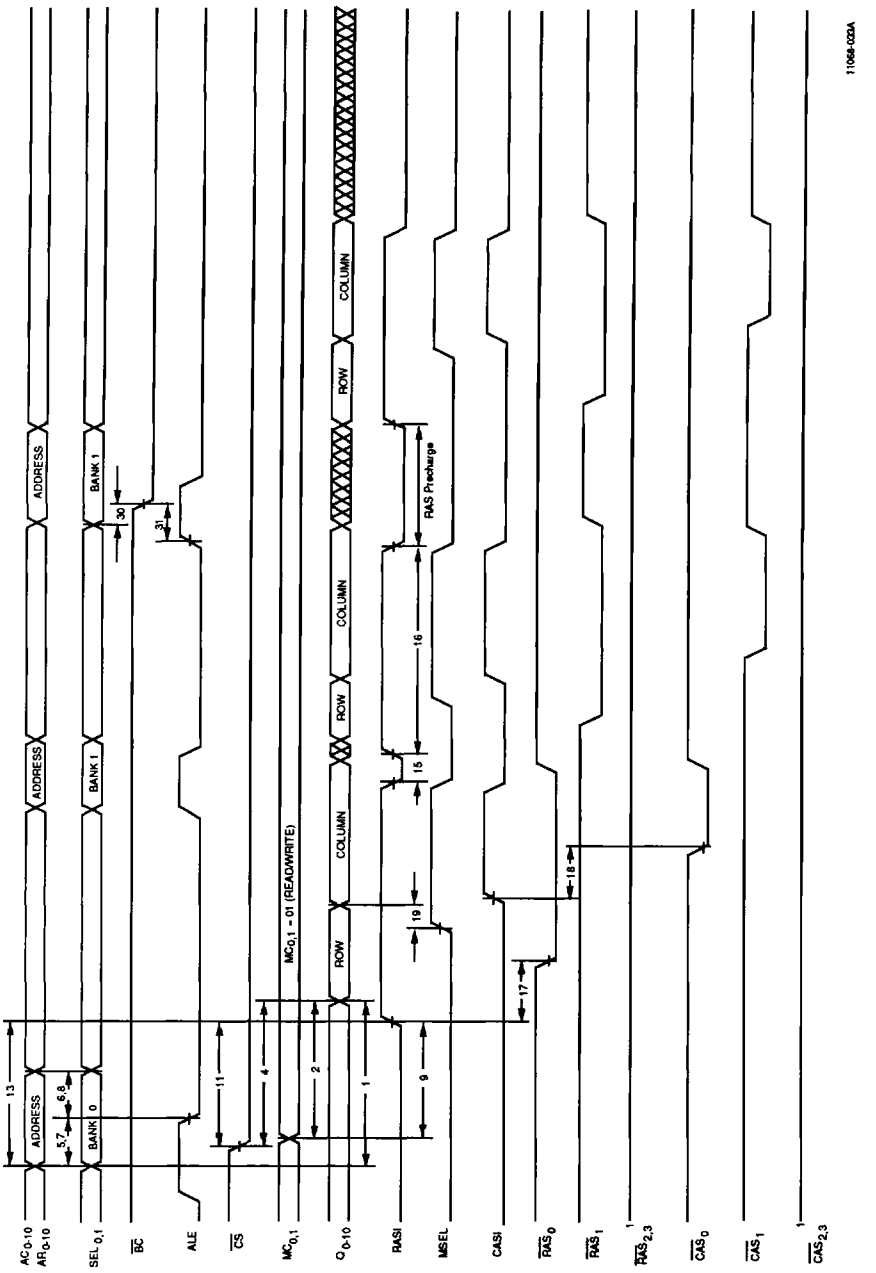


Figure 29. Bank Interleaved Accesses with External Timing

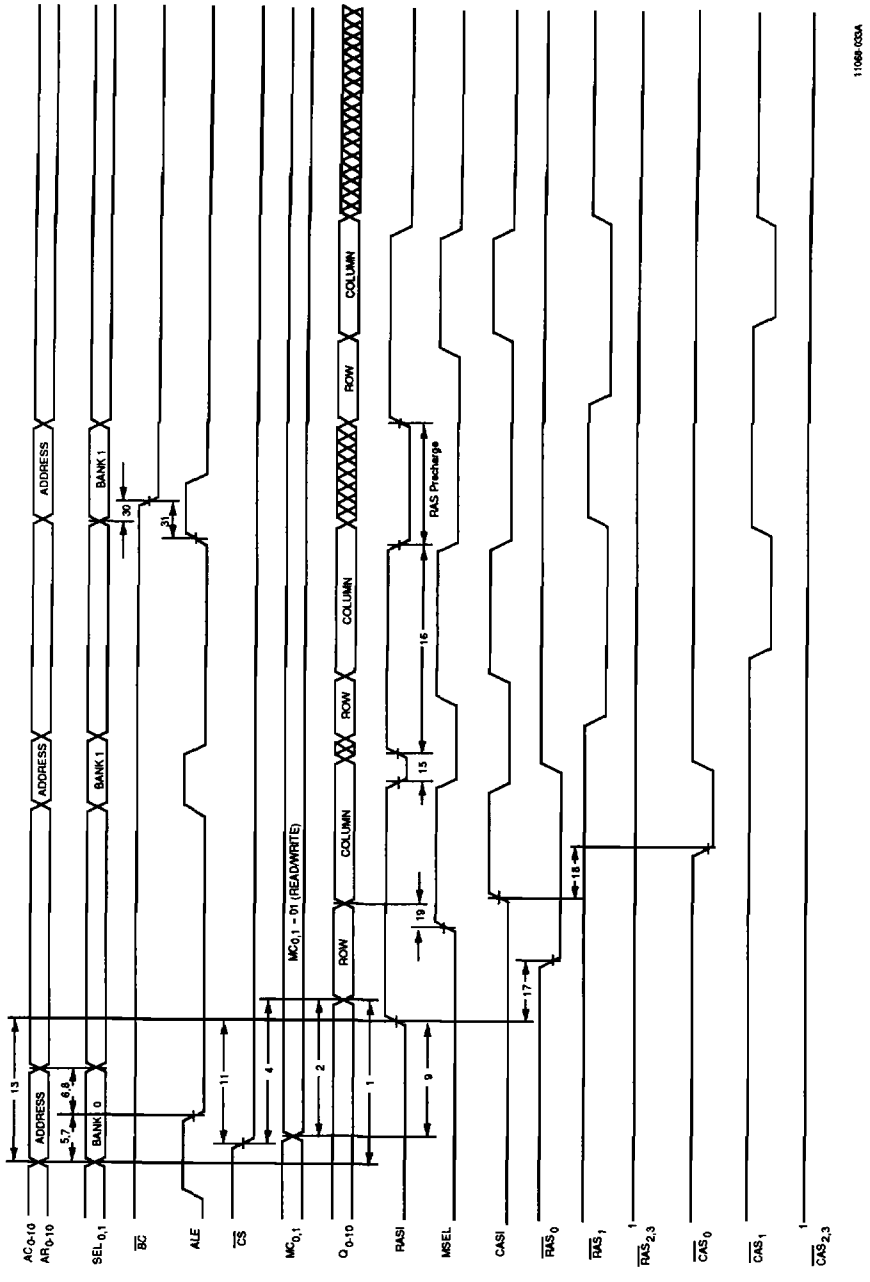


Figure 30. Bank Interleaved Accesses with Auto Timing