

μPD48576209

μPD48576218

μPD48576236

576M-BIT Low Latency DRAM Common I/O

R10DS0063EJ0300

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Description

The μPD48576209 is a 67,108,864-word by 9 bit, the μPD48576218 is a 33,554,432 word by 18 bit and the μPD48576236 is a 16,777,216 word by 36 bit synchronous double data rate Low Latency RAM fabricated with advanced CMOS technology using one-transistor memory cell.

The μPD48576209, μPD48576218 and μPD48576236 integrate unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (CK and CK#) are latched on the positive edge of CK and CK#. These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

Specification

- Density: 576M bit
- Organization
 - Common I/O: 8M words x 9 bits x 8 banks
4M words x 18 bits x 8 banks
2M words x 36 bits x 8 banks
- Operating frequency: 533 / 400 / 300 MHz
- Interface: HSTL I/O
- Package: 144-pin TAPE FBGA
 - Package size: 18.5 x 11
 - Leaded and Lead free
- Power supply
 - 2.5 V V_{EXT}
 - 1.8 V V_{DD}
 - 1.5 V or 1.8 V V_{DDQ}
- Refresh command
 - Auto Refresh
 - 16K cycle / 32 ms for each bank
 - 128K cycle / 32 ms for total
- Operating case temperature : T_c = 0 to 95°C

Features

- SRAM-type interface
- Double-data-rate architecture
- PLL circuitry
- Cycle time:
 - 1.875 ns @ t_{RC} = 15 ns
 - 2.5 ns @ t_{RC} = 15 ns
 - 2.5 ns @ t_{RC} = 20 ns
 - 3.3 ns @ t_{RC} = 20 ns
- Non-multiplexed addresses
- Multiplexing option is available.
- Data mask for WRITE commands
- Differential input clocks (CK and CK#)
- Differential input data clocks (DK and DK#)
- Data valid signal (QVLD)
- Programmable burst length: 2 / 4 / 8 (x9 / x18 / x36)
- User programmable impedance output (25 Ω - 60 Ω)
- JTAG boundary scan

Ordering Information

Part number	Cycle Time ns	Clock Frequency MHz	Random Cycle ns	Organization (word x bit)	Core Supply Voltage (V _{EXT}) V	Core Supply Voltage (V _{DD}) V	Output Supply Voltage (V _{DDQ}) V	Package
μPD48576209FF-E18-DW1-A	1.875	533	15	64 M x 9	2.5 + 0.13 2.5 – 0.12	1.8 ± 0.1	1.5 ± 0.1 or 1.8 ± 0.1	144-pin TAPE FBGA (18.5 x 11) Lead-free
μPD48576209FF-E24-DW1-A	2.5	400	15					
μPD48576209FF-E25-DW1-A	2.5	400	20					
μPD48576209FF-E33-DW1-A	3.3	300	20					
μPD48576218FF-E18-DW1-A	1.875	533	15	32 M x 18				
μPD48576218FF-E24-DW1-A	2.5	400	15					
μPD48576218FF-E25-DW1-A	2.5	400	20					
μPD48576218FF-E33-DW1-A	3.3	300	20					
μPD48576236FF-E18-DW1-A	1.875	533	15	16 M x 36				
μPD48576236FF-E24-DW1-A	2.5	400	15					
μPD48576236FF-E25-DW1-A	2.5	400	20					
μPD48576236FF-E33-DW1-A	3.3	300	20					
μPD48576209FF-E18-DW1	1.875	533	15	64 M x 9	2.5 + 0.13 2.5 – 0.12	1.8 ± 0.1	1.5 ± 0.1 or 1.8 ± 0.1	144-pin TAPE FBGA (18.5 x 11) Lead
μPD48576209FF-E24-DW1	2.5	400	15					
μPD48576209FF-E25-DW1	2.5	400	20					
μPD48576209FF-E33-DW1	3.3	300	20					
μPD48576218FF-E18-DW1	1.875	533	15	32 M x 18				
μPD48576218FF-E24-DW1	2.5	400	15					
μPD48576218FF-E25-DW1	2.5	400	20					
μPD48576218FF-E33-DW1	3.3	300	20					
μPD48576236FF-E18-DW1	1.875	533	15	16 M x 36				
μPD48576236FF-E24-DW1	2.5	400	15					
μPD48576236FF-E25-DW1	2.5	400	20					
μPD48576236FF-E33-DW1	3.3	300	20					

Pin Arrangement

indicates active LOW signal.

144-pin TAPE FBGA (18.5 x 11)
(Top View) [Common I/O x9]

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	Note 3 DNU	Note 3 DNU	VSSQ					VSSQ	DQ0	Note 3 DNU	VDD
C	VTT	Note 3 DNU	Note 3 DNU	VDDQ					VDDQ	DQ1	Note 3 DNU	VTT
D	Note 1 (A22)	Note 3 DNU	Note 3 DNU	VSSQ					VSSQ	QK0#	QK0	VSS
E	A21	Note 3 DNU	Note 3 DNU	VDDQ					VDDQ	DQ2	Note 3 DNU	A20
F	A5	Note 3 DNU	Note 3 DNU	VSSQ					VSSQ	DQ3	Note 3 DNU	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	BA2	A9	VSS	VSS					VSS	VSS	A4	A3
J	Note 2 NF	Note 2 NF	VDD	VDD					VDD	VDD	BA0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	BA1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	Note 3 DNU	Note 3 DNU	VSSQ					VSSQ	DQ4	Note 3 DNU	A19
P	A15	Note 3 DNU	Note 3 DNU	VDDQ					VDDQ	DQ5	Note 3 DNU	DM
R	VSS	Note 3 DNU	Note 3 DNU	VSSQ					VSSQ	DQ6	Note 3 DNU	VSS
T	VTT	Note 3 DNU	Note 3 DNU	VDDQ					VDDQ	DQ7	Note 3 DNU	VTT
U	VDD	Note 3 DNU	Note 3 DNU	VSSQ					VSSQ	DQ8	Note 3 DNU	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

- Notes 1.** Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to V_{SS}, or left open.
- 2.** No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to V_{SS}, or left open.
- 3.** Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to V_{SS}, or left open.

CK, CK#	: Input clock	TMS	: IEEE 1149.1 Test input
CS#	: Chip select	TDI	: IEEE 1149.1 Test input
WE#	: WRITE command	TCK	: IEEE 1149.1 Clock input
REF#	: Refresh command	TDO	: IEEE 1149.1 Test output
A0–A21	: Address inputs	VREF	: HSTL input reference input
A22	: Reserved for the future	VEXT	: Power Supply
BA0–BA2	: Bank address input	VDD	: Power Supply
DQ0–DQ8	: Data input/output	VDDQ	: DQ Power Supply
DK, DK#	: Input data clock	VSS	: Ground
DM	: Input data Mask	VSSQ	: DQ Ground
QK0, QK0#	: Output data clock	VTT	: Power Supply
QVLD	: Data Valid	NF	: No function
ZQ	: Output impedance matching	DNU	: Do not use

indicates active LOW signal.

144-pin TAPE FBGA (18.5 x 11)
(Top View) [Common I/O x18]

	1	2	3	4	5	6	7	8	9	10	11	12
A	V _{REF}	V _{SS}	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TMS	TCK
B	V _{DD}	Note 3 DNU	DQ4	V _{SSQ}					V _{SSQ}	DQ0	Note 3 DNU	V _{DD}
C	V _{TT}	Note 3 DNU	DQ5	V _{DDQ}					V _{DDQ}	DQ1	Note 3 DNU	V _{TT}
D	Note 1 (A22)	Note 3 DNU	DQ6	V _{SSQ}					V _{SSQ}	QK0#	QK0	V _{SS}
E	Note 1 (A21)	Note 3 DNU	DQ7	V _{DDQ}					V _{DDQ}	DQ2	Note 3 DNU	A20
F	A5	Note 3 DNU	DQ8	V _{SSQ}					V _{SSQ}	DQ3	Note 3 DNU	QVLD
G	A8	A6	A7	V _{DD}					V _{DD}	A2	A1	A0
H	BA2	A9	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A4	A3
J	Note 2 NF	Note 2 NF	V _{DD}	V _{DD}					V _{DD}	V _{DD}	BA0	CK
K	DK	DK#	V _{DD}	V _{DD}					V _{DD}	V _{DD}	BA1	CK#
L	REF#	CS#	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A14	A13
M	WE#	A16	A17	V _{DD}					V _{DD}	A12	A11	A10
N	A18	Note 3 DNU	DQ14	V _{SSQ}					V _{SSQ}	DQ9	Note 3 DNU	A19
P	A15	Note 3 DNU	DQ15	V _{DDQ}					V _{DDQ}	DQ10	Note 3 DNU	DM
R	V _{SS}	QK1	QK1#	V _{SSQ}					V _{SSQ}	DQ11	Note 3 DNU	V _{SS}
T	V _{TT}	Note 3 DNU	DQ16	V _{DDQ}					V _{DDQ}	DQ12	Note 3 DNU	V _{TT}
U	V _{DD}	Note 3 DNU	DQ17	V _{SSQ}					V _{SSQ}	DQ13	Note 3 DNU	V _{DD}
V	V _{REF}	ZQ	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TDO	TDI

Notes 1. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to V_{SS}, or left open.

2. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to V_{SS}, or left open.

3. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to V_{SS}, or left open.

CK, CK#	: Input clock	TMS	: IEEE 1149.1 Test input
CS#	: Chip select	TDI	: IEEE 1149.1 Test input
WE#	: WRITE command	TCK	: IEEE 1149.1 Clock input
REF#	: Refresh command	TDO	: IEEE 1149.1 Test output
A0–A20	: Address inputs	V _{REF}	: HSTL input reference input
A21–A22	: Reserved for the future	V _{EXT}	: Power Supply
BA0–BA2	: Bank address input	V _{DD}	: Power Supply
DQ0–DQ17	: Data input/output	V _{DDQ}	: DQ Power Supply
DK, DK#	: Input data clock	V _{SS}	: Ground
DM	: Input data Mask	V _{SSQ}	: DQ Ground
QK0–QK1, QK0#–QK1#	: Output data clock	V _{TT}	: Power Supply
QVLD	: Data Valid	NF	: No function
ZQ	: Output impedance matching	DNU	: Do not use

indicates active LOW signal.

144-pin TAPE FBGA (18.5 x 11)

(Top View) [Common I/O x36]

	1	2	3	4	5	6	7	8	9	10	11	12
A	V _{REF}	V _{SS}	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TMS	TCK
B	V _{DD}	DQ8	DQ9	V _{SSQ}					V _{SSQ}	DQ1	DQ0	V _{DD}
C	V _{TT}	DQ10	DQ11	V _{DDQ}					V _{DDQ}	DQ3	DQ2	V _{TT}
D	Note (A22)	DQ12	DQ13	V _{SSQ}					V _{SSQ}	QK0#	QK0	V _{SS}
E	Note (A21)	DQ14	DQ15	V _{DDQ}					V _{DDQ}	DQ5	DQ4	Note (A20)
F	A5	DQ16	DQ17	V _{SSQ}					V _{SSQ}	DQ7	DQ6	QVLD
G	A8	A6	A7	V _{DD}					V _{DD}	A2	A1	A0
H	BA2	A9	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A4	A3
J	DK0	DK0#	V _{DD}	V _{DD}					V _{DD}	V _{DD}	BA0	CK
K	DK1	DK1#	V _{DD}	V _{DD}					V _{DD}	V _{DD}	BA1	CK#
L	REF#	CS#	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A14	A13
M	WE#	A16	A17	V _{DD}					V _{DD}	A12	A11	A10
N	A18	DQ24	DQ25	V _{SSQ}					V _{SSQ}	DQ35	DQ34	A19
P	A15	DQ22	DQ23	V _{DDQ}					V _{DDQ}	DQ33	DQ32	DM
R	V _{SS}	QK1	QK1#	V _{SSQ}					V _{SSQ}	DQ31	DQ30	V _{SS}
T	V _{TT}	DQ20	DQ21	V _{DDQ}					V _{DDQ}	DQ29	DQ28	V _{TT}
U	V _{DD}	DQ18	DQ19	V _{SSQ}					V _{SSQ}	DQ27	DQ26	V _{DD}
V	V _{REF}	ZQ	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TDO	TDI

Note Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to V_{SS}, or left open.

CK, CK#	: Input clock	TMS	: IEEE 1149.1 Test input
CS#	: Chip select	TDI	: IEEE 1149.1 Test input
WE#	: WRITE command	TCK	: IEEE 1149.1 Clock input
REF#	: Refresh command	TDO	: IEEE 1149.1 Test output
A0–A19	: Address inputs	V _{REF}	: HSTL input reference input
A20–A22	: Reserved for the future	V _{EXT}	: Power Supply
BA0–BA2	: Bank address input	V _{DD}	: Power Supply
DQ0–DQ35	: Data input/output	V _{DDQ}	: DQ Power Supply
DK0–DK1, DK0#–DK1#	: Input data clock	V _{SS}	: Ground
DM	: Input data Mask	V _{SSQ}	: DQ Ground
QK0–QK1, QK0#–QK1#	: Output data clock	V _{TT}	: Power Supply
QVLD	: Data Valid		
ZQ	: Output impedance matching		

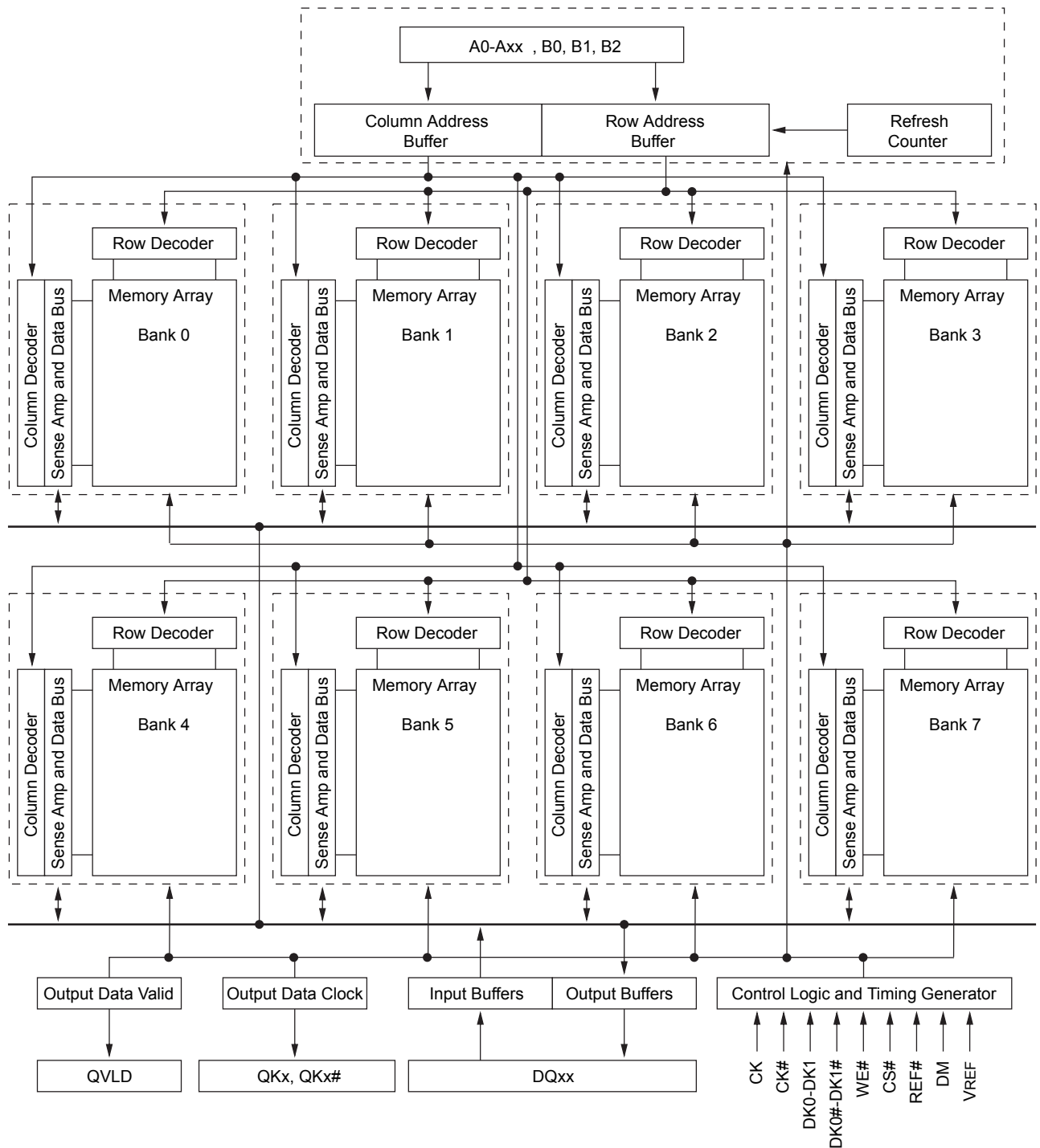
Pin Description

(1/2)

Symbol	Type	Description
CK, CK#	Input	Clock inputs: CK and CK# are differential clock inputs. This input clock pair registers address and control inputs on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip select CS# enables the commands when CS# is LOW and disables them when CS# is HIGH. When the command is disabled, new commands are ignored, but internal operations continue.
WE#, REF#	Input	WRITE command pin, Refresh command pin: WE#, REF# are sampled at the positive edge of CK, WE#, and REF# define (together with CS#) the command to be executed.
A0–A21	Input	Address inputs: A0–A21 define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK. In the x36 configuration, A20–A21 are reserved for address expansion; in the x18 configuration, A21 is reserved for address expansion. These expansion addresses can be treated as address inputs, but they do not affect the operation of the device.
A22	Input	Reserved for future use: These signals should be tied to V _{SS} or leave open.
BA0–BA2	Input	Bank address inputs; Select to which internal bank a command is being applied.
DQx–DQxx	Input /Output	Data input/output: The DQ signals form the 9/18/36 bit data bus. During READ commands, the data is referenced to both edges of QKx. During WRITE commands, the data is sampled at both edges of DKx. x 9 device uses DQ0 to DQ8. x18 device uses DQ0 to DQ17. x36 device uses DQ0 to DQ35.
QKx, QKx#	Output	Output data clocks: QKx and QKx# are opposite polarity, output data clocks. They are always free running and edge-aligned with data output from the μPD48576209/18/36. QKx# is ideally 180 degrees out of phase with QKx. For the x36 device, QK0 and QK0# are aligned with DQ0–DQ17. QK1 and QK1# are aligned with DQ18–DQ35. For the x18 device, QK0 and QK0# are aligned with DQ0–DQ8. QK1 and QK1# are aligned with DQ9–DQ17. For the x9 device, QK0 and QK0# are aligned with DQ0–DQ8.
DKx, DKx#	Input	Input data clock; DKx and DKx# are the differential input data clocks. All input data is referenced to both edges of DK. DK# is ideally 180 degrees out of phase with DK. For the x36 device, DQ0–DQ17 are referenced to DK0 and DK0#, and DQ18–DQ35 are referenced to DK1 and DK1#. For the x9 and x18 devices, all DQs are referenced to DK and DK#.
DM	Input	Input data mask; The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH along with the WRITE input data. DM is sampled on both edges of DK (DK1 for the x36 configuration). The signal should be V _{SS} if not used.
QVLD	Output	Data valid; The QVLD indicates valid output data. QVLD is edge-aligned with QKx and QKx#.

Symbol	Type	Description
ZQ	Input /Output	External impedance [25 Ω – 60 Ω]; This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 x RQ, where RQ is a resistor from this signal to V _{SS} . Connecting ZQ to V _{SS} invokes the minimum impedance mode. Connecting ZQ to V _{DDQ} invokes the maximum impedance mode. Refer to Figure 2-5. Mode Register Bit Map to activate this function.
TMS , TDI	Input	JTAG function pins: IEEE 1149.1 test inputs: These balls may be left as no connects if the JTAG function is not used in the circuit
TCK	Input	JTAG function pin; IEEE 1149.1 clock input: This ball must be tied to V _{SS} if the JTAG function is not used in the circuit.
TDO	Output	JTAG function pin; IEEE 1149.1 test output: JTAG output. This ball may be left as no connect if JTAG function is not used.
V _{REF}	Input	Input reference voltage; Nominally V _{DDQ} /2. Provides a reference voltage for the input buffers.
V _{EXT}	Supply	Power supply; 2.5 V nominal. See Recommended DC Operating Conditions for range.
V _{DD}	Supply	Power supply; 1.8 V nominal. See Recommended DC Operating Conditions for range.
V _{DDQ}	Supply	DQ power supply; Nominally, 1.5 V or 1.8 V. Isolated on the device for improved noise immunity. See Recommended DC Operating Conditions for range.
V _{SS}	Supply	Ground
V _{SSQ}	Supply	DQ ground; Isolated on the device for improved noise immunity.
V _{TT}	Supply	Power supply; Isolated termination supply. Nominally, V _{DDQ} /2. See Recommended DC Operating Conditions for range.
NF		No function; These balls may be connected to V _{SS} .
DNU		Do not use; These balls may be connected to V _{SS} .

Block Diagram



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1. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V _{EXT}		-0.3 to +2.8	V
Supply voltage	V _{DD}		-0.3 to +2.1	V
Output supply voltage, Input voltage, Input / Output voltage	V _{DDQ}		-0.3 to +2.1	V
Input / Output voltage	V _{IH} / V _{IL}		-0.3 to +2.1	V
Junction temperature	T _j MAX.		110	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

0°C ≤ T_C ≤ 95°C; 1.7 V ≤ V_{DD} ≤ 1.9 V, unless otherwise noted.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V _{EXT}		2.38	2.5	2.63	V	1
Supply voltage	V _{DD}		1.7	1.8	1.9	V	1
Output supply voltage	V _{DDQ}		1.4		V _{DD}	V	1, 2, 3
Reference Voltage	V _{REF}		0.49 x V _{DDQ}	0.5 x V _{DDQ}	0.51 x V _{DDQ}	V	1, 4, 5
Termination voltage	V _{TT}		0.95 x V _{REF}	V _{REF}	1.05 x V _{REF}	V	1, 6
Input HIGH voltage	V _{IH(DC)}		V _{REF} + 0.1			V	1
Input LOW voltage	V _{IL(DC)}				V _{REF} - 0.1	V	1

Notes 1. All voltage referenced to V_{SS} (GND).

2. During normal operation, V_{DDQ} must not exceed V_{DD}.
3. V_{DDQ} can be set to a nominal 1.5 V ± 0.1 V or 1.8 V ± 0.1 V supply.
4. Typically the value of V_{REF} is expected to be 0.5 x V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
5. Peak-to-peak AC noise on V_{REF} must not exceed ± 2% V_{REF(DC)}.
6. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

DC Characteristics

0°C ≤ T_C ≤ 95°C; 1.7 V ≤ V_{DD} ≤ 1.9 V, unless otherwise noted

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Note
Input leakage current	I _{LI}		-5	+5	μA	1,2
Output leakage current	I _{LO}		-5	+5	μA	1,2
Reference voltage current	I _{REF}		-5	+5	μA	1,2
Output high current	I _{OH}	V _{OH} = V _{DDQ} /2	(V _{DDQ} /2) / (1.15 × R _Q /5)	(V _{DDQ} /2) / (0.85 × R _Q /5)	mA	3,4
Output low current	I _{OL}	V _{OL} = V _{DDQ} /2	(V _{DDQ} /2) / (1.15 × R _Q /5)	(V _{DDQ} /2) / (0.85 × R _Q /5)	mA	3,4

- Notes**
1. Outputs are impedance-controlled. | I_{OH} | = (V_{DDQ}/2)/(R_Q/5) for values of 125 Ω ≤ R_Q ≤ 300 Ω.
 2. Outputs are impedance-controlled. I_{OL} = (V_{DDQ}/2)/(R_Q/5) for values of 125 Ω ≤ R_Q ≤ 300 Ω.
 3. I_{OH} and I_{OL} are defined as absolute values and are measured at V_{DDQ}/2. I_{OH} flows from the device, I_{OL} flows into the device.
 4. If MRS bit A8 is 0, use R_Q = 250 Ω in the equation in lieu of presence of an external impedance matched resistor.

Capacitance (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Address / Control Input capacitance	C _{IN}	V _{IN} = 0 V	1.5	2.5	pF
I/O, Output, Other capacitance (DQ, DM, QK, QVLD)	C _{I/O}	V _{I/O} = 0 V	3.5	5.0	pF
Clock Input capacitance	C _{clk}	V _{clk} = 0 V	2.0	3.0	pF
JTAG pins	C _J	V _J = 0 V	2.0	5.0	pF

Remark These parameters are periodically sampled and not 100% tested.
Capacitance is not tested on ZQ pin.

Recommended AC Operating Conditions

0°C ≤ T_C ≤ 95°C; 1.7 V ≤ V_{DD} ≤ 1.9 V, unless otherwise noted

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Input HIGH voltage	V _{IH(AC)}		V _{REF} + 0.2		V	1
Input LOW voltage	V _{IL(AC)}			V _{REF} - 0.2	V	1

Note 1. Overshoot: V_{IH(AC)} ≤ V_{DDQ} + 0.7 V for t ≤ t_{CK}/2

Undershoot: V_{IL(AC)} ≥ -0.5 V for t ≤ t_{CK}/2

Control input signals may not have pulse widths less than t_{CKH} (MIN.) or operate at cycle rates less than t_{CK} (MIN.).

DC Characteristics

I_{DD} / I_{SB} Operating Conditions

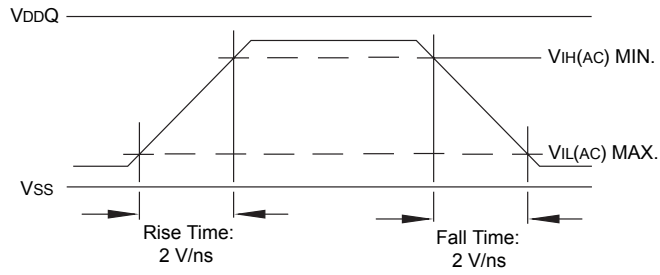
Parameter	Symbol	Test condition	MAX.				Unit		
			-E18	-E24	-E25	-E33			
Standby current	I _{SB1}	t _{CK} = Idle All banks idle, no inputs toggling	V _{DD}	x9/x18	55	55	55	55	mA
				x36	55	55	55	55	
			V _{EXT}	5	5	5	5		
Active standby current	I _{SB2}	CS# = HIGH, No commands, half bank / address / data change once every four clock cycles	V _{DD}	x9/x18	250	215	215	190	mA
				x36	250	215	215	190	
			V _{EXT}	5	5	5	5		
Operating current	I _{DD1}	BL=2, sequential bank access, bank transitions once every t _{RC} , half address transitions once every t _{RC} , read followed by write sequence, continuous data during WRITE commands.	V _{DD}	x9/x18	390	331	321	291	mA
				x36	407	346	336	306	
			V _{EXT}	10	10	10	10		
Operating current	I _{DD2}	BL=4, sequential bank access, bank transitions once every t _{RC} , half address transitions once every t _{RC} , read followed by write sequence, continuous data during WRITE commands.	V _{DD}	x9/x18	422	367	357	336	mA
				x36	445	387	377	353	
			V _{EXT}	10	10	10	10		
Operating current	I _{DD3}	BL=8, sequential bank access, bank transitions once every t _{RC} , half address transitions once every t _{RC} , read followed by write sequence, continuous data during WRITE commands.	V _{DD}	x9/x18	439	381	371	350	mA
				x36	488	419	409	388	
			V _{EXT}	15	15	15	15		
Burst refresh current	I _{REF1}	Eight bank cyclic refresh, continuous address/data, command bus remains in refresh for all banks	V _{DD}	x9/x18	692	540	540	419	mA
				x36	670	545	545	430	
			V _{EXT}	45	30	30	25		
Disturbed refresh current	I _{REF2}	Single bank refresh, sequential bank access, half address transitions once every t _{RC} , continuous data	V _{DD}	x9/x18	286	265	260	194	mA
				x36	295	265	260	215	
			V _{EXT}	10	10	10	10		
Operating burst write current	I _{DD2W}	BL=2, cyclic bank access, half of address bits change every clock cycle, continuous data, measurement is taken during continuous WRITE	V _{DD}	X9/x18	1078	872	872	716	mA
				X36	1105	891	891	731	
			V _{EXT}	40	35	35	30		
Operating burst write current	I _{DD4W}	BL=4, cyclic bank access, half of address bits change every two clocks, continuous data, measurement is taken during continuous WRITE	V _{DD}	x9/x18	784	645	645	538	mA
				x36	832	681	681	565	
			V _{EXT}	25	20	20	20		
Operating burst write current	I _{DD8W}	BL=8, cyclic bank access, half of address bits change every four clocks, continuous data, measurement is taken during continuous WRITE	V _{DD}	x9/x18	625	520	520	442	mA
				x36	706	579	579	487	
			V _{EXT}	25	20	20	20		
Operating burst read current	I _{DD2R}	BL=2, cyclic bank access, half of address bits change every clock cycle, measurement is taken during continuous READ	V _{DD}	x9/x18	949	735	735	566	mA
				x36	999	779	779	601	
			V _{EXT}	40	35	35	30		
Operating burst read current	I _{DD4R}	BL=4, cyclic bank access, half of address bits change every two clocks, measurement is taken during continuous READ	V _{DD}	x9/x18	659	503	503	400	mA
				x36	685	535	535	424	
			V _{EXT}	25	20	20	20		
Operating burst read current	I _{DD8R}	BL=8, cyclic bank access, half of address bits change every four clocks, measurement is taken during continuous READ	V _{DD}	x9/x18	497	389	389	308	mA
				x36	567	441	441	349	
			V _{EXT}	25	20	20	20		

- Remarks 1.** I_{DD} specifications are tested after the device is properly initialized. $0^{\circ}\text{C} \leq T_{\text{C}} \leq 95^{\circ}\text{C}$; $1.7\text{ V} \leq V_{\text{DD}} \leq 1.9\text{ V}$, $2.38\text{ V} \leq V_{\text{EXT}} \leq 2.63\text{ V}$, $1.4\text{ V} \leq V_{\text{DDQ}} \leq V_{\text{DD}}$, $V_{\text{REF}} = V_{\text{DDQ}}/2$
2. $t_{\text{CK}} = t_{\text{DK}} = \text{MIN.}$, $t_{\text{RC}} = \text{MIN.}$
 3. Input slew rate is specified in **Recommended DC Operating Conditions** and **Recommended AC Operating Conditions**.
 4. I_{DD} parameters are specified with ODT disabled.
 5. Continuous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycles (twice per clock).
 6. Continuous address is defined as half the address signals between HIGH and LOW every clock cycles (once per clock).
 7. Sequential bank access is defined as the bank address incrementing by one every t_{RC} .
 8. Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL=4 this is every other clock.
 9. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than per clock cycle.

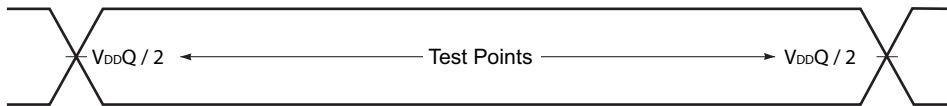
AC Characteristics

AC Test Conditions

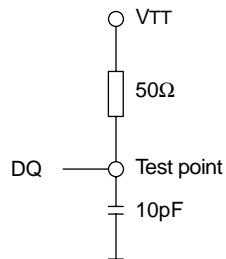
Input waveform



Output waveform



Output load condition



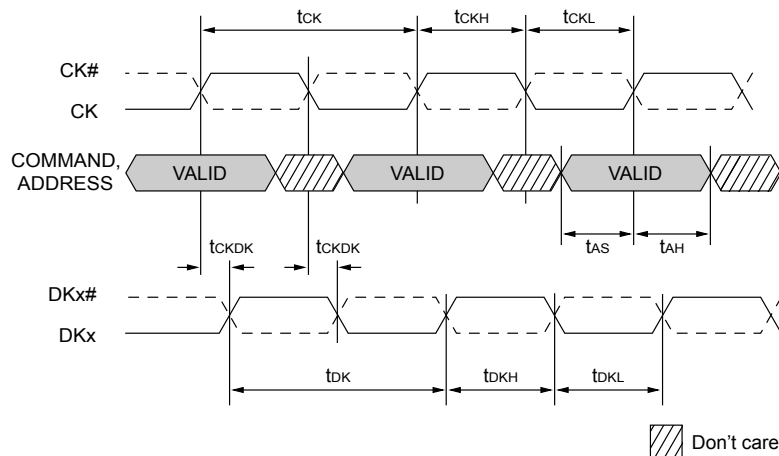
AC Characteristics <Read and Write Cycle>

Parameter	Symbol	-E18 (533 MHz)		-E24 (400 MHz)		-E25 (400 MHz)		-E33 (300 MHz)		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock											
Clock cycle time (CK,CK#,DK,DK#)	t _{CK} , t _{DK}	1.875	5.7	2.5	5.7	2.5	5.7	3.3	5.7	ns	
Clock frequency (CK,CK#,DK,DK#)	t _{CK} , t _{DK}	175	533	175	400	175	400	175	300	MHz	
Random Cycle time	t _{RC}	15		15		20		20		ns	
Clock Jitter: period	t _{JIT PER}	-100	100	-150	150	-150	150	-200	200	ps	1, 2
Clock Jitter: cycle-to-cycle	t _{JIT CC}		200		300		300		400	ps	
Clock HIGH time (CK,CK#,DK,DK#)	t _{CKH} , t _{DKH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	Cycle	
Clock LOW time (CK,CK#,DK,DK#)	t _{CKL} , t _{DKL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	Cycle	
Clock to input data clock	t _{CKDK}	-0.3	0.3	-0.45	0.5	-0.45	0.5	-0.45	1.0	ns	
Mode register set cycle time to any command	t _{MRSC}	6		6		6		6		Cycle	
PLL Lock time	t _{CK Lock}	15		15		15		15		μs	
Clock static to PLL reset	t _{CK Reset}	30		30		30		30		ns	
Output Times											
Output data clock HIGH time	t _{QKH}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t _{CKH}	
Output data clock LOW time	t _{QKL}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t _{CKL}	
QK edge to clock edge skew	t _{CKQK}	-0.2	0.2	-0.25	0.25	-0.25	0.25	-0.3	0.3	ns	
QK edge to output data edge	t _{QKQ0} , t _{QKQ1}	-0.12	0.12	-0.2	0.2	-0.2	0.2	-0.25	0.25	ns	3, 5
QK edge to any output data	t _{QKQ}	-0.22	0.22	-0.3	0.3	-0.3	0.3	-0.35	0.35	ns	4, 5
QK edge to QVLD	t _{QKVLD}	-0.22	0.22	-0.3	0.3	-0.3	0.3	-0.35	0.35	ns	
Setup Times											
Address/command and input	t _{AS} /t _{CS}	0.3		0.4		0.4		0.5		ns	
Data-in and data mask to DK	t _{DS}	0.17		0.25		0.25		0.3		ns	
Hold Times											
Address/command and input	t _{AH} /t _{CH}	0.3		0.4		0.4		0.5		ns	
Data-in and data mask to DK	t _{DH}	0.17		0.25		0.25		0.3		ns	

- Notes**
1. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
 2. Frequency drift is not allowed.
 3. t_{QKQ0} is referenced to DQ0–DQ17 in x36 and DQ0–DQ8 in x18.
t_{QKQ1} is referenced to DQ18–DQ35 in x36 and DQ9–DQ17 in x18.
 4. t_{QKQ} takes into account the skew between any QKx and any DQ.
 5. t_{QKQ}, t_{QKQX} are guaranteed by design.

Remark All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V_{REF} of the command, address, and data signals.

Figure 1-1. Clock / Input Data Clock Command / Address Timings



Temperature and Thermal Impedance

Temperature Limits

Parameter	Symbol	MIN.	MAX.	Unit	Note
Reliability junction temperature	T _J	0	+110	°C	1
Operating junction temperature	T _J	0	+100	°C	2
Operating case temperature	T _c	0	+95	°C	3

- Notes**
1. Temperatures greater than 110°C may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or above this is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the part.
 2. Junction temperature depends upon cycle time, loading, ambient temperature, and airflow.
 3. MAX operating case temperature; T_c is measured in the center of the package. Device functionality is not guaranteed if the device exceeds maximum T_c during operation.

Thermal Impedance

Substrate	Ball	θ _{ja} (°C/W)			θ _{jb} (°C/W)	θ _{jc} (°C/W)
		Air Flow = 0 m/s	Air Flow = 1 m/s	Air Flow = 2 m/s		
4 - Layer	Lead	21.49	17.33	16.15	10.29	1.22
4 - Layer	Lead free	21.32	17.18	16.01	10.13	1.22

2. Operation

2.1 Command Operation

According to the functional signal description, the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

Table 2-1. Address Widths at Different Burst Lengths

Burst Length	Configuration		
	x9	x18	x36
BL=2	A0–A21	A0–A20	A0–A19
BL=4	A0–A20	A0–A19	A0–A18
BL=8	A0–A19	A0–A18	A0–A17

Table 2-2. Command Table

Operation	Code	CS#	WE#	REF#	A0–An ^{Note1}	BA0–BA2	Note
Device DESELECT / No Operation	DESEL / NOP	H	X	X	X	X	
MRS: Mode Register Set	MRS	L	L	L	OPCODE	X	2
READ	READ	L	H	H	A	BA	3
WRITE	WRITE	L	L	H	A	BA	3
AUTO REFRESH	AREF	L	H	L	X	BA	

- Notes**
1. n = 21.
 2. Only A0–A17 are used for the MRS command.
 3. See **Table 2-1**.

Remark X = “Don’t Care”, H = logic HIGH, L = logic LOW, A = valid address, BA = valid bank address

2.2 Description of Commands

DESEL / NOP^{Note1}

The NOP command is used to perform a no operation to the μPD48576209/18/36, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.

MRS

The mode register is set via the address inputs A0–A17. See **Figure 2-5. Mode Register Bit Map** for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress.

READ

The READ command is used to initiate a burst read access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A21 selects the data location within the bank.

WRITE

The WRITE command is used to initiate a burst write access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A21 selects the data location within the bank. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written).

AREF

The AREF is used during normal operation of the μPD48576209/18/36 to refresh the memory content of a bank. The command is non-persistent, so it must be issued each time a refresh is required. The value on the BA0–BA2 inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a “Don’t Care” during the AREF command. The μPD48576209/18/36 requires 64K cycles at an average periodic interval of $0.244\mu\text{s}$ ^{Note2} (MAX.). To improve efficiency, eight AREF commands (one for each bank) can be posted to μPD48576209/18/36 at periodic intervals of $1.95\mu\text{s}$ ^{Note3}.

Within a period of 32 ms, the entire memory must be refreshed. The delay between the AREF command and a subsequent command to same bank must be at least t_{RC} as continuous refresh. Other refresh strategies, such as burst refresh, are also possible.

Notes 1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.

2. Actual refresh is $32\text{ ms} / 16\text{k} / 8 = 0.244\mu\text{s}$.

3. Actual refresh is $32\text{ ms} / 16\text{k} = 1.95\mu\text{s}$.

2.3 Initialization

The μPD48576209/18/36 must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device. The following sequence is used for Power-Up:

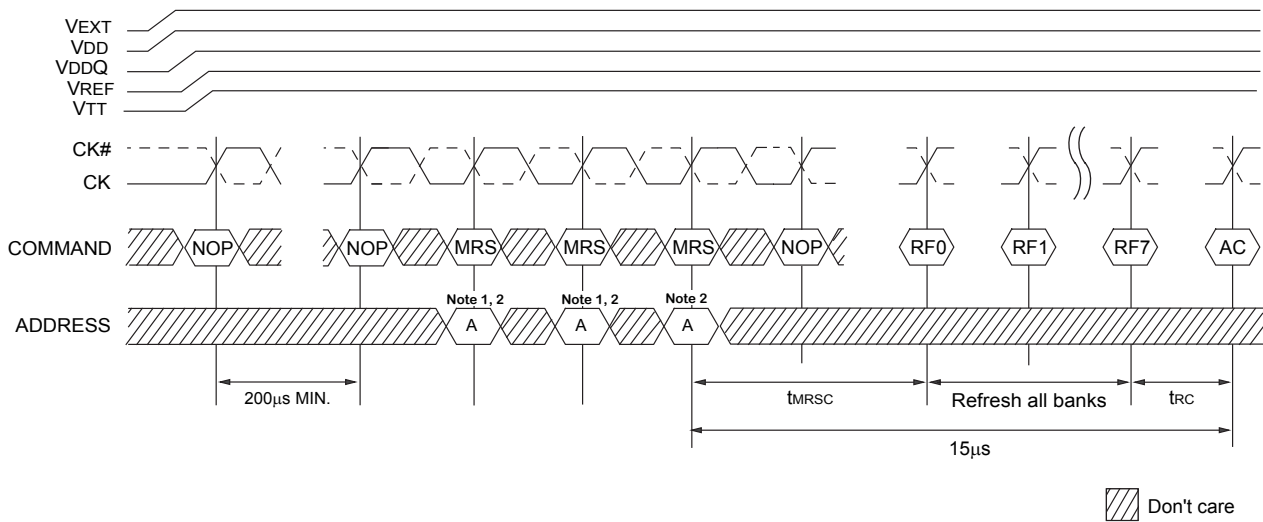
1. Apply power (V_{EXT} , V_{DD} , V_{DDQ} , V_{REF} , V_{TT}) and start clock as soon as the supply voltages are stable. Apply V_{DD} and V_{EXT} before or at the same time as V_{DDQ} . Apply V_{DDQ} before or at the same time as V_{REF} and V_{TT} . Although there is no timing relation between V_{EXT} and V_{DD} , the chip starts the power-up sequence only after both voltages are at their nominal levels. V_{DDQ} supply must not be applied before V_{DD} supply. $CK/CK\#$ must meet $V_{ID(DC)}$ prior to being applied. Maintain all remaining balls in NOP conditions.

Note No rule of apply power sequence is the design target.

2. Maintain stable conditions for $200\mu\text{s}$ (MIN.).
3. Issue at least three or more consecutive MRS commands: two dummies or more plus one valid MRS. It is recommended that all address pins are held LOW during the dummy MRS commands.
4. t_{MRSC} after valid MRS, an AUTO REFRESH command to all 8 banks must be issued and wait for $15\mu\text{s}$ with $CK/CK\#$ toggling in order to lock the PLL prior to normal operation.
5. After t_{RC} , the chip is ready for normal operation.

2.4 Power-On Sequence

Figure 2-1. Power-Up Sequence



- Notes 1. Recommended all address pins held LOW during dummy MRS commands.
- 2. A10-A17 must be LOW.

Remark MRS : MRS command
 RFp : REFRESH bank p
 AC : Any command

2.5 Programmable Impedance Output Buffer

The μPD48576209/18/36 is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and V_{SS}. The value of the resistor must be five times the desired impedance. For example, a 300 Ω resistor is required for an output impedance of 60 Ω. To ensure that output impedance is one fifth the value of RQ (within 15 percent), the range of RQ is 125 Ω to 300 Ω. Output impedance updates may be required because, over time, variations may occur in supply voltage and temperature. The device samples the value of RQ. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update.

2.6 PLL Reset

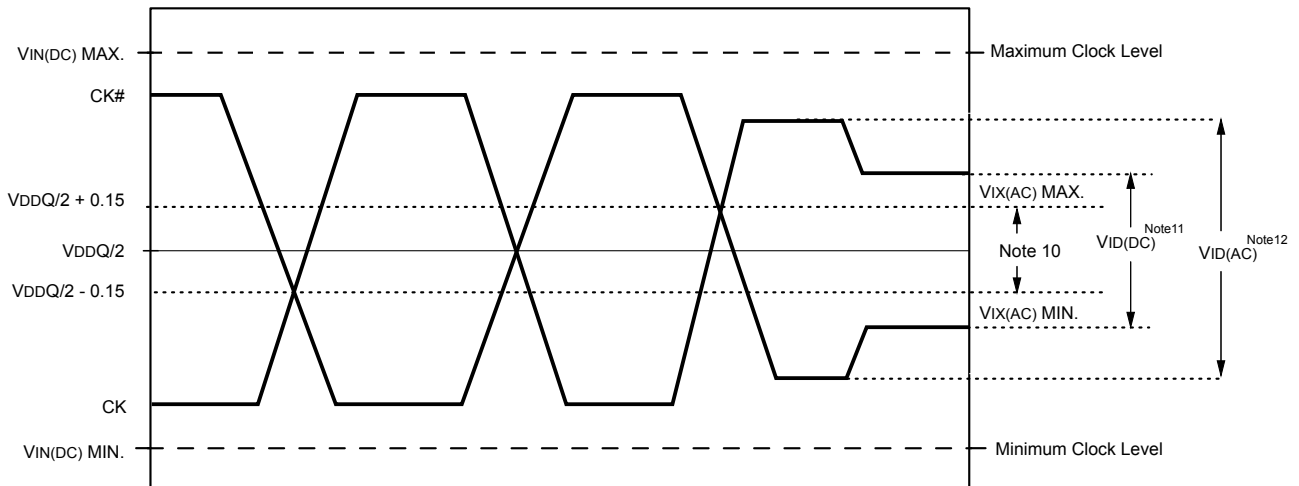
The μPD48576209/18/36 utilizes internal Phase-locked loops for maximum output, data valid windows. It can be placed into a stopped-clock state to minimize power with a modest restart time of 15 μs. The clock (CK/CK#) must be toggled for 15 μs in order to stabilize PLL circuits for next READ operation.

2.7 Clock Input

Table 2-3. Clock Input Operation Conditions

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock Input Voltage Level	V _{IN(DC)}	CK and CK#	-0.3	V _{DDQ} + 0.3	V	
Clock Input Differential Voltage Level	V _{ID(DC)}	CK and CK#	0.2	V _{DDQ} + 0.6	V	8
Clock Input Differential Voltage Level	V _{ID(AC)}	CK and CK#	0.4	V _{DDQ} + 0.6	V	8
Clock Input Crossing Point Voltage Level	V _{IX(AC)}	CK and CK#	V _{DDQ} /2 - 0.15	V _{DDQ} /2 + 0.15	V	9

Figure 2-2. Clock Input



Notes 1. DKx and DKx# have the same requirements as CK and CK#.

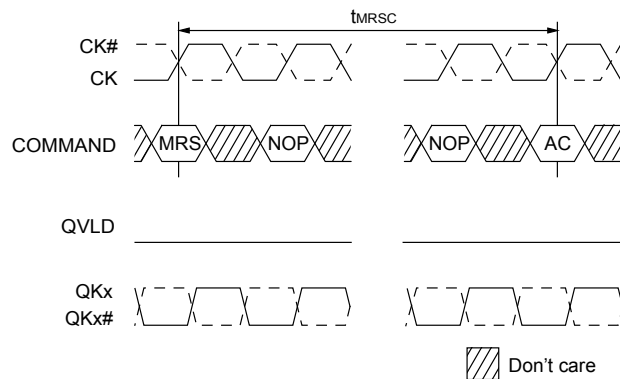
2. All voltages referenced to V_{SS} .
3. Tests for AC timing, I_{DD} and electrical AC and DC characteristics may be conducted at normal reference/supply voltage levels; but the related specifications and device operations are tested for the full voltage range specified.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or the crossing point for CK/CK#), and parameters specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the HSTL Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above[below] the DC input LOW[HIGH] level).
6. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signal other than CK/CK# is V_{REF} .
7. CK and CK# input slew rate must be $\geq 2V/ns$ ($\geq 4V/ns$ if measured differentially).
8. V_{ID} is the magnitude of the difference between the input level on CK and input level on CK#.
9. The value of V_{IX} is expected to equal $V_{DDQ}/2$ of the transmitting device and must track variations in the DC level of the same.
10. CK and CK# must cross within the region.
11. CK and CK# must meet at least $V_{ID(DC)}$ (MIN.) when static and centered around $V_{DDQ}/2$.
12. Minimum peak-to-peak swing.

2.8 Mode Register Set Command (MRS)

The mode register stores the data for controlling the operating modes of the memory. It programs the μPD48576209/18/36 configuration, burst length, and I/O options. During a MRS command, the address inputs A0–A17 are sampled and stored in the mode register. t_{MRSC} must be met before any command can be issued to the μPD48576209/18/36. The mode register may be set at any time during device operation. However, any pending operations are not guaranteed to successfully complete, and all memory cell data are not guaranteed.

Since MRS is used for internal test mode entry, bits A10–A17 must be set to all “0” at the MRS setting.

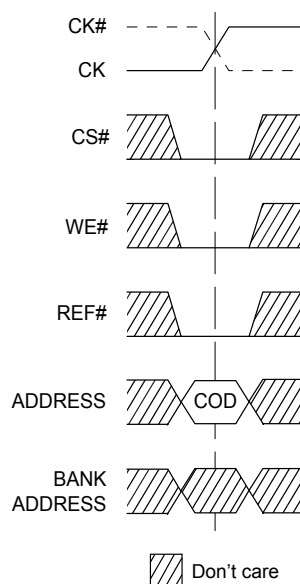
Figure 2-3. Mode Register Set Timing



Remark MRS: MRS command

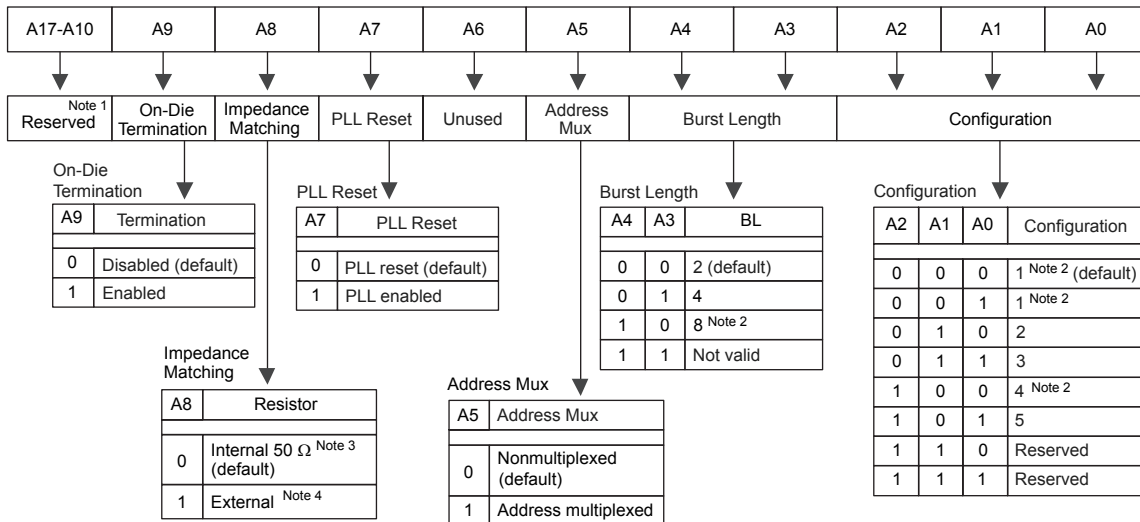
AC : any command

Figure 2-4. Mode Register Set



Remark COD: code to be loaded into the register.

Figure 2-5. Mode Register Bit Map



Notes 1. Bits A10–A17 must be set to all ‘0’. A18–An are “Don’t Care”.

2. BL=8 is not available for configuration 1 and 4.
3. ±30% temperature variation.
4. Within 15%.

2.9 Read & Write configuration (Non Multiplexed Address Mode)

Table 2-4 shows, for different operating frequencies, the different μPD48576209/18/36 configurations that can be programmed into the mode register. The READ and WRITE latency (t_{RL} and t_{WL}) values along with the row cycle times (t_{RC}) are shown in clock cycles as well as in nanoseconds.

Table 2-4. Configuration Table

Parameter	Configuration					Unit
	1 ^{Note2}	2	3	4 ^{Note2, 3}	5	
t _{RC}	4	6	8	3	5	t _{CK}
t _{RL}	4	6	8	3	5	t _{CK}
t _{WL}	5	7	9	4	6	t _{CK}
Valid frequency range	266-175	400-175	533-175	200-175	333-175	MHz

Notes 1. Apply to the entire table. t_{RC} < 20 ns in any configuration only available with –E24 and –E18 speed grades.

2. BL= 8 is not available.
3. The minimum t_{RC} is typically 3 cycles, except in the case of a WRITE followed by a READ to the same bank. In this instance the minimum t_{RC} is 4 cycles.

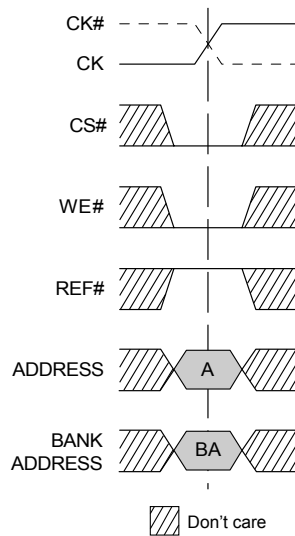
2.10 Write Operation (WRITE)

Write accesses are initiated with a WRITE command, as shown in **Figure 2-6**. Row and bank addresses are provided together with the WRITE command. During WRITE commands, data will be registered at both edges of DK according to the programmed burst length (BL). A WRITE latency (WL) one cycle longer than the programmed READ latency (RL + 1) is present, with the first valid data registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command. **Figure 2-10. WRITE Followed By READ: BL=2, RL=4, WL=5, Configuration 1** and **Figure 2-11. WRITE Followed By READ: BL=4, RL=4, WL=5, Configuration 1** illustrate the timing requirements for a WRITE followed by a READ for bursts of two and four, respectively.

Setup and hold times for incoming input data relative to the DK edges are specified as t_{DS} and t_{DH} . The input data is masked if the corresponding DM signal is HIGH. The setup and hold times for data mask are also t_{DS} and t_{DH} .

Figure 2-6. WRITE Command



Remark A : Address
 BA: Bank address

Figure 2-7. Basic WRITE Burst / DM Timing

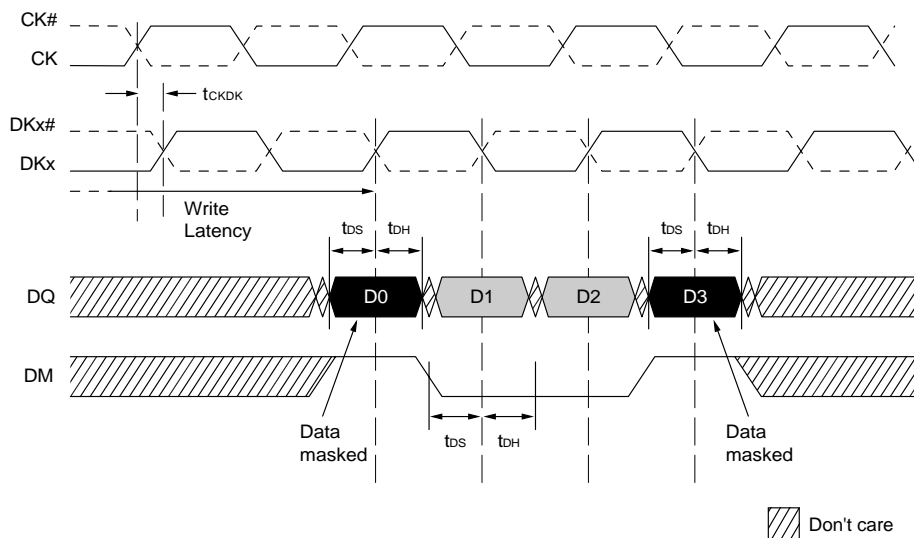


Figure 2-8. WRITE Burst Basic Sequence: BL=2, RL=4, WL=5, Configuration 1

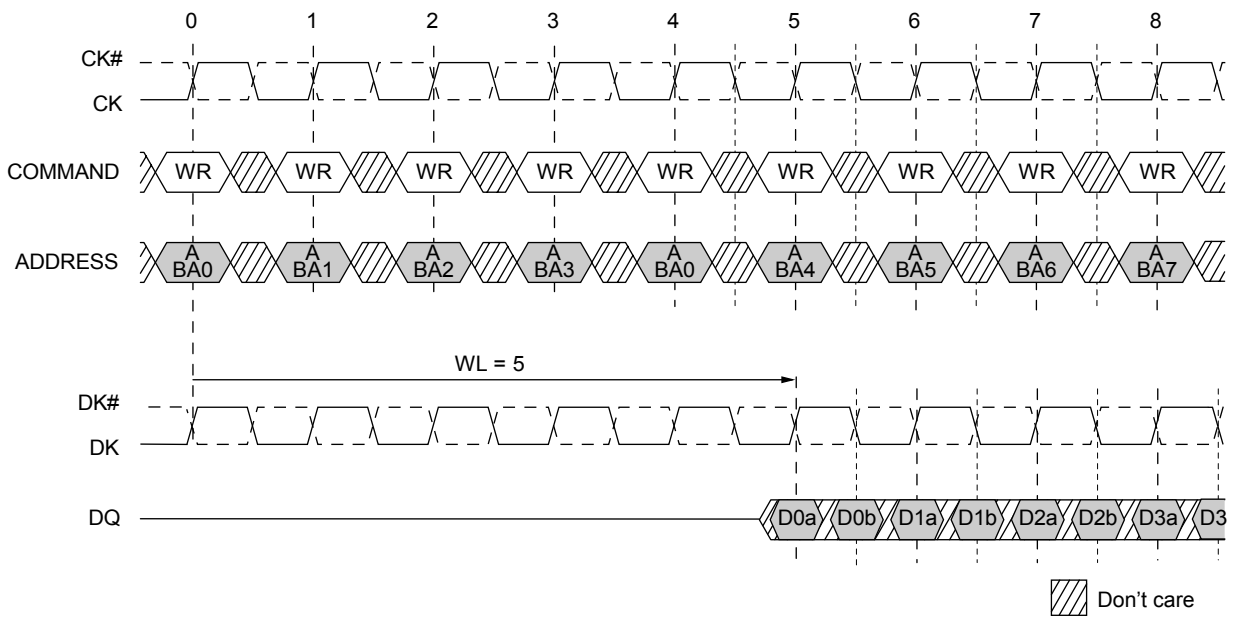
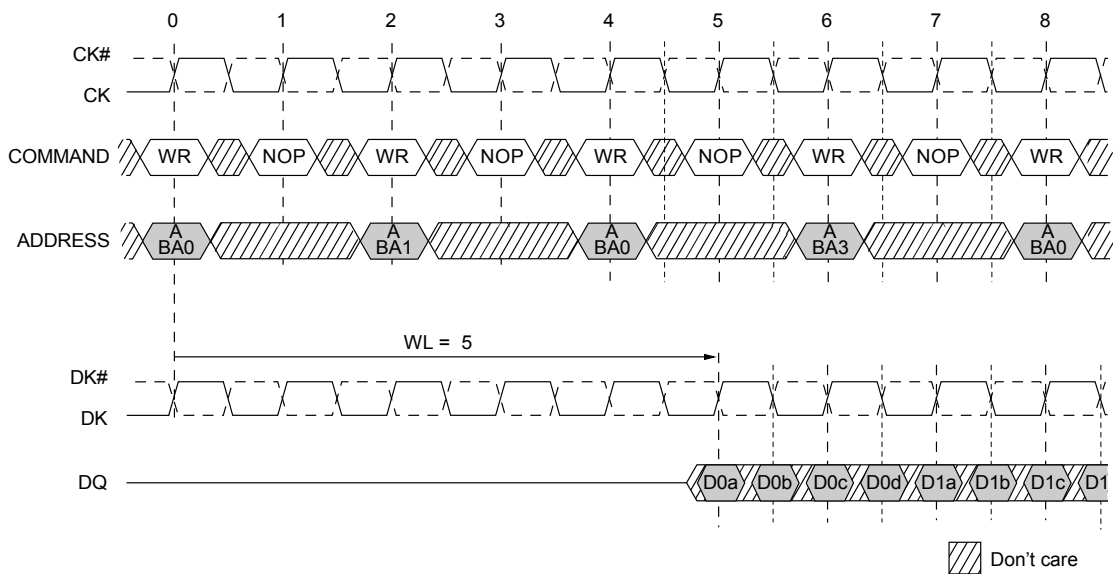


Figure 2-9. WRITE Burst Basic Sequence: BL=4, RL=4, WL=5, Configuration 1



- Remarks 1.**
- WR : WRITE command
 - A/Bap : Address A of bank p
 - WL : WRITE latency
 - Dpq : Data q to bank p

2. Any free bank may be used in any given command. The sequence shown is only one example of a bank sequence.

Figure 2-10. WRITE Followed By READ: BL=2, RL=4, WL=5, Configuration 1

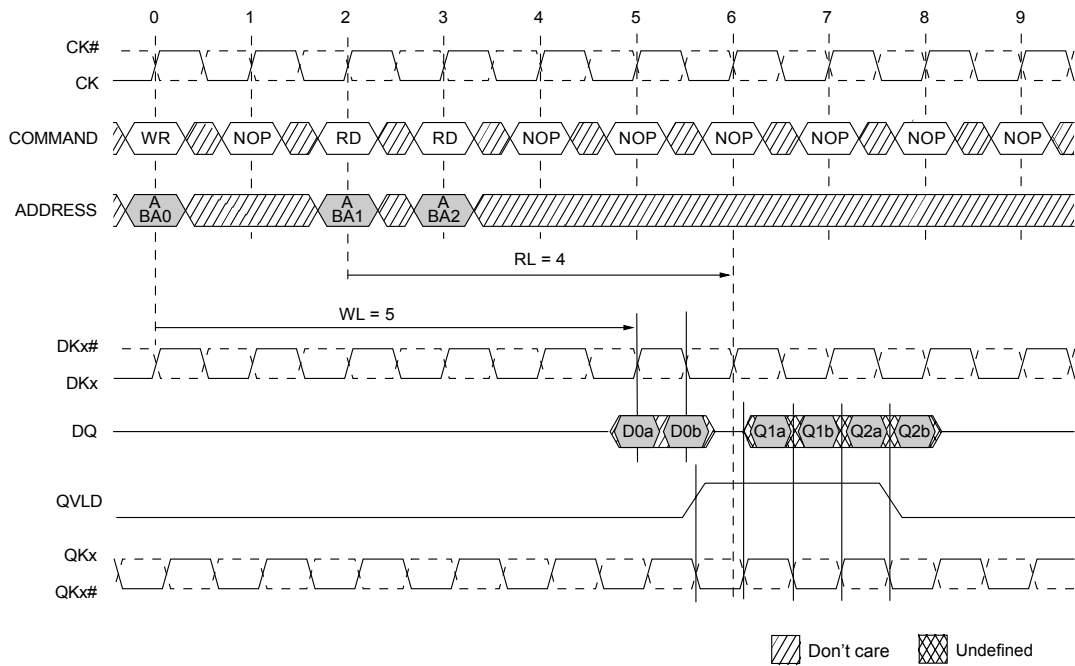
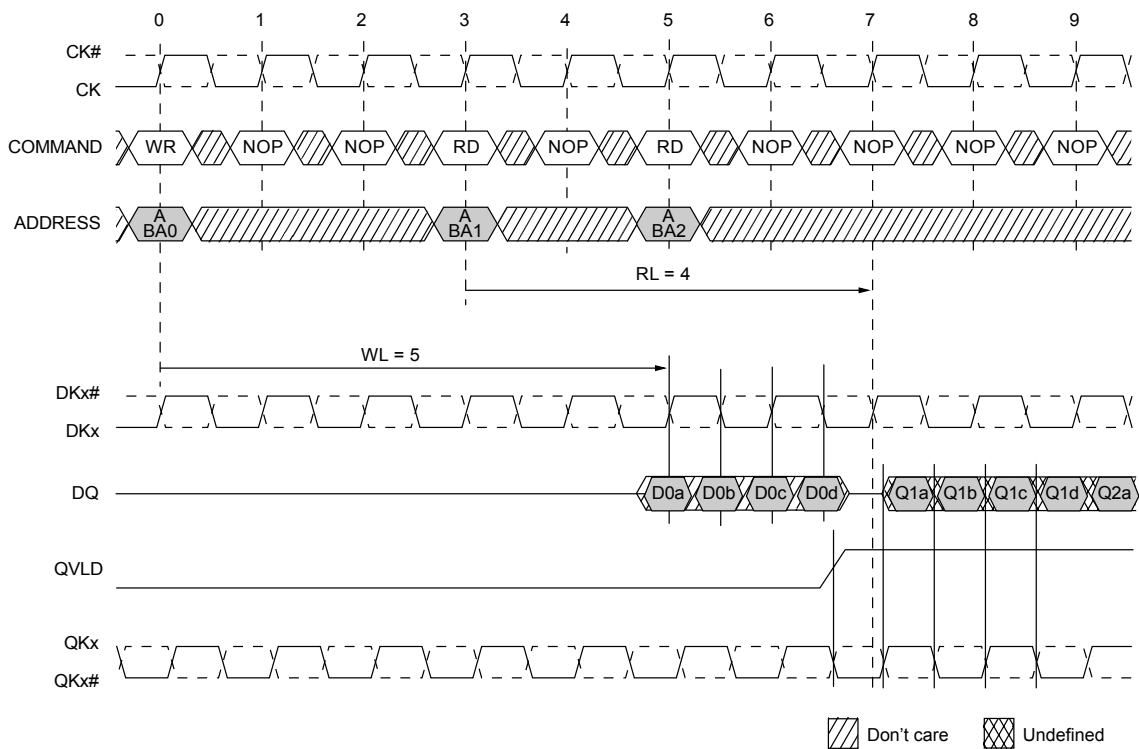


Figure 2-11. WRITE Followed By READ: BL=4, RL=4, WL=5, Configuration 1



Remark

- WR : WRITE command
- RD : READ command
- A/BA_p : Address A of bank p
- WL : WRITE latency
- RL : READ latency
- D_{pq} : Data q to bank p
- Q_{pq} : Data q from bank p

2.11 Read Operation (READ)

Read accesses are initiated with a READ command, as shown in **Figure 2-12**. Row and bank addresses are provided with the READ command.

During READ bursts, the memory device drives the read data edge-aligned with the QK signal. After a programmable READ latency, data is available at the outputs. The data valid signal indicates that valid data will be present in the next half clock cycle.

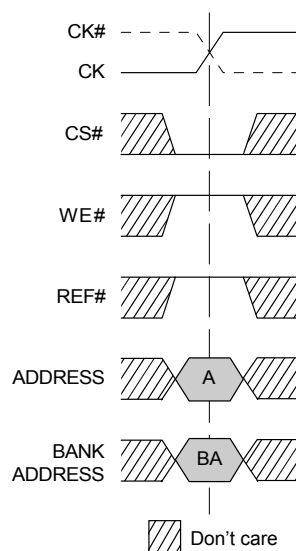
The skew between QK and the crossing point of CK is specified as t_{CKQK} . t_{QKQ0} is the skew between QK0 and the last valid data edge considered the data generated at the DQ0–DQ17 in x36 and DQ0–DQ8 in x18 data signals. t_{QKQ1} is the skew between QK1 and the last valid data edge considered the data generated at the DQ18–DQ35 in x36 and DQ9–DQ17 in x18 data signals. t_{QKQx} is derived at each QKx clock edge and is not cumulative over time.

After completion of a burst, assuming no other commands have been initiated, DQ will go High-Z. Back-to-back READ commands are possible, producing a continuous flow of output data.

Minimum READ data valid window can be expressed as $\text{MIN.}(t_{QKH}, t_{QKL}) - 2 \times \text{MAX.}(t_{QKQx})$

Any READ burst may be followed by a subsequent WRITE command. **Figure 2-16. READ followed by WRITE, BL=2, RL=4, WL=5, Configuration 1** and **Figure 2-17. READ followed by WRITE, BL=4, RL=4, WL=5, Configuration 1** illustrate the timing requirements for a READ followed by a WRITE.

Figure 2-12. READ Command



Remark A : Address

BA: Bank address

Figure 2-14. READ Burst Basic Sequence: BL=2, RL=4, Configuration 1

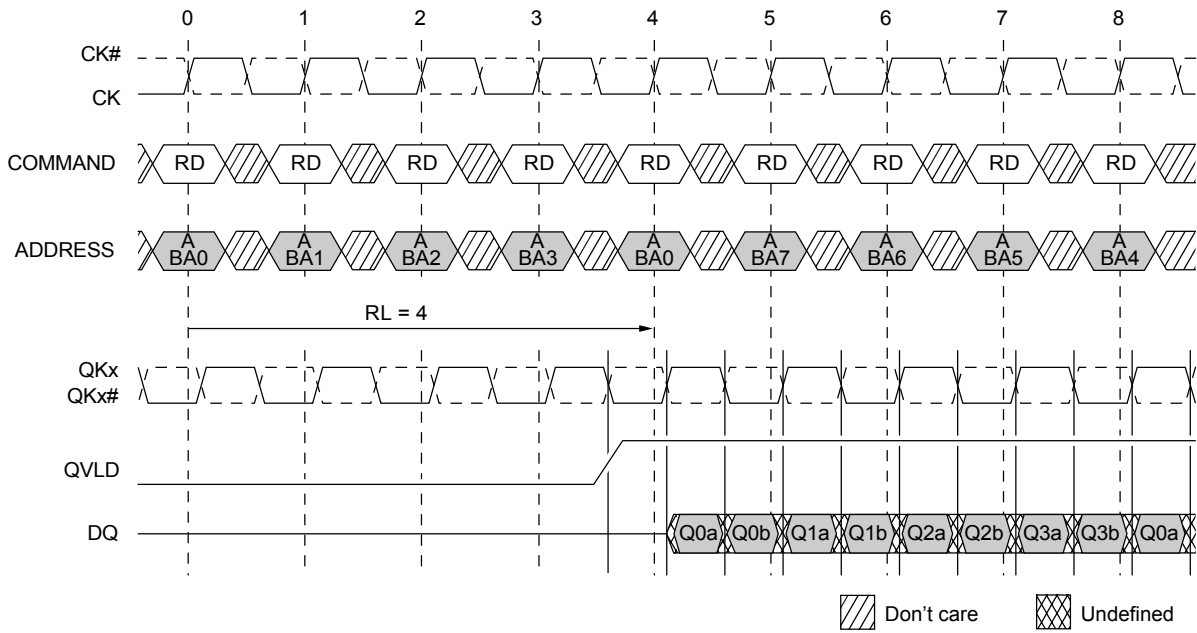
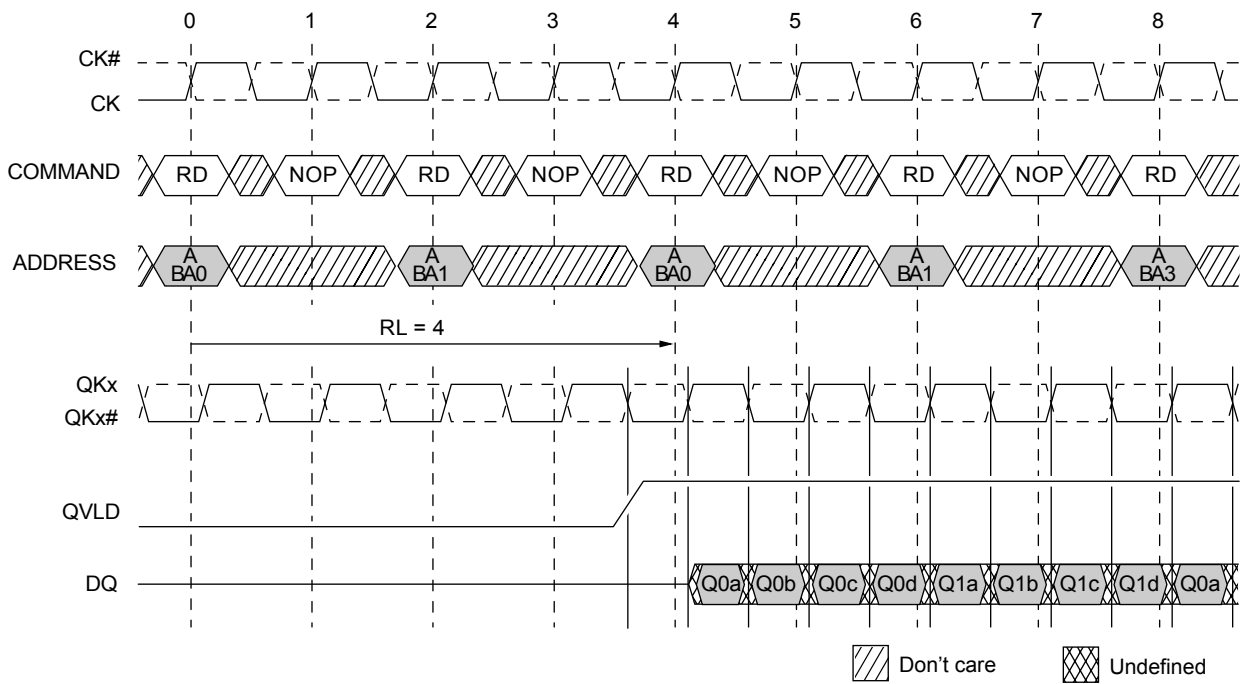


Figure 2-15. READ Burst Basic Sequence: BL=4, RL=4, Configuration 1



Remark RD : READ command
 A/BAp : Address A of bank p
 RL : READ latency
 Qpq : Data q from bank p

Figure 2-16. READ followed by WRITE, BL=2, RL=4, WL=5, Configuration 1

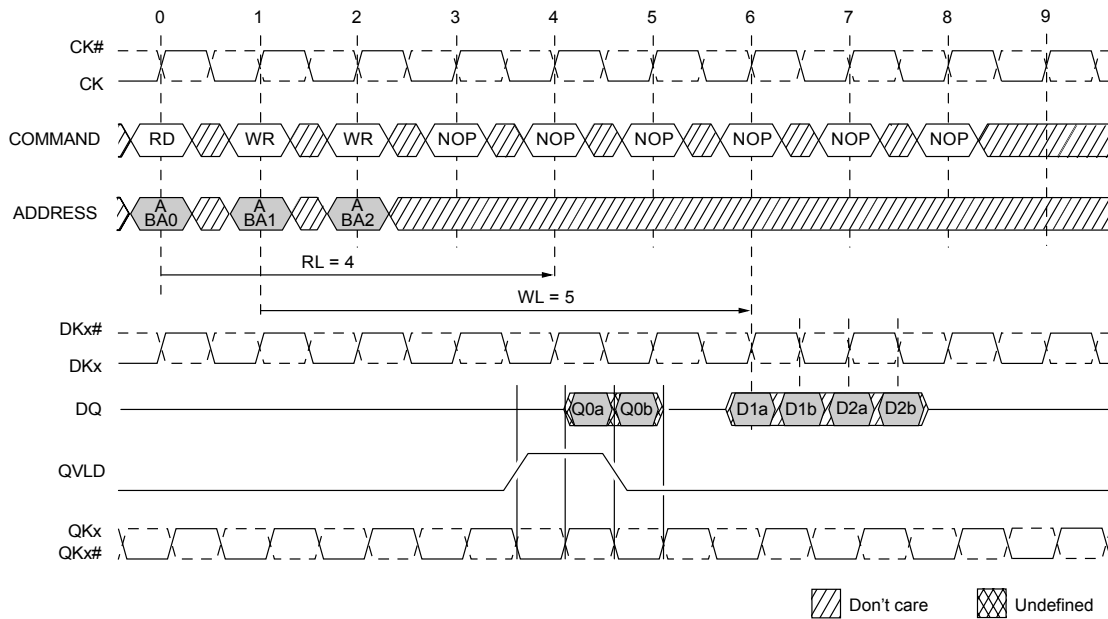
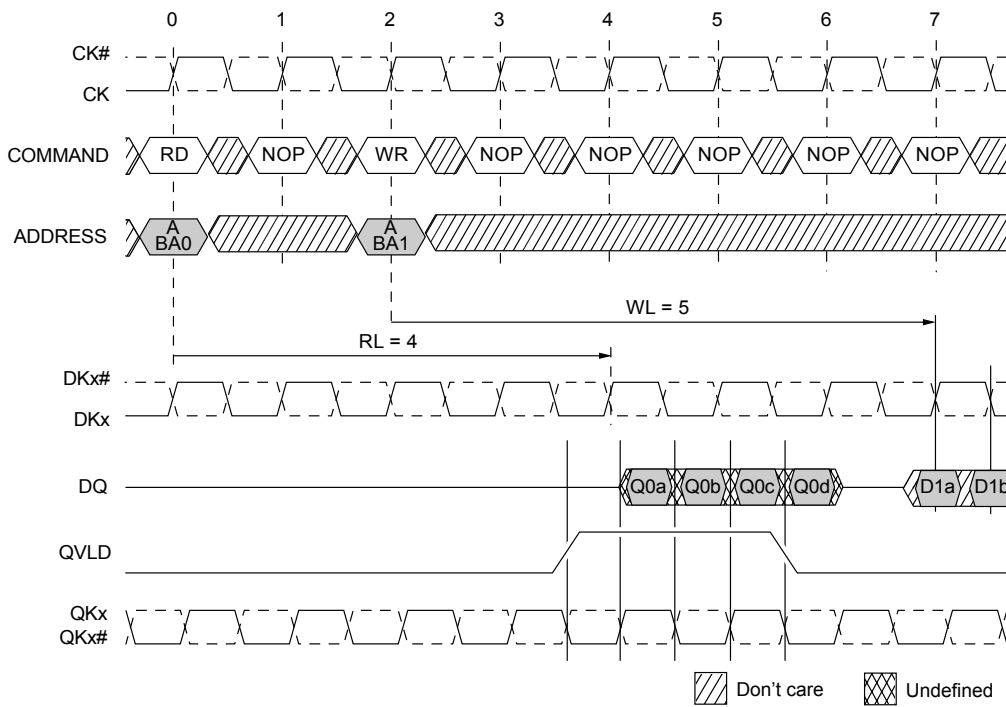


Figure 2-17. READ followed by WRITE, BL=4, RL=4, WL=5, Configuration 1



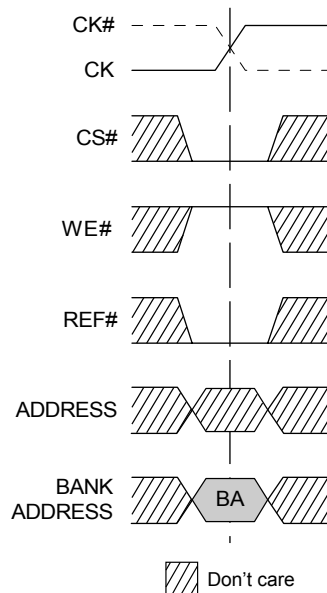
- Remark**
- WR : WRITE command
 - RD : READ command
 - A/BA_p : Address A of bank p
 - WL : WRITE latency
 - RL : READ latency
 - D_{pq} : Data q to bank p
 - Q_{pq} : Data q from bank p

2.12 Refresh Operation: AUTO REFRESH Command (AREF)

AREF is used to perform a REFRESH cycle on one row in a specific bank. The row addresses are generated by an internal refresh counter; external address balls are “Don’t Care.” The delay between the AREF command and a subsequent command to the same bank must be at least t_{RC} .

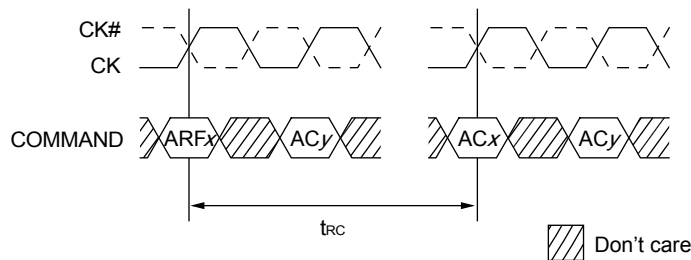
Within a period of 32 ms (t_{REF}), the entire memory must be refreshed. **Figure 2-19** illustrates an example of a continuous refresh sequence. Other refresh strategies, such as burst refresh, are also possible.

Figure 2-18. AUTO REFRESH Command



Remark BA: Bank address

Figure 2-19. AUTO REFRESH Cycle



- Remarks**
1. AC_x : Any command on bank x
 ARF_x : Auto refresh bank x
 AC_y : Any command on different bank.
 2. t_{RC} is configuration-dependent. Refer to **Table 2-4. Configuration Table**.

2.13 On-Die Termination

On-die termination (ODT) is enabled by setting A9 to “1” during an MRS command. With ODT on, all the DQs and DM are terminated to V_{TT} with a resistance R_{TT}. The command, address, and clock signals are not terminated. **Figure 2-20** below shows the equivalent circuit of a DQ receiver with ODT. ODTs are dynamically switched off during READ commands and are designed to be off prior to the μPD48576209/18/36 driving the bus. Similarly, ODTs are designed to switch on after the μPD48576209/18/36 has issued the last piece of data.

Table 2-5. On-Die Termination DC Parameters

Description	Symbol	MIN.	MAX.	Units	Note
Termination voltage	V _{TT}	0.95 x V _{REF}	1.05 x V _{REF}	V	1, 2
On-Die termination	R _{TT}	125	185	Ω	3

- Notes**
1. All voltages referenced to V_{SS} (GND).
 2. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
 3. The R_{TT} value is measured at 95°C T_C.

Figure 2-20. On- Die Termination-Equivalent Circuit

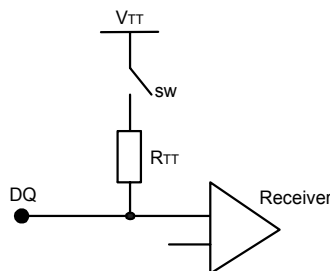
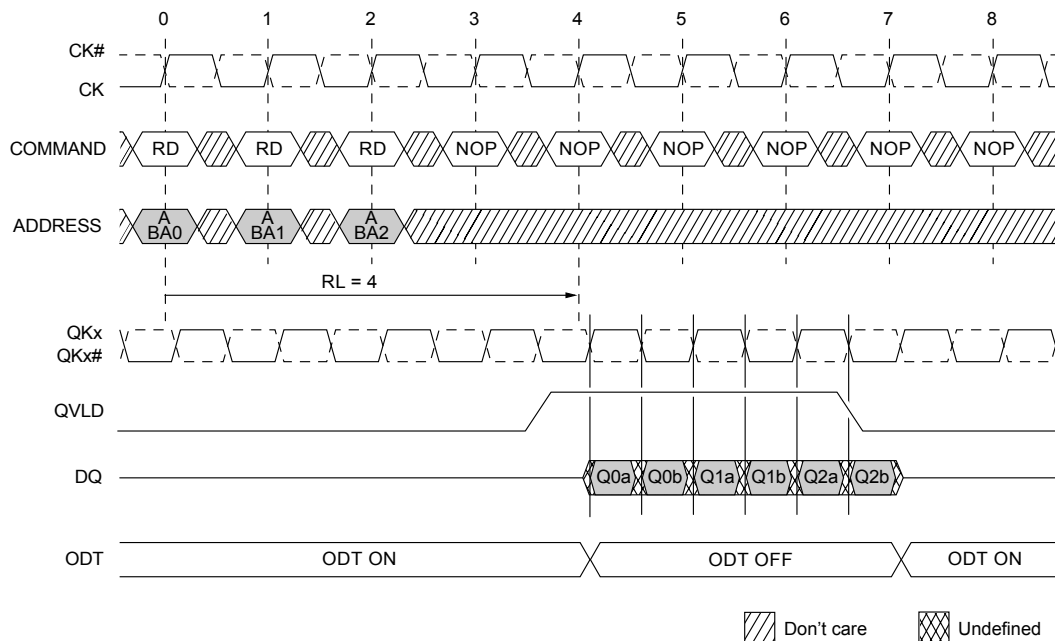


Figure 2-21. READ Burst with ODT: BL=2, Configuration 1



- Remark**
- RD : READ command
 - A/BA_p : Address A of bank p
 - RL : READ latency
 - Q_{pq} : Data q from bank p

Figure 2-22. READ NOP READ with ODT: BL=2, Configuration 1

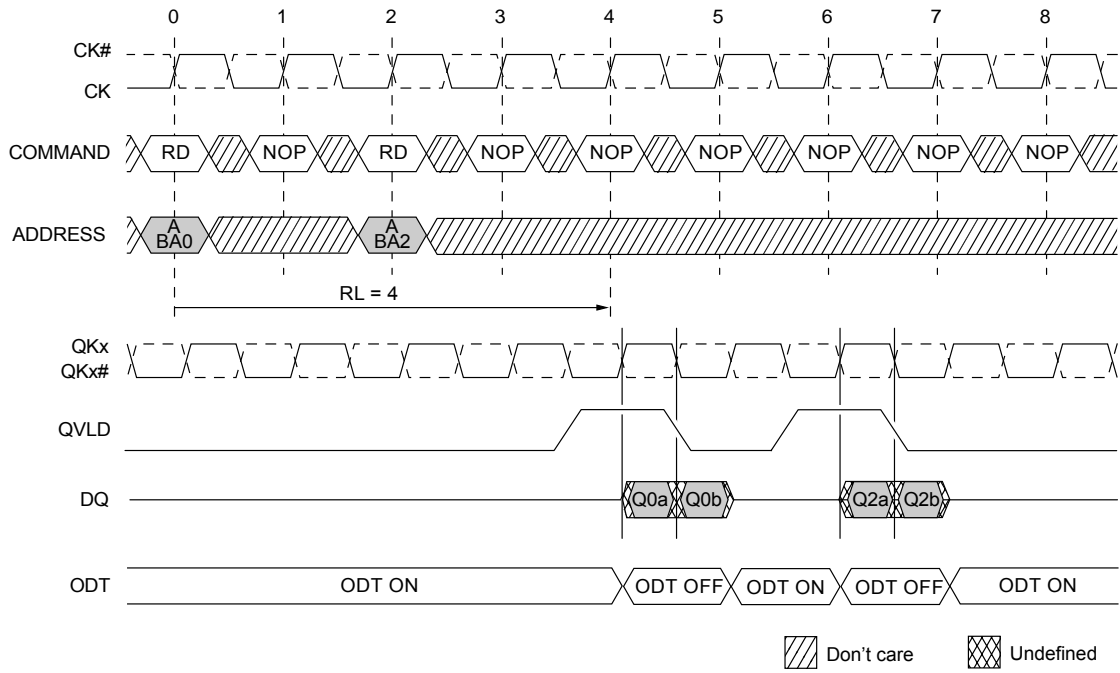
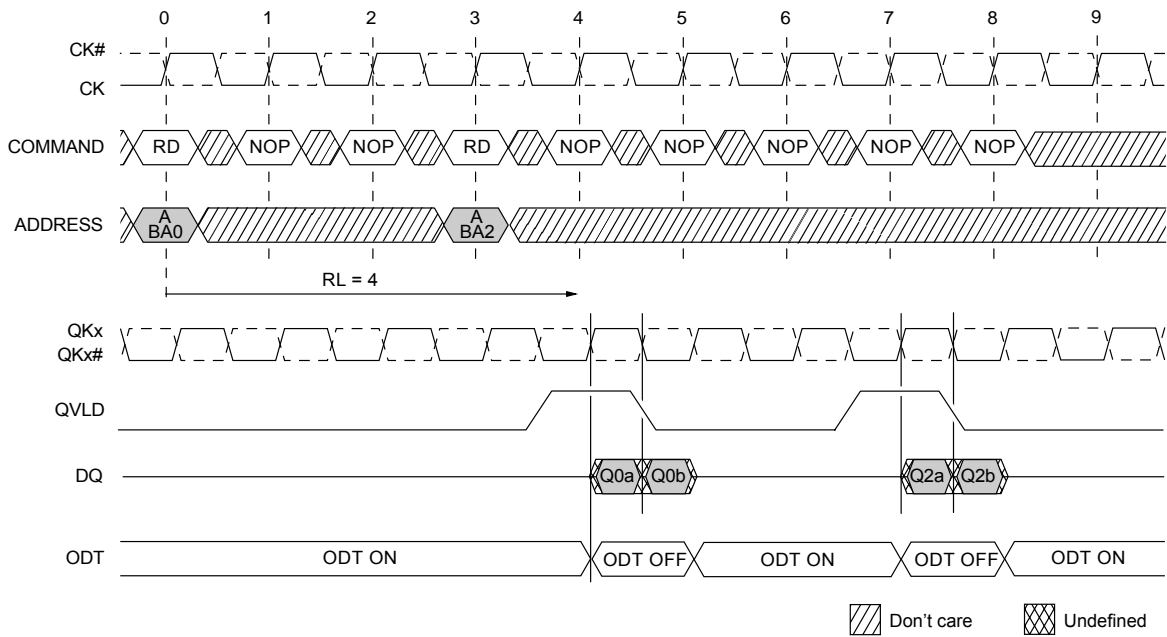


Figure 2-23. READ NOP NOP READ with ODT: BL=2, Configuration 1



Remark RD : READ command
 A/BAp: Address A of bank p
 RL : READ latency
 Qpq : Data q from bank p

Figure 2-24. READ followed by WRITE with ODT: BL=2, Configuration 1

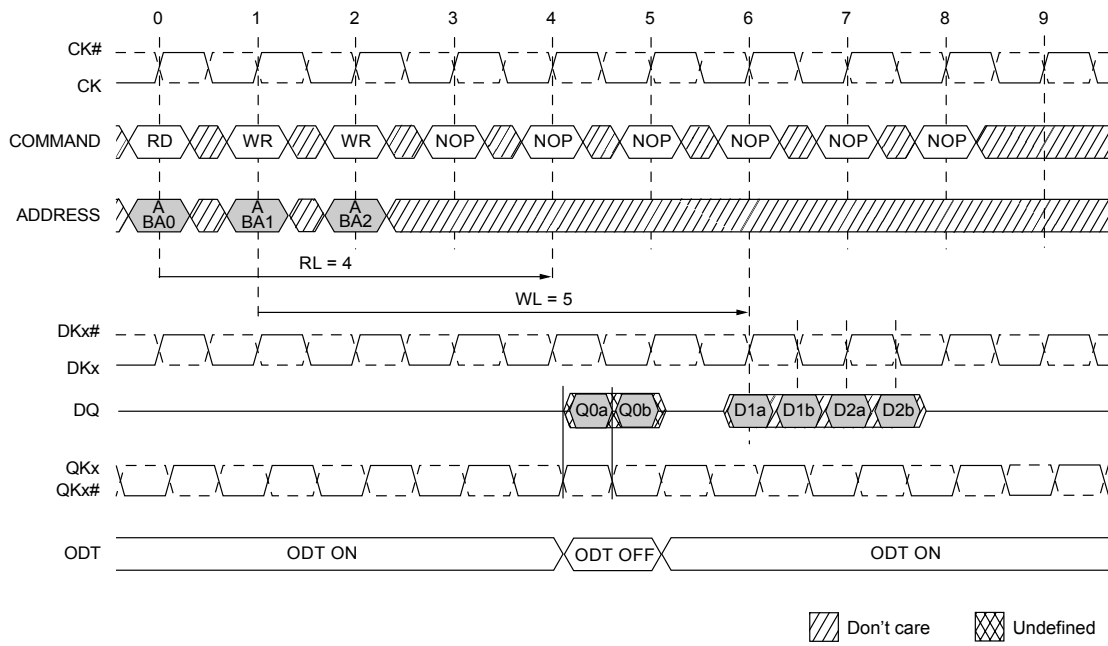
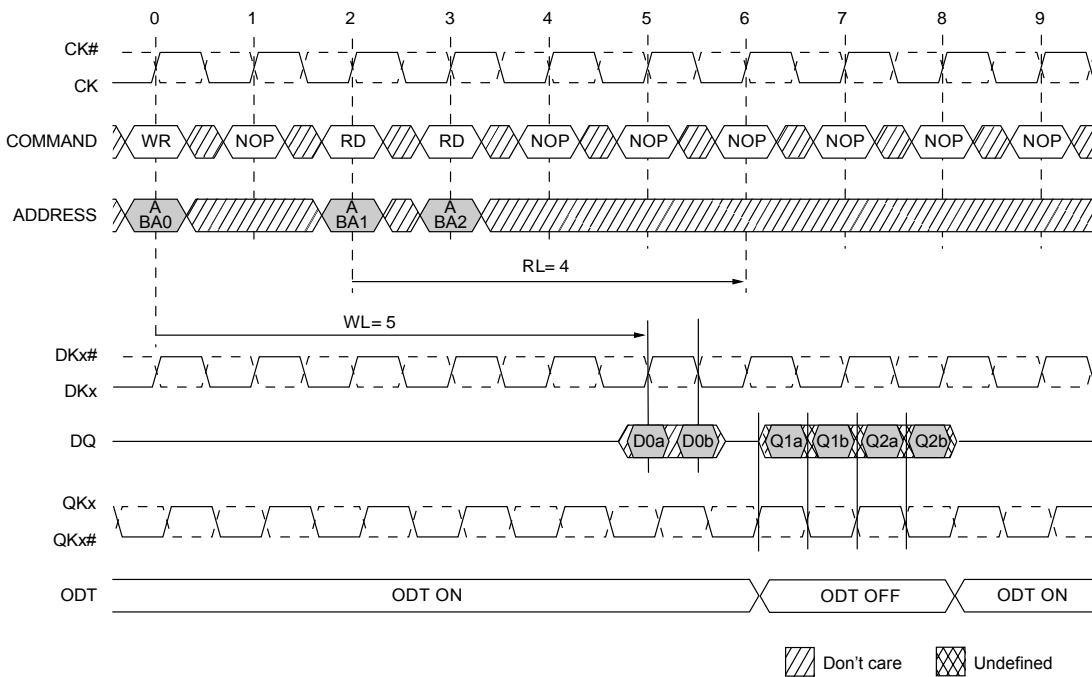


Figure 2-25. WRITE followed by READ with ODT: BL=2, Configuration 1



Remark

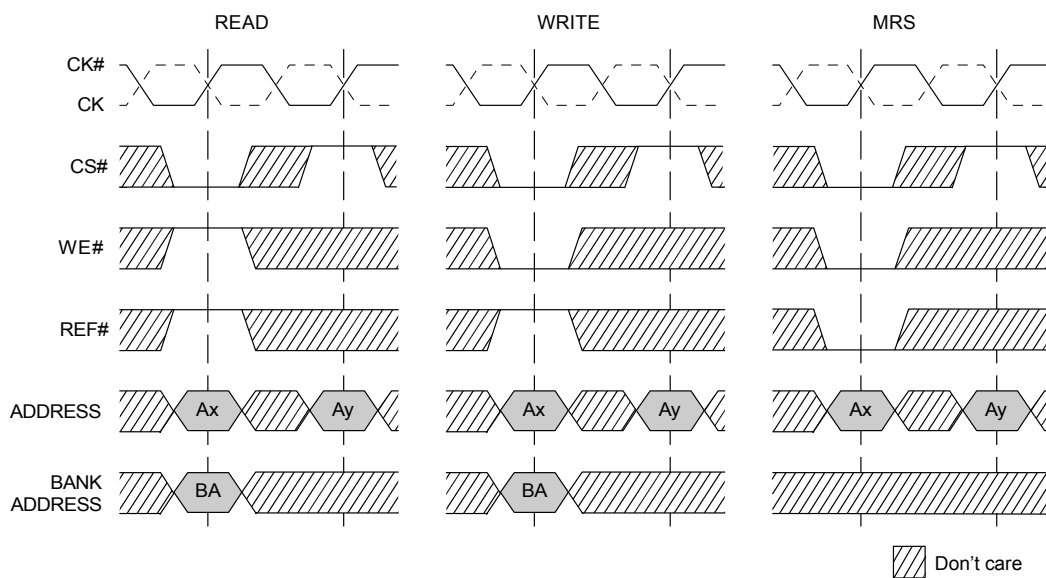
- RD : READ command
- WR : WRITE command
- A/BA_p : Address A of bank p
- RL : READ latency
- WL : WRITE latency
- Q_{pq} : Data q from bank p
- D_{pq} : Data q to bank p

2.14 Operation with Multiplexed Address

In multiplexed address mode, the address can be provided to the μPD48576209/18/36 in two parts that are latched into the memory with two consecutive rising clock edges. This provides the advantage that a maximum of 11 address balls are required to control the μPD48576209/18/36, reducing the number of balls on the controller side. The data bus efficiency in continuous burst mode is not affected for BL=4 and BL=8 since at least two clocks are required to read the data out of the memory. The bank addresses are delivered to the μPD48576209/18/36 at the same time as the WRITE command and the first address part, Ax.

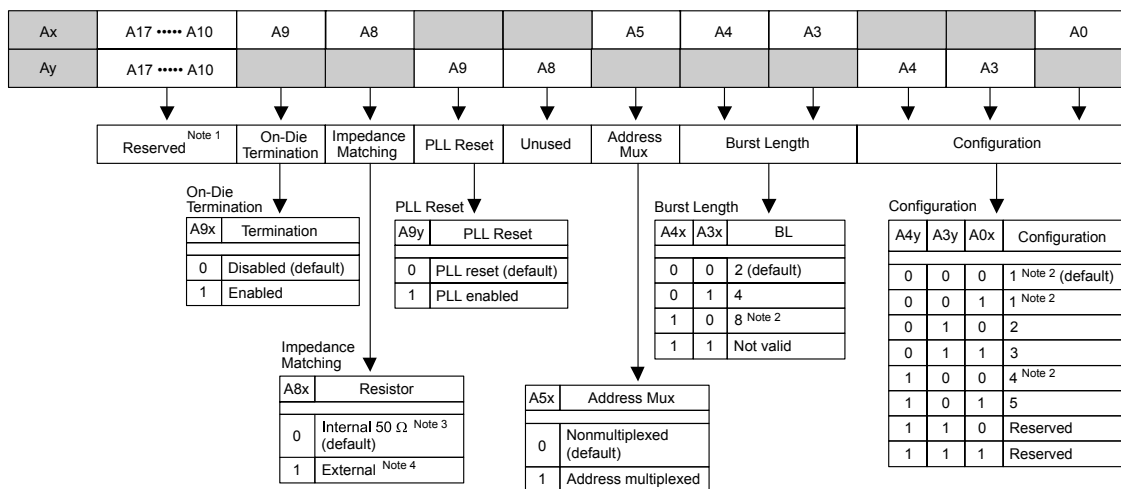
This option is available by setting bit A5 to “1” in the mode register. Once this bit is set, the READ, WRITE, and MRS commands follow the format described in **Figure 2-26**. See **Figure 2-28. Power-Up Sequence in Multiplexed Address Mode** for the power-up sequence.

Figure 2-26. Command Description in Multiplexed



- Remarks**
1. Ax, Ay : Address
BA : Bank Address
 2. The minimum setup and hold times of the two address parts are defined t_{AS} and t_{AH} .

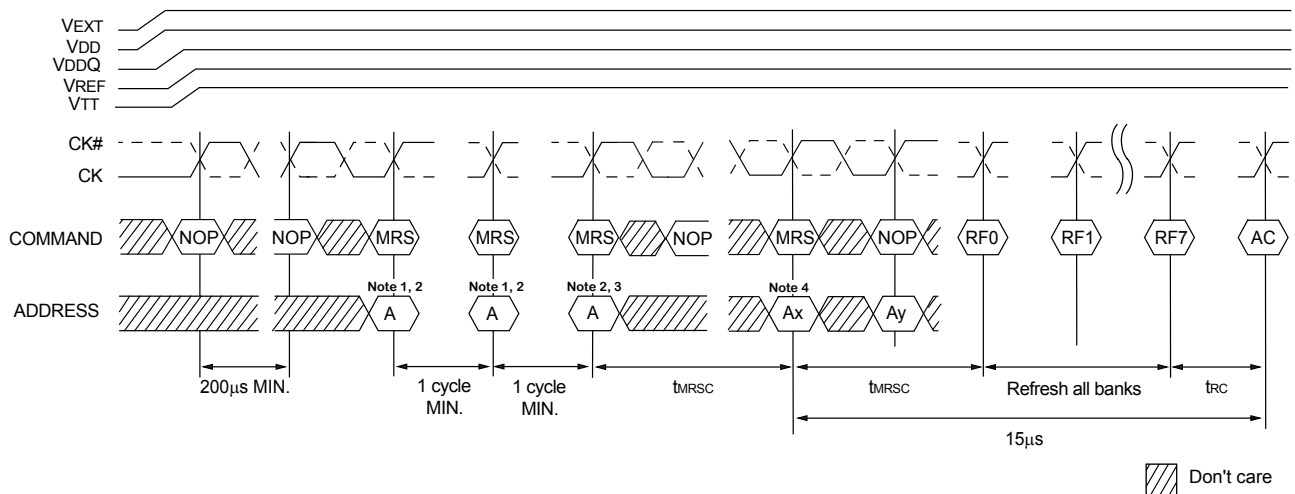
Figure 2-27. Mode Register Set Command in Multiplexed Address Mode



- Notes**
1. Bits A10–A17 must be set to all ‘0’.
 2. BL=8 is not available for configuration 1 and 4.
 3. ±30% temperature variation.
 4. Within 15%.

Remark The address A0, A3, A4, A5, A8, and A9 must be set as follows in order to activate the mode register in the multiplexed address mode.

Figure 2-28. Power-Up Sequence in Multiplexed Address Mode



- Notes**
1. Recommended all address pins held LOW during dummy MRS command.
 2. A10-A17 must be LOW.
 3. Address A5 must be set HIGH (muxed address mode setting when μPD48576209/18/36 is in normal mode of operation).
 4. Address A5 must be set HIGH (muxed address mode setting when μPD48576209/18/36 is already in muxed address mode).

Remark MRS : MRS command
 RFp : REFRESH Bank p
 AC : any command

2.15 Address Mapping in Multiplexed Mode

The address mapping is described in **Table 2-6** as a function of data width and burst length.

Table 2-6. Address Mapping in Multiplexed Address Mode

Data Width	Burst Length	Ball	Address										
			A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
x36	BL=2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL=4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL=8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x18	BL=2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL=4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL=8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x9	BL=2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	A21	A6	A7	A19	A11	A12	A16	A15
	BL=4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL=8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15

Remark X means “Don’t care”.

2.16 Read & Write configuration in Multiplexed Address Mode

In multiplexed address mode, the READ and WRITE latencies are increased by one clock cycle. The μPD48576209/18/36 cycle time remains the same, as described in **Table 2-7**.

Table 2-7. Configuration in Multiplexed Address Mode

Parameter	Configuration					Unit
	Note2 1	2	3	Note2, 3 4	5	
t _{RC}	4	6	8	3	5	t _{CK}
t _{RL}	5	7	9	4	6	t _{CK}
t _{WL}	6	8	10	5	7	t _{CK}
Valid frequency range	266-175	400-175	533-175	200-175	333-175	MHz

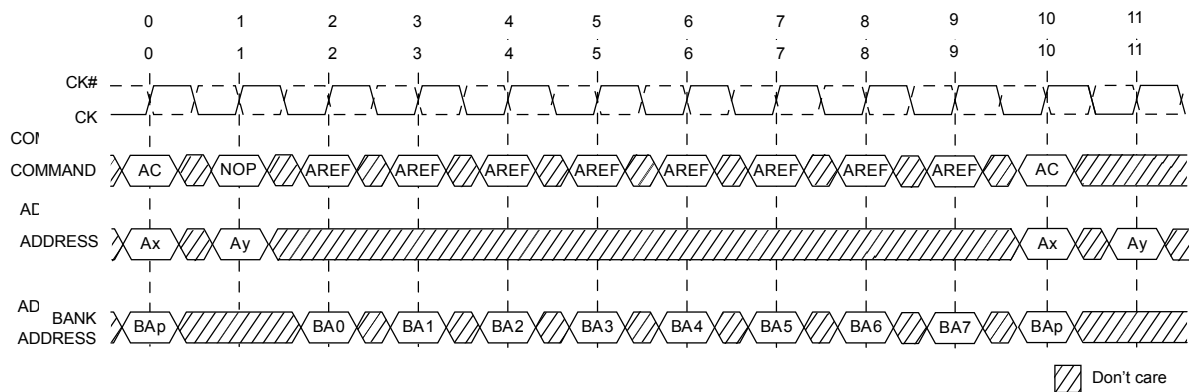
Notes 1. Apply to the entire table. t_{RC} < 20 ns in any configuration is only available with –E24 and –E18 speed grades.

- 2. BL = 8 is not available.
- 3. The minimum t_{RC} is typically 3 cycles, except in the case of a WRITE followed by a READ to the same bank. In this instance the minimum t_{RC} is 4 cycles.

2.17 Refresh Command in Multiplexed Address Mode

Similar to other commands, the refresh command is executed on the next rising clock edge when in the multiplexed address mode. However, since only bank address is required for AREF, the next command can be applied on the following clock. The operation of the AREF command and any other command is represented in **Figure 2-29**.

Figure 2-29. Burst REFRESH Operation



- Remark**
- AREF : AUTO REFRESH
 - AC : Any command
 - Ax : First part Ax of address
 - Ay : Second part Ay of address
 - BA_p : Bank p is chosen so that t_{RC} is met.

Figure 2-30. WRITE Burst Basic Sequence: BL=4, with Multiplexed Addresses, Configuration 1

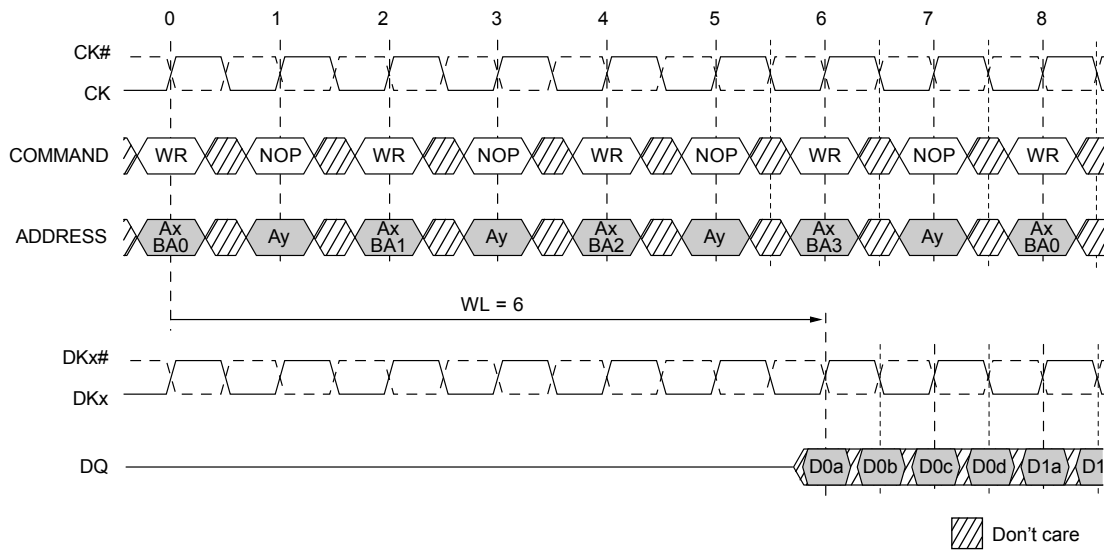
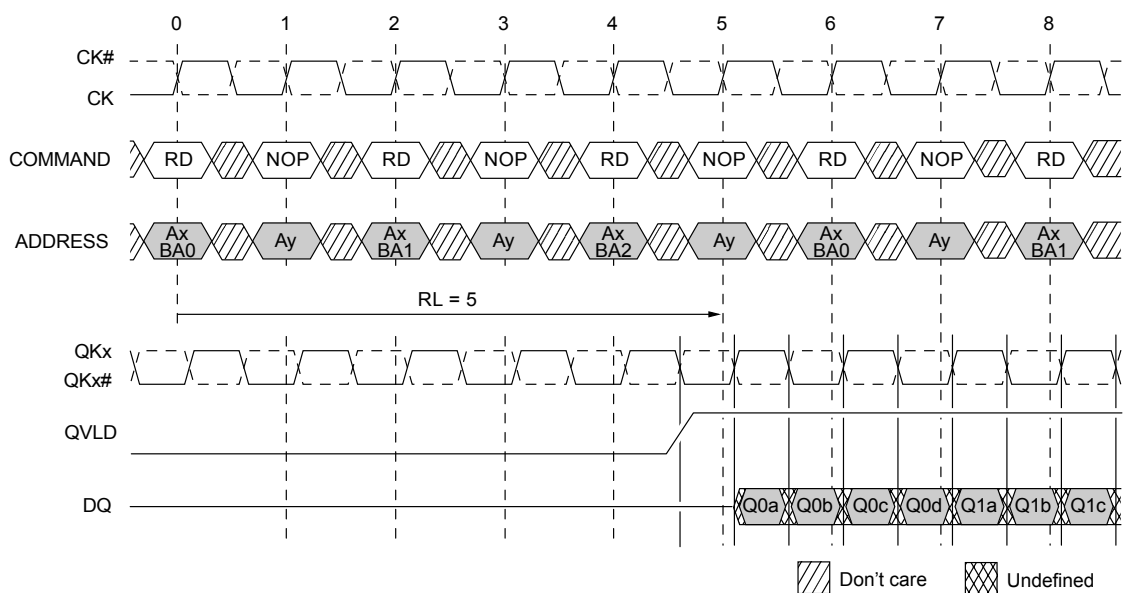


Figure 2-31. READ Burst Basic Sequence: BL=4, with Multiplexed Addresses, Configuration 1, RL=5



- Remark**
- WR : WRITE command
 - RD : READ command
 - Ax/BAp : Address Ax of bank p
 - Ay : Address Ay of bank p
 - Dpq : Data q to bank p
 - Qpq : Data q from bank p
 - WL : WRITE latency
 - RL : READ latency

2.18 Input Slew Rate Derating

Table 2-8 on page 40 and **Table 2-9** on page 41 define the address, command, and data setup and hold derating values. These values are added to the default tAS/tCS/tDS and tAH/tCH/tDH specifications when the slew rate of any of these input signals is less than the 2 V/ns the nominal setup and hold specifications are based upon.

To determine the setup and hold time needed for a given slew rate, add the tAS/tCS default specification to the “tAS/tCS V_{REF} to CK/CK# Crossing” and the tAH/tCH default specification to the “tAH/tCH CK/CK# Crossing to V_{REF}” derated values on **Table 2-8**. The derated data setup and hold values can be determined in a like manner using the “tDS V_{REF} to CK/CK# Crossing” and “tDH to CK/CK# Crossing to V_{REF}” values on **Table 2-9**.

The derating values on **Table 2-8** and **Table 2-9** apply to all speed grades.

The setup times on **Table 2-8** and **Table 2-9** represent a rising signal. In this case, the time from which the rising signal crosses V_{IH(AC)} MIN to the CK/CK# cross point is static and must be maintained across all slew rates. The derated setup timing represents the point at which the rising signal crosses V_{REF(DC)} to the CK/CK# cross point. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between V_{IH(AC)} MIN and the CK/CK# cross point. The setup values in **Table 2-8** and **Table 2-9** are also valid for falling signals (with respect to V_{IL[AC]} MAX and the CK/CK# cross point).

The hold times in **Table 2-8** and **Table 2-9** represent falling signals. In this case, the time from the CK/CK# cross point to when the signal crosses V_{IH(DC)} MIN is static and must be maintained across all slew rates. The derated hold timing represents the delta between the CK/CK# cross point to when the falling signal crosses V_{REF(DC)}. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between the CK/CK# cross point and V_{IH(DC)}. The hold values in **Table 2-8** and **Table 2-9** are also valid for rising signals (with respect to V_{IL[DC]} MAX and the CK and CK# cross point).

Note: The above descriptions also pertain to data setup and hold derating when CK/CK# are replaced with DK/DK#.

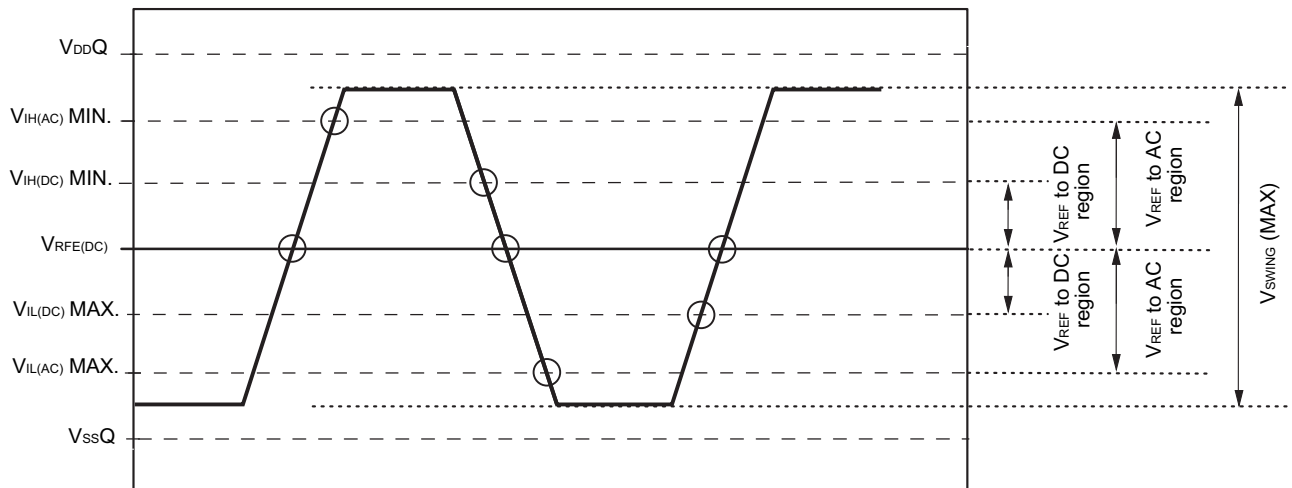
Table 2-8. Address and Command Setup and Hold Derating Values

Command/ Address Slew Rate (V/ns)	tAS/tCS VREF to CK/CK# Crossing	tAS/tCS VIH(AC) MIN to CK/CK# Crossing	tAH/tCH CK/CK# Crossing to VREF	tAH/tCH CK/CK# Crossing to VIH(DC) MIN	Unit
CK, CK# Differential Slew Rate: 2.0 V/ns					
2.0	0	-100	0	-50	ps
1.9	5	-100	3	-50	ps
1.8	11	-100	6	-50	ps
1.7	18	-100	9	-50	ps
1.6	25	-100	13	-50	ps
1.5	33	-100	17	-50	ps
1.4	43	-100	22	-50	ps
1.3	54	-100	27	-50	ps
1.2	67	-100	34	-50	ps
1.1	82	-100	41	-50	ps
1.0	100	-100	50	-50	ps
CK, CK# Differential Slew Rate: 1.5 V/ns					
2.0	30	-70	30	-20	ps
1.9	35	-70	33	-20	ps
1.8	41	-70	36	-20	ps
1.7	48	-70	39	-20	ps
1.6	55	-70	43	-20	ps
1.5	63	-70	47	-20	ps
1.4	73	-70	52	-20	ps
1.3	84	-70	57	-20	ps
1.2	97	-70	64	-20	ps
1.1	112	-70	71	-20	ps
1.0	130	-70	80	-20	ps
CK, CK# Differential Slew Rate: 1.0 V/ns					
2.0	60	-40	60	10	ps
1.9	65	-40	63	10	ps
1.8	71	-40	66	10	ps
1.7	78	-40	69	10	ps
1.6	85	-40	73	10	ps
1.5	93	-40	77	10	ps
1.4	103	-40	82	10	ps
1.3	114	-40	87	10	ps
1.2	127	-40	94	10	ps
1.1	142	-40	101	10	ps
1.0	160	-40	110	10	ps

Table 2-9. Data Setup and Hold Derating Values

Data Slew Rate (V/ns)	tDS V _{REF} to DK/DK# Crossing	tDS V _{IH(AC)} MIN to DK/DK# Crossing	tDH DK/DK# Crossing to V _{REF}	tDH DK/DK# Crossing to V _{IH(DC)} MIN	Unit
DK, DK# Differential Slew Rate: 2.0 V/ns					
2.0	0	-100	0	-50	ps
1.9	5	-100	3	-50	ps
1.8	11	-100	6	-50	ps
1.7	18	-100	9	-50	ps
1.6	25	-100	13	-50	ps
1.5	33	-100	17	-50	ps
1.4	43	-100	22	-50	ps
1.3	54	-100	27	-50	ps
1.2	67	-100	34	-50	ps
1.1	82	-100	41	-50	ps
1.0	100	-100	50	-50	ps
DK, DK# Differential Slew Rate: 1.5 V/ns					
2.0	30	-70	30	-20	ps
1.9	35	-70	33	-20	ps
1.8	41	-70	36	-20	ps
1.7	48	-70	39	-20	ps
1.6	55	-70	43	-20	ps
1.5	63	-70	47	-20	ps
1.4	73	-70	52	-20	ps
1.3	84	-70	57	-20	ps
1.2	97	-70	64	-20	ps
1.1	112	-70	71	-20	ps
1.0	130	-70	80	-20	ps
DK, DK# Differential Slew Rate: 1.0 V/ns					
2.0	60	-40	60	10	ps
1.9	65	-40	63	10	ps
1.8	71	-40	66	10	ps
1.7	78	-40	69	10	ps
1.6	85	-40	73	10	ps
1.5	93	-40	77	10	ps
1.4	103	-40	82	10	ps
1.3	114	-40	87	10	ps
1.2	127	-40	94	10	ps
1.1	142	-40	101	10	ps
1.0	160	-40	110	10	ps

Figure 2-32. Nominal tAS/tCS/tDS and tAH/tCH/tDH Slew Rate



3. JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Table 3-1. Test Access Port (TAP) Pins

Pin name	Pin assignments	Description
TCK	12A	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	11A	Test Mode Select. This is the command input for the TAP controller state
TDI	12V	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently
TDO	11V	Test Data Output. This is the output side of the serial registers placed between TDI and TDO. Output changes in response to the falling edge of TCK.

Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held HIGH for five rising edges of TCK. The TAP controller state is also reset on the POWER-UP.

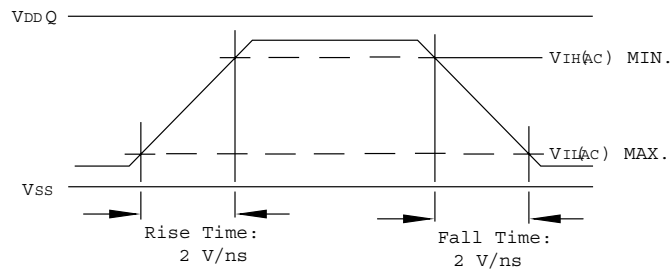
Table 3-2. JTAG DC Characteristics (0°C ≤ Tc ≤ 95°C, 1.7 V ≤ VDD ≤ 1.9 V, unless otherwise noted)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Notes
JTAG Input leakage current	I _{LI}	0 V ≤ V _{IN} ≤ V _{DD}	-5.0	+5.0	μA	
JTAG I/O leakage current	I _{LO}	0 V ≤ V _{IN} ≤ V _{DD} Q , Outputs disabled	-5.0	+5.0	μA	
JTAG input HIGH voltage	V _{IH}		V _{REF} + 0.15	V _{DD} + 0.3	V	1, 2
JTAG input LOW voltage	V _{IL}		V _{SSQ} - 0.3	V _{REF} - 0.15	V	1, 2
JTAG output HIGH voltage	V _{OH1}	I _{OHC} = 100 μA	V _{DDQ} - 0.2		V	
	V _{OH2}	I _{OHT} = 2 mA	V _{DDQ} - 0.4		V	
JTAG output LOW voltage	V _{OL1}	I _{OLC} = 100 μA		0.2	V	1
	V _{OL2}	I _{OLT} = 2 mA		0.4	V	1

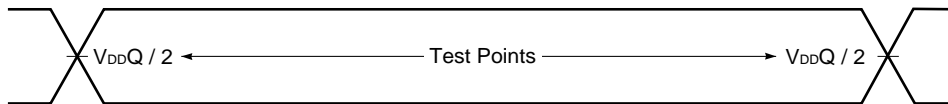
- Note**
- All voltages referenced to V_{SS} (GND).
 - Overshoot: V_{IH(AC)} ≤ V_{DD} + 0.7 V for t ≤ t_{CK}/2.
Undershoot: V_{IL(AC)} ≥ -0.5 V for t ≤ t_{CK}/2.
During normal operation, V_{DDQ} must not exceed V_{DD}.

JTAG AC Test Conditions

Input waveform



Output waveform



Output load condition

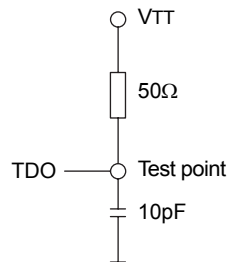


Table 3-3. JTAG AC Characteristics (0°C ≤ Tc ≤ 95°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock						
Clock cycle time	t _{THTH}		20		ns	
Clock frequency	f _{TF}			50	MHz	
Clock HIGH time	t _{HTHL}		10		ns	
Clock LOW time	t _{LTHT}		10		ns	
Output time						
TCK LOW to TDO	t _{TLOX}		0		ns	
TCK LOW to TDO valid	t _{TLOV}			10	ns	
Setup time						
TMS setup time	t _{MVTH}		5		ns	
TDI valid to TCK HIGH	t _{DVTH}		5		ns	
Capture setup time	t _{CSJ}		5		ns	1
Hold time						
TMS hold time	t _{THMX}		5		ns	
TCK HIGH to TDI invalid	t _{THDX}		5		ns	
Capture hold time	t _{CHJ}		5		ns	1

Note 1. t_{CSJ} and t_{CHJ} refer to the setup and hold time requirements of latching data from the boundary scan register.

JTAG Timing Diagram

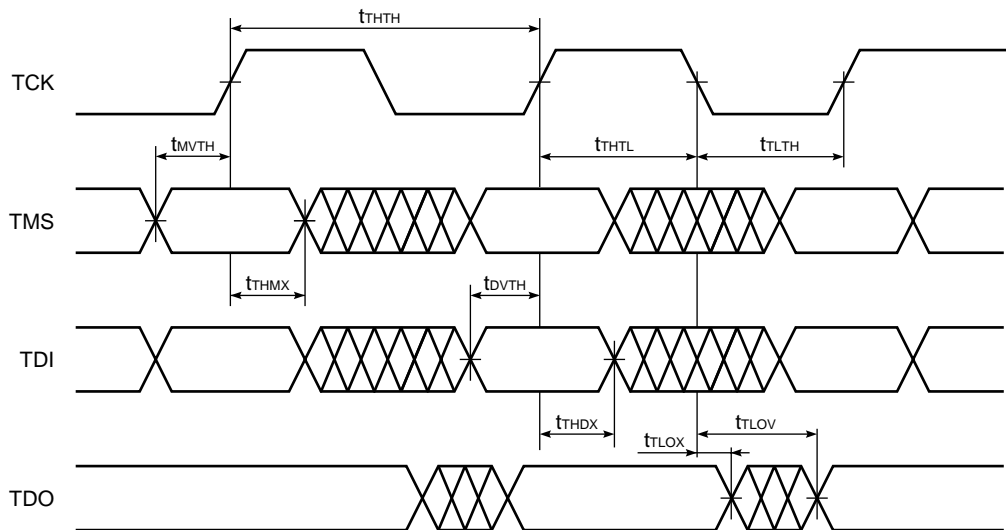


Table 3-4. Scan Register Definition (1)

Register name	Description
Instruction register	The 8 bit instruction registers hold the instructions that are executed by the TAP controller. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible. The bypass register is set LOW (VSS) when the bypass instruction is executed.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Table 3-5. Scan Register Definition (2)

Register name	Bit size	Unit
Instruction register	8	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	113	bit

Table 3-6. ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD48576209	64M x 9	0000	0001 0001 1010 0111	00000010000	1
μPD48576218	32M x 18	0001	0001 0001 1010 0111	00000010000	1
μPD48576236	16M x 36	0010	0001 0001 1010 0111	00000010000	1

Table 3-7. SCAN Exit Order

Bit no.	Signal name			Bump ID	Bit no.	Signal name			Bump ID	Bit no.	Signal name			Bump ID
	x9	x18	x36			x9	x18	x36			x9	x18	x36	
1	DK	DK	DK1	K1	39	DNU	DNU	DQ30	R11	77	DNU	DNU	DQ2	C11
2	DK#	DK#	DK1#	K2	40	DNU	DNU	DQ30	R11	78	DNU	DNU	DQ2	C11
3	CS#	CS#	CS#	L2	41	DNU	DNU	DQ32	P11	79	DQ1	DQ1	DQ3	C10
4	REF#	REF#	REF#	L1	42	DNU	DNU	DQ32	P11	80	DQ1	DQ1	DQ3	C10
5	WE#	WE#	WE#	M1	43	DQ5	DQ10	DQ33	P10	81	DNU	DNU	DQ0	B11
6	A17	A17	A17	M3	44	DQ5	DQ10	DQ33	P10	82	DNU	DNU	DQ0	B11
7	A16	A16	A16	M2	45	DNU	DNU	DQ34	N11	83	DQ0	DQ0	DQ1	B10
8	A18	A18	A18	N1	46	DNU	DNU	DQ34	N11	84	DQ0	DQ0	DQ1	B10
9	A15	A15	A15	P1	47	DQ4	DQ9	DQ35	N10	85	DNU	DQ4	DQ9	B3
10	DNU	DQ14	DQ25	N3	48	DQ4	DQ9	DQ35	N10	86	DNU	DQ4	DQ9	B3
11	DNU	DQ14	DQ25	N3	49	DM	DM	DM	P12	87	DNU	DNU	DQ8	B2
12	DNU	DNU	DQ24	N2	50	A19	A19	A19	N12	88	DNU	DNU	DQ8	B2
13	DNU	DNU	DQ24	N2	51	A11	A11	A11	M11	89	DNU	DQ5	DQ11	C3
14	DNU	DQ15	DQ23	P3	52	A12	A12	A12	M10	90	DNU	DQ5	DQ11	C3
15	DNU	DQ15	DQ23	P3	53	A10	A10	A10	M12	91	DNU	DNU	DQ10	C2
16	DNU	DNU	DQ22	P2	54	A13	A13	A13	L12	92	DNU	DNU	DQ10	C2
17	DNU	DNU	DQ22	P2	55	A14	A14	A14	L11	93	DNU	DQ6	DQ13	D3
18	DNU	QK1	QK1	R2	56	BA1	BA1	BA1	K11	94	DNU	DQ6	DQ13	D3
19	DNU	QK1#	QK1#	R3	57	CK#	CK#	CK#	K12	95	DNU	DNU	DQ12	D2
20	DNU	DNU	DQ20	T2	58	CK	CK	CK	J12	96	DNU	DNU	DQ12	D2
21	DNU	DNU	DQ20	T2	59	BA0	BA0	BA0	J11	97	DNU	DNU	DQ14	E2
22	DNU	DQ16	DQ21	T3	60	A4	A4	A4	H11	98	DNU	DNU	DQ14	E2
23	DNU	DQ16	DQ21	T3	61	A3	A3	A3	H12	99	DNU	DQ7	DQ15	E3
24	DNU	DNU	DQ18	U2	62	A0	A0	A0	G12	100	DNU	DQ7	DQ15	E3
25	DNU	DNU	DQ18	U2	63	A2	A2	A2	G10	101	DNU	DNU	DQ16	F2
26	DNU	DQ17	DQ19	U3	64	A1	A1	A1	G11	102	DNU	DNU	DQ16	F2
27	DNU	DQ17	DQ19	U3	65	A20	A20	(A20)	E12	103	DNU	DQ8	DQ17	F3
28	ZQ	ZQ	ZQ	V2	66	QVLD	QVLD	QVLD	F12	104	DNU	DQ8	DQ17	F3
29	DQ8	DQ13	DQ27	U10	67	DQ3	DQ3	DQ7	F10	105	A21	(A21)	(A21)	E1
30	DQ8	DQ13	DQ27	U10	68	DQ3	DQ3	DQ7	F10	106	A5	A5	A5	F1
31	DNU	DNU	DQ26	U11	69	DNU	DNU	DQ6	F11	107	A6	A6	A6	G2
32	DNU	DNU	DQ26	U11	70	DNU	DNU	DQ6	F11	108	A7	A7	A7	G3
33	DQ7	DQ12	DQ29	T10	71	DQ2	DQ2	DQ5	E10	109	A8	A8	A8	G1
34	DQ7	DQ12	DQ29	T10	72	DQ2	DQ2	DQ5	E10	110	BA2	BA2	BA2	H1
35	DNU	DNU	DQ28	T11	73	DNU	DNU	DQ4	E11	111	A9	A9	A9	H2
36	DNU	DNU	DQ28	T11	74	DNU	DNU	DQ4	E11	112	NF	NF	DK0#	J2
37	DQ6	DQ11	DQ31	R10	75	QK0	QK0	QK0	D11	113	NF	NF	DK0	J1
38	DQ6	DQ11	DQ31	R10	76	QK0#	QK0#	QK0#	D10					

Note Any unused balls that are in the order will read as a logic “0”.

JTAG Instructions

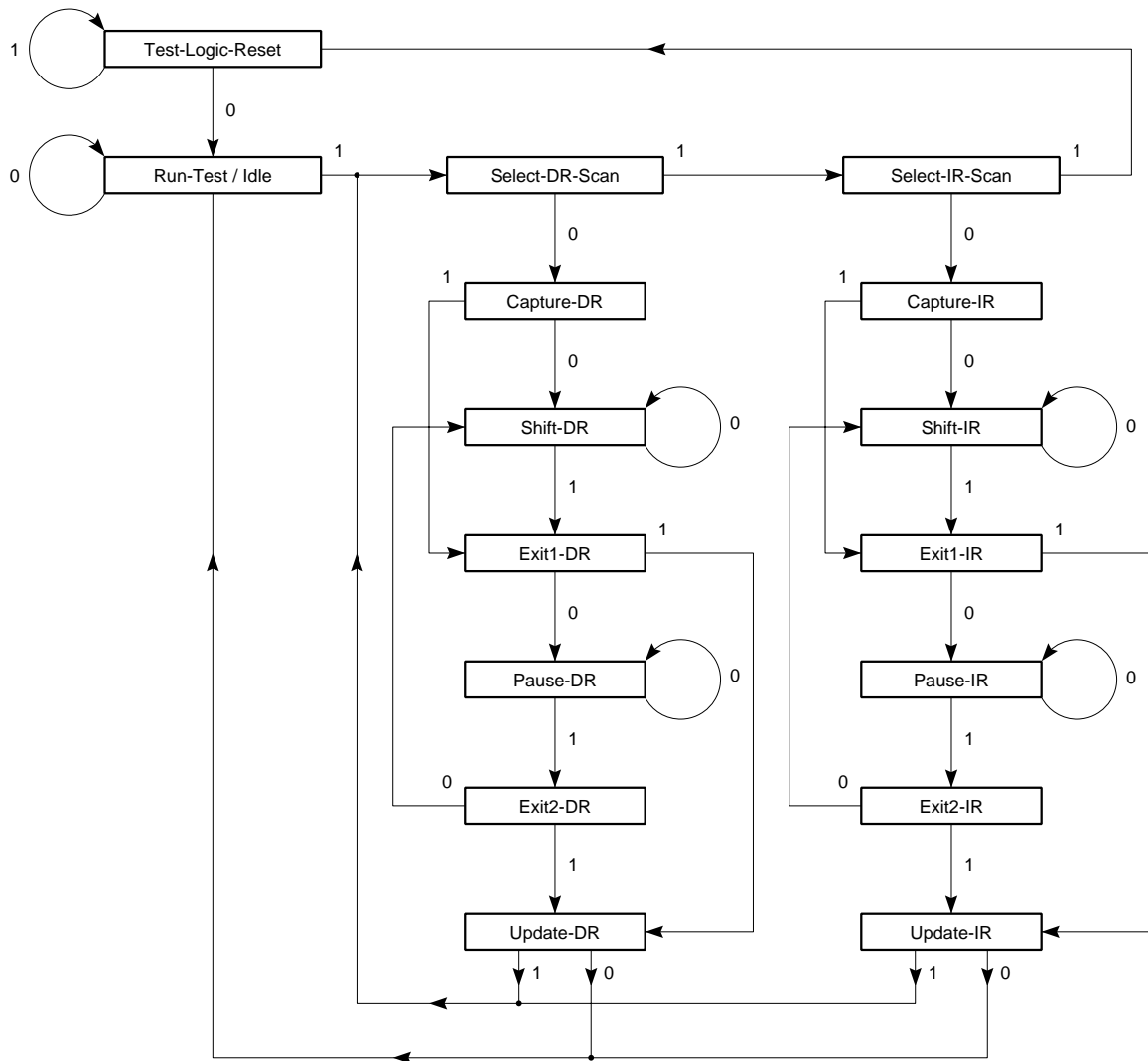
Many different instructions (2⁸) are possible with the 8-bit instruction register. All used combinations are listed in **Table 3-8**, Instruction Codes. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RAM is fully compliant to the 1149.1 convention. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

Table 3-8

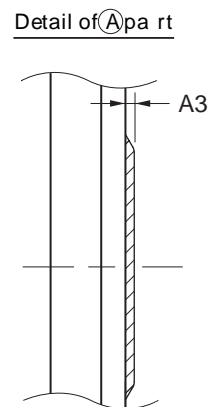
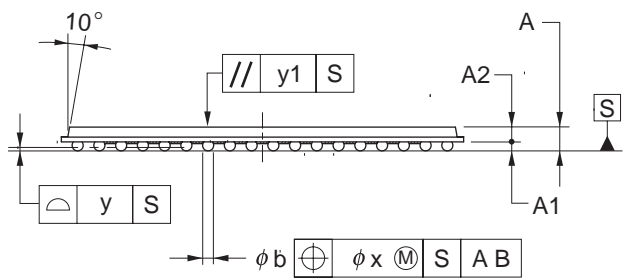
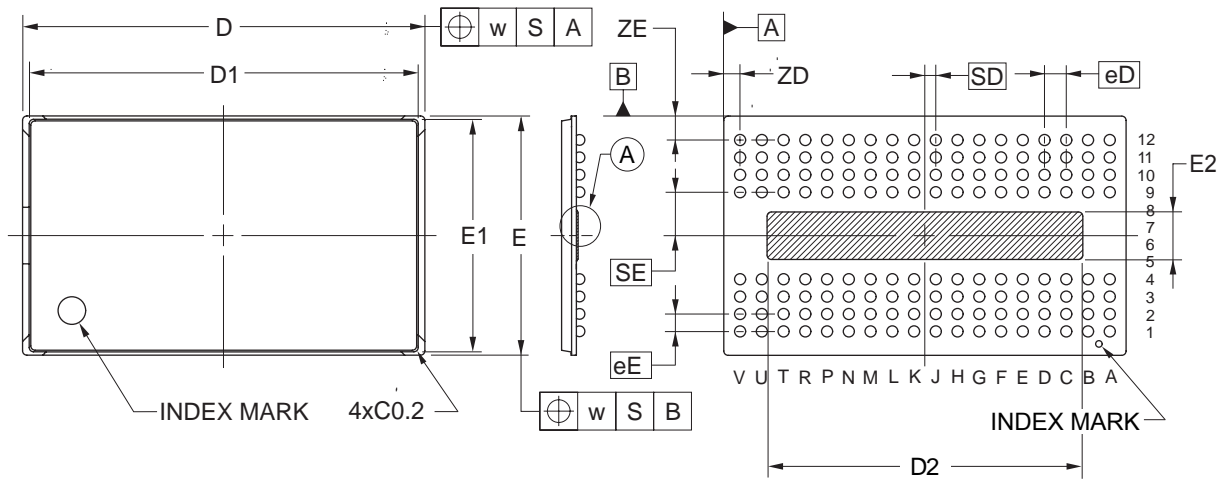
Instructions	Instruction Code [7:0]	Description
EXTEST	0000 0000	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	0010 0001	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
SAMPLE / PRELOAD	0000 0101	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and DQ pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t _{CS} plus t _{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins.
CLAMP	0000 0111	When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary scan register. Selects the bypass register to be connected between TDI and TDO. Data driven by output balls are determined from values held in the boundary scan register.
High-Z	0000 0011	The High-z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RAMs outputs into a High-Z state. Selects the bypass register to be connected between TDI and TDO. All outputs are forced into high impedance state.
BYPASS	1111 1111	When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
Reserved for Future Use	–	The remaining instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



4. Package Dimension

144-PIN TAPE FBGA (μBGA) (18.5x11)



(UNIT:mm)

ITEM	DIMENSIONS
D	18.50±0.10
D1	17.90
D2	14.52
E	11.00±0.10
E1	10.70
E2	2.184
w	0.20
A	1.07±0.10
A1	0.39±0.05
A2	0.68
A3	0.08 MAX.
eD	1.00
eE	0.80
SD	0.50
SE	2.00
b	0.51±0.05
x	0.15
y	0.10
y1	0.20
ZD	0.75
ZE	1.10

P144FF-80-DW1

5. Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

Types of Surface Mount Devices

μPD48576209FF-DW1 : 144-pin TAPE FBGA (18.5 x 11)

μPD48576218FF-DW1 : 144-pin TAPE FBGA (18.5 x 11)

μPD48576236FF-DW1 : 144-pin TAPE FBGA (18.5 x 11)

Quality Grade

- A quality grade of the products is “Standard”.
- Anti-radioactive design is not implemented in the products.
- Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

Revision History	μPD48576209, μPD48576218, μPD48576236
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Rev.	Date	Description	
		Page	Summary
Rev.0.01	'10.11.08	-	New Preliminary Data Sheet
Rev.1.00	'11.09.27	- P12 P16	New Data Sheet Update DC Characteristics Update Thermal Impedance
Rev.2.00	'12.05.10	P39, P40 P41, P42	Update Input Slew Rate Derating
Rev.3.00	'12.10.01	P18,P19 P35	Update Power-On Sequence

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141