

# μPD48288118AF1

## 288M-BIT Low Latency DRAM Separate I/O

R10DS0255EJ0101

Rev. 1.01

Jan. 15, 2016

### Description

The μPD48288118AF1 is a 16,777,216-word by 18 bit synchronous double data rate Low Latency RAM fabricated with advanced CMOS technology using one-transistor memory cell.

The μPD48288118AF1 integrate unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (CK and CK#) are latched on the positive edge of CK and CK#. These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

### Specification

- Density: 288M bit
- Organization
  - Separate I/O: 2M words x 18 bits x 8 banks
- Operating frequency: 533 / 400 / 300 MHz
- Interface: HSTL I/O
- Package: 144-pin FBGA
  - Package size: 18.5 x 11
  - Lead free
- Power supply
  - 2.5 V V<sub>EXT</sub>
  - 1.8 V V<sub>DD</sub>
  - 1.5 V or 1.8 V V<sub>DDQ</sub>
- Refresh command
  - Auto Refresh
  - 8192 cycle / 32 ms for each bank
  - 64K cycle / 32 ms for total
- Operating case temperature : T<sub>c</sub> = 0 to 95°C

### Features

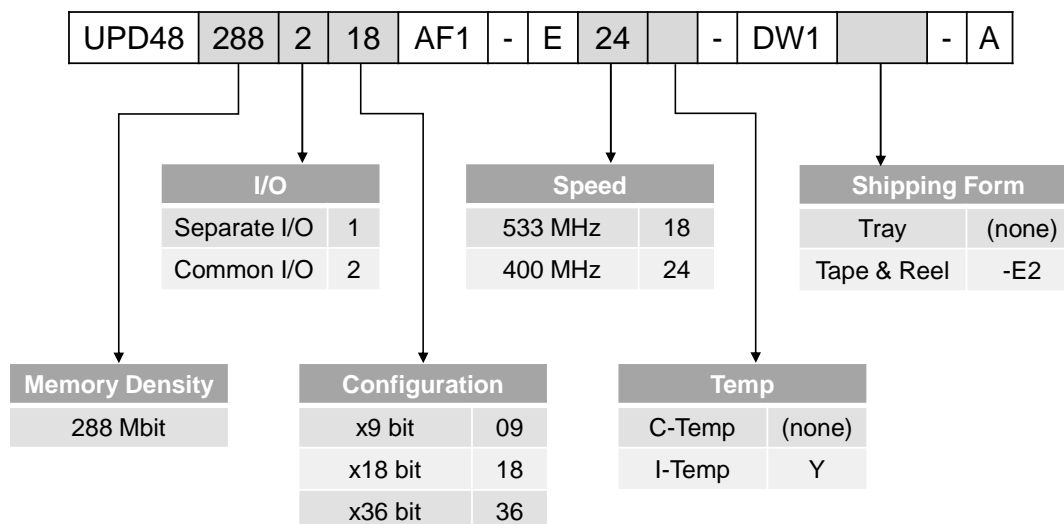
- SRAM-type interface
- Double-data-rate architecture
- PLL circuitry
- Cycle time:
  - 1.875 ns @ t<sub>RC</sub> = 15 ns
  - 2.5 ns @ t<sub>RC</sub> = 15 ns
  - 2.5 ns @ t<sub>RC</sub> = 20 ns
  - 3.3 ns @ t<sub>RC</sub> = 20 ns
- Non-multiplexed addresses
- Multiplexing option is available.
- Data mask for WRITE commands
- Differential input clocks (CK and CK#)
- Differential input data clocks (DK and DK#)
- Data valid signal (QVLD)
- Programmable burst length: 2 / 4 / 8 (x18)
- User programmable impedance output (25 Ω - 60 Ω)
- JTAG boundary scan

## Ordering Information

Part number	Cycle Time ns	Clock Frequency MHz	Random Cycle ns	Organization (word x bit)	Core Supply Voltage (V <sub>EXT</sub> ) V	Core Supply Voltage (V <sub>DD</sub> ) V	Output Supply Voltage (V <sub>DDQ</sub> ) V	Package
μPD48288118AF1-E18-DW1-A	1.875	533	15	16 M x 18	2.5 + 0.13 2.5 - 0.12	1.8 ± 0.1	1.5 ± 0.1 or 1.8 ± 0.1	144-pin FBGA (18.5 x 11) Lead-free
μPD48288118AF1-E24-DW1-A	2.5	400	15					

## Part Number Definition

Example) UPD48288218AF1-E24-DW1-A



## Pin Arrangement

144-pin FBGA (18.5 x 11)  
(Top View) [Separate I/O x18]

	1	2	3	4	5	6	7	8	9	10	11	12
A	V <sub>REF</sub>	V <sub>SS</sub>	V <sub>EXT</sub>	V <sub>SS</sub>					V <sub>SS</sub>	V <sub>EXT</sub>	TMS	TCK
B	V <sub>DD</sub>	D4	Q4	V <sub>SSQ</sub>					V <sub>SSQ</sub>	Q0	D0	V <sub>DD</sub>
C	V <sub>TT</sub>	D5	Q5	V <sub>DDQ</sub>					V <sub>DDQ</sub>	Q1	D1	V <sub>TT</sub>
D	Note 1 (A22)	D6	Q6	V <sub>SSQ</sub>					V <sub>SSQ</sub>	QK0#	QK0	V <sub>SS</sub>
E	Note 1 (A21)	D7	Q7	V <sub>DDQ</sub>					V <sub>DDQ</sub>	Q2	D2	Note 1 (A20)
F	A5	D8	Q8	V <sub>SSQ</sub>					V <sub>SSQ</sub>	Q3	D3	QVLD
G	A8	A6	A7	V <sub>DD</sub>					V <sub>DD</sub>	A2	A1	A0
H	BA2	A9	V <sub>SS</sub>	V <sub>SS</sub>					V <sub>SS</sub>	V <sub>SS</sub>	A4	A3
J	Note 2 NF	Note 2 NF	V <sub>DD</sub>	V <sub>DD</sub>					V <sub>DD</sub>	V <sub>DD</sub>	BA0	CK
K	DK	DK#	V <sub>DD</sub>	V <sub>DD</sub>					V <sub>DD</sub>	V <sub>DD</sub>	BA1	CK#
L	REF#	CS#	V <sub>SS</sub>	V <sub>SS</sub>					V <sub>SS</sub>	V <sub>SS</sub>	A14	A13
M	WE#	A16	A17	V <sub>DD</sub>					V <sub>DD</sub>	A12	A11	A10
N	A18	D14	Q14	V <sub>SSQ</sub>					V <sub>SSQ</sub>	Q9	D9	A19
P	A15	D15	Q15	V <sub>DDQ</sub>					V <sub>DDQ</sub>	Q10	D10	DM
R	V <sub>SS</sub>	QK1	QK1#	V <sub>SSQ</sub>					V <sub>SSQ</sub>	Q11	D11	V <sub>SS</sub>
T	V <sub>TT</sub>	D16	Q16	V <sub>DDQ</sub>					V <sub>DDQ</sub>	Q12	D12	V <sub>TT</sub>
U	V <sub>DD</sub>	D17	Q17	V <sub>SSQ</sub>					V <sub>SSQ</sub>	Q13	D13	V <sub>DD</sub>
V	V <sub>REF</sub>	ZQ	V <sub>EXT</sub>	V <sub>SS</sub>					V <sub>SS</sub>	V <sub>EXT</sub>	TDO	TDI

**Notes 1.** Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to V<sub>SS</sub>, or left open.

**2.** No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to V<sub>SS</sub>, or left open.

CK, CK#	: Input clock	ZQ	: Output impedance matching
CS#	: Chip select	TMS	: IEEE 1149.1 Test input
WE#	: WRITE command	TDI	: IEEE 1149.1 Test input
REF#	: Refresh command	TCK	: IEEE 1149.1 Clock input
A0–A19	: Address inputs	TDO	: IEEE 1149.1 Test output
A20–A22	: Reserved for the future	V <sub>REF</sub>	: HSTL input reference input
BA0–BA2	: Bank address input	V <sub>EXT</sub>	: Power Supply
D0–D17	: Data input	V <sub>DD</sub>	: Power Supply
Q0–Q17	: Data output	V <sub>DDQ</sub>	: DQ Power Supply
DK, DK#	: Input data clock	V <sub>SS</sub>	: Ground
DM	: Input data Mask	V <sub>SSQ</sub>	: DQ Ground
QK0–QK1, QK0#–QK1#	: Output data clock	V <sub>TT</sub>	: Power Supply
QVLD	: Data Valid	NF	: No function

# indicates active LOW signal.

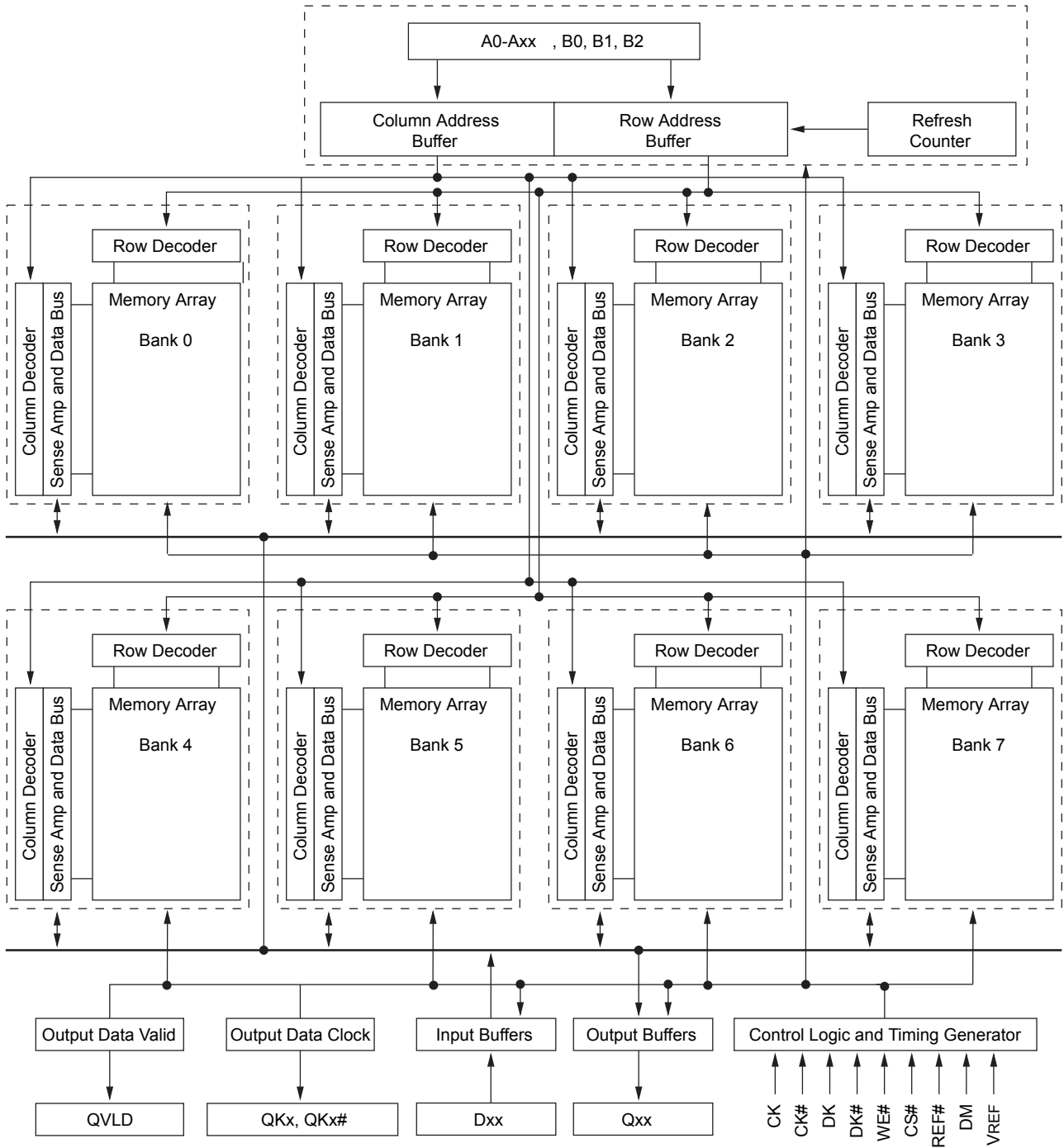
Pin Description

(1/2)

Symbol	Type	Description
CK, CK#	Input	Clock inputs: CK and CK# are differential clock inputs. This input clock pair registers address and control inputs on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip select CS# enables the commands when CS# is LOW and disables them when CS# is HIGH. When the command is disabled, new commands are ignored, but internal operations continue.
WE#, REF#	Input	WRITE command pin, Refresh command pin: WE#, REF# are sampled at the positive edge of CK, WE#, and REF# define (together with CS#) the command to be executed.
A0–A20	Input	Address inputs: A0–A20 define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK. A20 is reserved for address expansion. This expansion address can be treated as address input, but it does not affect the operation of the device.
A21–A22	Input	Reserved for future use: These signals should be tied to V <sub>SS</sub> or leave open.
BA0–BA2	Input	Bank address inputs; Select to which internal bank a command is being applied.
D0–D17	Input	Data input: The D signals form the 18-bit input data bus. During WRITE commands, the data is referenced to both edges of DK.
Q0–Q17	Output	Data output: The Q signals form the 18-bit output data bus. During READ commands, the data is referenced to both edges of QK.
QKx, QKx#	Output	Output data clocks: QKx and QKx# are opposite polarity, output data clocks. They are always free running and edge-aligned with data output from the μPD48288118AF1. QKx# is ideally 180 degrees out of phase with QKx. QK0 and QK0# are aligned with Q0–Q8. QK1 and QK1# are aligned with Q9–Q17.
DK, DK#	Input	Input data clock; DK and DK# are the differential input data clocks. All input data is referenced to both edges of DK. DK# is ideally 180 degrees out of phase with DK. All Ds are referenced to DK and DK#.
DM	Input	Input data mask; The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH along with the WRITE input data. DM is sampled on both edges of DK. The signal should be V <sub>SS</sub> if not used.
QVLD	Output	Data valid; The QVLD indicates valid output data. QVLD is edge-aligned with QKx and QKx#.

Symbol	Type	Description
ZQ	Input /Output	External impedance [25 Ω – 60 Ω]; This signal is used to tune the device outputs to the system data bus impedance. Q output impedance is set to 0.2 x RQ, where RQ is a resistor from this signal to V <sub>SS</sub> . Connecting ZQ to V <sub>SS</sub> invokes the minimum impedance mode. Connecting ZQ to V <sub>DDQ</sub> invokes the maximum impedance mode. Refer to <b>Figure 2-5. Mode Register Bit Map</b> to activate this function.
TMS , TDI	Input	JTAG function pins: IEEE 1149.1 test inputs: These balls may be left as no connects if the JTAG function is not used in the circuit
TCK	Input	JTAG function pin; IEEE 1149.1 clock input: This ball must be tied to V <sub>SS</sub> if the JTAG function is not used in the circuit.
TDO	Output	JTAG function pin; IEEE 1149.1 test output: JTAG output. This ball may be left as no connect if JTAG function is not used.
V <sub>REF</sub>	Input	Input reference voltage; Nominally V <sub>DDQ</sub> /2. Provides a reference voltage for the input buffers.
V <sub>EXT</sub>	Supply	Power supply; 2.5 V nominal. See <b>Recommended DC Operating Conditions</b> for range.
V <sub>DD</sub>	Supply	Power supply; 1.8 V nominal. See <b>Recommended DC Operating Conditions</b> for range.
V <sub>DDQ</sub>	Supply	DQ power supply; Nominally, 1.5 V or 1.8 V. Isolated on the device for improved noise immunity. See <b>Recommended DC Operating Conditions</b> for range.
V <sub>SS</sub>	Supply	Ground
V <sub>SSQ</sub>	Supply	DQ ground; Isolated on the device for improved noise immunity.
V <sub>TT</sub>	Supply	Power supply; Isolated termination supply. Nominally, V <sub>DDQ</sub> /2. See <b>Recommended DC Operating Conditions</b> for range.
NF		No function; These balls may be connected to V <sub>SS</sub> .
DNU		Do not use; These balls may be connected to V <sub>SS</sub> .

Block Diagram



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## 1. Electrical Characteristics

### Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V <sub>EXT</sub>		-0.3 to +2.8	V
Supply voltage	V <sub>DD</sub>		-0.3 to +2.1	V
Output supply voltage, Input voltage, Input / Output voltage	V <sub>DDQ</sub>		-0.3 to +2.1	V
Input / Output voltage	V <sub>IH</sub> / V <sub>IL</sub>		-0.3 to +2.1	V
Junction temperature	T <sub>j</sub> MAX.		110	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Recommended DC Operating Conditions

0°C ≤ T<sub>c</sub> ≤ 95°C; 1.7 V ≤ V<sub>DD</sub> ≤ 1.9 V, unless otherwise noted.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V <sub>EXT</sub>		2.38	2.5	2.63	V	1
Supply voltage	V <sub>DD</sub>		1.7	1.8	1.9	V	1
Output supply voltage	V <sub>DDQ</sub>		1.4		V <sub>DD</sub>	V	1, 2, 3
Reference Voltage	V <sub>REF</sub>		0.49 x V <sub>DDQ</sub>	0.5 x V <sub>DDQ</sub>	0.51 x V <sub>DDQ</sub>	V	1, 4, 5
Termination voltage	V <sub>TT</sub>		0.95 x V <sub>REF</sub>	V <sub>REF</sub>	1.05 x V <sub>REF</sub>	V	1, 6
Input HIGH voltage	V <sub>IH(DC)</sub>		V <sub>REF</sub> + 0.1			V	1
Input LOW voltage	V <sub>IL(DC)</sub>				V <sub>REF</sub> - 0.1	V	1

**Notes** 1. All voltage referenced to V<sub>SS</sub> (GND).

2. During normal operation, V<sub>DDQ</sub> must not exceed V<sub>DD</sub>.

3. V<sub>DDQ</sub> can be set to a nominal 1.5 V ± 0.1 V or 1.8 V ± 0.1 V supply.

4. Typically the value of V<sub>REF</sub> is expect to be 0.5 x V<sub>DDQ</sub> of the transmitting device. V<sub>REF</sub> is expected to track variations in V<sub>DDQ</sub>.

5. Peak-to-peak AC noise on V<sub>REF</sub> must not exceed ± 2% V<sub>REF(DC)</sub>.

6. V<sub>TT</sub> is expected to be set equal to V<sub>REF</sub> and must track variations in the DC level of V<sub>REF</sub>.



**DC Characteristics**

0°C ≤ T<sub>C</sub> ≤ 95°C; 1.7 V ≤ V<sub>DD</sub> ≤ 1.9 V, unless otherwise noted

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Note
Input leakage current	I <sub>LI</sub>		-5	+5	μA	1,2
Output leakage current	I <sub>LO</sub>		-5	+5	μA	1,2
Reference voltage current	I <sub>REF</sub>		-5	+5	μA	1,2
Output high current	I <sub>OH</sub>	V <sub>OH</sub> = V <sub>DD</sub> Q/2	(V <sub>DD</sub> Q/2) / (1.15 x RQ/5)	(V <sub>DD</sub> Q/2) / (0.85 x RQ/5)	mA	3,4
Output low current	I <sub>OL</sub>	V <sub>OL</sub> = V <sub>DD</sub> Q/2	(V <sub>DD</sub> Q/2) / (1.15 x RQ/5)	(V <sub>DD</sub> Q/2) / (0.85 x RQ/5)	mA	3,4

- Notes**
1. Outputs are impedance-controlled. | I<sub>OH</sub> | = (V<sub>DD</sub>Q/2)/(RQ/5) for values of 125 Ω ≤ RQ ≤ 300 Ω.
  2. Outputs are impedance-controlled. I<sub>OL</sub> = (V<sub>DD</sub>Q/2)/(RQ/5) for values of 125 Ω ≤ RQ ≤ 300 Ω.
  3. I<sub>OH</sub> and I<sub>OL</sub> are defined as absolute values and are measured at V<sub>DD</sub>Q/2. I<sub>OH</sub> flows from the device, I<sub>OL</sub> flows into the device.
  4. If MRS bit A8 is 0, use RQ = 250 Ω in the equation in lieu of presence of an external impedance matched resistor.

**Capacitance (T<sub>A</sub> = 25 °C, f = 1MHz)**

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Address / Control Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	1.5	2.5	pF
I/O, Output, Other capacitance (D, Q, DM, QK, QVLD)	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V	3.5	5.0	pF
Clock Input capacitance	C <sub>clk</sub>	V <sub>clk</sub> = 0 V	2.0	3.0	pF
JTAG pins	C <sub>J</sub>	V <sub>J</sub> = 0 V	2.0	5.0	pF

**Remark** These parameters are periodically sampled and not 100% tested.  
Capacitance is not tested on ZQ pin.

**Recommended AC Operating Conditions**

0°C ≤ T<sub>C</sub> ≤ 95°C; 1.7 V ≤ V<sub>DD</sub> ≤ 1.9 V, unless otherwise noted

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Input HIGH voltage	V <sub>IH(AC)</sub>		V <sub>REF</sub> + 0.2		V	1
Input LOW voltage	V <sub>IL(AC)</sub>			V <sub>REF</sub> - 0.2	V	1

**Note** Overshoot: V<sub>IH(AC)</sub> ≤ V<sub>DD</sub>Q + 0.7 V for t ≤ t<sub>CK</sub>/2  
 Undershoot: V<sub>IL(AC)</sub> ≥ -0.5 V for t ≤ t<sub>CK</sub>/2  
 Control input signals may not have pulse widths less than t<sub>CKH</sub> (MIN.) or operate at cycle rates less than t<sub>CK</sub> (MIN.).

DC Characteristics

I<sub>DD</sub> / I<sub>SB</sub> Operating Conditions

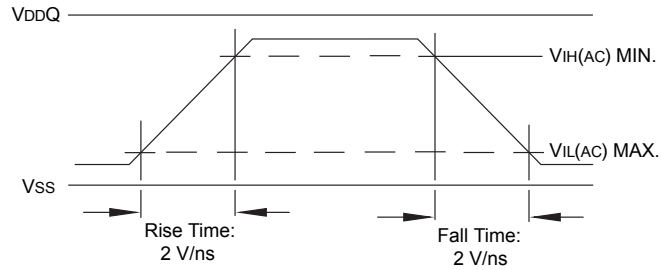
Parameter	Symbol	Test condition	MAX.				Unit	
			-E18		-E24			
			t <sub>RC</sub> =15ns		t <sub>RC</sub> =20ns			
			533MHz	400MHz	400MHz	300MHz		
Standby current	I <sub>SB1</sub>	t <sub>CK</sub> = Idle All banks idle, no inputs toggling	V <sub>DD</sub>	55	55	55	55	mA
			V <sub>EXT</sub>	5	5	5	5	
Active standby current	I <sub>SB2</sub>	CS# = HIGH, No commands, half bank / address / data change once every four clock cycles	V <sub>DD</sub>	250	215	215	190	mA
			V <sub>EXT</sub>	5	5	5	5	
Operating current	I <sub>DD1</sub>	BL=2, sequential bank access, bank transitions once every t <sub>RC</sub> , half address transitions once every t <sub>RC</sub> , read followed by write sequence, continuous data during WRITE commands.	V <sub>DD</sub>	333	302	266	239	mA
			V <sub>EXT</sub>	10	10	10	10	
Operating current	I <sub>DD2</sub>	BL=4, sequential bank access, bank transitions once every t <sub>RC</sub> , half address transitions once every t <sub>RC</sub> , read followed by write sequence, continuous data during WRITE commands.	V <sub>DD</sub>	360	345	288	262	mA
			V <sub>EXT</sub>	10	10	10	10	
Operating current	I <sub>DD3</sub>	BL=8, sequential bank access, bank transitions once every t <sub>RC</sub> , half address transitions once every t <sub>RC</sub> , read followed by write sequence, continuous data during WRITE commands.	V <sub>DD</sub>	377	357	299	276	mA
			V <sub>EXT</sub>	15	15	15	15	
Burst refresh current	I <sub>REF1</sub>	Eight bank cyclic refresh, continuous address/data, command bus remains in refresh for all banks	V <sub>DD</sub>	604	464	464	362	mA
			V <sub>EXT</sub>	45	30	30	25	
Disturbed refresh current	I <sub>REF2</sub>	Single bank refresh, sequential bank access, half address transitions once every t <sub>RC</sub> , continuous data	V <sub>DD</sub>	260	219	205	173	mA
			V <sub>EXT</sub>	10	10	10	10	
Operating burst write current	I <sub>DD2W</sub>	BL=2, cyclic bank access, half of address bits change every clock cycle, continuous data, measurement is taken during continuous WRITE	V <sub>DD</sub>	890	691	691	542	mA
			V <sub>EXT</sub>	40	35	35	30	
Operating burst write current	I <sub>DD4W</sub>	BL=4, cyclic bank access, half of address bits change every two clocks, continuous data, measurement is taken during continuous WRITE	V <sub>DD</sub>	609	478	478	380	mA
			V <sub>EXT</sub>	25	20	20	20	
Operating burst write current	I <sub>DD8W</sub>	BL=8, cyclic bank access, half of address bits change every four clocks, continuous data, measurement is taken during continuous WRITE	V <sub>DD</sub>	478	378	378	303	mA
			V <sub>EXT</sub>	25	20	20	20	
Operating burst read current	I <sub>DD2R</sub>	BL=2, cyclic bank access, half of address bits change every clock cycle, measurement is taken during continuous READ	V <sub>DD</sub>	927	712	712	551	mA
			V <sub>EXT</sub>	40	35	35	30	
Operating burst read current	I <sub>DD4R</sub>	BL=4, cyclic bank access, half of address bits change every two clocks, measurement is taken during continuous READ	V <sub>DD</sub>	619	477	477	377	mA
			V <sub>EXT</sub>	25	20	20	20	
Operating burst read current	I <sub>DD8R</sub>	BL=8, cyclic bank access, half of address bits change every four clocks, measurement is taken during continuous READ	V <sub>DD</sub>	475	368	368	292	mA
			V <sub>EXT</sub>	25	20	20	20	

- Remarks 1.** I<sub>DD</sub> specifications are tested after the device is properly initialized.  $0^{\circ}\text{C} \leq T_c \leq 95^{\circ}\text{C}$ ;  $1.7\text{ V} \leq V_{DD} \leq 1.9\text{ V}$ ,  $2.38\text{ V} \leq V_{EXT} \leq 2.63\text{ V}$ ,  $1.4\text{ V} \leq V_{DDQ} \leq V_{DD}$ ,  $V_{REF} = V_{DDQ}/2$
2.  $t_{CK} = t_{DK} = \text{MIN.}$ ,  $t_{RC} = \text{MIN.}$
  3. Input slew rate is specified in **Recommended DC Operating Conditions** and **Recommended AC Operating Conditions**.
  4. I<sub>DD</sub> parameters are specified with ODT disabled.
  5. Continuous data is defined as half the D or Q signals changing between HIGH and LOW every half clock cycles (twice per clock).
  6. Continuous address is defined as half the address signals between HIGH and LOW every clock cycles (once per clock).
  7. Sequential bank access is defined as the bank address incrementing by one ever  $t_{RC}$ .
  8. Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL=4 this is every other clock.
  9. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than per clock cycle.

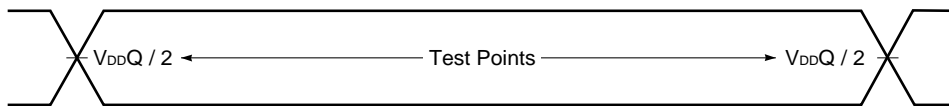
AC Characteristics

AC Test Conditions

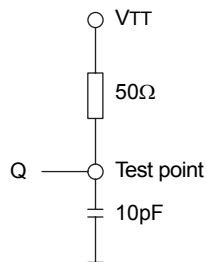
Input waveform



Output waveform



Output load condition



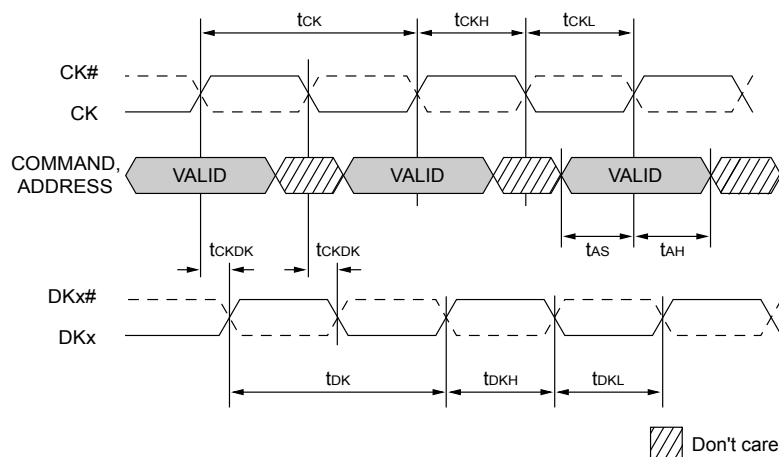
AC Characteristics <Read and Write Cycle>

Parameter	Symbol	-E18 (533 MHz)		-E24 (400 MHz)   (300 MHz)				Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
		<b>Clock</b>							
Clock cycle time (CK,CK#,DK,DK#)	t <sub>CK</sub> , t <sub>DK</sub>	1.875	5.7	2.5	5.7	3.3	5.7	ns	
Clock frequency (CK,CK#,DK,DK#)	t <sub>CK</sub> , t <sub>DK</sub>	175	533	175	400	175	300	MHz	
Random Cycle time	t <sub>RC</sub>	15		15		20		ns	
Clock Jitter: period	t <sub>JIT PER</sub>	-100	100	-150	150	-200	200	ps	1, 2
Clock Jitter: cycle-to-cycle	t <sub>JIT CC</sub>		200		300		400	ps	
Clock HIGH time (CK,CK#,DK,DK#)	t <sub>CKH</sub> , t <sub>DKH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	Cycle	
Clock LOW time (CK,CK#,DK,DK#)	t <sub>CKL</sub> , t <sub>DKL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	Cycle	
Clock to input data clock	t <sub>CKDK</sub>	-0.3	0.3	-0.45	0.5	-0.45	1.0	ns	
Mode register set cycle time to any command	t <sub>MRSC</sub>	6		6		6		Cycle	
PLL Lock time	t <sub>CK Lock</sub>	15		15		15		μs	
Clock static to PLL reset	t <sub>CK Reset</sub>	30		30		30		ns	
<b>Output Times</b>									
Output data clock HIGH time	t <sub>QKH</sub>	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CKH</sub>	
Output data clock LOW time	t <sub>QKL</sub>	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CKL</sub>	
QK edge to clock edge skew	t <sub>CKQK</sub>	-0.2	0.2	-0.25	0.25	-0.3	0.3	ns	
QK edge to output data edge	t <sub>QKQ0</sub> , t <sub>QKQ1</sub>	-0.12	0.12	-0.2	0.2	-0.25	0.25	ns	3, 5
QK edge to any output data	t <sub>QKQ</sub>	-0.22	0.22	-0.3	0.3	-0.35	0.35	ns	4, 5
QK edge to QVLD	t <sub>QKVLD</sub>	-0.22	0.22	-0.3	0.3	-0.35	0.35	ns	
<b>Setup Times</b>									
Address/command and input	t <sub>AS</sub> /t <sub>CS</sub>	0.3		0.4		0.5		ns	
Data-in and data mask to DK	t <sub>DS</sub>	0.17		0.25		0.3		ns	
<b>Hold Times</b>									
Address/command and input	t <sub>AH</sub> /t <sub>CH</sub>	0.3		0.4		0.5		ns	
Data-in and data mask to DK	t <sub>DH</sub>	0.17		0.25		0.3		ns	

- Notes**
1. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
  2. Frequency drift is not allowed.
  3. t<sub>QKQ0</sub> is referenced to Q0–Q8 and t<sub>QKQ1</sub> is referenced to Q9–Q17.
  4. t<sub>QKQ</sub> takes into account the skew between any QKx and any Q.
  5. t<sub>QKQ</sub>, t<sub>QKQX</sub> are guaranteed by design.

**Remark** All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V<sub>REF</sub> of the command, address, and data signals.

Figure 1-1. Clock / Input Data Clock Command / Address Timings



Temperature and Thermal Impedance

Temperature Limits

Parameter	Symbol	MIN.	MAX.	Unit	Note
Reliability junction temperature	T <sub>J</sub>	0	+110	°C	1
Operating junction temperature	T <sub>J</sub>	0	+100	°C	2
Operating case temperature	T <sub>c</sub>	0	+95	°C	3

- Notes**
1. Temperatures greater than 110°C may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or above this is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the part.
  2. Junction temperature depends upon cycle time, loading, ambient temperature, and airflow.
  3. MAX operating case temperature; T<sub>c</sub> is measured in the center of the package. Device functionality is not guaranteed if the device exceeds maximum T<sub>c</sub> during operation.

Thermal Impedance

Substrate	Ball	θ <sub>ja</sub> (°C/W)			θ <sub>jb</sub> (°C/W)	θ <sub>jc</sub> (°C/W)
		Air Flow = 0 m/s	Air Flow = 1 m/s	Air Flow = 2 m/s		
4 - Layer	Lead free	18.9	15.2	14.4	9.1	3.0

## 2. Operation

### 2.1 Command Operation

According to the functional signal description, the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

**Table 2-1. Address Widths at Different Burst Lengths**

Burst Length	Configuration
	x18
BL=2	A0–A19
BL=4	A0–A18
BL=8	A0–A17

**Table 2-2. Command Table**

Operation	Code	CS#	WE#	REF#	A0–An <sup>Note1</sup>	BA0–BA2	Note
Device DESELECT / No Operation	DESEL / NOP	H	X	X	X	X	
MRS: Mode Register Set	MRS	L	L	L	OPCODE	X	2
READ	READ	L	H	H	A	BA	3
WRITE	WRITE	L	L	H	A	BA	3
AUTO REFRESH	AREF	L	H	L	X	BA	

- Notes**
1. n = 20.
  2. Only A0–A17 are used for the MRS command.
  3. See **Table 2-1**.

**Remark** X = “Don’t Care”, H = logic HIGH, L = logic LOW, A = valid address, BA = valid bank address

### 2.2 Description of Commands

#### DESEL / NOP <sup>Note1</sup>

The NOP command is used to perform a no operation to the μPD48288118AF1, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.

#### MRS

The mode register is set via the address inputs A0–A17. See **Figure 2-5. Mode Register Bit Map** for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress.

#### READ

The READ command is used to initiate a burst read access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A20 selects the data location within the bank.

#### WRITE

The WRITE command is used to initiate a burst write access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A20 selects the data location within the bank. Input data appearing on the D is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written).

**AREF**

The AREF is used during normal operation of the μPD48288118AF1 to refresh the memory content of a bank. The command is non-persistent, so it must be issued each time a refresh is required. The value on the BA0–BA2 inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a “Don’t Care” during the AREF command. The μPD48288118AF1 requires 64K cycles at an average periodic interval of 0.49μs<sup>Note2</sup> (MAX.). To improve efficiency, eight AREF commands (one for each bank) can be posted to μPD48288118AF1 at periodic intervals of 3.9 μs<sup>Note3</sup>.

Within a period of 32 ms, the entire memory must be refreshed. The delay between the AREF command and a subsequent command to same bank must be at least  $t_{RC}$  as continuous refresh. Other refresh strategies, such as burst refresh, are also possible.

**Notes** 1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.

2. Actual refresh is  $32 \text{ ms} / 8k / 8 = 0.488 \mu\text{s}$ .

3. Actual refresh is  $32 \text{ ms} / 8k = 3.90 \mu\text{s}$ .

**2.3 Initialization**

The μPD48288118AF1 must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device. The following sequence is used for Power-Up:

1. Apply power ( $V_{EXT}$ ,  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ ,  $V_{TT}$ ) and start clock as soon as the supply voltages are stable. Apply  $V_{DD}$  and  $V_{EXT}$  before or at the same time as  $V_{DDQ}$ . Apply  $V_{DDQ}$  before or at the same time as  $V_{REF}$  and  $V_{TT}$ . Although there is no timing relation between  $V_{EXT}$  and  $V_{DD}$ , the chip starts the power-up sequence only after both voltages are at their nominal levels.  $V_{DDQ}$  supply must not be applied before  $V_{DD}$  supply.  $CK/CK\#$  must meet  $V_{ID(DC)}$  prior to being applied. Maintain all remaining balls in NOP conditions.

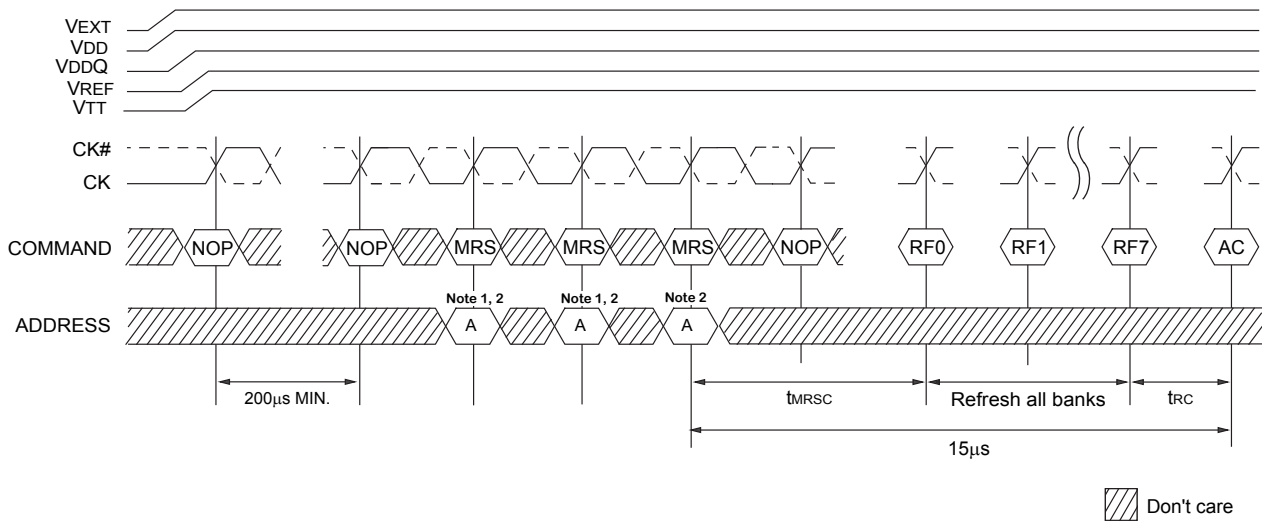
**Note** No rule of apply power sequence is the design target.

2. Maintain stable conditions for 200 μs (MIN.).
3. Issue at least three or more consecutive MRS commands: two dummies or more plus one valid MRS. It is recommended that all address pins are held LOW during the dummy MRS commands.
4.  $t_{MRSC}$  after valid MRS, an AUTO REFRESH command to all 8 banks must be issued and wait for 15 μs with  $CK/CK\#$  toggling in order to lock the PLL prior to normal operation.
5. After  $t_{RC}$ , the chip is ready for normal operation.



2.4 Power-On Sequence

Figure 2-1. Power-Up Sequence



- Notes**
1. Recommended all address pins held LOW during dummy MRS commands.
  2. A10-A17 must be LOW.

**Remark** MRS : MRS command

RFp : REFRESH bank p

AC : Any command

2.5 Programmable Impedance Output Buffer

The μPD48288118AF1 is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and Vss. The value of the resistor must be five times the desired impedance. For example, a 300 Ω resistor is required for an output impedance of 60 Ω. To ensure that output impedance is one fifth the value of RQ (within 15 percent), the range of RQ is 125 Ω to 300 Ω. Output impedance updates may be required because, over time, variations may occur in supply voltage and temperature. The device samples the value of RQ. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update.

2.6 PLL Reset

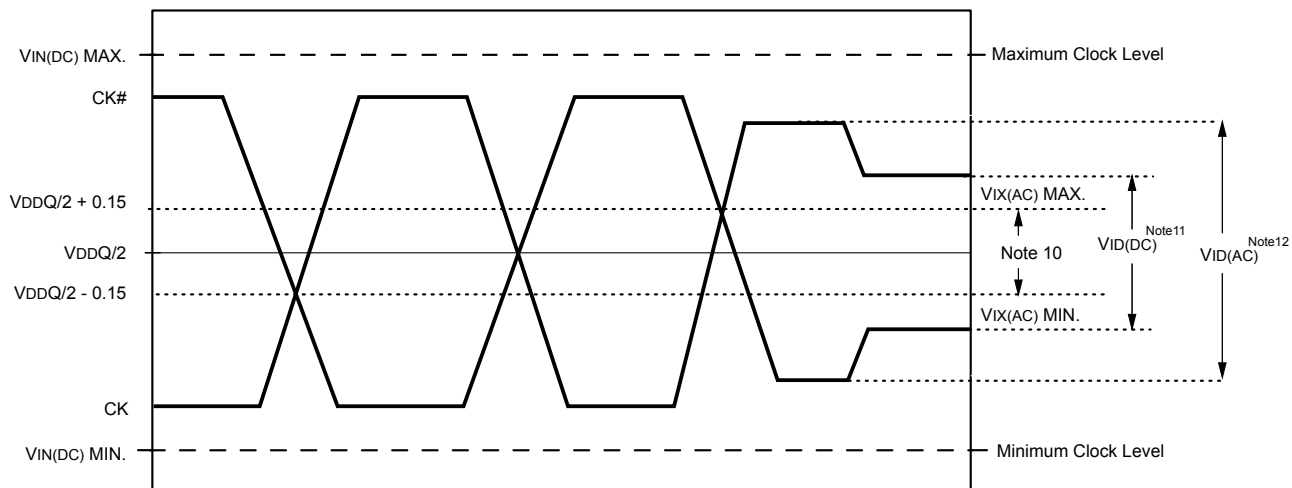
The μPD48288118AF1 utilizes internal Phase-locked loops for maximum output, data valid windows. It can be placed into a stopped-clock state to minimize power with a modest restart time of 15 μs. The clock (CK/CK#) must be toggled for 15 μs in order to stabilize PLL circuits for next READ operation.

2.7 Clock Input

Table 2-3. Clock Input Operation Conditions

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock Input Voltage Level	V <sub>IN(DC)</sub>	CK and CK#	-0.3	V <sub>DDQ</sub> + 0.3	V	
Clock Input Differential Voltage Level	V <sub>ID(DC)</sub>	CK and CK#	0.2	V <sub>DDQ</sub> + 0.6	V	8
Clock Input Differential Voltage Level	V <sub>ID(AC)</sub>	CK and CK#	0.4	V <sub>DDQ</sub> + 0.6	V	8
Clock Input Crossing Point Voltage Level	V <sub>IX(AC)</sub>	CK and CK#	V <sub>DDQ</sub> /2 - 0.15	V <sub>DDQ</sub> /2 + 0.15	V	9

Figure 2-2. Clock Input



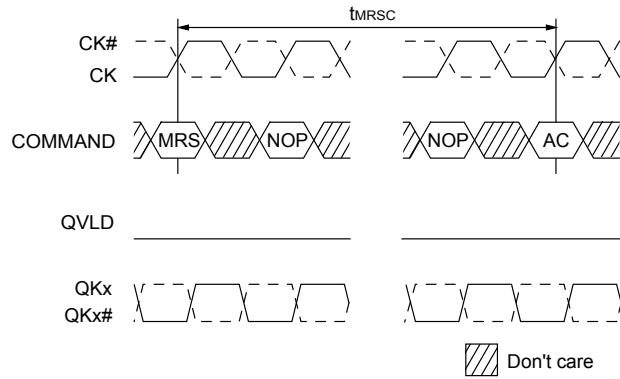
- Notes**
1. DKx and DKx# have the same requirements as CK and CK#.
  2. All voltages referenced to V<sub>SS</sub>.
  3. Tests for AC timing, IDD and electrical AC and DC characteristics may be conducted at normal reference/supply voltage levels; but the related specifications and device operations are tested for the full voltage range specified.
  4. AC timing and IDD tests may use a V<sub>IL</sub> to V<sub>IH</sub> swing of up to 1.5 V in the test environment, but input timing is still referenced to V<sub>REF</sub> (or the crossing point for CK/CK#), and parameters specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2V/ns in the range between V<sub>IL(AC)</sub> and V<sub>IH(AC)</sub>.
  5. The AC and DC input level specifications are as defined in the HSTL Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above[below] the DC input LOW[HIGH] level).
  6. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signal other than CK/CK# is V<sub>REF</sub>.
  7. CK and CK# input slew rate must be  $\geq 2V/ns$  ( $\geq 4V/ns$  if measured differentially).
  8. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and input level on CK#.
  9. The value of V<sub>IX</sub> is expected to equal V<sub>DDQ</sub>/2 of the transmitting device and must track variations in the DC level of the same.
  10. CK and CK# must cross within the region.
  11. CK and CK# must meet at least V<sub>ID(DC)</sub> (MIN.) when static and centered around V<sub>DDQ</sub>/2.
  12. Minimum peak-to-peak swing.

**2.8 Mode Register Set Command (MRS)**

The mode register stores the data for controlling the operating modes of the memory. It programs the μPD48288118AF1 configuration, burst length, and I/O options. During a MRS command, the address inputs A0–A17 are sampled and stored in the mode register.  $t_{MRSC}$  must be met before any command can be issued to the μPD48288118AF1. The mode register may be set at any time during device operation. However, any pending operations are not guaranteed to successfully complete, and all memory cell data are not guaranteed.

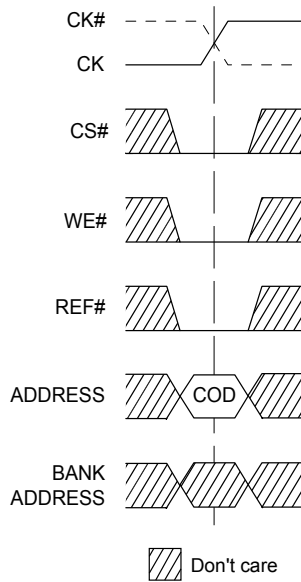
Since MRS is used for internal test mode entry, bits A10–A17 must be set to all “0” at the MRS setting.

**Figure 2-3. Mode Register Set Timing**



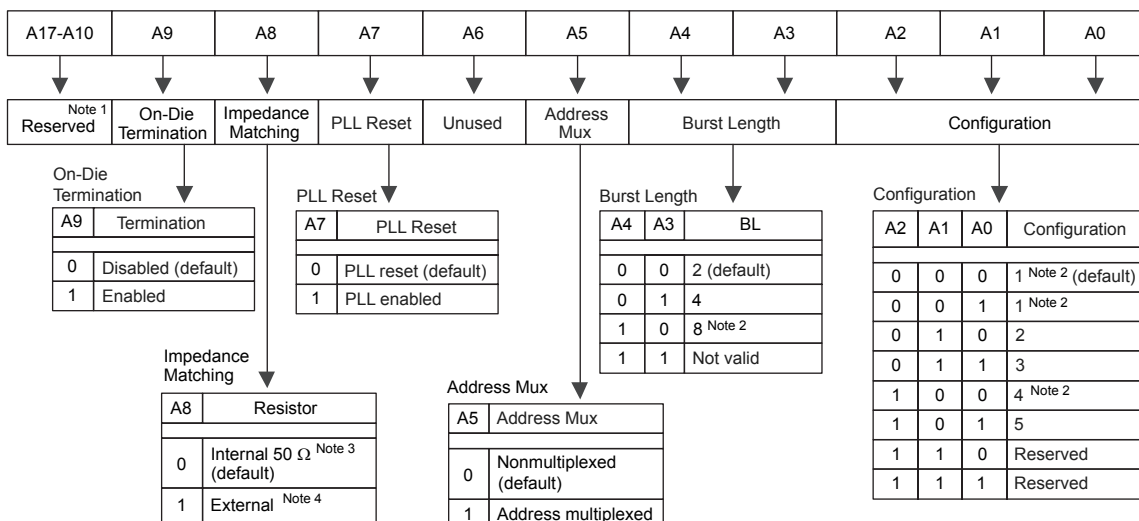
**Remark** MRS: MRS command  
 AC : any command

**Figure 2-4. Mode Register Set**



**Remark** COD: code to be loaded into the register.

Figure 2-5. Mode Register Bit Map



- Notes**
- Bits A10–A17 must be set to all ‘0’. A18–An are “Don’t Care”.
  - BL=8 is not available for configuration 1 and 4.
  - ±30% temperature variation.
  - Within 15%.

**2.9 Read & Write configuration (Non Multiplexed Address Mode)**

Table 2-4 shows, for different operating frequencies, the different μPD48288118AF1 configurations that can be programmed into the mode register. The READ and WRITE latency (t<sub>RL</sub> and t<sub>WL</sub>) values along with the row cycle times (t<sub>RC</sub>) are shown in clock cycles as well as in nanoseconds.

Table 2-4. Configuration Table

Parameter	Configuration					Unit
	1 <sup>Note1</sup>	2	3	4 <sup>Note1, 2</sup>	5	
t <sub>RC</sub>	4	6	8	3	5	t <sub>CK</sub>
t <sub>RL</sub>	4	6	8	3	5	t <sub>CK</sub>
t <sub>WL</sub>	5	7	9	4	6	t <sub>CK</sub>
Valid frequency range	266-175	400-175	533-175	200-175	333-175	MHz

- Notes**
- BL= 8 is not available.
  - The minimum t<sub>RC</sub> is typically 3 cycles, except in the case of a WRITE followed by a READ to the same bank. In this instance the minimum t<sub>RC</sub> is 4 cycles.

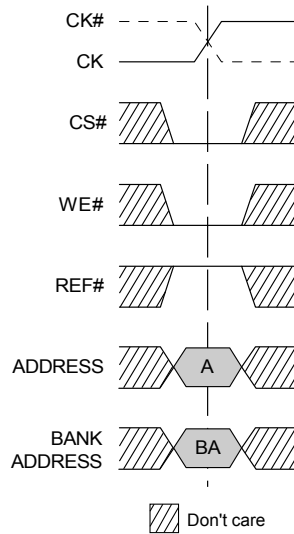
**2.10 Write Operation (WRITE)**

Write accesses are initiated with a WRITE command, as shown in **Figure 2-6**. Row and bank addresses are provided together with the WRITE command. During WRITE commands, data will be registered at both edges of DK according to the programmed burst length (BL). A WRITE latency (WL) one cycle longer than the programmed READ latency (RL + 1) is present, with the first valid data registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command. **Figure 2-10. WRITE Followed By READ: BL=2, RL=4, WL=5, Configuration 1** and **Figure 2-11. WRITE Followed By READ: BL=4, RL=4, WL=5, Configuration 1** illustrate the timing requirements for a WRITE followed by a READ for bursts of two and four, respectively.

Setup and hold times for incoming input data relative to the DK edges are specified as  $t_{DS}$  and  $t_{DH}$ . The input data is masked if the corresponding DM signal is HIGH. The setup and hold times for data mask are also  $t_{DS}$  and  $t_{DH}$ .

**Figure 2-6. WRITE Command**



**Remark** A : Address  
 BA: Bank address

**Figure 2-7. Basic WRITE Burst / DM Timing**

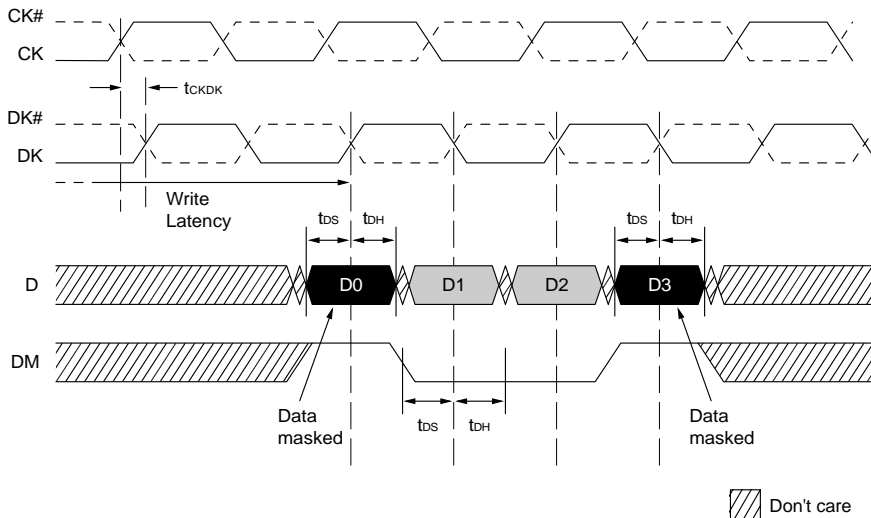


Figure 2-8. WRITE Burst Basic Sequence: BL=2, RL=4, WL=5, Configuration 1

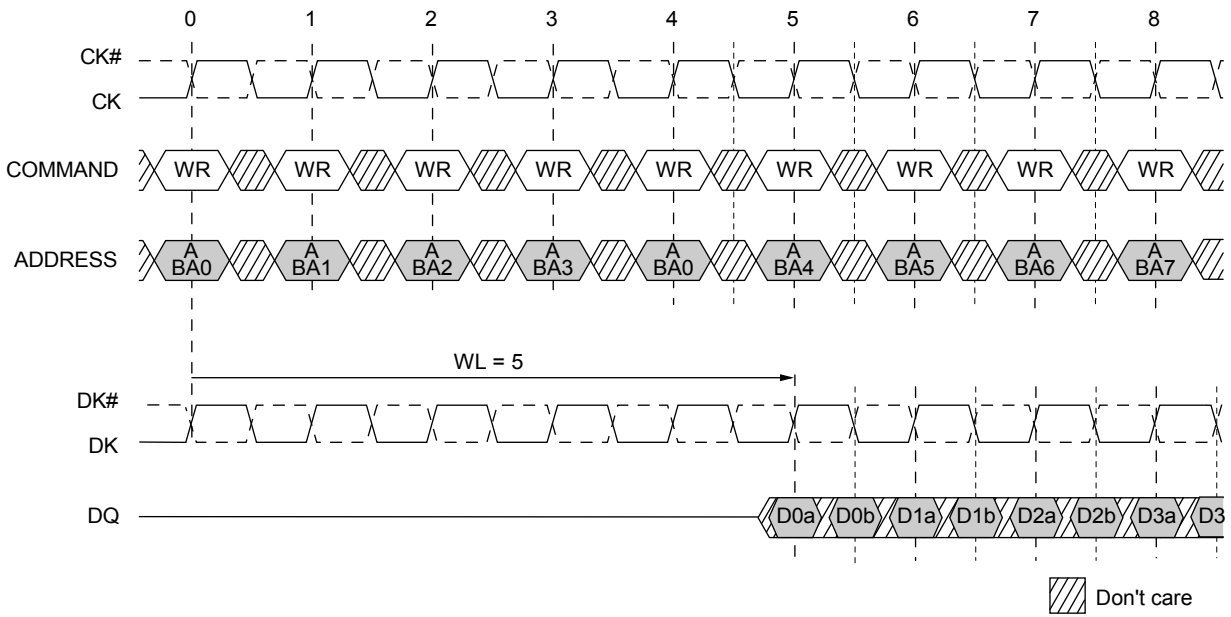
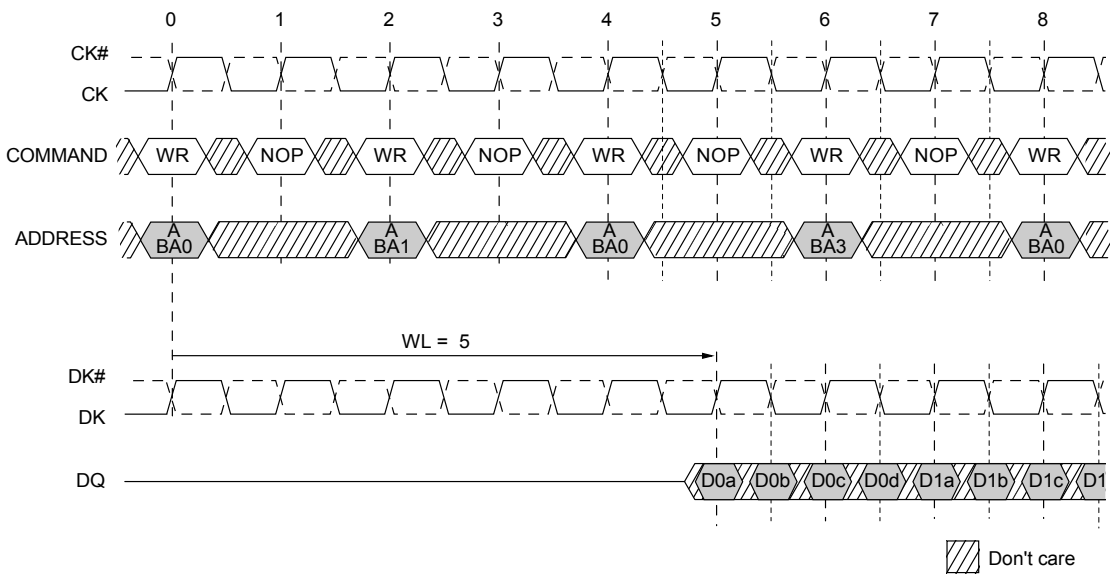


Figure 2-9. WRITE Burst Basic Sequence: BL=4, RL=4, WL=5, Configuration 1



- Remarks 1.**
- WR : WRITE command
  - A/Bap : Address A of bank p
  - WL : WRITE latency
  - Dpq : Data q to bank p
- 2.** Any free bank may be used in any given command. The sequence shown is only one example of a bank sequence.

Figure 2-10. WRITE Followed By READ: BL=2, RL=4, WL=5, Configuration 1

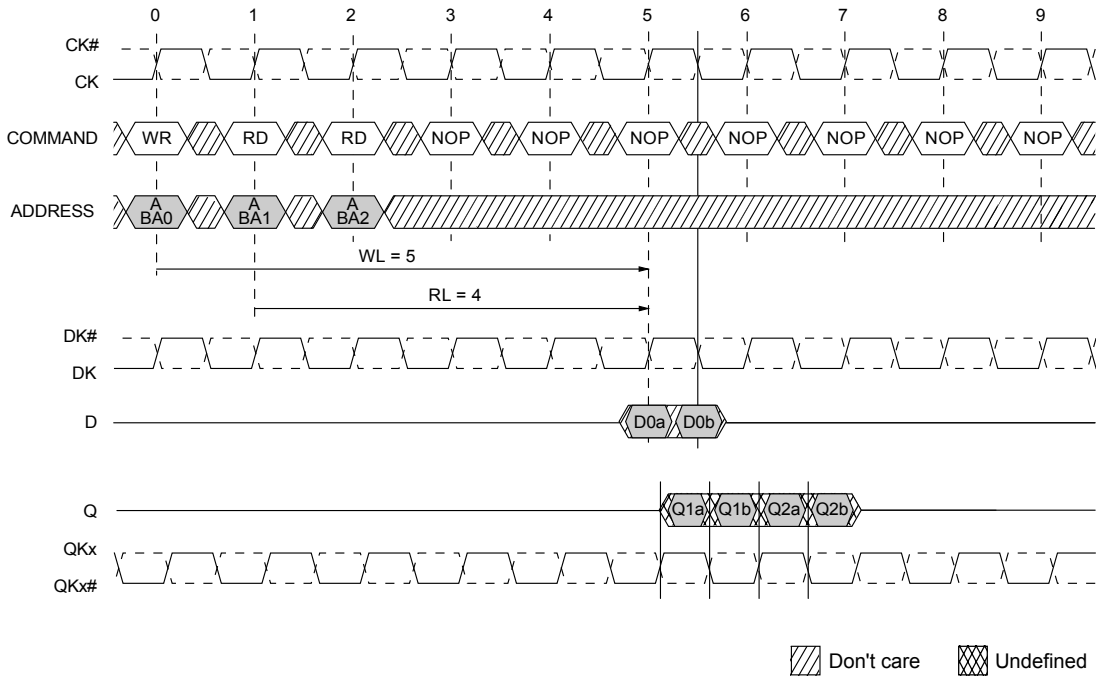
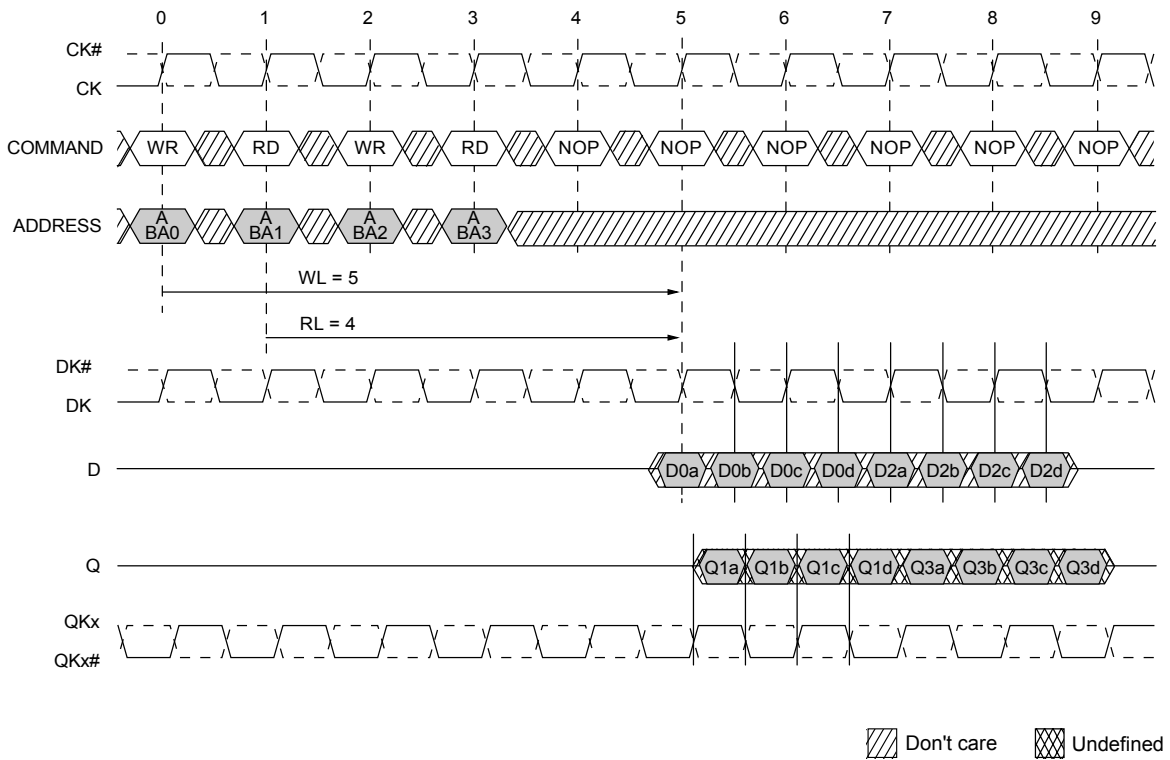


Figure 2-11. WRITE Followed By READ: BL=4, RL=4, WL=5, Configuration 1



**Remark**

- WR : WRITE command
- RD : READ command
- A/BAp : Address A of bank p
- WL : WRITE latency
- RL : READ latency
- Dpq : Data q to bank p
- Qpq : Data q from bank p

**2.11 Read Operation (READ)**

Read accesses are initiated with a READ command, as shown in **Figure 2-12**. Row and bank addresses are provided with the READ command.

During READ bursts, the memory device drives the read data edge-aligned with the QK signal. After a programmable READ latency, data is available at the outputs. The data valid signal indicates that valid data will be present in the next half clock cycle.

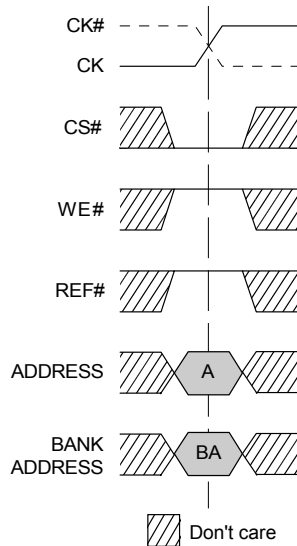
The skew between QK and the crossing point of CK is specified as  $t_{CKQK}$ .  $t_{QKQ0}$  is the skew between QK0 and the last valid data edge considered the data generated at the Q0–Q8.  $t_{QKQ1}$  is the skew between QK1 and the last valid data edge considered the data generated at the Q9–Q17.  $t_{QKQx}$  is derived at each QKx clock edge and is not cumulative over time.

After completion of a burst, assuming no other commands have been initiated, Q will go High-Z. Back-to-back READ commands are possible, producing a continuous flow of output data.

Minimum READ data valid window can be expressed as  $\text{MIN.}(t_{QKH}, t_{QKL}) - 2 \times \text{MAX.}(t_{QKQx})$

Any READ burst may be followed by a subsequent WRITE command. **Figure 2-16. READ followed by WRITE, BL=2, RL=4, WL=5, Configuration 1** and **Figure 2-17. READ followed by WRITE, BL=4, RL=4, WL=5, Configuration 1** illustrate the timing requirements for a READ followed by a WRITE.

**Figure 2-12. READ Command**



**Remark** A : Address  
 BA: Bank address





Figure 2-14. READ Burst Basic Sequence: BL=2, RL=4, Configuration 1

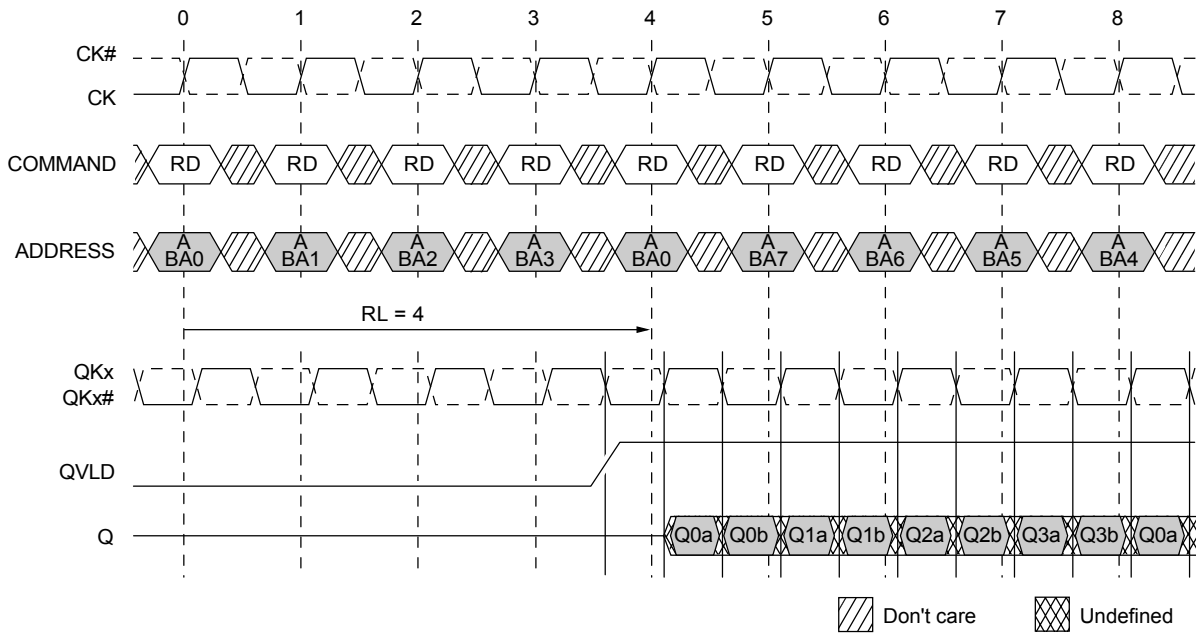
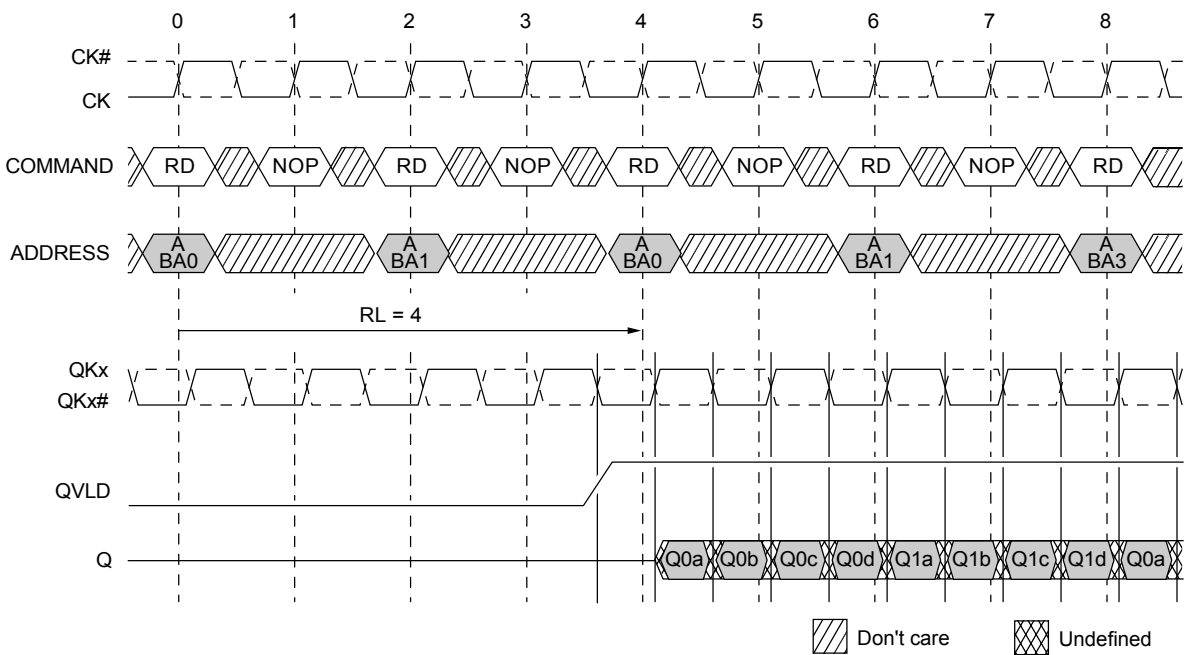


Figure 2-15. READ Burst Basic Sequence: BL=4, RL=4, Configuration 1



**Remark** RD : READ command  
 A/BAp : Address A of bank p  
 RL : READ latency  
 Qpq : Data q from bank p

Figure 2-16. READ followed by WRITE, BL=2, RL=4, WL=5, Configuration 1

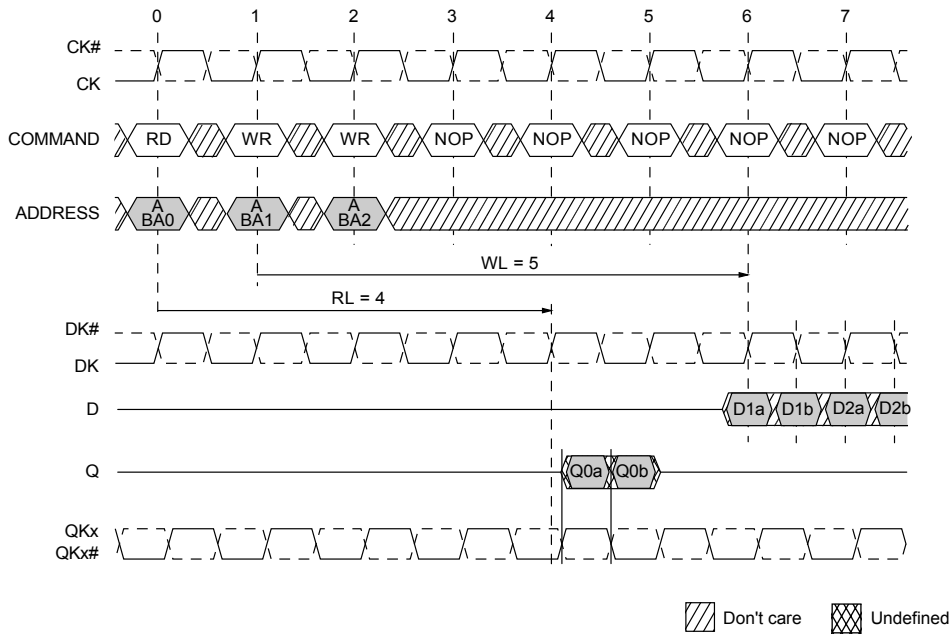
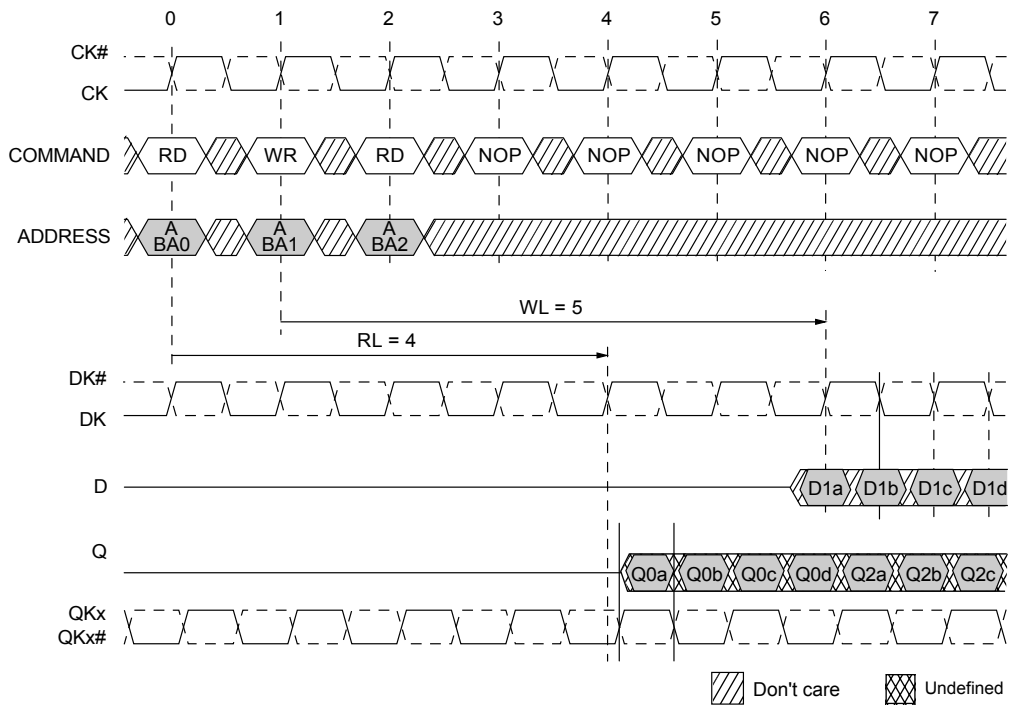


Figure 2-17. READ followed by WRITE, BL=4, RL=4, WL=5, Configuration 1



**Remark**

- WR : WRITE command
- RD : READ command
- A/BAp : Address A of bank p
- WL : WRITE latency
- RL : READ latency
- Dpq : Data q to bank p
- Qpq : Data q from bank p

Figure 2-18. READ/WRITE Interleave: BL=4, t<sub>RC</sub>=6, WL=7, Configuration 2

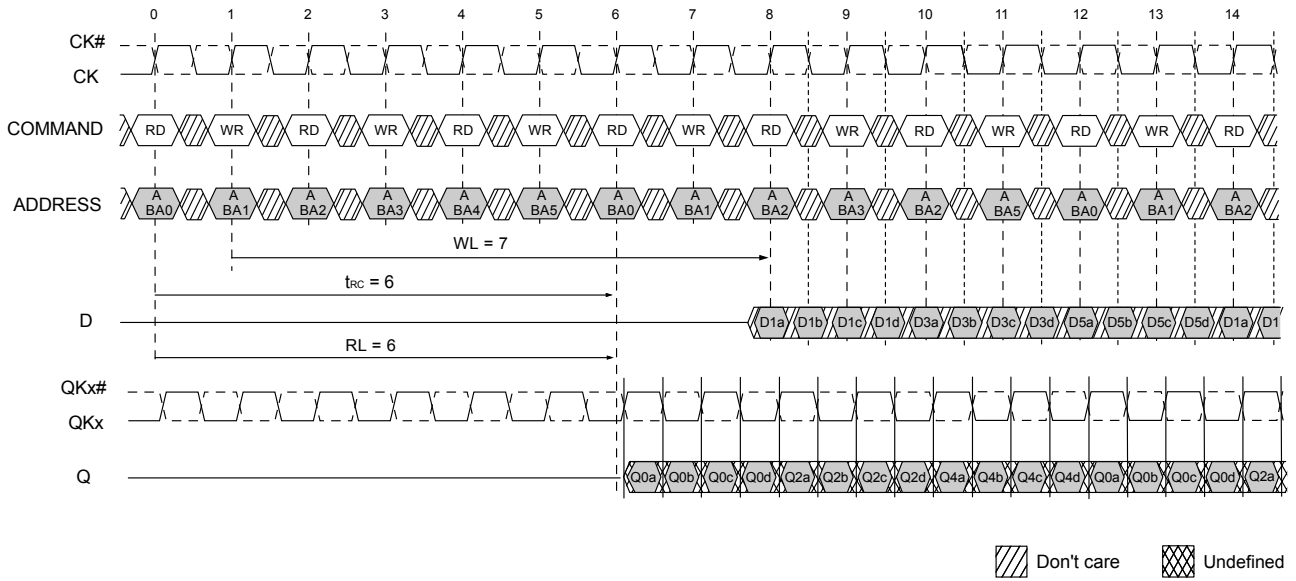
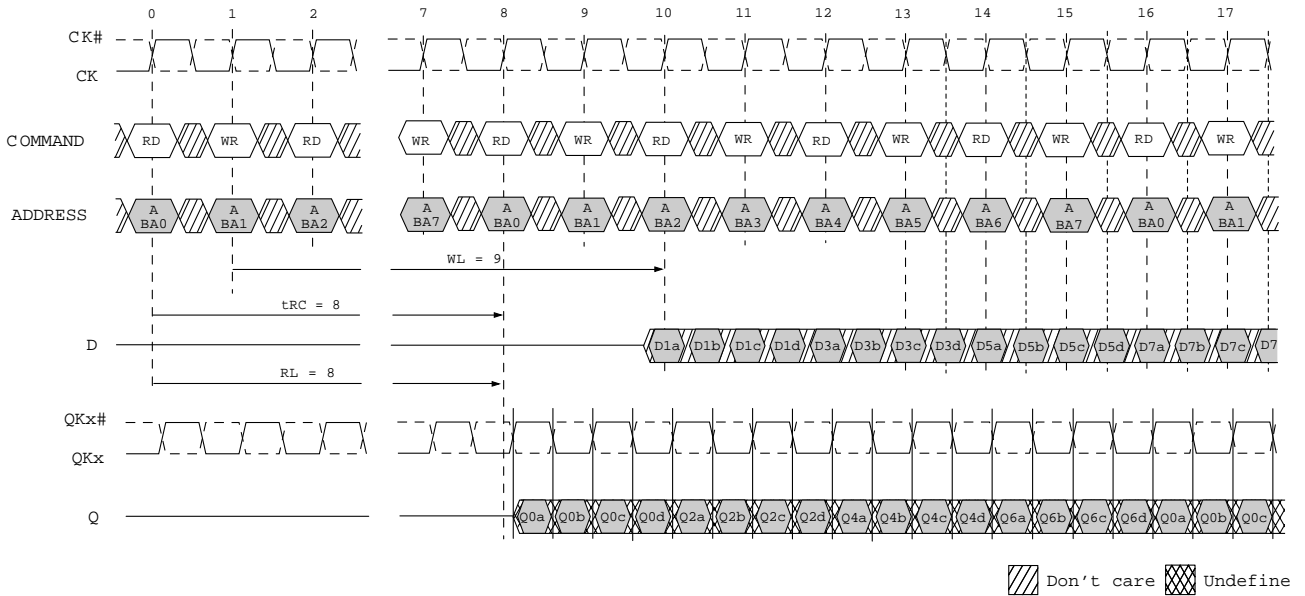


Figure 2-19. READ/WRITE Interleave: BL=4, t<sub>RC</sub>=8, WL=9, Configuration 3



**Remark**

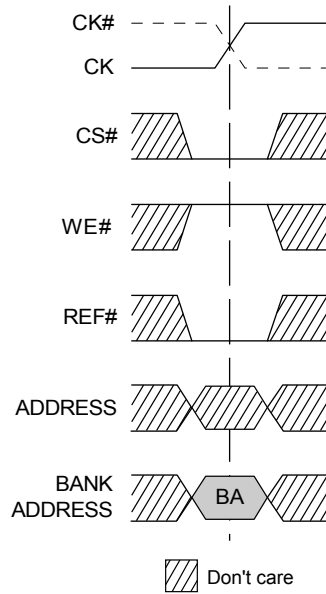
- WR : WRITE command
- RD : READ command
- A/BA<sub>p</sub> : Address A of bank p
- WL : WRITE latency
- RL : READ latency
- D<sub>pq</sub> : Data q to bank p
- Q<sub>pq</sub> : Data q from bank p

**2.12 Refresh Operation: AUTO REFRESH Command (AREF)**

AREF is used to perform a REFRESH cycle on one row in a specific bank. The row addresses are generated by an internal refresh counter; external address balls are “Don’t Care.” The delay between the AREF command and a subsequent command to the same bank must be at least  $t_{RC}$ .

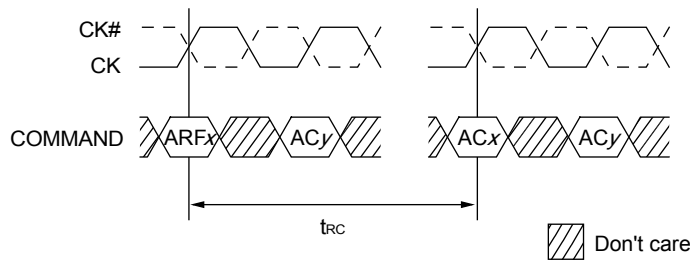
Within a period of 32 ms ( $t_{REF}$ ), the entire memory must be refreshed. **Figure 2-21** illustrates an example of a continuous refresh sequence. Other refresh strategies, such as burst refresh, are also possible.

**Figure 2-20. AUTO REFRESH Command**



**Remark** BA: Bank address

**Figure 2-21. AUTO REFRESH Cycle**



- Remarks**
1. ACx : Any command on bank x  
 ARFx : Auto refresh bank x  
 ACy : Any command on different bank.
  2.  $t_{RC}$  is configuration-dependent. Refer to **Table 2-4. Configuration Table**.

2.13 On-Die Termination

On-die termination (ODT) is enabled by setting A9 to “1” during an MRS command. With ODT on, all the Ds and DM are terminated to V<sub>TT</sub> with a resistance R<sub>TT</sub>. The command, address, and clock signals are not terminated. **Figure 2-22.** below shows the equivalent circuit of a D receiver with ODT. ODTs are dynamically switched off during READ commands and are designed to be off prior to the μPD48288118AF1 driving the bus. Similarly, ODTs are designed to switch on after the μPD48288118AF1 has issued the last piece of data. ODT at the D inputs and DM are always on.

Table 2-5. On-Die Termination DC Parameters

Description	Symbol	MIN.	MAX.	Units	Note
Termination voltage	V <sub>TT</sub>	0.95 x V <sub>REF</sub>	1.05 x V <sub>REF</sub>	V	1, 2
On-Die termination	R <sub>TT</sub>	125	185	Ω	3

- Notes**
1. All voltages referenced to V<sub>SS</sub> (GND).
  2. V<sub>TT</sub> is expected to be set equal to V<sub>REF</sub> and must track variations in the DC level of V<sub>REF</sub>.
  3. The R<sub>TT</sub> value is measured at 95°C T<sub>c</sub>.

Figure 2-22. On- Die Termination-Equivalent Circuit

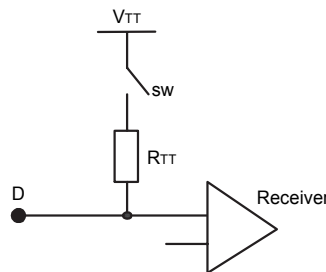
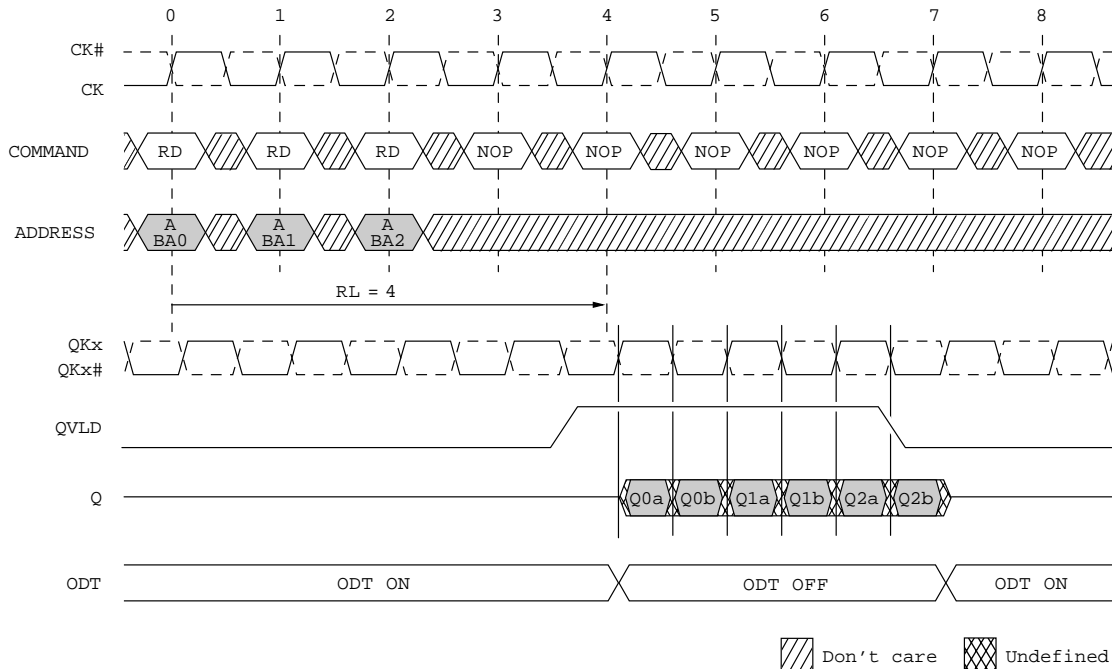


Figure 2-23. READ Burst with ODT: BL=2, Configuration 1



- Remark**
- RD : READ command
  - A/BA<sub>p</sub> : Address A of bank p
  - RL : READ latency
  - Q<sub>pq</sub> : Data q from bank p

Figure 2-24. READ NOP READ with ODT: BL=2, Configuration 1

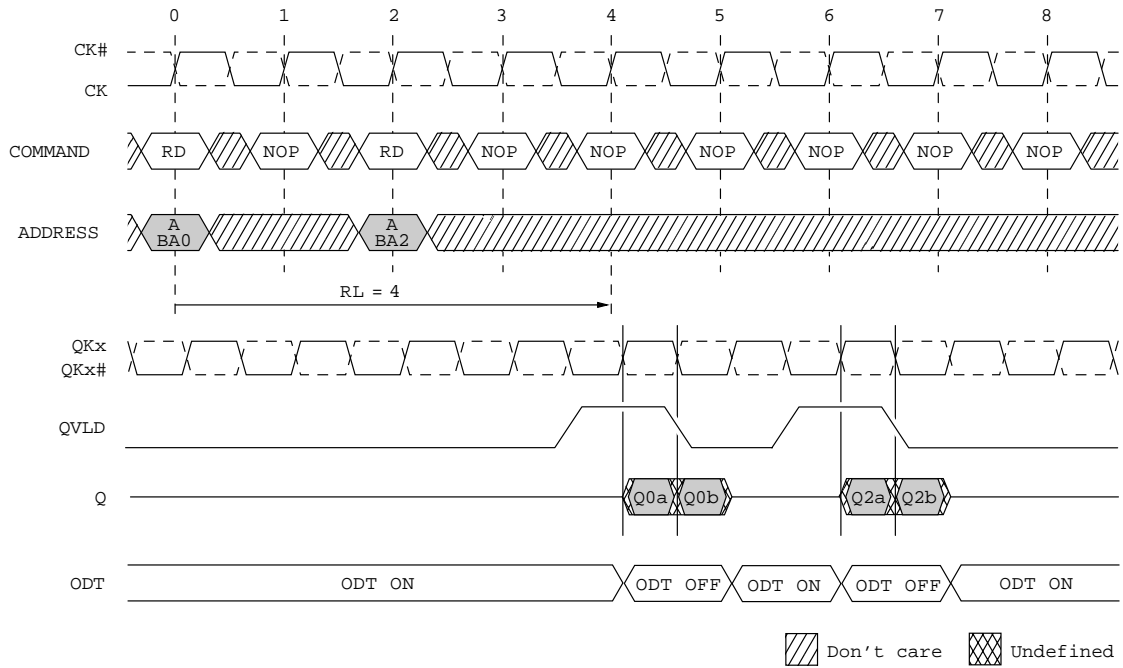
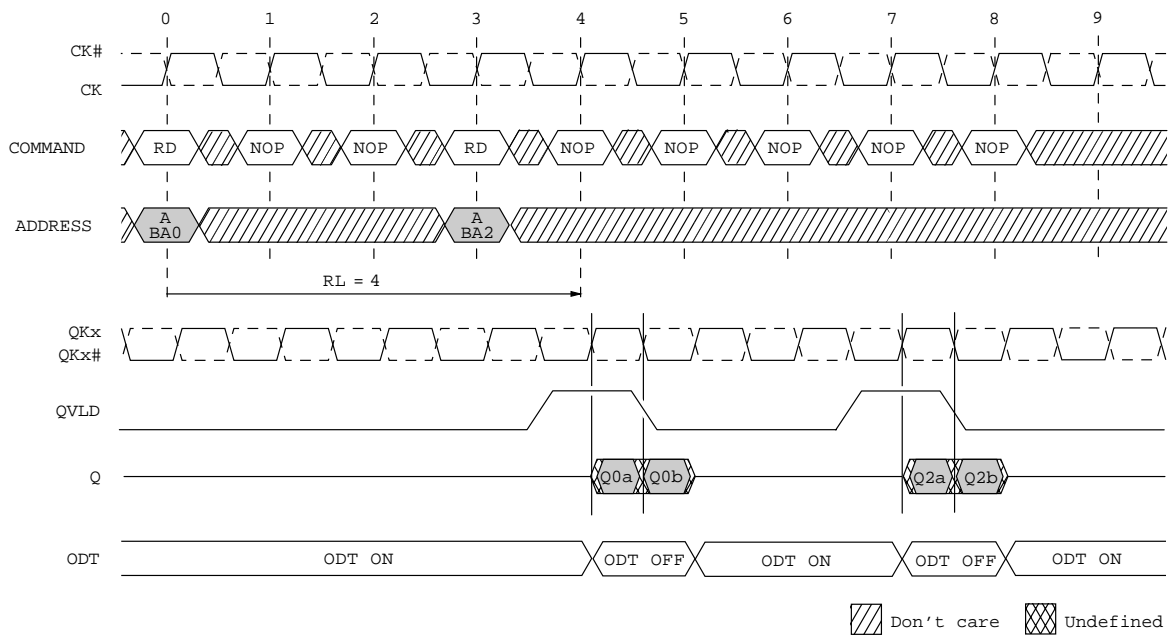


Figure 2-25. READ NOP NOP READ with ODT: BL=2, Configuration 1



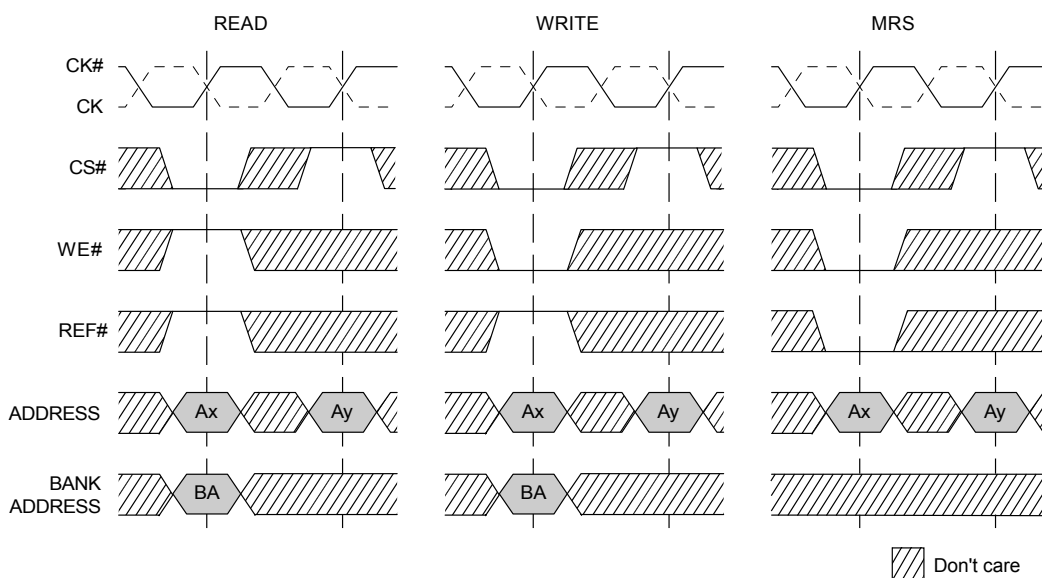
**Remark** RD : READ command  
 A/BAp : Address A of bank p  
 RL : READ latency  
 Qpq : Data q from bank p

2.14 Operation with Multiplexed Address

In multiplexed address mode, the address can be provided to the μPD48288118AF1 in two parts that are latched into the memory with two consecutive rising clock edges. This provides the advantage that a maximum of 11 address balls are required to control the μPD48288118AF1, reducing the number of balls on the controller side. The data bus efficiency in continuous burst mode is not affected for BL=4 and BL=8 since at least two clocks are required to read the data out of the memory. The bank addresses are delivered to the μPD48288118AF1 at the same time as the WRITE command and the first address part, Ax.

This option is available by setting bit A5 to “1” in the mode register. Once this bit is set, the READ, WRITE, and MRS commands follow the format described in Figure 2-26. See Figure 2-28. Power-Up Sequence in Multiplexed Address Mode for the power-up sequence.

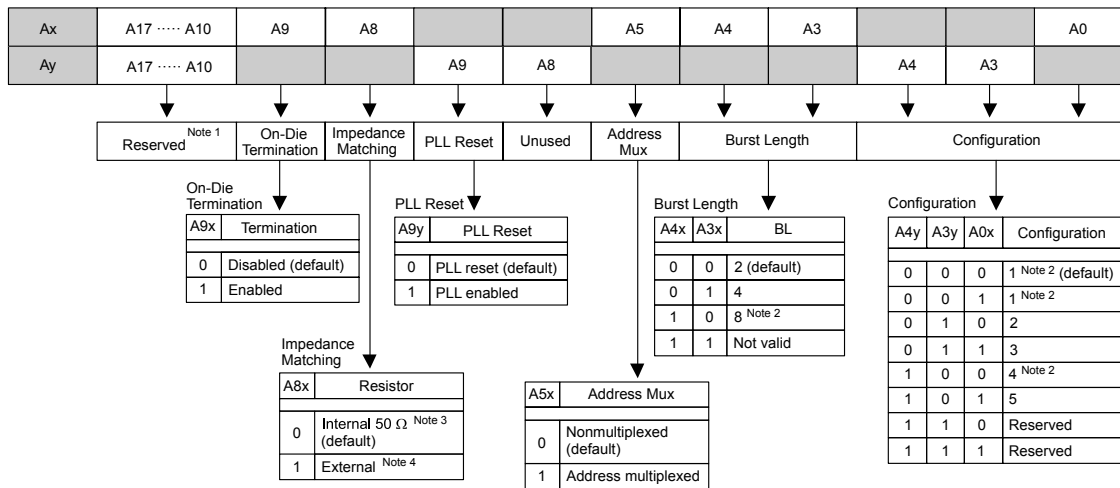
Figure 2-26. Command Description in Multiplexed



- Remarks**
1. Ax, Ay : Address  
BA : Bank Address
  2. The minimum setup and hold times of the two address parts are defined t<sub>AS</sub> and t<sub>AH</sub>.



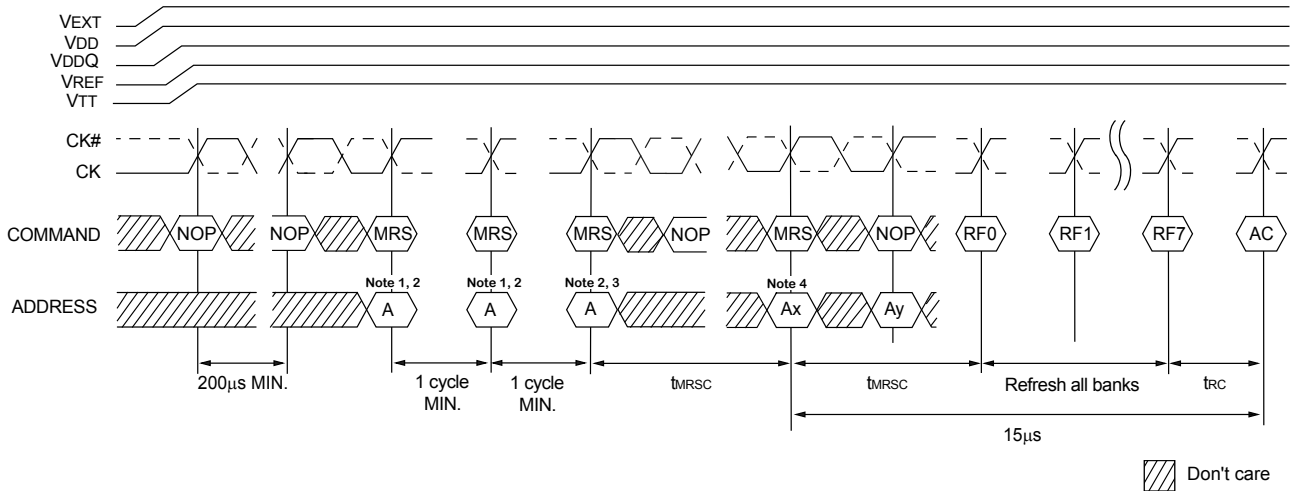
Figure 2-27. Mode Register Set Command in Multiplexed Address Mode



- Notes**
- Bits A10–A17 must be set to all ‘0’. A18 is “Don’t Care”.
  - BL=8 is not available for configuration 1 and 4.
  - ±30% temperature variation.
  - Within 15%.

**Remark** The address A0, A3, A4, A5, A8, and A9 must be set as follows in order to activate the mode register in the multiplexed address mode.

Figure 2-28. Power-Up Sequence in Multiplexed Address Mode



- Notes**
- Recommended all address pins held LOW during dummy MRS command.
  - A10-A17 must be LOW.
  - Address A5 must be set HIGH (muxed address mode setting when μPD48288118AF1 is in normal mode of operation).
  - Address A5 must be set HIGH (muxed address mode setting when μPD48288118AF1 is already in muxed address mode).

**Remark** MRS : MRS command  
 RFp : REFRESH Bank p  
 AC : any command

**2.15 Address Mapping in Multiplexed Mode**

The address mapping is described in **Table 2-6** as a function of data width and burst length.

**Table 2-6. Address Mapping in Multiplexed Address Mode**

Data Width	Burst Length	Ball	Address										
			A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
x18	BL=2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL=4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL=8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15

**Remark** X means “Don’t care”.

**2.16 Read & Write configuration in Multiplexed Address Mode**

In multiplexed address mode, the READ and WRITE latencies are increased by one clock cycle. The μPD48288118AF1 cycle time remains the same, as described in **Table 2-7**.

**Table 2-7. Configuration in Multiplexed Address Mode**

Parameter	Configuration					Unit
	1 <sup>Note1</sup>	2	3	4 <sup>Note1, 2</sup>	5	
t <sub>RC</sub>	4	6	8	3	5	tck
t <sub>RL</sub>	5	7	9	4	6	tck
t <sub>WL</sub>	6	8	10	5	7	tck
Valid frequency range	266-175	400-175	533-175	200-175	333-175	MHz

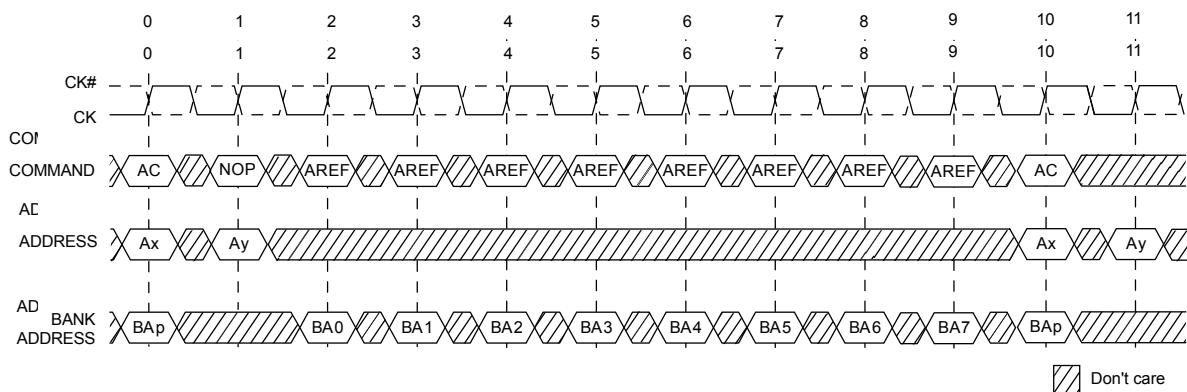
**Notes 1.** BL = 8 is not available.

**2.** The minimum t<sub>RC</sub> is typically 3 cycles, except in the case of a WRITE followed by a READ to the same bank. In this instance the minimum t<sub>RC</sub> is 4 cycles.

**2.17 Refresh Command in Multiplexed Address Mode**

Similar to other commands, the refresh command is executed on the next rising clock edge when in the multiplexed address mode. However, since only bank address is required for AREF, the next command can be applied on the following clock. The operation of the AREF command and any other command is represented in **Figure 2-29**.

**Figure 2-29. Burst REFRESH Operation**



**Remark**

- AREF : AUTO REFRESH
- AC : Any command
- Ax : First part Ax of address
- Ay : Second part Ay of address
- BA<sub>p</sub> : Bank p is chosen so that t<sub>rc</sub> is met.

Figure 2-30. WRITE Burst Basic Sequence: BL=4, with Multiplexed Addresses, Configuration 1

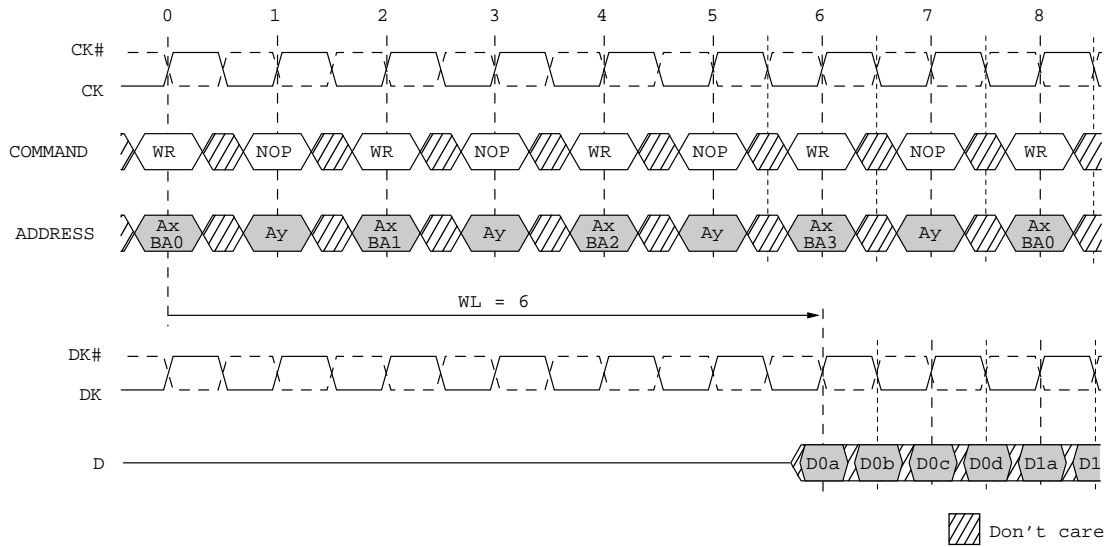
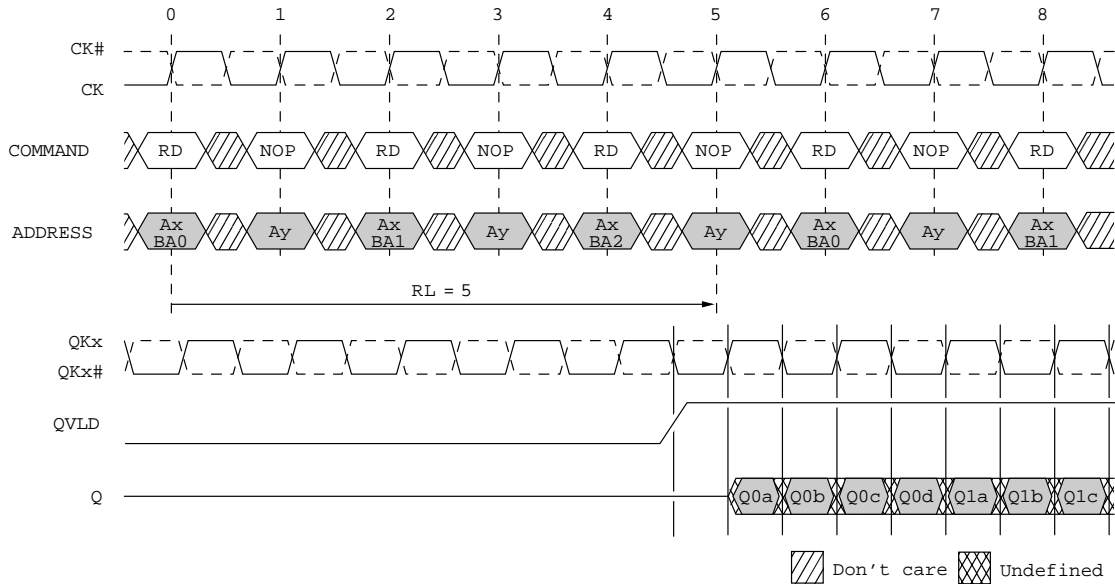


Figure 2-31. READ Burst Basic Sequence: BL=4, with Multiplexed Addresses, Configuration 1, RL=5



- Remark**
- WR : WRITE command
  - RD : READ command
  - Ax/BAp : Address Ax of bank p
  - Ay : Address Ay of bank p
  - Dpq : Data q to bank p
  - Qpq : Data q from bank p
  - WL : WRITE latency
  - RL : READ latency

## 2.18 Input Slew Rate Derating

**Table 2-8** on page 38 and **Table 2-9** on page 39 define the address, command, and data setup and hold derating values. These values are added to the default tAS/tCS/tDS and tAH/tCH/tDH specifications when the slew rate of any of these input signals is less than the 2 V/ns the nominal setup and hold specifications are based upon.

To determine the setup and hold time needed for a given slew rate, add the tAS/tCS default specification to the “tAS/tCS V<sub>REF</sub> to CK/CK# Crossing” and the tAH/tCH default specification to the “tAH/tCH CK/CK# Crossing to V<sub>REF</sub>” derated values on **Table 2-8**. The derated data setup and hold values can be determined in a like manner using the “tDS V<sub>REF</sub> to CK/CK# Crossing” and “tDH to CK/CK# Crossing to V<sub>REF</sub>” values on **Table 2-9**.

The derating values on **Table 2-8** and **Table 2-9** apply to all speed grades.

The setup times on **Table 2-8** and **Table 2-9** represent a rising signal. In this case, the time from which the rising signal crosses V<sub>IH(AC)</sub> MIN to the CK/CK# cross point is static and must be maintained across all slew rates. The derated setup timing represents the point at which the rising signal crosses V<sub>REF(DC)</sub> to the CK/CK# cross point. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between V<sub>IH(AC)</sub> MIN and the CK/CK# cross point. The setup values in **Table 2-8** and **Table 2-9** are also valid for falling signals (with respect to V<sub>IL(AC)</sub> MAX and the CK/CK# cross point).

The hold times in **Table 2-8** and **Table 2-9** represent falling signals. In this case, the time from the CK/CK# cross point to when the signal crosses V<sub>IH(DC)</sub> MIN is static and must be maintained across all slew rates. The derated hold timing represents the delta between the CK/CK# cross point to when the falling signal crosses V<sub>REF(DC)</sub>. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between the CK/CK# cross point and V<sub>IH(DC)</sub>. The hold values in **Table 2-8** and **Table 2-9** are also valid for rising signals (with respect to V<sub>IL(DC)</sub> MAX and the CK and CK# cross point).

**Note** The above descriptions also pertain to data setup and hold derating when CK/CK# are replaced with DK/DK#.

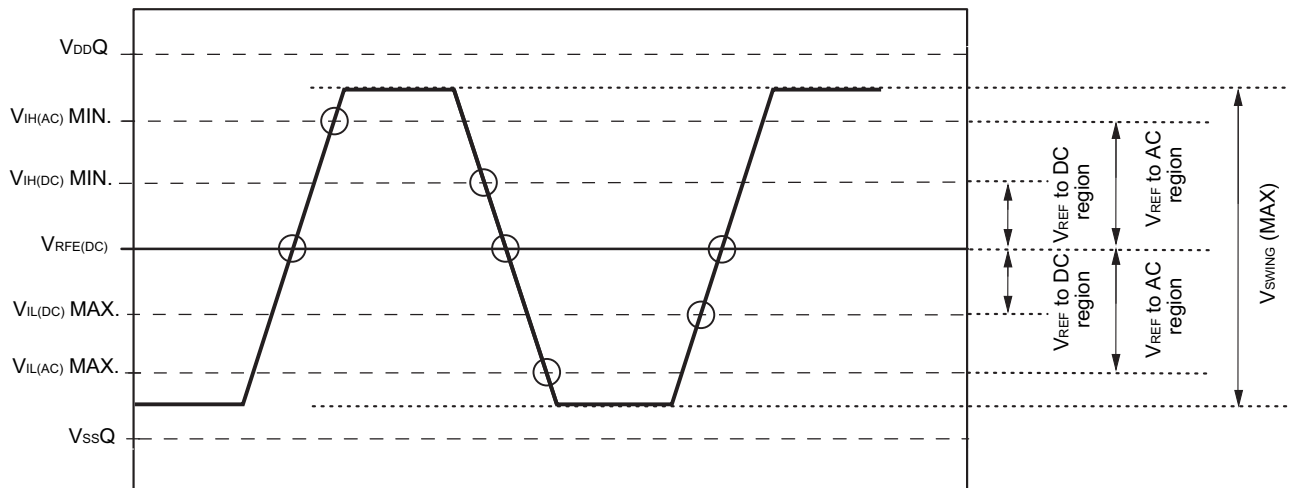
Table 2-8. Address and Command Setup and Hold Derating Values

Command/ Address Slew Rate (V/ns)	tAS/CS VREF to CK/CK# Crossing	tAS/CS VIH(AC) MIN to CK/CK# Crossing	tAH/CH CK/CK# Crossing to VREF	tAH/CH CK/CK# Crossing to VIH(DC) MIN	Unit
CK, CK# Differential Slew Rate: 2.0 V/ns					
2.0	0	-100	0	-50	ps
1.9	5	-100	3	-50	ps
1.8	11	-100	6	-50	ps
1.7	18	-100	9	-50	ps
1.6	25	-100	13	-50	ps
1.5	33	-100	17	-50	ps
1.4	43	-100	22	-50	ps
1.3	54	-100	27	-50	ps
1.2	67	-100	34	-50	ps
1.1	82	-100	41	-50	ps
1.0	100	-100	50	-50	ps
CK, CK# Differential Slew Rate: 1.5 V/ns					
2.0	30	-70	30	-20	ps
1.9	35	-70	33	-20	ps
1.8	41	-70	36	-20	ps
1.7	48	-70	39	-20	ps
1.6	55	-70	43	-20	ps
1.5	63	-70	47	-20	ps
1.4	73	-70	52	-20	ps
1.3	84	-70	57	-20	ps
1.2	97	-70	64	-20	ps
1.1	112	-70	71	-20	ps
1.0	130	-70	80	-20	ps
CK, CK# Differential Slew Rate: 1.0 V/ns					
2.0	60	-40	60	10	ps
1.9	65	-40	63	10	ps
1.8	71	-40	66	10	ps
1.7	78	-40	69	10	ps
1.6	85	-40	73	10	ps
1.5	93	-40	77	10	ps
1.4	103	-40	82	10	ps
1.3	114	-40	87	10	ps
1.2	127	-40	94	10	ps
1.1	142	-40	101	10	ps
1.0	160	-40	110	10	ps

Table 2-9. Data Setup and Hold Derating Values

Data Slew Rate (V/ns)	tDS V <sub>REF</sub> to DK/DK# Crossing	tDS V <sub>IH(AC)</sub> MIN to DK/DK# Crossing	tDH DK/DK# Crossing to V <sub>REF</sub>	tDH DK/DK# Crossing to V <sub>IH(DC)</sub> MIN	Unit
DK, DK# Differential Slew Rate: 2.0 V/ns					
2.0	0	-100	0	-50	ps
1.9	5	-100	3	-50	ps
1.8	11	-100	6	-50	ps
1.7	18	-100	9	-50	ps
1.6	25	-100	13	-50	ps
1.5	33	-100	17	-50	ps
1.4	43	-100	22	-50	ps
1.3	54	-100	27	-50	ps
1.2	67	-100	34	-50	ps
1.1	82	-100	41	-50	ps
1.0	100	-100	50	-50	ps
DK, DK# Differential Slew Rate: 1.5 V/ns					
2.0	30	-70	30	-20	ps
1.9	35	-70	33	-20	ps
1.8	41	-70	36	-20	ps
1.7	48	-70	39	-20	ps
1.6	55	-70	43	-20	ps
1.5	63	-70	47	-20	ps
1.4	73	-70	52	-20	ps
1.3	84	-70	57	-20	ps
1.2	97	-70	64	-20	ps
1.1	112	-70	71	-20	ps
1.0	130	-70	80	-20	ps
DK, DK# Differential Slew Rate: 1.0 V/ns					
2.0	60	-40	60	10	ps
1.9	65	-40	63	10	ps
1.8	71	-40	66	10	ps
1.7	78	-40	69	10	ps
1.6	85	-40	73	10	ps
1.5	93	-40	77	10	ps
1.4	103	-40	82	10	ps
1.3	114	-40	87	10	ps
1.2	127	-40	94	10	ps
1.1	142	-40	101	10	ps
1.0	160	-40	110	10	ps

Figure 2-32. Nominal tAS/tCS/tDS and tAH/tCH/tDH Slew Rate





### 3. JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

**Table 3-1. Test Access Port (TAP) Pins**

Pin name	Pin assignments	Description
TCK	12A	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	11A	Test Mode Select. This is the command input for the TAP controller state
TDI	12V	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in
TDO	11V	Test Data Output. This is the output side of the serial registers placed between TDI and TDO. Output changes in response to the falling edge of TCK.

**Remark** The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held HIGH for five rising edges of TCK. The TAP controller state is also reset on the POWER-UP.

**Table 3-2. JTAG DC Characteristics (0°C ≤ Tc ≤ 95°C, 1.7 V ≤ VDD ≤ 1.9 V, unless otherwise noted)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Notes
JTAG Input leakage current	ILI	0 V ≤ VIN ≤ VDD	-5.0	+5.0	μA	
JTAG I/O leakage current	ILO	0 V ≤ VIN ≤ VDD Q , Outputs disabled	-5.0	+5.0	μA	
JTAG input HIGH voltage	VIH		VREF + 0.15	VDD + 0.3	V	1, 2
JTAG input LOW voltage	VIL		VSSQ - 0.3	VREF - 0.15	V	1, 2
JTAG output HIGH voltage	VOH1	IOHC   = 100 μA	VDDQ - 0.2		V	
	VOH2	IOHT   = 2 mA	VDDQ - 0.4		V	
JTAG output LOW voltage	VOL1	IOLC = 100 μA		0.2	V	1
	VOL2	IOLT = 2 mA		0.4	V	1

**Notes 1.** All voltages referenced to VSS (GND).

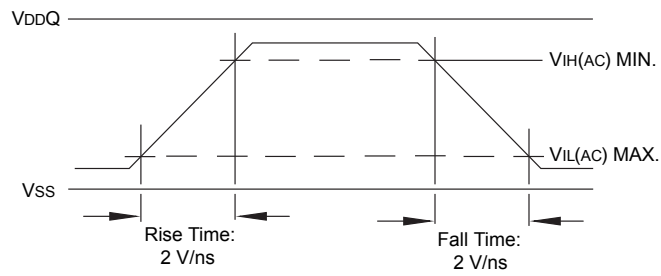
**2.** Overshoot:  $V_{IH(AC)} \leq V_{DD} + 0.7 \text{ V}$  for  $t \leq t_{CK}/2$ .

Undershoot:  $V_{IL(AC)} \geq -0.5 \text{ V}$  for  $t \leq t_{CK}/2$ .

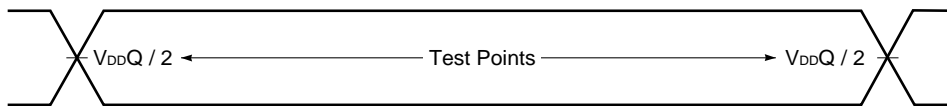
During normal operation,  $V_{DDQ}$  must not exceed  $V_{DD}$ .

JTAG AC Test Conditions

Input waveform



Output waveform



Output load condition

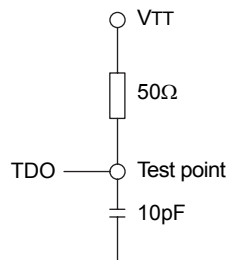
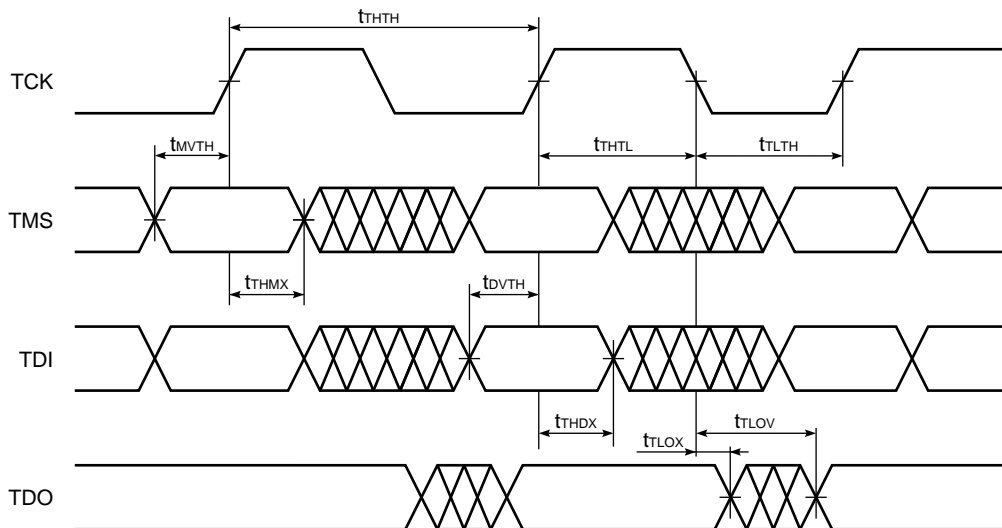


Table 3-3. JTAG AC Characteristics (0°C ≤ Tc ≤ 95°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Clock						
Clock cycle time	t <sub>THTH</sub>		20		ns	
Clock frequency	f <sub>TF</sub>			50	MHz	
Clock HIGH time	t <sub>HTL</sub>		10		ns	
Clock LOW time	t <sub>TLH</sub>		10		ns	
Output time						
TCK LOW to TDO unknown	t <sub>TLOX</sub>		0		ns	
TCK LOW to TDO valid	t <sub>TLOV</sub>			10	ns	
Setup time						
TMS setup time	t <sub>MVTH</sub>		5		ns	
TDI valid to TCK HIGH	t <sub>DVTH</sub>		5		ns	
Capture setup time	t <sub>CSJ</sub>		5		ns	1
Hold time						
TMS hold time	t <sub>THMX</sub>		5		ns	
TCK HIGH to TDI invalid	t <sub>THDX</sub>		5		ns	
Capture hold time	t <sub>CHJ</sub>		5		ns	1

**Note** t<sub>CSJ</sub> and t<sub>CHJ</sub> refer to the setup and hold time requirements of latching data from the boundary scan register.

**JTAG Timing Diagram**



**Table 3-4. Scan Register Definition (1)**

Register name	Description
Instruction register	The 8 bit instruction registers hold the instructions that are executed by the TAP controller. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible. The bypass register is set LOW (VSS) when the bypass instruction is executed.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

**Table 3-5. Scan Register Definition (2)**

Register name	Bit size	Unit
Instruction register	8	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	113	bit

**Table 3-6. ID Register Definition**

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD48288118AF1	16M x 18	0101	0001 1000 1010 0111	00000010000	1

Table 3-7. SCAN Exit Order

Bit no.	Signal name	Bump ID
	x18	
1	DK	K1
2	DK#	K2
3	CS#	L2
4	REF#	L1
5	WE#	M1
6	A17	M3
7	A16	M2
8	A18	N1
9	A15	P1
10	Q14	N3
11	Q14	N3
12	D14	N2
13	D14	N2
14	Q15	P3
15	Q15	P3
16	D15	P2
17	D15	P2
18	QK1	R2
19	QK1#	R3
20	D16	T2
21	D16	T2
22	Q16	T3
23	Q16	T3
24	D17	U2
25	D17	U2
26	Q17	U3
27	Q17	U3
28	ZQ	V2
29	Q13	U10
30	Q13	U10
31	D13	U11
32	D13	U11
33	Q12	T10
34	Q12	T10
35	D12	T11
36	D12	T11
37	Q11	R10
38	Q11	R10

Bit no.	Signal name	Bump ID
	x18	
39	D11	R11
40	D11	R11
41	D10	P11
42	D10	P11
43	Q10	P10
44	Q10	P10
45	D9	N11
46	D9	N11
47	Q9	N10
48	Q9	N10
49	DM	P12
50	A19	N12
51	A11	M11
52	A12	M10
53	A10	M12
54	A13	L12
55	A14	L11
56	BA1	K11
57	CK#	K12
58	CK	J12
59	BA0	J11
60	A4	H11
61	A3	H12
62	A0	G12
63	A2	G10
64	A1	G11
65	(A20)	E12
66	QVLD	F12
67	Q3	F10
68	Q3	F10
69	D3	F11
70	D3	F11
71	Q2	E10
72	Q2	E10
73	D2	E11
74	D2	E11
75	QK0	D11
76	QK0#	D10

Bit no.	Signal name	Bump ID
	x18	
77	D1	C11
78	D1	C11
79	Q1	C10
80	Q1	C10
81	D0	B11
82	D0	B11
83	Q0	B10
84	Q0	B10
85	Q4	B3
86	Q4	B3
87	D4	B2
88	D4	B2
89	Q5	C3
90	Q5	C3
91	D5	C2
92	D5	C2
93	Q6	D3
94	Q6	D3
95	D6	D2
96	D6	D2
97	D7	E2
98	D7	E2
99	Q7	E3
100	Q7	E3
101	D8	F2
102	D8	F2
103	Q8	F3
104	Q8	F3
105	(A21)	E1
106	A5	F1
107	A6	G2
108	A7	G3
109	A8	G1
110	BA2	H1
111	A9	H2
112	NF	J2
113	NF	J1

**Note** Any unused balls that are in the order will read as a logic “0”.

JTAG Instructions

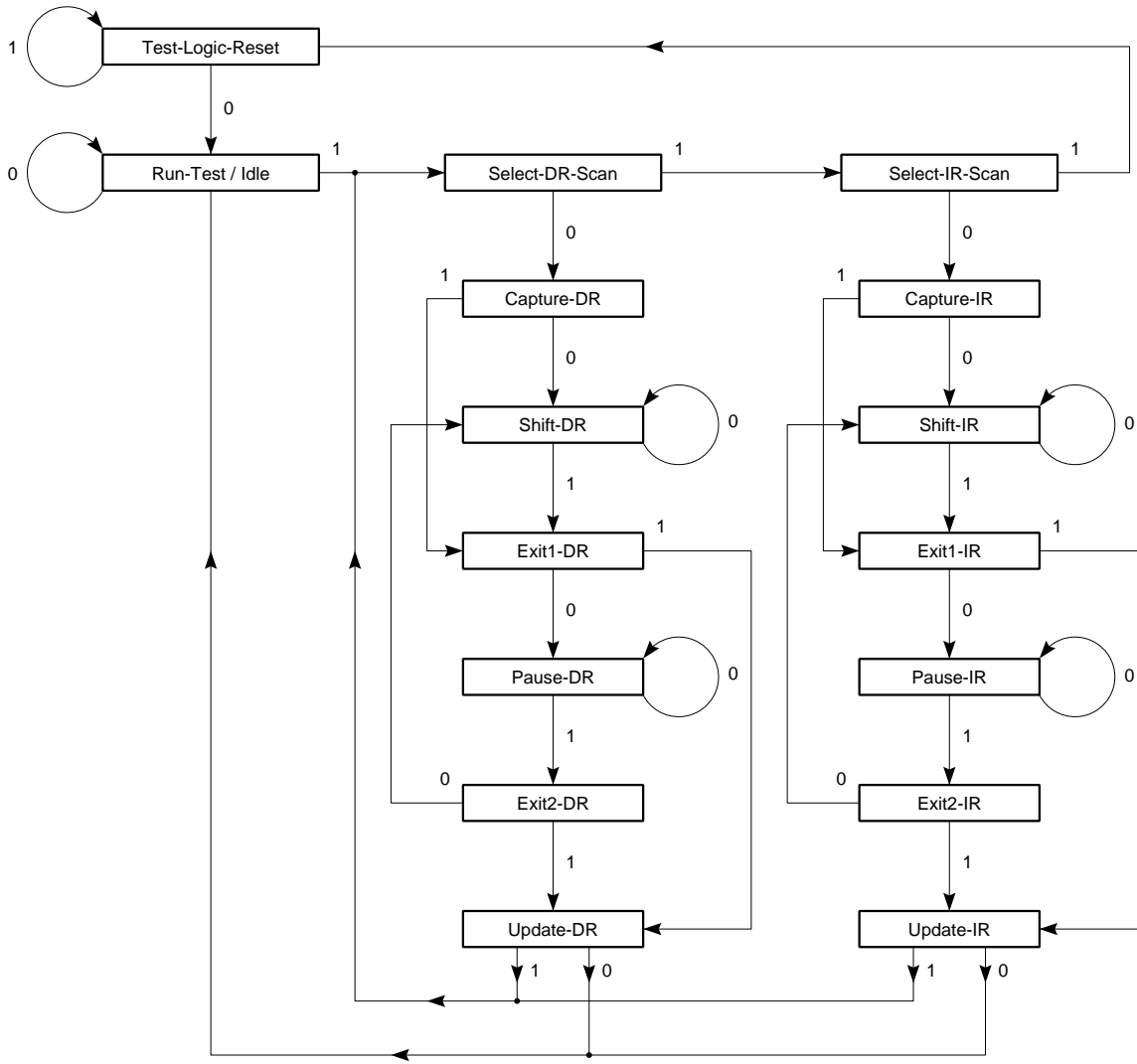
Many different instructions (2<sup>8</sup>) are possible with the 8-bit instruction register. All used combinations are listed in **Table 3-8**, Instruction Codes. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RAM is fully compliant to the 1149.1 convention. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

**Table 3-8**

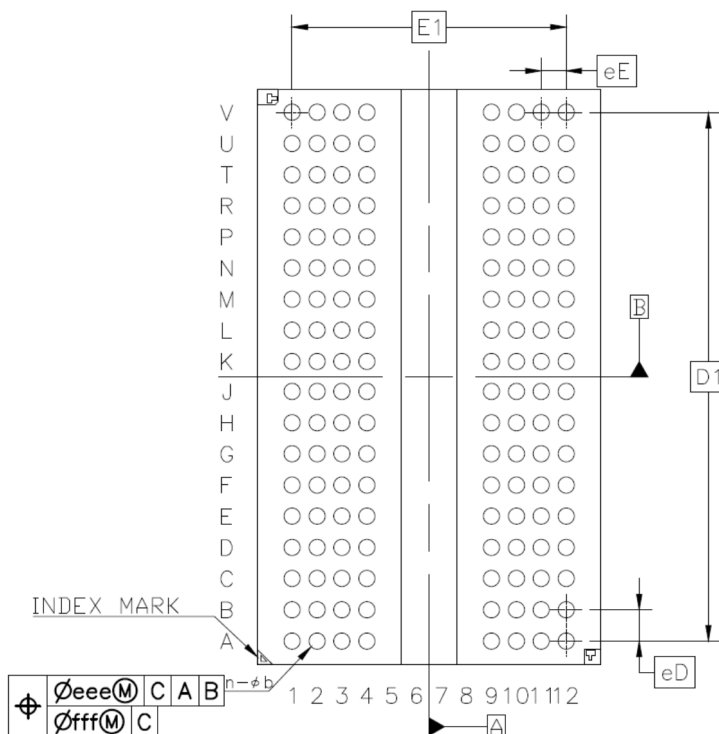
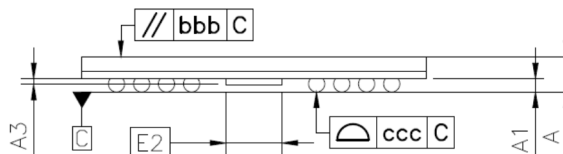
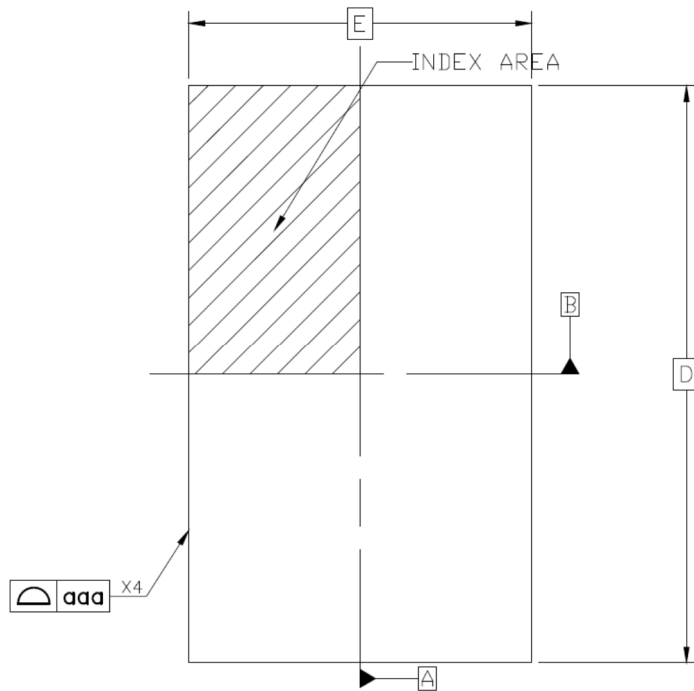
Instructions	Instruction Code [7:0]	Description
EXTEST	0000 0000	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	0010 0001	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
SAMPLE / PRELOAD	0000 0101	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and Q pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t <sub>CS</sub> plus t <sub>CH</sub> ). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins.
CLAMP	0000 0111	When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary scan register. Selects the bypass register to be connected between TDI and TDO. Data driven by output balls are determined from values held in the boundary scan register.
High-Z	0000 0011	The High-z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RAMs outputs into a High-Z state. Selects the bypass register to be connected between TDI and TDO. All outputs are forced into high impedance state.
BYPASS	1111 1111	When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
Reserved for Future Use	–	The remaining instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



4. Package Dimensions

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-TFBGA-11x18.5-0.80	PTBG0144GC-A	-	0.39



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	18.40	18.50	18.60
E	10.90	11.00	11.10
D1	—	17.00	—
E1	—	8.80	—
A	—	—	1.20
A1	0.37	0.42	0.47
A3	—	—	0.18
b	0.47	0.52	0.57
eD	—	1.00	—
eE	—	0.80	—
aaa	—	—	0.10
bbb	—	—	0.20
ccc	—	—	0.10
eee	—	—	0.15
fff	—	—	0.08
n	—	144	—
E2	1.75	1.80	1.85



### Top Marking Information

Due to space limitation of the package, top marking is different from part number. About marking code of I/O, configuration, speed grade and temperature range, refer to the Part Number Definition (see Page 2).



- |     |           |                                 |
|-----|-----------|---------------------------------|
| (1) | D48288    | : 288Mbit LLDRAM                |
|     | XXX       | : I/O, Configuration Code       |
|     | AF1       | : Fixed                         |
| (2) | E         | : Fixed                         |
|     | XX        | : Speed Grade, Temp. Range Code |
|     | -DW1-A    | : Fixed                         |
| (3) | YY        | : Year Code (last 2-digits)     |
|     | WW        | : Week Code                     |
|     | XXXXXX    | : Serial Code                   |
| (4) | Laser dot | : Lead-free identification dot  |
|     | TAIWAN    | : (Assembly) country of origin  |
| (5) | Laser dot | : INDEX Mark                    |

## 5. Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

### Types of Surface Mount Devices

μPD48288118AF1-DW1 : 144-pin FBGA (18.5 x 11)

### Quality Grade

- A quality grade of the products is “Standard”.
- Anti-radioactive design is not implemented in the products.
- Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

<b>Revision History</b>	<b>μPD48288118AF1</b>
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Rev.	Date	Description	
		Page	Summary
Rev. 1.00	'15.07.01	-	New Data Sheet
Rev. 1.01	'16.01.15	P. 2 P. 48 P. 49	Added part number definition Updated package bottom view Added top marking information

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