National Semiconductor

DP8430V/31V/32V-33 microCMOS Programmable 256k/1M/4M Dynamic RAM Controller/Drivers

General Description

The DP8430V/31V/32V dynamic RAM controllers provide a low cost, single chip interface between dynamic RAM and all 8-, 16- and 32-bit systems. The DP8430V/31V/32V generate all the required access control signal timing for DRAMs. An on-chip refresh request clock is used to automatically refresh the DRAM array. Refreshes and accesses are arbitrated on chip. If necessary, a $\overline{WAIT}$ or $\overline{DTACK}$ output inserts wait states into system access cycles, including burst mode accesses. $\overline{RAS}$ low time during refreshes and $\overline{RAS}$ precharge time after refreshes and back to back accesses are guaranteed through the insertion of wait states. Separate on-chip precharge counters for each $\overline{RAS}$ output can be used for memory interleaving to avoid delayed back to back accesses because of precharge. An additional feature of the DP8432V is two access ports to simplify dual accessing. Arbitration among these ports and refresh is done on chip.

Features

- On chip high precision delay line to guarantee critical DRAM access timing parameters
- microCMOS process for low power
- High capacitance drivers for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DRAM address on chip
- On chip support for nibble, page and static column DRAMs
- Byte enable signals on chip allow byte writing in a word size up to 32 bits with no external logic
- Can use a single clock source. Up to 33 MHz operating frequency
- On board Port A/Port B (DP8432V only)/refresh arbitration logic
- Direct interface to all major microprocessors
- 4 $\overline{RAS}$ and 4 $\overline{CAS}$ drivers (the $\overline{RAS}$ and $\overline{CAS}$ configuration is programmable)

Control	# of Pins (PLCC)	# of Address Outputs	Largest DRAM Possible	Direct Drive Memory Capacity	Access Ports Available
DP8430V	68	9	256 kbit	4 Mbytes	Single Access Port
DP8431V	68	10	1 Mbit	16 Mbytes	Single Access Port
DP8432V	84	11	4 Mbit	64 Mbytes	Dual Access Ports (A and B)

Block Diagram

DP8430V/31V/32V DRAM Controller

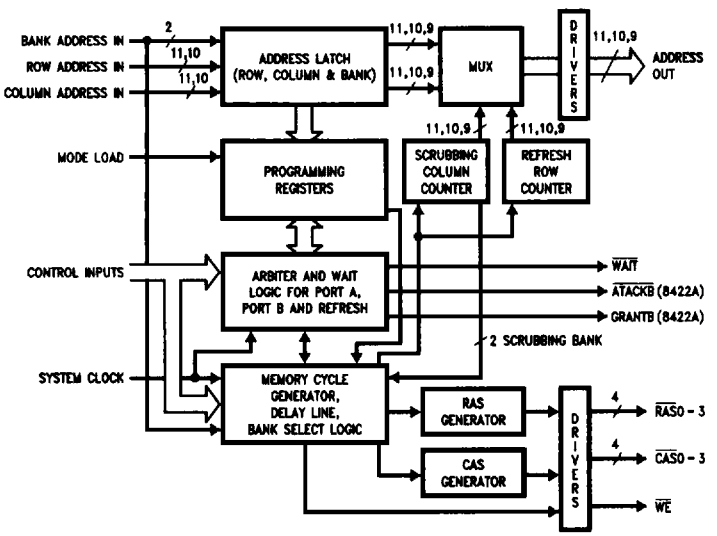

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FIGURE 1

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1.0 Introduction

The DP8430V/31V/32V DRAM controllers are the latest devices based upon the DP8420A/21A/22A predecessors. The DP8430V/31V/32V implement changes which do not allow them to be pin compatible with any of the DP842XA or the DP842XV DRAM controllers. Two changes have been made: The limits for the input frequency to DELCLK have been increased making possible the use of a single clock source. A RESET input is now available making the reset procedure easier. These changes, although minimal, facilitate the use of the controllers and make them even more attractive for high performance applications. The controllers incorporate address latches, refresh counter, row/column/refresh address multiplexer, delay line, refresh/access/precharge arbitration logic and high capacitive drivers. The DP8430V/31V/32V DRAM controllers allow any manufacturer's CPU or bus to directly interface to DRAM arrays up to 64 Mbytes in size.

Reset:

The user must reset the controller before programming it. Reset is achieved by asserting the $\overline{\text{RESET}}$ input for at least 16 positive edges of clock.

Programming:

After reset, the user can program the controller by either one of two methods: Mode Load Only Programming or Chip Select Access Programming. The chip is programmed through the address bus.

Initialization Period:

Once the DP8430V/31V/32V has been programmed for the first time, a 60 ms initialization period is entered. During this time the DRC performs refreshes to the DRAM array so further warm up cycles are unnecessary. The initialization period is entered only after the first programming after a reset.

Accessing Modes:

After resetting and programming the chip, the DP8430V/31V/32V is ready to access the DRAM. There are two modes of accessing with these controllers. Mode 0, which indicates $\overline{\text{RAS}}$ synchronously and Mode 1, which indicates $\overline{\text{RAS}}$ asynchronously.

Refresh Modes:

Two refresh modes can be programmed. The user can choose Automatic Internal Refresh or Externally Controlled Refresh. With any refresh mode the user can perform burst refreshes.

Refresh Types:

There are three types of refreshing available: Conventional, Staggered and Error Scrubbing. Any refresh control mode can be used with any type of refresh.

Wait Support:

The DP8430V/31V/32V have wait support available as $\overline{\text{DTACK}}$ or $\overline{\text{WAIT}}$. Both are programmable. $\overline{\text{DTACK}}$, Data Transfer ACKnowledge, is useful for processors whose wait signal is active high. $\overline{\text{WAIT}}$ is useful for those processors whose wait signal is active low. The user can choose either at programming. These signals are used by the on chip arbiter to insert wait states to guarantee the arbitration between accesses, refreshes and precharge. Both signals are independent of the access mode chosen and both signals can be dynamically delayed further through the $\overline{\text{WAITIN}}$ signal to the DP8430V/31V/32V.

Sequential Accesses (Static Column/Page Mode):

The DP8430V/31V/32V have address latches, used to latch the bank, row and column address inputs. Once the address is latched, a COLumn INCrement (COLINC) feature can be used to increment the column address. The address latches can also be programmed to be fall through. COLINC can be used for Sequential Accesses of Static Column DRAMs. Also, COLINC in conjunction with $\overline{\text{ECAS}}$ inputs can be used for Sequential Accesses to Page Mode DRAMs.

$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Configuration (Byte Writing):

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ drivers can be configured to drive a one, two or four bank memory array up to 32 bits in width. The $\overline{\text{ECAS}}$ signals can then be used to select one of four $\overline{\text{CAS}}$ drivers for Byte Writing with no extra logic.

Memory Interleaving:

When configuring the DP8430V/31V/32V for more than one bank, Memory Interleaving can be used. By tying the low order address bits to the bank select lines B0 and B1, sequential back to back accesses will not be delayed since these controllers have separate precharge counters per bank.

Address Pipelining:

The DP8430V/31V/32V are capable of performing Address Pipelining. In address pipelining, the DRC will guarantee the column address hold time and switch the internal multiplexor to place the row address on the address bus. At this time, another memory access to another bank can be initiated.

Dual Accessing:

Finally, the DP8432V has all the features previously mentioned and unlike the DP8430V/31V, the DP8432V has a second port to allow a second CPU to access the same memory array. The DP8432V has four signals to support Dual Accessing, these signals are $\overline{\text{AREQB}}$, $\overline{\text{ATACKB}}$, $\overline{\text{LOCK}}$ and GRANTB. All arbitration for the two ports and refresh is done on chip by the controller through the insertion of wait states. Since the DP8432V has only one input address bus, the address lines must be multiplexed externally. The signal GRANTB can be used for this purpose.

Terminology:

The following explains the terminology used in this data sheet. The terms negated and asserted are used. Asserted refers to a "true" signal. Thus, "$\overline{\text{ECAS0}}$ asserted" means the $\overline{\text{ECAS0}}$ input is at a logic 0. The term "COLINC asserted" means the COLINC input is at a logic 1. The term negated refers to a "false" signal. Thus, "$\overline{\text{ECAS0}}$ negated" means the $\overline{\text{ECAS0}}$ input is at a logic 1. The term "COLINC negated" means the input COLINC is at a logic 0. The table shown below clarifies this terminology.

Signal	Action	Logic Level
Active High	Asserted	High
Active High	Negated	Low
Active Low	Asserted	Low
Active Low	Negated	High

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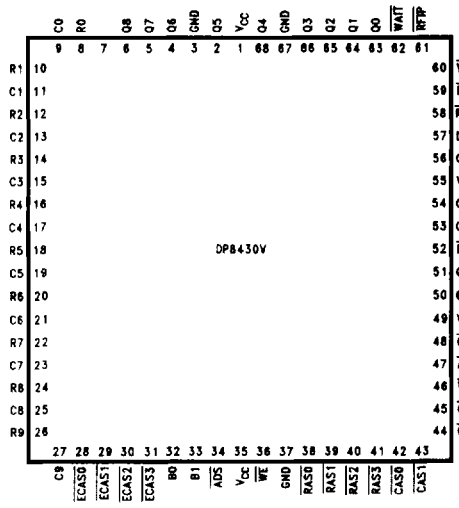
Connection Diagrams



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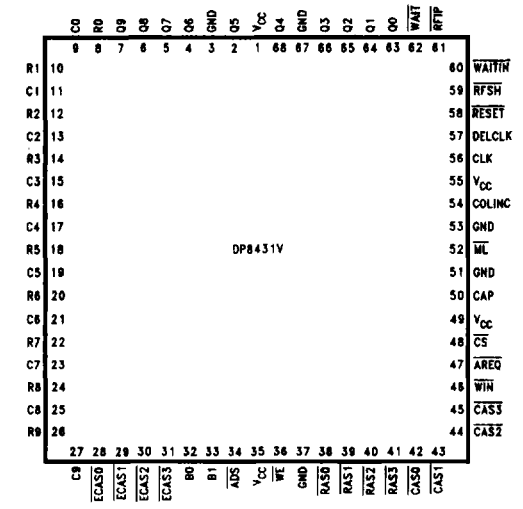
Top View

FIGURE 2

Order Number DP8430V-33
See NS Package Number V68A



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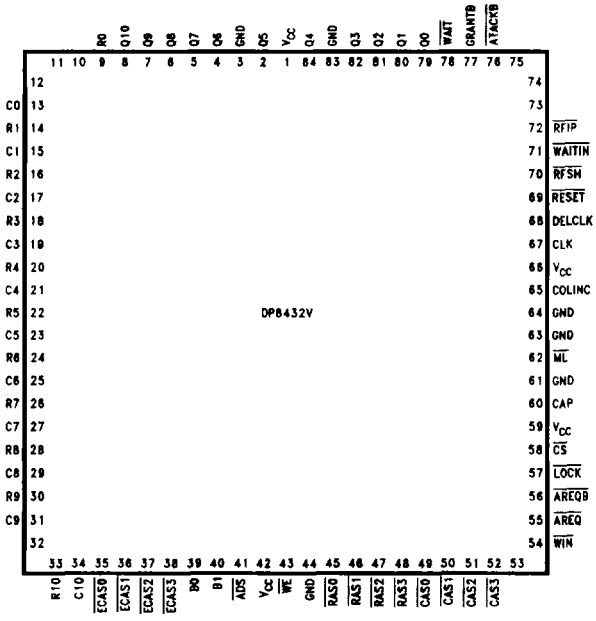
Top View

FIGURE 3

Order Number DP8431V-33
See NS Package Number V68A



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Top View

FIGURE 4

Order Number DP8432V-33
See NS Package Number V84A

2.0 Signal Descriptions

Pin Name	Device (If not Applicable to All)	Input/ Output	Description
2.1 ADDRESS, R/W AND PROGRAMMING SIGNALS			
R0–10 R0–9	DP8432V DP8430V/31V	I I	**ROW ADDRESS:** These inputs are used to specify the row address during an access to the DRAM. They are also used to program the chip when $\overline{ML}$ is asserted (except R10).
C0–10 C0–9	DP8432V DP8430V/31V	I I	**COLUMN ADDRESS:** These inputs are used to specify the column address during an access to the DRAM. They are also used to program the chip when $\overline{ML}$ is asserted (except C10).
B0, B1		I	**BANK SELECT:** Depending on programming, these inputs are used to select a group of $\overline{RAS}$ and $\overline{CAS}$ outputs to assert during an access. They are also used to program the chip when $\overline{ML}$ is asserted.
$\overline{ECAS}$0–3		I	**ENABLE $\overline{CAS}$:** These inputs are used to enable a single or group of $\overline{CAS}$ outputs when asserted. In combination with the B0, B1 and the programming bits, these inputs select which $\overline{CAS}$ output or $\overline{CAS}$ outputs will assert during an access. The $\overline{ECAS}$ signals can also be used to toggle a group of $\overline{CAS}$ outputs for page/nibble mode accesses. They also can be used for byte write operations. If $\overline{ECAS}$0 is negated during programming, continuing to assert the $\overline{ECAS}$0 while negating $\overline{AREQ}$ or $\overline{AREQB}$ during an access, will cause the $\overline{CAS}$ outputs to be extended while the $\overline{RAS}$ outputs are negated (the $\overline{ECAS}$n inputs have no effect during scrubbing refreshes).
$\overline{RESET}$		I	**RESET:** At power up, this input is used to reset the DRAM controller. The user must keep $\overline{RESET}$ low for at least 16 positive edges of clock. After programming this input must remain negated (high) to avoid an unwanted reset.
$\overline{WIN}$		I	**WRITE ENABLE IN:** This input is used to signify a write operation to the DRAM. If $\overline{ECAS}$0 is asserted during programming, the $\overline{WE}$ output will follow this input. This input asserted will also cause $\overline{CAS}$ to delay to the next positive clock edge if address bit C9 is asserted during programming.
COLINC (EXTNDRF)		I I	**COLUMN INCREMENT:** When the address latches are used, and $\overline{RFIP}$ is negated, this input functions as COLINC. Asserting this signal causes the column address to be incremented by one. When $\overline{RFIP}$ is asserted, this signal is used to extend the refresh cycle by any number of periods of CLK until it is negated.
$\overline{ML}$		I	**MODE LOAD:** This input signal, when low, enables the internal programming register that stores the programming information.
2.2 DRAM CONTROL SIGNALS			
Q0–10 Q0–9 Q0–8	DP8432V DP8431V DP8430V	O O O	**DRAM ADDRESS:** These outputs are the multiplexed output of the R0–9, 10 and C0–9, 10 and form the DRAM address bus. These outputs contain the refresh address whenever $\overline{RFIP}$ is asserted. They contain high capacitive drivers with 20Ω series damping resistors.
$\overline{RAS}$0–3		O	**ROW ADDRESS STROBES:** These outputs are asserted to latch the row address contained on the outputs Q0–8, 9, 10 into the DRAM. When $\overline{RFIP}$ is asserted, the $\overline{RAS}$ outputs are used to latch the refresh row address contained on the Q0–8, 9, 10 outputs in the DRAM. These outputs contain high capacitive drivers with 20Ω series damping resistors.
$\overline{CAS}$0–3		O	**COLUMN ADDRESS STROBES:** These outputs are asserted to latch the column address contained on the outputs Q0–8, 9, 10 into the DRAM. These outputs have high capacitive drivers with 20Ω series damping resistors.
$\overline{WE}$ ($\overline{RFRQ}$)		O O	**WRITE ENABLE** or **REFRESH REQUEST:** This output asserted specifies a write operation to the DRAM. When negated, this output specifies a read operation to the DRAM. When the DP8430V/31V/32V is programmed in address pipelining mode or when $\overline{ECAS}$0 is negated during programming, this output will function as $\overline{RFRQ}$. $\overline{RFRQ}$ asserted, specifies that 13 μs or 15 μs have passed. $\overline{RFRQ}$ can be used to externally request a refresh through the input $\overline{RFSH}$. This output has a high capacitive driver and a 20Ω series damping resistor.

2.0 Signal Descriptions (Continued)

Pin Name	Device (If not Applicable to All)	Input/ Output	Description
2.3 REFRESH SIGNALS			
$\overline{RFIP}$		O	**REFRESH IN PROGRESS:** This output is asserted prior to a refresh cycle and is negated when all the $\overline{RAS}$ outputs are negated for that refresh.
$\overline{RFSH}$		I	**REFRESH:** This input asserted will request a refresh. If this input is continually asserted, the DP8430V/31V/32V will perform refresh cycles in a burst refresh fashion until the input is negated.
2.4 PORT A ACCESS SIGNALS			
$\overline{ADS}$ (ALE)		I I	**ADDRESS STROBE** or **ADDRESS LATCH ENABLE:** Depending on programming, this input can function as $\overline{ADS}$ or ALE. In mode 0, the input functions as ALE and when asserted along with $\overline{CS}$ causes an internal latch to be set. Once this latch is set an access will start from the positive clock edge of CLK as soon as possible. In Mode 1, the input functions as $\overline{ADS}$ and when asserted along with $\overline{CS}$, causes the access $\overline{RAS}$ to assert if no other event is taking place. If an event is taking place, $\overline{RAS}$ will be asserted from the positive edge of CLK as soon as possible. In both cases, the low going edge of this signal latches the bank, row and column address if programmed to do so.
$\overline{CS}$		I	**CHIP SELECT:** This input signal must be asserted to enable a Port A access.
$\overline{AREQ}$		I	**ACCESS REQUEST:** This input signal in Mode 0 must be asserted some time after the first positive clock edge after ALE has been asserted. When this signal is negated, $\overline{RAS}$ is negated for the access. In Mode 1, this signal must be asserted before $\overline{ADS}$ can be negated. When this signal is negated, $\overline{RAS}$ is negated for the access.
$\overline{WAIT}$ ($\overline{DTACK}$)		O O	**WAIT** or **DTACK:** This output can be programmed to insert wait states into a CPU access cycle. With R7 negated during programming, the output will function as a $\overline{WAIT}$ type output. In this case, the output will be active low to signal a wait condition. With R7 asserted during programming, the output will function as $\overline{DTACK}$. In this case, the output will be negated to signify a wait condition and will be asserted to signify the access has taken place. Each of these signals can be delayed by a number of positive clock edges or negative clock levels of CLK to increase the microprocessor's access cycle through the insertion of wait states.
$\overline{WAITIN}$		I	**WAIT INCREASE:** This input can be used to dynamically increase the number of positive clock edges of CLK until $\overline{DTACK}$ will be asserted or $\overline{WAIT}$ will be negated during a DRAM access.
2.5 PORT B ACCESS SIGNALS			
$\overline{AREQB}$	DP8432V only	I	**PORT B ACCESS REQUEST:** This input asserted will latch the row, column and bank address if programmed, and requests an access to take place for Port B. If the access can take place, $\overline{RAS}$ will assert immediately. If the access has to be delayed, $\overline{RAS}$ will assert as soon as possible from a positive edge of CLK.
$\overline{ATACKB}$	DP8432V only	O	**ADVANCED TRANSFER ACKNOWLEDGE PORT B:** This output is asserted when the access $\overline{RAS}$ is asserted for a Port B access. This signal can be used to generate the appropriate $\overline{DTACK}$ or $\overline{WAIT}$ type signal for Port B's CPU or bus.

2.0 Signal Descriptions (Continued)

Pin Name	Device (If not Applicable to All)	Input/ Output	Description
2.6 COMMON DUAL PORT SIGNALS			
GRANTB	DP8432V only	O	**GRANT B:** This output indicates which port is currently granted access to the DRAM array. When GRANTB is asserted, Port B has access to the array. When GRANTB is negated, Port A has access to the DRAM array. This signal is used to multiplex the signals R0–8, 9, 10; C0–8, 9, 10; B0–1; $\overline{WIN}$; $\overline{LOCK}$ and $\overline{ECAS}$0–3 to the DP8432V when using dual accessing.
$\overline{LOCK}$	DP8432V only	I	**LOCK:** This input can be used by the currently granted port to "lock out" the other port from the DRAM array by inserting wait states into the locked out port's access cycle until $\overline{LOCK}$ is negated.
2.7 POWER SIGNALS AND CAPACITOR INPUT			
V_{CC}		I	**POWER:** Supply Voltage.
GND		I	**GROUND:** Supply Voltage Reference.
CAP		I	**CAPACITOR:** This input is used by the internal PLL for stabilization. The value of the ceramic capacitor should be 0.1 μF and should be connected between this input and ground.

2.8 CLOCK INPUTS

There are two clock inputs to the DP8430V/31V/32V, CLK and DELCLK. These two clocks may both be tied to the same clock input, or they may be two separate clocks, running at different frequencies, asynchronous to each other.

CLK		I	**SYSTEM CLOCK:** This input may be in the range of 0 Hz up to 25 MHz. This input is generally a constant frequency but it may be controlled externally to change frequencies or perhaps be stopped for some arbitrary period of time. This input provides the clock to the internal state machine that arbitrates between accesses and refreshes. This clock's positive edges and negative levels are used to extend the $\overline{WAIT}$ ($\overline{DTACK}$) signals. Ths clock is also used as the reference for the $\overline{RAS}$ precharge time and $\overline{RAS}$ low time during refresh. All Port A and Port B accesses are assumed to be synchronous to the system clock CLK.
DELCLK		I	**DELAY LINE CLOCK:** The input frequency to DELCLK should be in the range of 12 MHz to 40 MHz. This frequency will be internally divided by choosing a divisor when programming the part. The result of the division should be a frequency of 2 MHz. This is because the Phase Lock Loop that generates the delay line assumes an input clock frequency of 2 MHz. If after dividing DELCLK by one of the internal divisors (6, 8, 10, 12, 14, 16, 18 or 20) the resulting frequency is not 2 MHz, the delay line will suffer. For example, if the DELCLK frequency is 18 MHz and a divide by 8 is chosen, programming bits C0–2, the resulting frequency will be 2.25 which is 12.5% off of 2 MHz. Therefore, the DP8430V/31V/32V will produce delays that are shorter (faster delays) than what is intended. On the other hand, if divide by 10 was chosen, the resulting frequency will be 1.8 MHz, this frequency will produce delays that are longer (slower delays) than intended. This clock is also divided to create the internal refresh clock.

3.0 Programming and Resetting

The DP8430V/31V/32V must be reset before it can be programmed. After reset, the DRAM controller is programmed through the address bus by either one of two methods; Mode Load Only Programming or Chip Select Access Programming. After the first programming after a reset, the chip enters a 60 ms initialization period. During this period the controller performs refreshes every 13 μs or 15 μs, this makes further DRAM warm up cycles unnecessary. After this stage the DRAM controller can be programmed as many times as the user wishes and the 60 ms initialization period will not be entered into unless the chip is reset and programmed again. During the 60 ms initialization period, $\overline{RFIP}$ is asserted and $\overline{RAS}$ toggles every 13 μs or 15 μs depending on the programming bit for refresh (C3). $\overline{CAS}$ will be negated and the Q outputs will count from 0 to 2047 refreshing the entire DRAM array. The initialization time period is given by the following formula. T = 4096 * (Clock Divisor Select) * (Refresh Clock Fine Tune)/(DELCLK Frq.)

3.1 RESET

The DP8430V/31V/32V have a $\overline{RESET}$ input pin which facilitates the reset procedure required for proper operation. Reset is accomplished by asserting the $\overline{RESET}$ input for at least 16 positive edges of clock as shown in *Figure 5*.

The DRC may be programmed anytime on the fly, but the user must make sure that no access or refresh is in progress. $\overline{RESET}$ is asynchronous.

3.2 PROGRAMMING METHODS

3.2.1 Mode Load Only Programming

To use this method the user asserts $\overline{ML}$ enabling the internal programming register. After $\overline{ML}$ is asserted, a valid programming selection is placed on the address bus, B0, B1 and $\overline{ECAS0}$ inputs, then $\overline{ML}$ is negated. When $\overline{ML}$ is negated the programming bits are latched into the internal programming register and the DP8430V/31V/32V is programmed, see *Figure 6*. When programming the chip, the controller must not be refreshing, $\overline{RFIP}$ must be high (1) to have a successful programming.

3.2.2 Chip Selected Access Programming

The chip can also be programmed by performing a chip selected access. To program the chip using this method, $\overline{ML}$ is asserted, then $\overline{CS}$ is asserted and a valid programming selection is placed on the address bus. When $\overline{AREQ}$ is asserted, the programming bits affecting the wait logic become effective immediately, then $\overline{DTACK}$ is asserted allowing the access to terminate. After the access, $\overline{ML}$ is negated and the rest of the programming bits take effect.

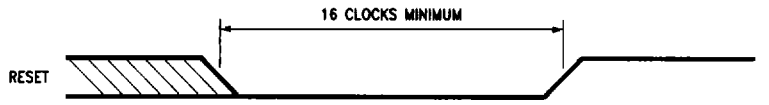

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FIGURE 5. Reset

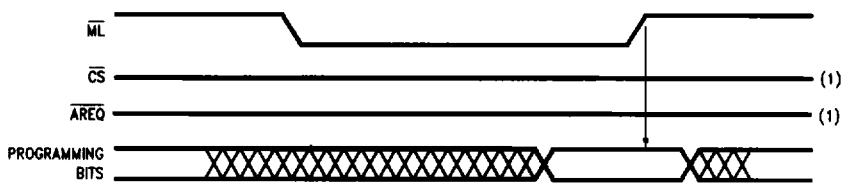

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FIGURE 6. $\overline{ML}$ Only Programming

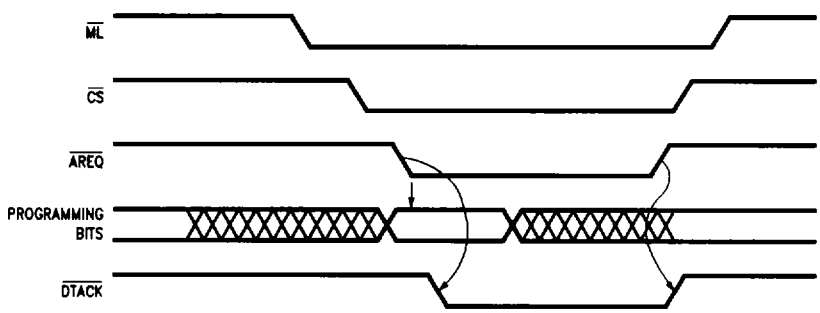

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FIGURE 7. $\overline{CS}$ Access Programming

3.0 Programming and Resetting (Continued)

3.3 PROGRAMMING BIT DEFINITIONS

Symbol	Description
ECAS0	**Extend $\overline{CAS}$/Refresh Request Select**
0	The $\overline{CAS}$n outputs will be negated with the $\overline{RAS}$n outputs when $\overline{AREQ}$ (or $\overline{AREQB}$, DP8432V only) is negated. The $\overline{WE}$ output pin will function as write enable. Automatic Internal Refresh selected.
1	The $\overline{CAS}$n outputs will be negated, during an acccess (Port A (or Port B, DP8432V only)) when their corresponding $\overline{ECAS}$n inputs are negated. This feature allows the $\overline{CAS}$ outputs to be extended beyond the $\overline{RAS}$ outputs negating. Scrubbing refreshes are NOT affected. During scrubbing refreshes the $\overline{CAS}$ outputs will negate along with the $\overline{RAS}$ outputs regardless of the state of the $\overline{ECAS}$ inputs. Externally Controlled Refresh selected, $\overline{WE}$ will function as ReFresh ReQuest ($\overline{RFRQ}$).
B1	**Access Mode Select**
0	**ACCESS MODE 0:** ALE pulsing high sets an internal latch. On the next positive edge of CLK, the access ($\overline{RAS}$) will start. $\overline{AREQ}$ will terminate the access.
1	**ACCESS MODE 1:** $\overline{ADS}$ asserted starts the access ($\overline{RAS}$) immediately. $\overline{AREQ}$ will terminate the access.
B0	**Address Latch Mode**
0	$\overline{ADS}$ or ALE asserted for Port A or $\overline{AREQB}$ asserted for Port B with the appropriate GRANT latch the input row, column and bank address.
1	The row, column and bank latches are fall through.
C9	**Delay $\overline{CAS}$ during WRITE Accesses**
0	$\overline{CAS}$ is treated the same for both READ and WRITE accesses.
1	During WRITE accesses, $\overline{CAS}$ will be asserted by the event that occurs last: $\overline{CAS}$ asserted by the internal delay line or $\overline{CAS}$ asserted on the positive edge of CLK after $\overline{RAS}$ is asserted.
C8	**Row Address Hold Time**
0	Row Address Hold Time = 25 ns minimum
1	Row Address Hold Time = 15 ns minimum
C7	**Column Address Setup Time**
0	Column Address Setup Time = 10 ns miniumum
1	Column Address Setup Time = 0 ns minimum
C6, C5, C4	**$\overline{RAS}$ and $\overline{CAS}$ Configuration Modes/Error Scrubbing during Refresh**
0, 0, 0	$\overline{RAS}$0–3 and $\overline{CAS}$0–3 are all selected during an access. $\overline{ECAS}$n must be asserted for $\overline{CAS}$n to be asserted. B0 and B1 are not used during an access. Error scrubbing during refresh.
0, 0, 1	$\overline{RAS}$ and $\overline{CAS}$ pairs are selected during an access by B1. $\overline{ECAS}$n must be asserted for $\overline{CAS}$n to be asserted. B1 = 0 during an access selects $\overline{RAS}$0–1 and $\overline{CAS}$0–1. B1 = 1 during an access selects $\overline{RAS}$2–3 and $\overline{CAS}$2–3. B0 is not used during an Access. Error scrubbing during refresh.
0, 1, 0	RAS and CAS singles are selected during an access by B0–1. $\overline{ECAS}$n must be asserted for $\overline{CAS}$n to be asserted. B1 = 0, B0 = 0 during an access selects $\overline{RAS}$0 and $\overline{CAS}$0. B1 = 0, B0 = 1 during an access selects $\overline{RAS}$1 and $\overline{CAS}$1. B1 = 1, B0 = 0 during an access selects $\overline{RAS}$2 and $\overline{CAS}$2. B1 = 1, B0 = 1 during an access selects $\overline{RAS}$3 and $\overline{CAS}$3. Error scrubbing during refresh.
0, 1, 1	$\overline{RAS}$0–3 and $\overline{CAS}$0–3 are all selected during an access. $\overline{ECAS}$n must be asserted for $\overline{CAS}$n to be asserted. B1, B0 are not used during an access. No error scrubbing. ($\overline{RAS}$ only refreshing)
1, 0, 0	$\overline{RAS}$ pairs are selected by B1. $\overline{CAS}$0–3 are all selected. $\overline{ECAS}$n must be asserted for $\overline{CAS}$n to be asserted. B1 = 0 during an access selects $\overline{RAS}$0–1 and $\overline{CAS}$0–3. B1 = 1 during an access selects $\overline{RAS}$2–3 and $\overline{CAS}$0–3. B0 is not used during an access. No error scrubbing.

3.0 Programming and Resetting (Continued)

3.3 PROGRAMMING BIT DEFINITIONS (Continued)

Symbol	Description
C6, C5, C4	**$\overline{RAS}$ and $\overline{CAS}$ Configuration Modes** (Continued)
1, 0, 1	$\overline{RAS}$ and $\overline{CAS}$ pairs are selected by B1. $\overline{ECAS}$n must be asserted for $\overline{CAS}$n to be asserted. B1 = 0 during an access selects $\overline{RAS}$0–1 and $\overline{CAS}$0–1. B1 = 1 during an access selects $\overline{RAS}$2–3 and $\overline{CAS}$2–3. B0 is not used during an access. No error scrubbing.
1, 1, 0	$\overline{RAS}$ singles are selected by B0–1. $\overline{CAS}$0–3 are all selected. $\overline{ECAS}$n must be asserted for $\overline{CAS}$n to be asserted. B1 = 0, B0 = 0 during an access selects $\overline{RAS}$0 and $\overline{CAS}$0–3. B1 = 0, B0 = 1 during an access selects $\overline{RAS}$1 and $\overline{CAS}$0–3. B1 = 1, B0 = 0 during an access selects $\overline{RAS}$2 and $\overline{CAS}$0–3. B1 = 1, B0 = 1 during an access selects $\overline{RAS}$3 and $\overline{CAS}$0–3. No error scrubbing.
1, 1, 1	$\overline{RAS}$ and $\overline{CAS}$ singles are selected by B0, 1. $\overline{ECAS}$n must be asserted for $\overline{CAS}$n to be asserted. B1 = 0, B0 = 0 during an access selects $\overline{RAS}$0 and $\overline{CAS}$0. B1 = 0, B0 = 1 during an access selects $\overline{RAS}$1 and $\overline{CAS}$1. B1 = 1, B0 = 0 during an access selects $\overline{RAS}$2 and $\overline{CAS}$2. B1 = 1, B0 = 1 during an access selects $\overline{RAS}$3 and $\overline{CAS}$3. No error scrubbing.
C3	**Refresh Clock Fine Tune Divisor**
0	Divide delay line/refresh clock further by 30 (If DELCLK/Refresh Clock Clock Divisor = 2 MHz = 15 μs refresh period).
1	Divide delay line/refresh clock further by 26 (If DELCLK/Refresh Clock Clock Divisor = 2 MHz = 13 μs refresh period).
C2, C1, C0	**Delay Line/Refresh Clock Divisor Select**
0, 0, 0	Divide DELCLK by 20 to get as close to 2 MHz as possible.
0, 0, 1	Divide DELCLK by 18 to get as close to 2 MHz as possible.
0, 1, 0	Divide DELCLK by 16 to get as close to 2 MHz as possible.
0, 1, 1	Divide DELCLK by 14 to get as close to 2 MHz as possible.
1, 0, 0	Divide DELCLK by 12 to get as close to 2 MHz as possible.
1, 0, 1	Divide DELCLK by 10 to get as close to 2 MHz as possible.
1, 1, 0	Divide DELCLK by 8 to get as close to 2 MHz as possible.
1, 1, 1	Divide DELCLK by 6 to get as close to 2 MHz as possible.
R9	**Refresh Mode Select**
0	$\overline{RAS}$0–3 will all assert and negate at the same time during a refresh.
1	Staggered Refresh. $\overline{RAS}$ outputs during refresh are separated by one positive clock edge. Depending on the configuration mode chosen, either one or two $\overline{RAS}$s will be asserted.
R8	**Address Pipelining Select**
0	Address pipelining is selected. The DRAM controller will switch the DRAM column address back to the row address after guaranteeing the column address hold time.
1	Non-address pipelining is selected. The DRAM controller will hold the column address on the DRAM address bus until the access $\overline{RAS}$s are negated.
R7	**$\overline{WAIT}$ or $\overline{DTACK}$ Select**
0	$\overline{WAIT}$ type output is selected.
1	$\overline{DTACK}$ (Data Transfer ACKnowledge) type output is selected.
R6	**Add Wait States to the Current Access If $\overline{WAITIN}$ is Low**
0	$\overline{WAIT}$ or $\overline{DTACK}$ will be delayed by one additional positive edge of CLK.
1	$\overline{WAIT}$ or $\overline{DTACK}$ will be delayed by two additional positive edges of CLK.

3.0 Programming and Resetting (Continued)

3.3 PROGRAMMING BIT DEFINITIONS (Continued)

Symbol	Description
R5, R4	**$\overline{\text{WAIT}}/\overline{\text{DTACK}}$ during Burst (See Section 5.1.2 or 5.2.2)**
0, 0	NO WAIT STATES; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will remain negated during burst portion of access. If R7 = 1 programming, $\overline{\text{DTACK}}$ will remain asserted during burst portion of access.
0, 1	1T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will assert when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. $\overline{\text{WAIT}}$ will negate from the positive edge of CLK after the $\overline{\text{ECAS}}$s have been asserted. If R7 = 1 during programming, $\overline{\text{DTACK}}$ will negate when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. $\overline{\text{DTACK}}$ will assert from the positive edge of CLK after the $\overline{\text{ECAS}}$s have been asserted.
1, 0	½T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will assert when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. $\overline{\text{WAIT}}$ will negate on the negative level of CLK after the $\overline{\text{ECAS}}$s have been asserted. If R7 = 1 during programming, $\overline{\text{DTACK}}$ will negate when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. $\overline{\text{DTACK}}$ will assert from the negative level of CLK after the $\overline{\text{ECAS}}$s have been asserted.
1, 1	0T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will assert when the $\overline{\text{ECAS}}$ inputs are negated. $\overline{\text{WAIT}}$ will negate when the $\overline{\text{ECAS}}$ inputs are asserted. If R7 = 1 during programming, $\overline{\text{DTACK}}$ will negate when the $\overline{\text{ECAS}}$ inputs are negated. $\overline{\text{DTACK}}$ will assert when the $\overline{\text{ECAS}}$ inputs are asserted.
R3, R2	**$\overline{\text{WAIT}}/\overline{\text{DTACK}}$ Delay Times (See Section 5.1.1 or 5.2.1)**
0, 0	NO WAIT STATES; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will remain high during non-delayed accesses. $\overline{\text{WAIT}}$ will negate when $\overline{\text{RAS}}$ is negated during delayed accesses. NO WAIT STATES; If R7 = 1 during programming, $\overline{\text{DTACK}}$ will be asserted when $\overline{\text{RAS}}$ is asserted.
0, 1	½T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will negate on the negative level of CLK, after the access $\overline{\text{RAS}}$. 1T; If R7 = 1 during programming, $\overline{\text{DTACK}}$ will be asserted on the positive edge of CLK after the access $\overline{\text{RAS}}$.
1, 0	NO WAIT STATES, ½T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will remain high during non-delayed accesses. $\overline{\text{WAIT}}$ will negate on the negative level of CLK, after the access $\overline{\text{RAS}}$, during delayed accesses. ½T; If R7 = 1 during programming, $\overline{\text{DTACK}}$ will be asserted on the negative level of CLK after the access $\overline{\text{RAS}}$.
1, 1	1T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will negate on the positive edge of CLK after the access $\overline{\text{RAS}}$. 1½T; If R7 = 1 during programming, $\overline{\text{DTACK}}$ will be asserted on the negative level of CLK after the positive edge of CLK after the access $\overline{\text{RAS}}$.
R1, R0	**$\overline{\text{RAS}}$ Low and $\overline{\text{RAS}}$ Precharge Time**
0, 0	$\overline{\text{RAS}}$ asserted during refresh = 2 positive edges of CLK. $\overline{\text{RAS}}$ precharge time = 1 positive edge of CLK. $\overline{\text{RAS}}$ will start from the first positive edge of CLK after GRANTB transitions (DP8432V).
0, 1	$\overline{\text{RAS}}$ asserted during refresh = 3 positive edges of CLK. $\overline{\text{RAS}}$ precharge time = 2 positive edges of CLK. $\overline{\text{RAS}}$ will start from the second positive edge of CLK after GRANTB transitions (DP8432V).
1, 0	$\overline{\text{RAS}}$ asserted during refresh = 2 positive edges of CLK. $\overline{\text{RAS}}$ precharge time = 2 positive edges of CLK. $\overline{\text{RAS}}$ will start from the first positive edge of CLK after GRANTB transitions (DP8432V).
1, 1	$\overline{\text{RAS}}$ asserted during refresh = 4 positive edges of CLK. $\overline{\text{RAS}}$ precharge time = 3 positive edges of CLK. $\overline{\text{RAS}}$ will start from the second positive edge of CLK after GRANTB transitions (DP8432V).

4.0 Port A Access Modes

The DP8430V/31V/32V have two general purpose access modes. Mode 0 $\overline{RAS}$ synchronous and Mode 1 $\overline{RAS}$ asynchronous. One of these modes is selected at programming through the B1 input. A Port A access to DRAM is initiated by two input signals: $\overline{ADS}$ (ALE) and $\overline{CS}$. The access is always terminated by one signal: $\overline{AREQ}$. These input signals should be synchronous to the input clock.

4.1 ACCESS MODE 0

Mode 0, synchronous access, is selected by negating the input B1 during programming (B1 = 0). To initiate a Mode 0 access, ALE is pulse high and $\overline{CS}$ is asserted. If precharge time was met, a refresh of DRAM or a Port B access was not in progress, the $\overline{RAS}$ ($\overline{RAS}$s) would be asserted on the first rising edge of clock. If a refresh or a Port B access is in progress or precharge time is required, the controller will wait until these events have taken place and assert $\overline{RAS}$ ($\overline{RAS}$s) on the next positive edge of clock.

Sometime after the first positive edge of clock after ALE and $\overline{CS}$ have been asserted, the input $\overline{AREQ}$ must be asserted. In single port applications, once $\overline{AREQ}$ is asserted, $\overline{CS}$ can be negated. On the other hand, ALE can stay asserted several periods of clock; however, ALE must be negated before or during the period of CLK in which $\overline{AREQ}$ is negated.

The controller samples $\overline{AREQ}$ on the every rising edge of clock after $\overline{DTACK}$ is asserted. The access will end when $\overline{AREQ}$ is sampled negated.

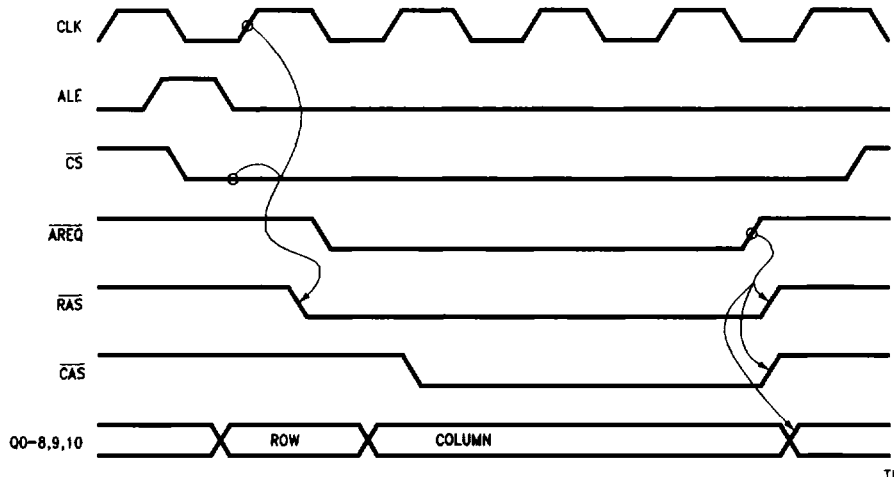

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FIGURE 8a. Access Mode 0

4.0 Port A Access Modes (Continued)

4.2 ACCESS MODE 1

Mode 1, asynchronous access, is selected by asserting the input B1 during programming (B1 = 1). This mode allows accesses to start immediately from the access request input, $\overline{ADS}$. To initiate a Mode 1 access, $\overline{CS}$ is asserted followed by $\overline{ADS}$ asserted. If precharge time was met, a refresh of the DRAM or a Port B access was not in progress, the $\overline{RAS}$ ($\overline{RAS}$s) would be asserted from $\overline{ADS}$ being asserted. If a refresh or Port B access is in progress or precharge time is required, the controller will wait until these events have taken place and assert $\overline{RAS}$ ($\overline{RAS}$s) from the next rising edge of clock.

When $\overline{ADS}$ is asserted or sometime after, $\overline{AREQ}$ must be asserted. At this time, $\overline{ADS}$ can be negated and $\overline{AREQ}$ will continue the access. Also, $\overline{ADS}$ can continue to be asserted after $\overline{AREQ}$ has been asserted and negated; however, a new access will not start until $\overline{ADS}$ is negated and asserted again. When address pipelining is not implemented, $\overline{ADS}$ and $\overline{AREQ}$ can be tied together.

The access will end when $\overline{AREQ}$ is negated.

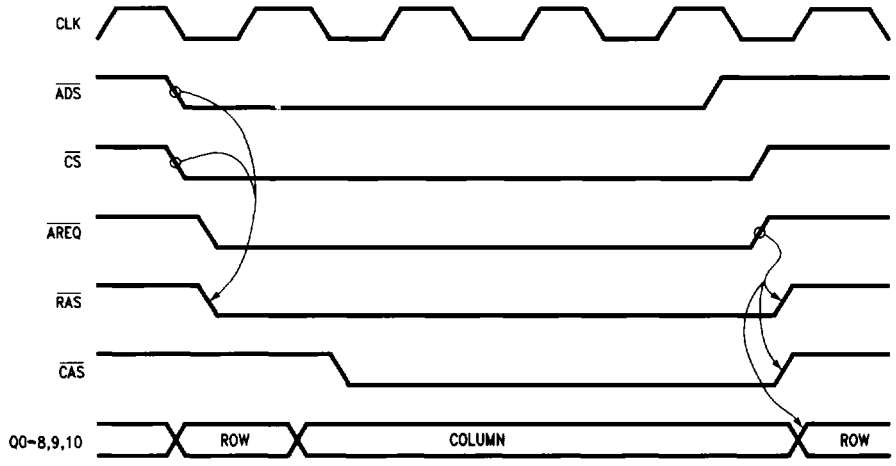

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FIGURE 8b. Access Mode 1

4.0 Port A Access Modes (Continued)

4.3 EXTENDING CAS WITH EITHER ACCESS MODE

In both access modes, once $\overline{AREQ}$ is negated, $\overline{RAS}$ and $\overline{DTACK}$ if programmed will be negated. If $\overline{ECAS}0$ was asserted (0) during programming, $\overline{CAS}$ ($\overline{CAS}s$) will be negated with $\overline{AREQ}$. If $\overline{ECAS}0$ was negated (1) during programming, $\overline{CAS}$ ($\overline{CAS}s$) will continue to be asserted after $\overline{RAS}$ has been negated, given that the appropriate $\overline{ECAS}$ inputs are asserted. This allows a DRAM to have data present on the data out bus while gaining $\overline{RAS}$ precharge time.

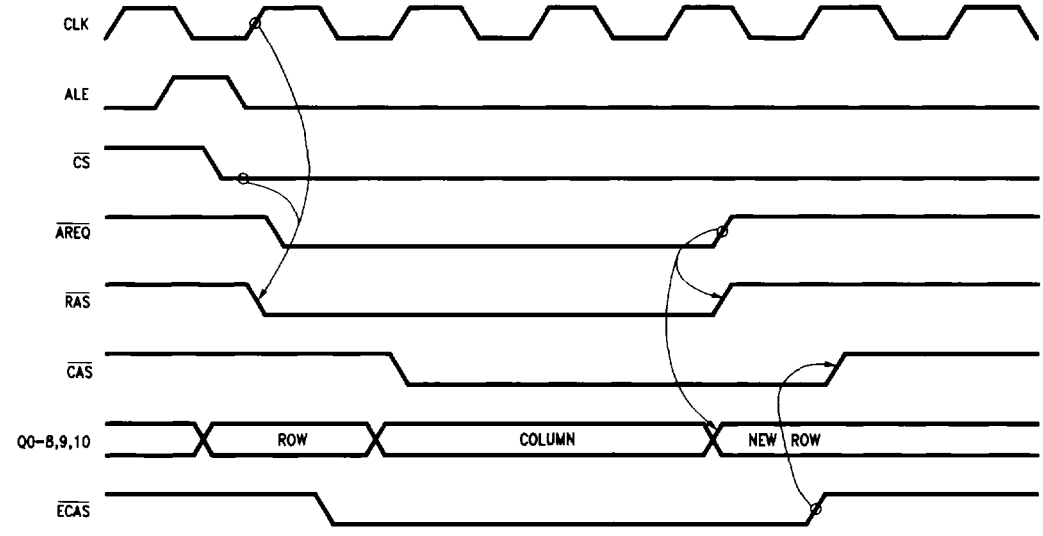

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FIGURE 9a. Access Mode 0 Extending $\overline{CAS}$

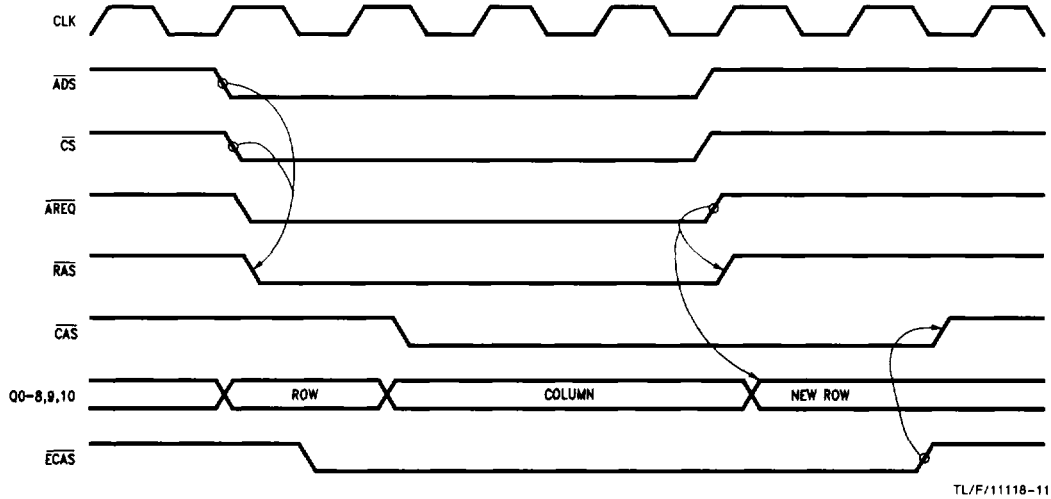

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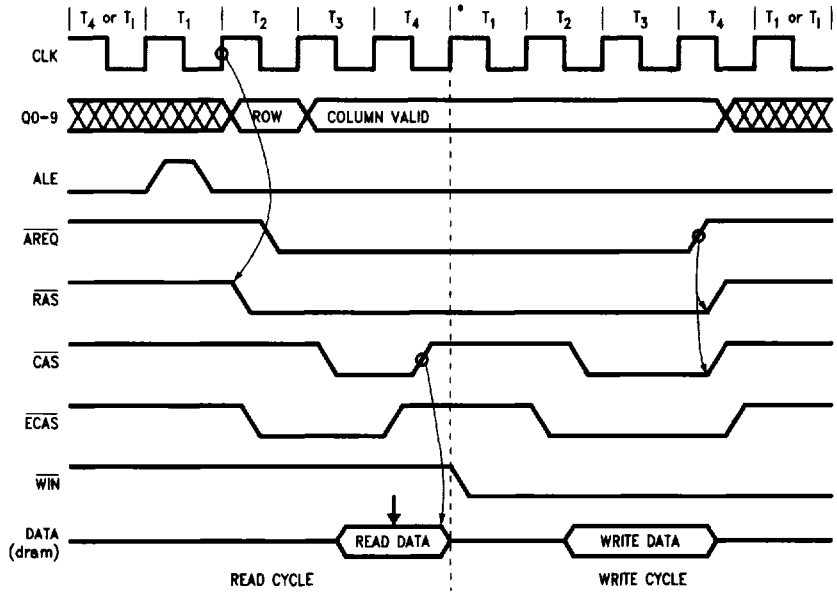
FIGURE 9b. Access Mode 1 Extending $\overline{CAS}$

4.0 Port A Access Modes (Continued)

4.4 READ-MODIFY-WRITE CYCLES WITH EITHER ACCESS MODE

There are 2 methods by which this chip can be used to do read-modify-write access cycles. The first method involves doing a late write access where the $\overline{WIN}$ input is asserted some delay after $\overline{CAS}$ is asserted. The second method involves doing a page mode read access followed by a page mode write access with $\overline{RAS}$ held low (see *Figure 9c*).

$\overline{CAS}$n must be toggled using the $\overline{ECAS}$n inputs and $\overline{WIN}$ has to be changed from negated to asserted (read to write) while $\overline{CAS}$ is negated. This method is better than changing $\overline{WIN}$ from negated to asserted in a late write access because here a problem may arise with DATA IN and DATA OUT being valid at the same time. This may result in a data line trying to drive two different levels simultaneously. The page mode method of a read-modify-write access allows the user to have transceivers in the system because the data in (read data) is guaranteed to be high impedance during the time the data out (write data) is valid.



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*There may be idle states inserted here by the CPU.

FIGURE 9c. Read-Modify-Write Access Cycle

4.0 Port A Access Modes (Continued)

4.5 ADDITIONAL ACCESS SUPPORT FEATURES

To support the different modes of accessing, the DP8430V/31V/32V offer other access features. These additional features include: Address Latches and Column Increment (for page/burst mode support), Address Pipelining, and Delay $\overline{CAS}$ (to allow the user with a multiplexed bus to ensure valid data is present before $\overline{CAS}$ is asserted).

4.5.1 Address Latches and Column Increment

The Address Latches can be programmed, through programming bit B0. They can be programmed to either latch the address or remain in a fall-through mode. If the address latches are used to latch the address, the controller will function as follows:

In Mode 0, the rising edge of ALE places the latches in fall-through, once ALE is negated, the address present in the row, column and bank input is latched.

In Mode 1, the address latches are in fall through mode until $\overline{ADS}$ is asserted. $\overline{ADS}$ asserted latches the address.

Once the address is latched, the column address can be incremented with the input COLINC. COLINC can be used for sequential accesses of static column DRAMs. COLINC can also be used with the $\overline{ECAS}$ inputs to support sequential accesses to page mode DRAMs as shown in *Figure 10.* COLINC should only be asserted when the signal $\overline{RFIP}$ is negated during an access since this input functions as extended refresh when $\overline{RFIP}$ is asserted. COLINC must be negated (0) when the address is being latched ($\overline{ADS}$ falling edge in Mode 1). If COLINC is asserted with all of the bits of the column address asserted (ones), the column address will return to zero.

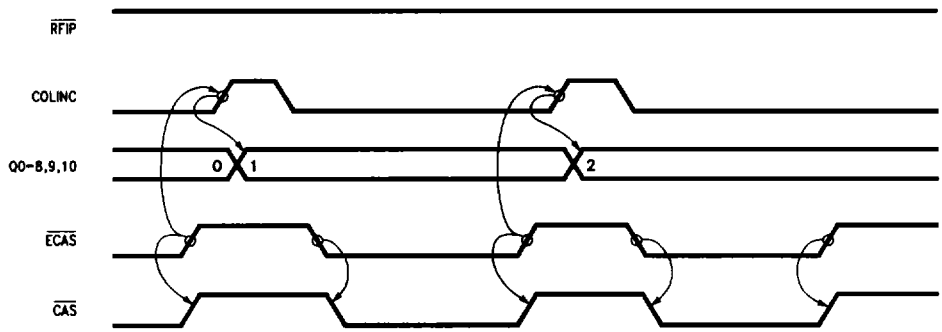

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FIGURE 10. Column Increment

The address latches function differently with the DP8432V. The DP8432V will latch the address of the currently granted port. If Port A is currently granted, the address will be latched as described in Section 4.5.1. If Port A is not granted, and requests an access, the address will be latched on the first or second positive edge of CLK after GRANTB has been negated depending on the programming bits R0, R1.

For Port B, if GRANTB is asserted, the address will be latched with $\overline{AREQB}$ asserted. If GRANTB is negated, the address will latch on the first or second positive edge of CLK after GRANTB is asserted depending on the programming bits R0, R1.

4.0 Port A Access Modes (Continued)

4.5.2 Address Pipelining

Address pipelining is the overlapping of accesses to different banks of DRAM. If the majority of successive accesses are to a different bank, the accesses can be overlapped. Because of this overlapping, the cycle time of the DRAM accesses are greatly reduced. The DP8430V/31V/32V can be programmed to allow a new row address to be placed on the DRAM address bus after the column address hold time has been met. At this time, a new access can be initiated with $\overline{ADS}$ or ALE, depending on the access mode, while $\overline{AREQ}$ is used to sustain the current access. The DP8432V supports address pipelining for Port A only. This mode cannot be used with page, static column or nibble modes of operations because the DRAM column address is switched back to the row address after $\overline{CAS}$ is asserted. This mode is programmed through address bit R8 (see *Figures 11a* and *11b*).

During address pipelining in Mode 0, shown in *Figure 11c*, ALE cannot be pulsed high to start another access until $\overline{AREQ}$ has been asserted for the previous access for at least one period of CLK. $\overline{DTACK}$, if programmed, will be negated once $\overline{AREQ}$ is negated. $\overline{WAIT}$, if programmed to insert wait states, will be asserted once ALE and $\overline{CS}$ are asserted.

In Mode 1, shown in *Figure 11d*, $\overline{ADS}$ can be negated once $\overline{AREQ}$ is asserted. After meeting the minimum negated pulse width for $\overline{ADS}$, $\overline{ADS}$ can again be asserted to start a new access. $\overline{DTACK}$, if programmed, will be negated once $\overline{AREQ}$ is negated. $\overline{WAIT}$, if programmed, will be asserted once $\overline{ADS}$ is asserted.

In either mode with either type of wait programmed, the DP8430V/31V/32V will still delay the access for precharge if sequential accesses are to the same bank or if a refresh takes place.

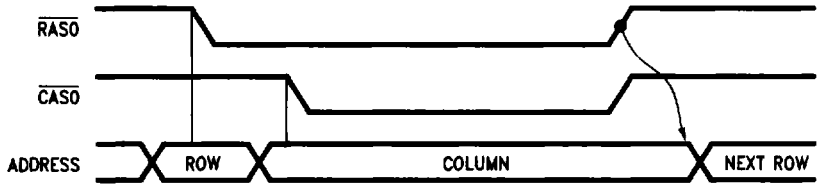

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FIGURE 11a. Non-Address Pipelined Mode

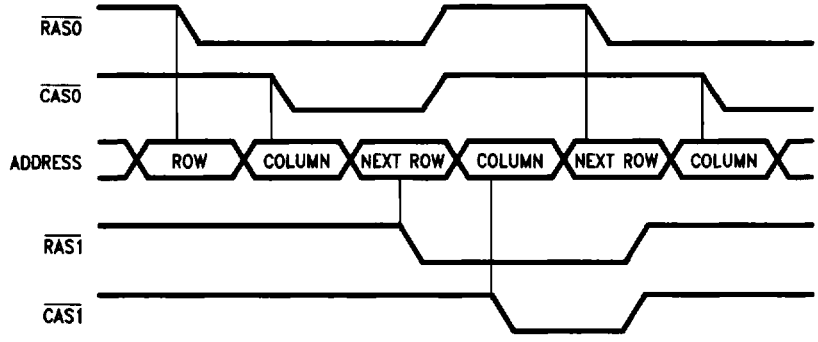

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FIGURE 11b. Address Pipelined Mode

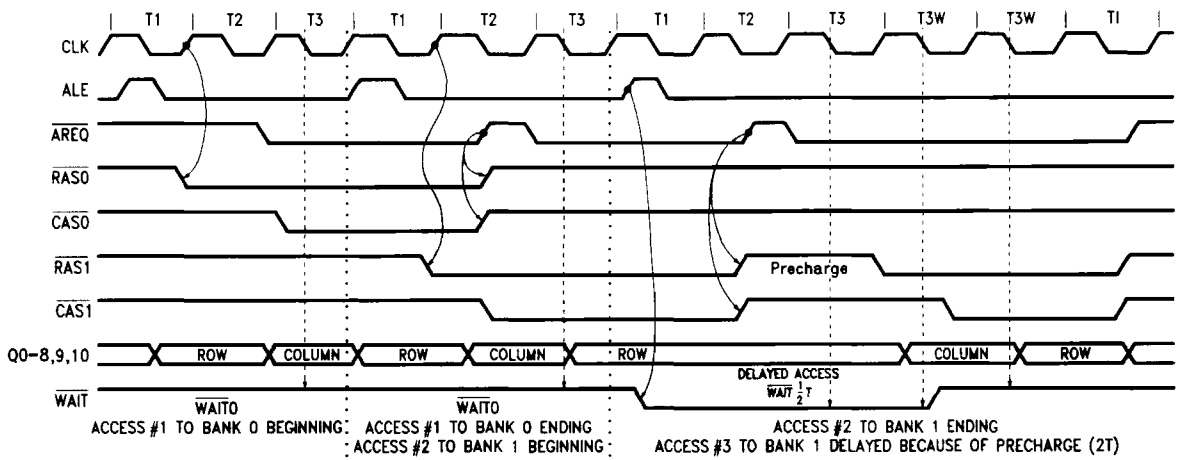

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FIGURE 11c. Mode 0 Address Pipelining (WAIT of 0, ½T Has Been Programmed. WAIT is Sampled at the "T3" Falling Clock Edge)

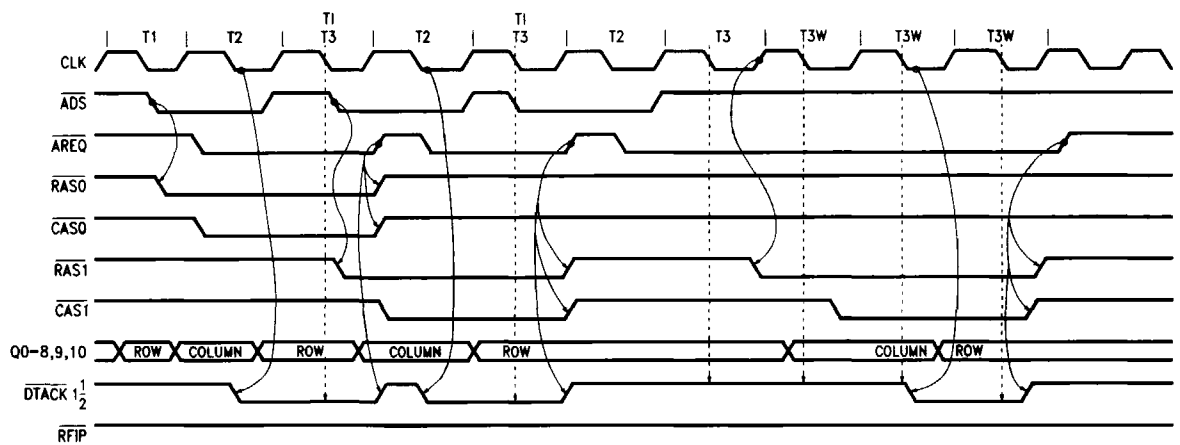

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FIGURE 11d. Mode 1 Address Pipelining (DTACK 1½T Programmed, DTACK is Sampled at the "T3" Falling Clock Edge)

4.0 Port A Access Modes (Continued)

4.5.3 Delay $\overline{CAS}$ during Write Accesses

Address bit C9 asserted during programming will cause $\overline{CAS}$ to be delayed until the first positive edge of CLK after $\overline{RAS}$ is asserted when the input $\overline{WIN}$ is asserted. Delaying $\overline{CAS}$ during write accesses ensures that the data to be written to DRAM will be setup to $\overline{CAS}$ asserting as shown in *Figures 12a* and *12b*. If the possibility exists that data still may not be present after the first positive edge of CLK, $\overline{CAS}$ can be delayed further with the $\overline{ECAS}$ inputs. If address bit C9 is negated during programming, read and write accesses will be treated the same (with regard to $\overline{CAS}$).

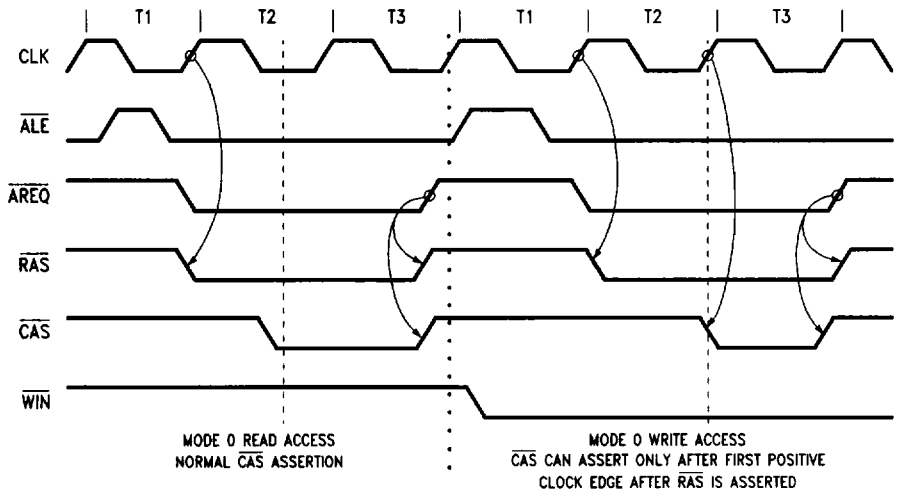

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FIGURE 12a. Mode 0 Delay $\overline{CAS}$

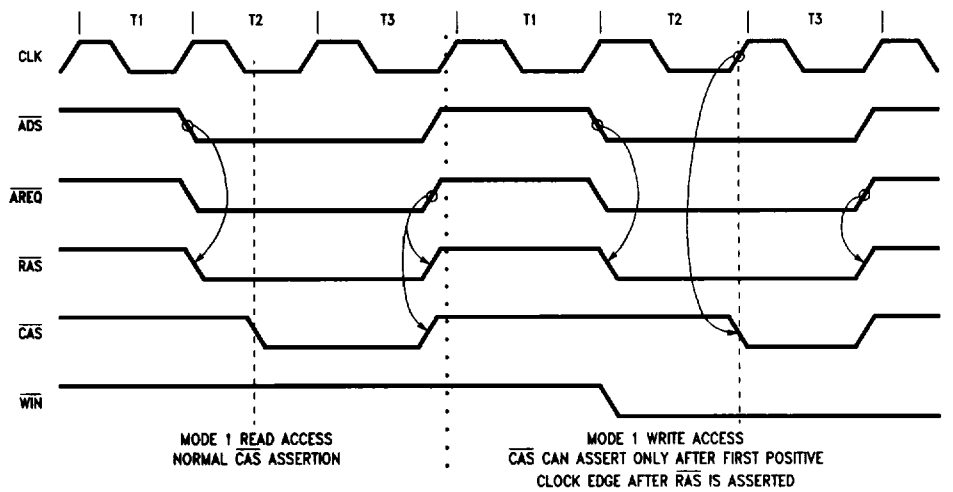

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FIGURE 12b. Mode 1 Delay $\overline{CAS}$

5.0 Refresh Options

The DP8430V/31V/32V support two refresh control mode options:

1. Automatic Internally Controlled Refresh.

2. Externally Controlled Refresh.

With each of the control modes above, three types of refresh can be performed.

1. All $\overline{RAS}$ Refresh.

2. Staggered Refresh.

3. Error Scrubbing During All $\overline{RAS}$ Refresh.

There are two inputs, EXTNDRF and $\overline{RFSH}$ and two outputs, $\overline{RFIP}$ and $\overline{RFRQ}$, associated with refresh. There are also ten programming bits: R0–1, R9, C0–6 and ECAS0 used to program the various types of refreshing.

Asserting the input EXTNDRF, extends the refresh cycle for a single or multiple integral periods of CLK.

The output $\overline{RFIP}$ is asserted one period of CLK before the first refresh $\overline{RAS}$ is asserted. If an access is currently in progress, $\overline{RFIP}$ will be asserted up to one period of CLK before the first refresh $\overline{RAS}$, after $\overline{AREQ}$ or $\overline{AREQB}$ is negated for the access (see *Figure 13*).

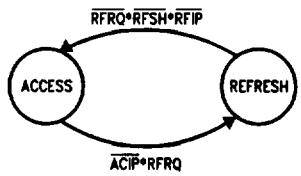
The DP8430V/31V/32V will increment the refresh address counter automatically, independent of the refresh mode used. The refresh address counter will be incremented once all the refresh $\overline{RAS}$s have been negated.

In every combination of refresh control mode and refresh type, the DP8430V/31V/32V is programmed to keep $\overline{RAS}$ asserted a number of CLK periods. The time values of $\overline{RAS}$ low during refresh are programmed through programming bits R0 and R1.

5.1 REFRESH CONTROL MODES

5.1.1. Automatic Internal Refresh

To select Automatic Internal Refresh, the user must choose $\overline{ECAS0}$ = 0 during programming. The DP8430V/31V/32V have an internal refresh clock. The period of the refresh clock is generated from the programming bits C0–3. Every period of the refresh clock, an internal refresh request is generated. As long as a DRAM access is not currently in progress and precharge time has been met, the internal refresh request will generate an automatic internal refresh. If a DRAM access is in progress, the DP8430V/31V/32V on-chip arbitration logic will wait until the access is finished before performing the refresh. The refresh/access arbitration logic can insert a refresh cycle between two address pipelined accesses. However, the refresh arbitration logic can not interrupt an access cycle to perform a refresh.



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Explanation of Terms

RFRQ = ReFresh ReQuest internal to the DP8430V/31V/32V. RFRQ has the ability to hold off a pending access.

RFSH = Externally requested ReFreSH

RFIP = ReFresh in Progress

ACIP = Port A or Port B (DP8432V only) ACcess in Progress. This means that either RAS is low for an access or is in the process of transitioning low for an access.

FIGURE 13. DP8430V/31V/32V Access/Refresh Arbitration State Program

5.0 Refresh Options (Continued)

5.1.2 Externally Controlled Refresh Mode

To choose this refresh mode, the user must program $\overline{ECAS0}$ = 1. When this mode is selected, the user is responsible for generating refresh requests by asserting the input $\overline{RFSH}$ every time a refresh cycle is to be performed. In this refresh mode, the output $\overline{WE}$ functions a $\overline{RFRQ}$.

When Externally Controlled Refresh is selected, the user may choose to monitor the output ReFresh ReQuest ($\overline{RFRQ}$) for an indication from the DRAM controller that a refresh is needed. When this output asserts, it indicates that the internal refresh clock has expired and that another refresh is necessary. Then the user has two options. First, he can answer immediately asserting the input $\overline{RFSH}$ requesting a refresh cycle. In this case a refresh will take place immediately if no access is in progress and precharge time for the previous access has been met. See *Figure 14a.*

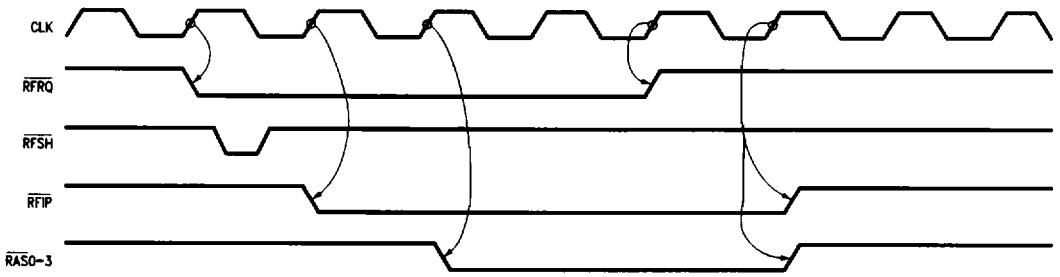

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FIGURE 14a. Automatic Internal Refresh with Refresh Request (3T of $\overline{RAS}$ Low during Refresh Programmed)

Second, the user may choose not to assert the $\overline{RFSH}$ input delaying the refresh until later. $\overline{RFRQ}$ will go high and then assert (toggle) if additional periods of the internal refresh clock have expired and the user has not performed a refresh by asserting the input $\overline{RFSH}$. See *Figure 14b.* If a time critical event, or a long access like page or static column mode can not be interrupted, $\overline{RFRQ}$ pulsing high can be used to increment an external counter. This counter can later be used to perform a burst refresh of the number of refreshes missed (through the $\overline{RFSH}$ input). This scheme can be thought of as Refresh Request/Acknowledge.

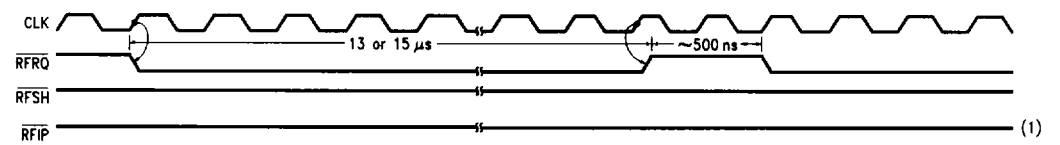

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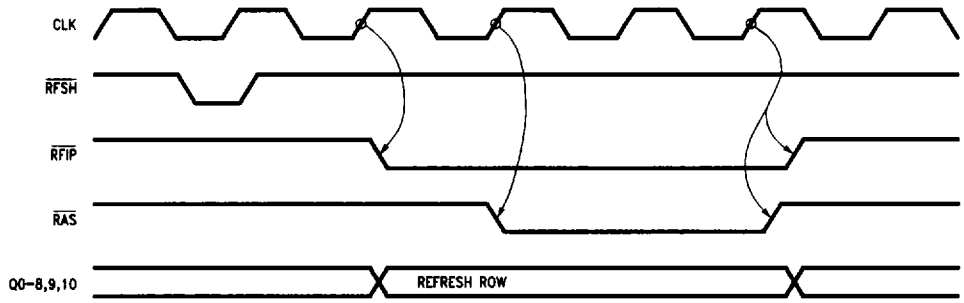
FIGURE 14b. Refresh Request Timing

5.0 Refresh Options (Continued)

In Externally Controlled Refresh the user does not have to wait for $\overline{RFRQ}$ to perform a refresh. The user can at any time assert the $\overline{RFSH}$ input. Pulsing $\overline{RFSH}$ low, sets an internal latch that is used to produce the internal refresh request. The refresh cycle will take place on the next positive edge of clock, as shown in *Figure 15a*. If an access to the DRAM is in progress or precharge time for the last access has not been met, the refresh will be delayed. Since pulsing $\overline{RFSH}$ low sets a latch, the user doesn't have to keep $\overline{RFSH}$ low until the refresh starts. When the last refresh $\overline{RAS}$ negates, the internal refresh request latch is cleared.

By keeping the input $\overline{RFSH}$ asserted past the positive edge of CLK which ends the refresh cycle as shown in *Figure 15b*, the user will perform another refresh cycle. Each refresh cycle during a burst refresh will meet the refresh $\overline{RAS}$ low time and the $\overline{RAS}$ precharge time (programming bits R0–1). This scheme can be thought of as Externally Controlled Burst Refresh. If the user desires to burst refresh the entire DRAM, he could generate an end of count signal (burst refresh finished), by looking at one of the DP8430V/31V/32V high address outputs (Q7, Q8, Q9 or Q10) and the $\overline{RFIP}$ output. The Qn outputs function as a decode of how many row addresses have been refreshed. (Q7 = 128 refreshes, Q8 = 256 refreshes, Q9 = 512 refreshes and Q10 = 1024 refreshes).



TL/F/11118–23

FIGURE 15a. Single Externally Refreshes (2 Periods of $\overline{RAS}$ Low during Refresh Programmed)

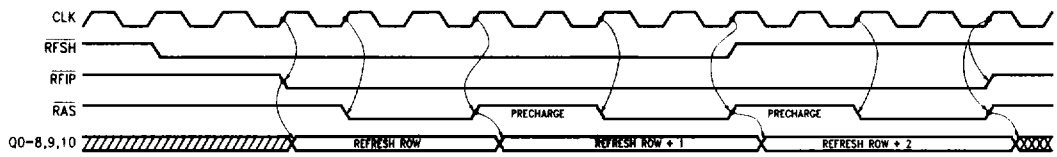


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FIGURE 15b. External Burst Refresh
(2 Periods of $\overline{RAS}$ Precharge, 2 Periods of Refresh $\overline{RAS}$ Low during Refresh Programmed)

5.0 Refresh Options (Continued)

5.2 REFRESH CYCLE TYPES

Three different types of refresh cycles are available for use. The three different types are mutually exclusive and can be used with any of the three modes of refresh control. The three different refresh cycle types are: all $\overline{RAS}$ refresh, staggered $\overline{RAS}$ refresh and error scrubbing during all $\overline{RAS}$ refresh. In all refresh cycle types, the $\overline{RAS}$ precharge time is guaranteed: between the previous access $\overline{RAS}$ ending and the refresh $\overline{RAS}0$ starting; between refresh $\overline{RAS}3$ ending and access $\overline{RAS}$ beginning; between burst refresh $\overline{RAS}$s.

5.2.1 Conventional $\overline{RAS}$ Refresh

A conventional refresh cycle causes $\overline{RAS}0-3$ to all assert from the first positive edge of CLK after $\overline{RFIP}$ is asserted as shown in *Figure 16*. $\overline{RAS}0-3$ will stay asserted until the number of positive edges of CLK programmed have passed. On the last positive edge, $\overline{RAS}0-3$, and $\overline{RFIP}$ will be negated. This type of refresh cycle is programmed by negating address bit R9 during programming.

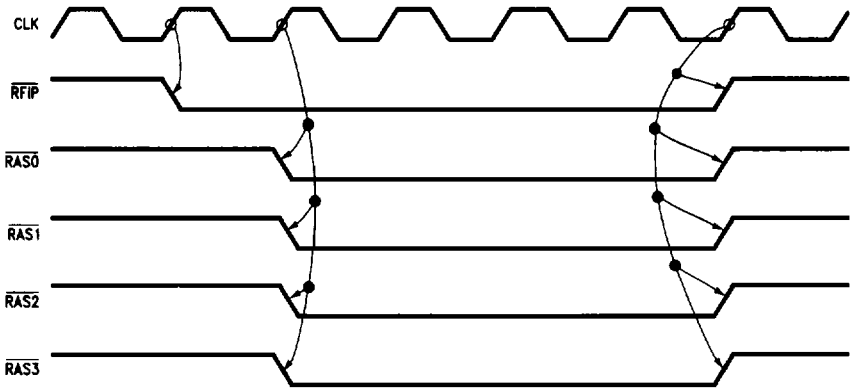

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FIGURE 16. Conventional $\overline{RAS}$ Refresh

5.2.2 Staggered $\overline{RAS}$ Refresh

A staggered refresh staggers each $\overline{RAS}$ or group of $\overline{RAS}$s by a positive edge of CLK as shown in *Figure 17*. The number of $\overline{RAS}$s, which will be asserted on each positive edge of CLK, is determined by the $\overline{RAS}$, $\overline{CAS}$ configuration mode programming bits C4–C6. If single $\overline{RAS}$ outputs are selected during programming, then each $\overline{RAS}$ will assert on successive positive edges of CLK. If two $\overline{RAS}$ outputs are selected during programming then $\overline{RAS}0$ and $\overline{RAS}1$ will assert on the first positive edge of CLK after $\overline{RFIP}$ is asserted. $\overline{RAS}2$ and $\overline{RAS}3$ will assert on the second positive edge of CLK after $\overline{RFIP}$ is asserted. If all $\overline{RAS}$ outputs were selected during programming, all $\overline{RAS}$ outputs would assert on the first positive edge of CLK after $\overline{RFIP}$ is asserted. Each $\overline{RAS}$ or group of $\overline{RAS}$s will meet the programmed $\overline{RAS}$ low time and then negate.

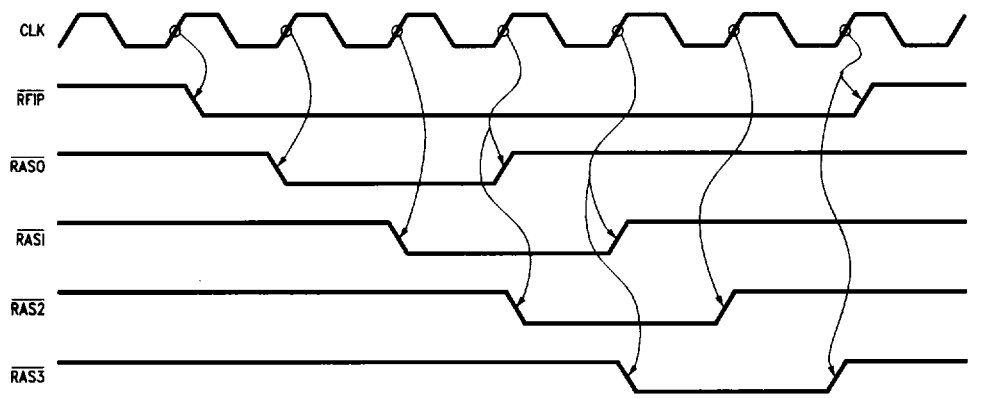

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FIGURE 17. Staggered $\overline{RAS}$ Refresh

5.0 Refresh Options (Continued)

5.2.3 Error Scrubbing during Refresh

The DP8430V/31V/32V support error scrubbing during all $\overline{RAS}$ DRAM refreshes. Error scrubbing during refresh is selected through bits C4–C6 with bit R9 negated during programming. Error scrubbing can not be used with staggered refresh (see Section 8.0). Error scrubbing during refresh allows a $\overline{CAS}$ or group of $\overline{CAS}$s to assert during the all $\overline{RAS}$ refresh as shown in *Figure 18*. This allows data to be read from the DRAM array and passed through an Error Detection And Correction Chip, EDAC. If the EDAC determines that the data contains a single bit error and corrects that error, the refresh cycle can be extended with the input extend refresh, EXTNDRF, and a read-modify-write operation can be performed by asserting $\overline{WE}$. It is the responsibility of the designer to ensure that $\overline{WE}$ is negated. The DP8432V has a 24-bit internal refresh address counter that contains the 11 row, 11 column and 2 bank addresses. The DP8430V/31V have a 22-bit internal refresh address counter that contains the 10 row, 10 column and 2 bank addresses. These counters are configured as bank, column, row with the row address as the least significant bits. The bank counter bits are then used with the programming selection to determine which $\overline{CAS}$ or group of $\overline{CAS}$s will assert during a refresh.

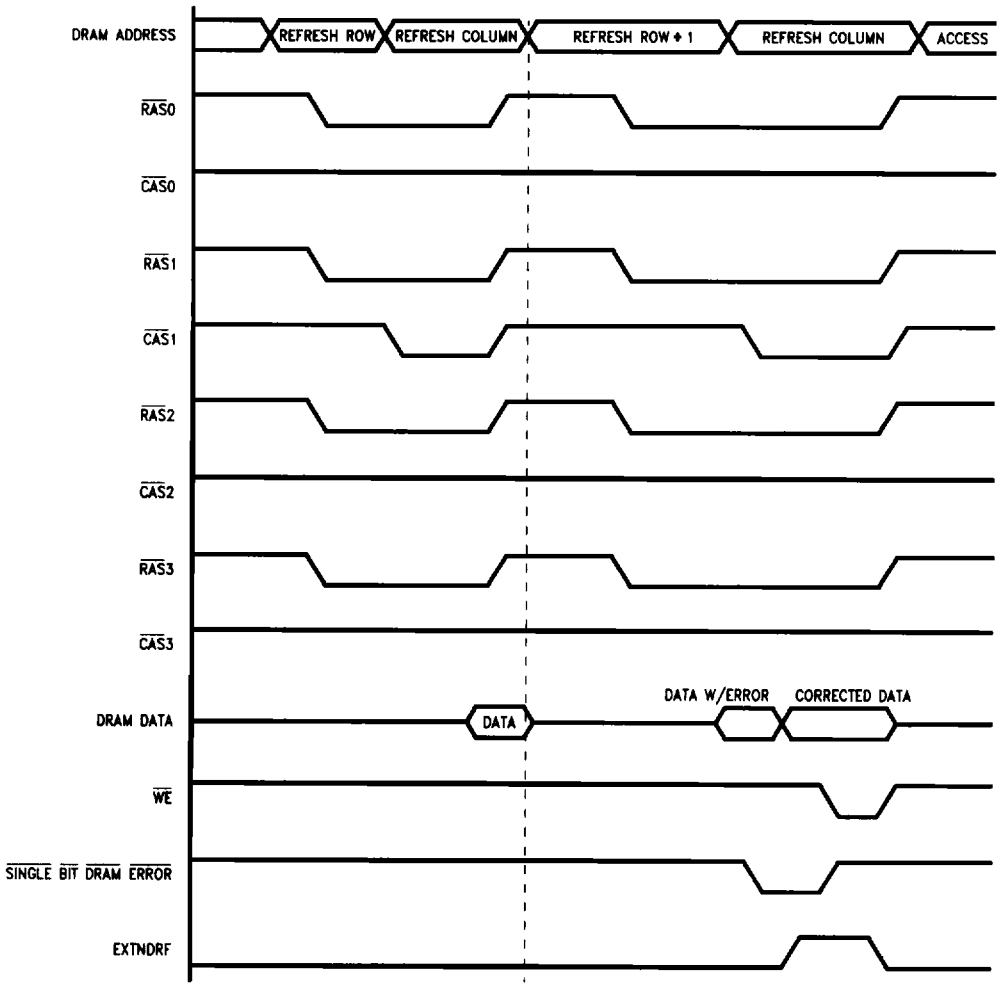

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FIGURE 18. Error Scrubbing during Refresh (Two Refresh Cycles Shown)

5.0 Refresh Options (Continued)

5.3 EXTENDING REFRESH

The programmed number of periods of CLK that refresh $\overline{\text{RAS}}$s are asserted can be extended by one or multiple periods of CLK. Only the all $\overline{\text{RAS}}$ (with or without error scrubbing) type of refresh can be extended. To extend a refresh cycle, the input extend refresh, EXTNDRF, must be asserted before the positive edge of CLK that would have negated all the $\overline{\text{RAS}}$ outputs during the refresh cycle and after the positive edge of CLK which starts all $\overline{\text{RAS}}$ outputs during the refresh as shown in *Figure 19*. This will extend the refresh to the next positive edge of CLK and EXTNDRF will be sampled again. The refresh cycle will continue until EXTNDRF is sampled low on a positive edge of CLK.

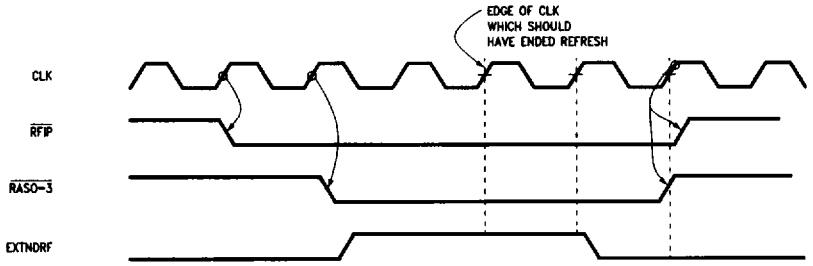

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FIGURE 19. Extending Refresh with the Extend Refresh (EXTNDRF) Input

6.0 Port A Wait State Support

Wait states allow a CPU's access cycle to be increased by one or multiple CPU clock periods. The wait or ready input is named differently by CPU manufacturers. However, any CPU's wait or ready input is compatible with either the $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ output of the DP8430V/31V/32V. The user determines whether to program $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ (R7) and which value to select for $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ (R2, R3) depending upon the CPU used and where the CPU samples its wait input during an access cycle.

The decision to terminate the CPU access cycle is directly affected by the speed of the DRAMs used. The system designer must ensure that the data from the DRAMs will be present for the CPU to sample or that the data has been written to the DRAM before allowing the CPU access cycle to terminate.

The insertion of wait states also allows a CPU's access cycle to be extended until the DRAM access has taken place. The DP8430V/31V/32V insert wait states into CPU access cycles due to; guaranteeing precharge time, refresh currently in progress, user programmed wait states, the $\overline{\text{WAITIN}}$ signal being asserted and GRANTB not being valid (DP8432V only). If one of these events is taking place and the CPU starts an access, the DP8430V/31V/32V will insert wait states into the access cycle, thereby increasing the length of the CPU's access. Once the event has been completed, the DP8430V/31V/32V will allow the access to take place and stop inserting wait states.

There are six programming bits, R2–R7; an input, $\overline{\text{WAITIN}}$; and an output that functions as $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$.

6.1 $\overline{\text{WAIT}}$ TYPE OUTPUT

With the R7 address bit negated during programming, the user selects the $\overline{\text{WAIT}}$ output. As long as $\overline{\text{WAIT}}$ is sampled asserted by the CPU, wait states (extra clock periods) are inserted into the current access cycle as shown in *Figure 20*. Once $\overline{\text{WAIT}}$ is sampled negated, the access cycle is completed by the CPU. $\overline{\text{WAIT}}$ is asserted at the beginning of a chip selected access and is programmed to negate a number of positive edges and/or negative levels of CLK from the event that starts the access. $\overline{\text{WAIT}}$ can also be programmed to function in page/burst mode applications. Once $\overline{\text{WAIT}}$ is negated during an access, and the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted, $\overline{\text{WAIT}}$ can be programmed to toggle, following the $\overline{\text{ECAS}}$ inputs. Once $\overline{\text{AREQ}}$ is negated, ending the access, $\overline{\text{WAIT}}$ will stay negated until the next chip selected access. For more details about $\overline{\text{WAIT}}$ Type Output, see Application Note AN-773.

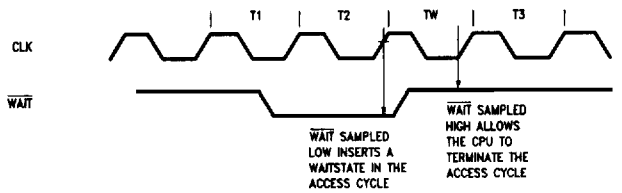

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FIGURE 20. $\overline{\text{WAIT}}$ Type Output

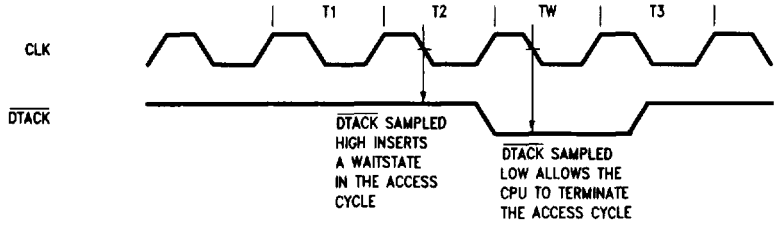
6.0 Port A Wait State Support (Continued)

6.2 $\overline{\text{DTACK}}$ TYPE OUTPUT

With the R7 address bit asserted during programming, the user selects the $\overline{\text{DTACK}}$ type output. As long as $\overline{\text{DTACK}}$ is sampled negated by the CPU, wait states are inserted into the current access cycle as shown in *Figure 21*. Once $\overline{\text{DTACK}}$ is sampled asserted, the access cycle is completed by the CPU. $\overline{\text{DTACK}}$, which is normally negated, is programmed to assert a number of positive edges and/or negative levels from the event that starts $\overline{\text{RAS}}$ for the access. $\overline{\text{DTACK}}$ can also be programmed to function during page/burst mode accesses. Once $\overline{\text{DTACK}}$ is asserted and the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted, $\overline{\text{DTACK}}$ can be programmed to negate and assert from the $\overline{\text{ECAS}}$ inputs toggling to perform a page/burst mode operation. Once $\overline{\text{AREQ}}$ is negated, ending the access, $\overline{\text{DTACK}}$ will be negated and stays negated until the next chip selected access. For more details about $\overline{\text{DTACK}}$ type output see Application Note AN-773.

6.3 DYNAMICALLY INCREASING THE NUMBER OF WAIT STATES

The user can increase the number of positive edges of CLK before $\overline{\text{DTACK}}$ is asserted or $\overline{\text{WAIT}}$ is negated. With the input $\overline{\text{WAITIN}}$ asserted, the user can delay $\overline{\text{DTACK}}$ asserting or $\overline{\text{WAIT}}$ negating either one or two more positive edges of CLK. The number of edges is programmed through address bit R6. If the user is increasing the number of positive edges in a delay that contains a negative level, the positive edges will be met before the negative level. For example if the user programmed $\overline{\text{DTACK}}$ of ½T, asserting $\overline{\text{WAITIN}}$, programmed as 2T, would increase the number of positive edges resulting in $\overline{\text{DTACK}}$ of 2½T as shown in *Figure 22a*. Similarly, $\overline{\text{WAITIN}}$ can increase the number of positive edges in a page/burst access. $\overline{\text{WAITIN}}$ can be permanently asserted in systems requiring an increased number of wait states. $\overline{\text{WAITIN}}$ can also be asserted and negated, depending on the type of access. As an example, a user could invert the $\overline{\text{WRITE}}$ line from the CPU and connect the output to $\overline{\text{WAITIN}}$. This could be used to perform write accesses with 1 wait state and read accesses with 2 wait states as shown in *Figure 22b*.



TL/F/11118-30

FIGURE 21. $\overline{\text{DTACK}}$ Type Output

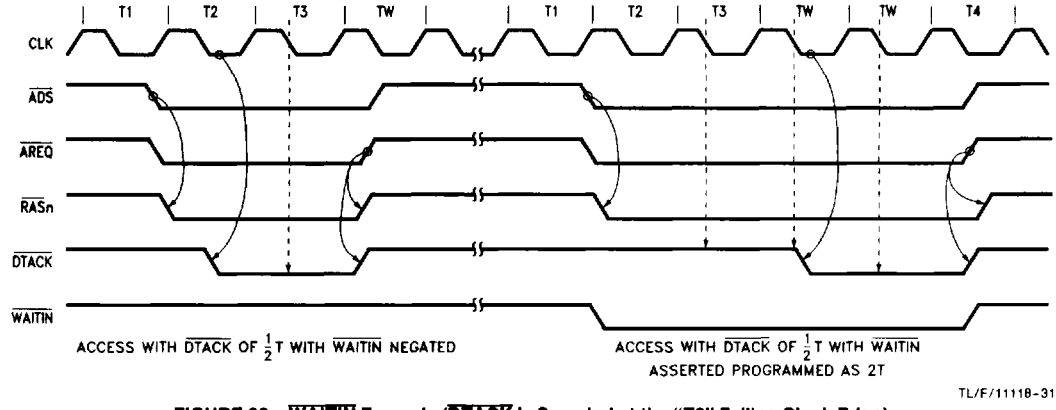


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FIGURE 22a. $\overline{\text{WAITIN}}$ Example ($\overline{\text{DTACK}}$ is Sampled at the "T3" Falling Clock Edge)

6.0 Port A Wait State Support (Continued)

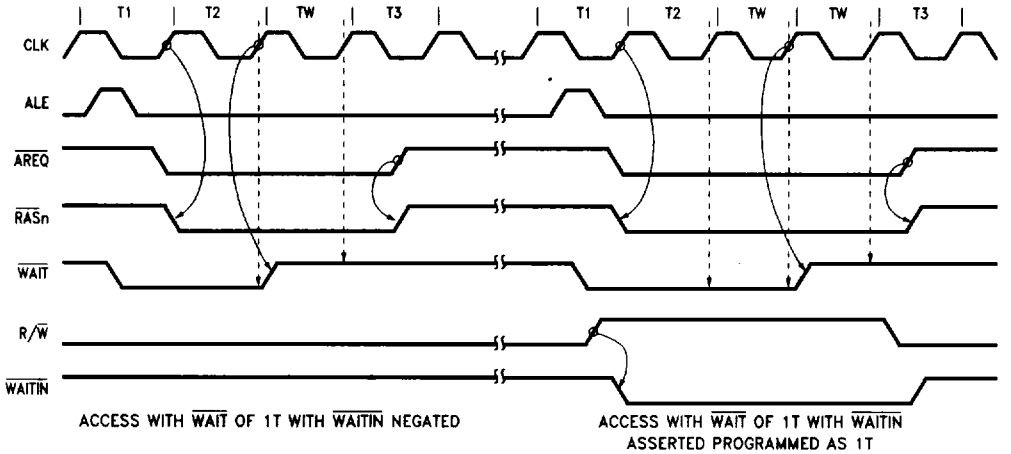

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FIGURE 22b. WAITIN Example (WAIT is Sampled at the End of "T2").

6.4 GUARANTEEING RAS LOW TIME AND RAS PRECHARGE TIME

The DP8430V/31V/32V will guarantee RAS precharge time between accesses; between refreshes; and between access and refreshes. The programming bits R0 and R1 are used to program combinations of RAS precharge time and RAS low time referenced by positive edges of CLK. RAS low time is programmed for refreshes only. During an access, the system designer guarantees the time RAS is asserted through the DP8430V/31V/32V wait logic. Since inserting wait states into an access increases the length of the CPU signals which are used to create ADS or ALE and AREQ, the time that RAS is asserted can be guaranteed.

The precharge time is also guaranteed by the DP8430V/31V/32V. Each RAS output has a separate positive edge of CLK counter. AREQ is negated setup to a positive edge of CLK to terminate the access. That positive edge is 1T. The next positive edge is 2T. RAS will not be asserted until the programmed number of positive edges of CLK have passed as shown in *Figure 23*. Once the programmed precharge time has been met, RAS will be asserted from the positive edge of CLK. However, since there is a precharge counter per RAS, an access using another RAS will not be delayed. Precharge time before a refresh is always referenced from the access RAS negating before RAS0 for the refresh asserting. After a refresh, precharge time is referenced from RAS3 negating, for the refresh, to the access RAS asserting.

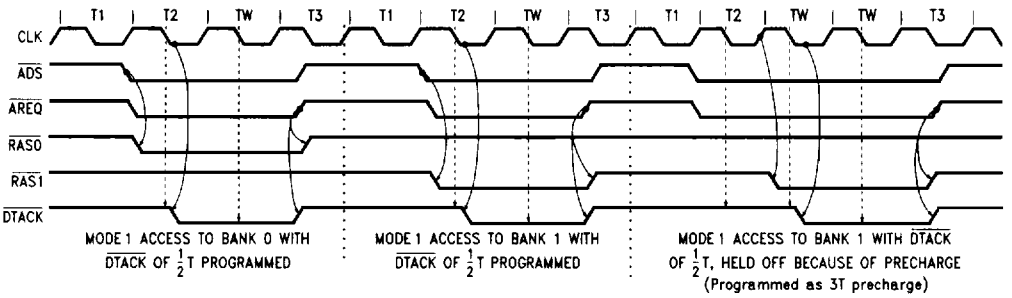

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FIGURE 23. Guaranteeing RAS Precharge (DTACK is Sampled at the "T2" Falling Clock Edge)

7.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes

The DP8430V/31V/32V allow the user to configure the DRAM array to contain one, two or four banks of DRAM. Depending on the functions used, certain considerations must be used when determining how to set up the DRAM array. Programming address bits C4, C5 and C6 along with bank selects, B0–1, and $\overline{CAS}$ enables, $\overline{ECAS}$0–3, determine which $\overline{RAS}$ or group of $\overline{RAS}$s and which $\overline{CAS}$ or group of $\overline{CAS}$s will be asserted during an access. Different memory schemes are described. The DP8430V/31V/32V is specified driving a heavy load of 72 DRAMs, representing four banks of DRAM with 16-bit words and 2 parity bits. The DP8430V/31V/32V can drive more than 72 DRAMs, but the AC timing must be increased. Since the $\overline{RAS}$ and $\overline{CAS}$ outputs are configurable, all $\overline{RAS}$ and $\overline{CAS}$ outputs should be used for the maximum amount of drive.

7.1 BYTE WRITING

By selecting a configuration in which all $\overline{CAS}$ outputs are selected during an access, the $\overline{ECAS}$ inputs enable a single or group of $\overline{CAS}$ outputs to select a byte (or bytes) in a word size of up to 32 bits. In this case, the $\overline{RAS}$ outputs are used to select which of up to 4 banks is to be used as shown in *Figures 24a* and *24b*. In systems with a word size of 16 bits, the byte enables can be gated with a high order address bit to produce four byte enables which gives an equivalent to 8 banks of 16-bit words as shown in *Figure 24d*. If less memory is required, each $\overline{CAS}$ should be used to drive each nibble in the 16-bit word as shown in *Figure 24c*.

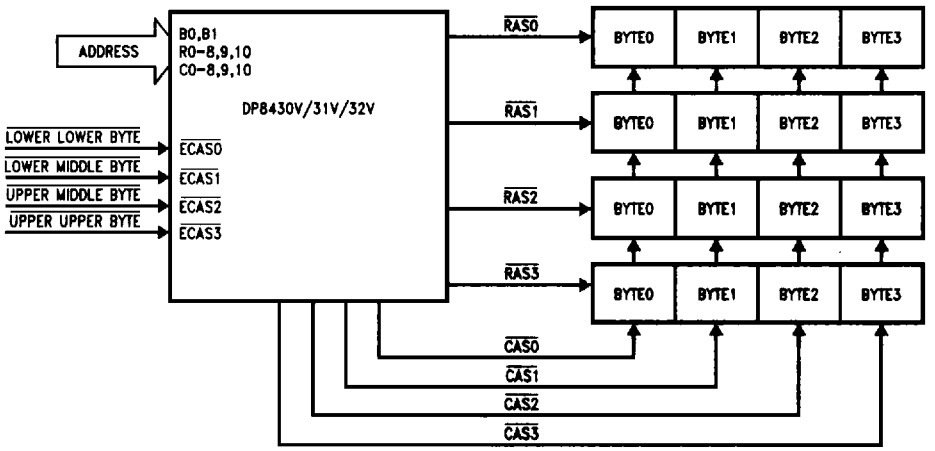

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FIGURE 24a. DRAM Array Setup for 32-Bit System (C6, C5, C4 = 1, 1, 0 during Programming)

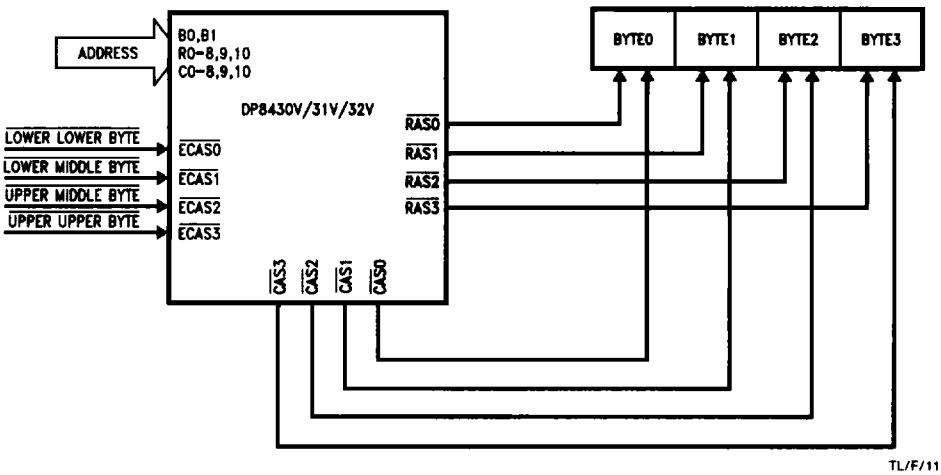

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FIGURE 24b. DRAM Array Setup for 32-Bit, 1 Bank System (C6, C5, C4 = 0, 0, 0 Allowing Error Scrubbing or C6, C5, C4 = 0, 1, 1 No Error Scrubbing during Programming)

7.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes (Continued)

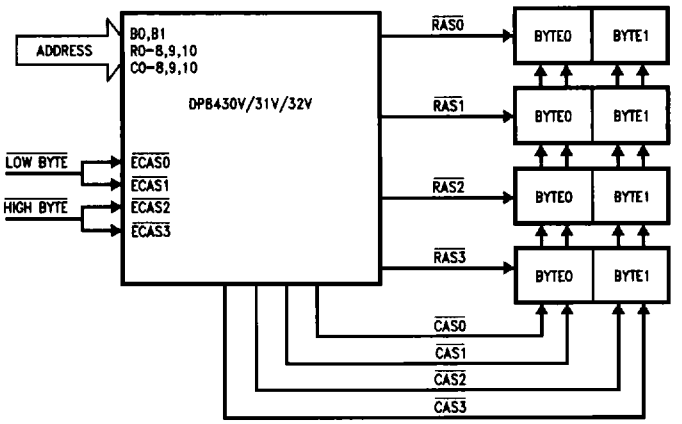

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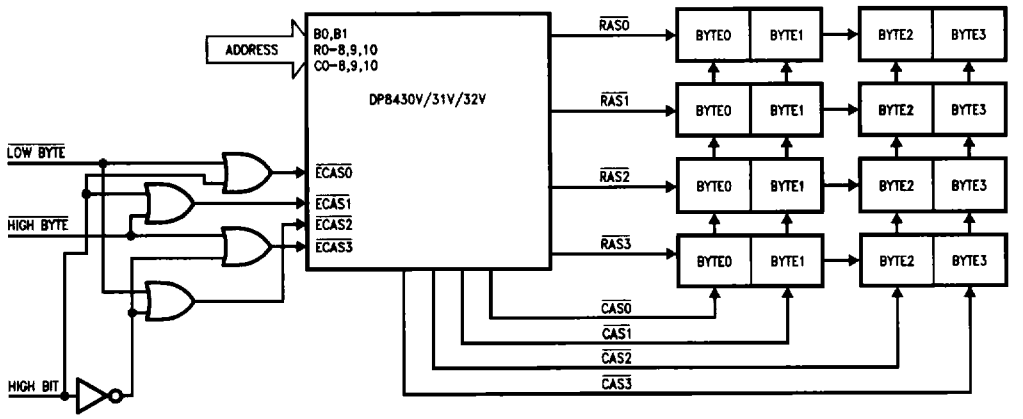
FIGURE 24c. DRAM Array Setup for 16-Bit System (C6, C5, C4 = 1, 1, 0 during Programming)



TL/F/11118–37

FIGURE 24d. 8 Bank DRAM Array for 16-Bit System (C6, C5, C4 = 1, 1, 0 during Programming)

7.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes (Continued)

7.2 MEMORY INTERLEAVING

Memory interleaving allows the cycle time of DRAMs to be reduced by having sequential accesses to different memory banks. Since the DP8430V/31V/32V have separate precharge counters per bank, sequential accesses will not be delayed if the accessed banks use different $\overline{RAS}$ outputs. To ensure different $\overline{RAS}$ outputs will be used, a mode is selected where either one or two $\overline{RAS}$ outputs will be asserted during an access. The bank select or selects, B0 and B1, are then tied to the least significant address bits, causing a different group of $\overline{RAS}$s to assert during each sequential access as shown in *Figure 25*. In this figure there should be at least one clock period of all $\overline{RAS}$'s negated between different $\overline{RAS}$'s being asserted to avoid the condition of a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

7.3 ADDRESS PIPELINING

Address pipelining allows several access $\overline{RAS}$s to be asserted at once. Because $\overline{RAS}$s can overlap, each bank requires either a mode where one $\overline{RAS}$ and one $\overline{CAS}$ are used per bank as shown in *Figure 26a* or where two $\overline{RAS}$s and two $\overline{CAS}$s are used per bank as shown in *Figure 26b*. Byte writing can be accomplished in a 16-bit word system if two $\overline{RAS}$s and two $\overline{CAS}$s are used per bank. In other systems, $\overline{WE}$s (or external gating on the $\overline{CAS}$ outputs) must be used to perform byte writing. If $\overline{WE}$s are used separate data in and data out buffers must be used. If the array is not layed out this way, a $\overline{CAS}$ to a bank can be low before $\overline{RAS}$, which will cause a refresh of the DRAM, not an access. To take full advantage of address pipelining, memory interleaving is used. To memory interleave, the least significant address bits should be tied to the bank select inputs to ensure that all "back to back" sequential accesses are not delayed, since different memory banks are accessed.

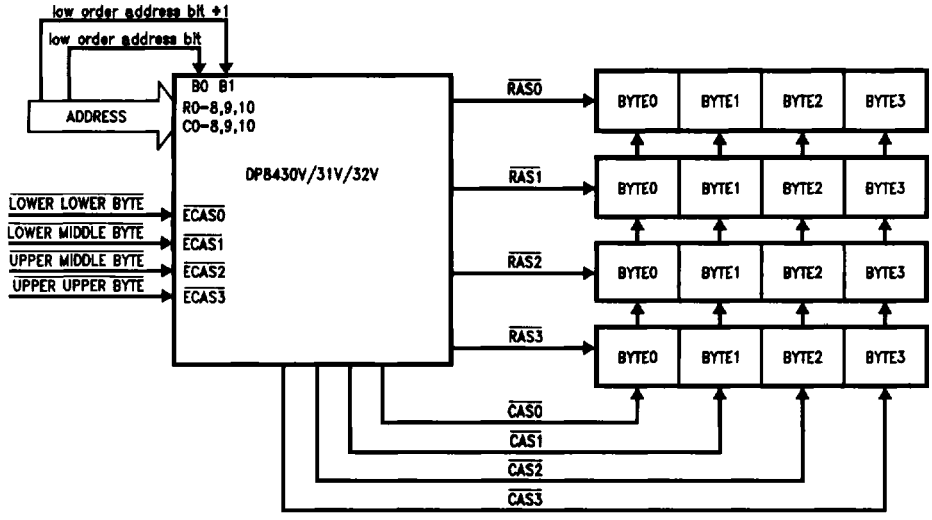


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FIGURE 25. Memory Interleaving (C6, C5, C4 = 1, 1, 0 during Programming)

7.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes (Continued)

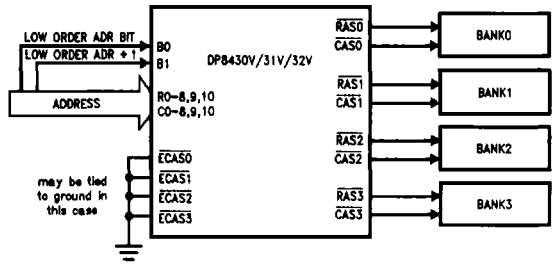

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FIGURE 26a. DRAM Array Setup for 4 Banks Using Address Pipelining (C6, C5, C4 = 1, 1, 1 or C6, C5, C4 = 0, 1, 0 (Also Allowing Error Scrubbing) during Programming)

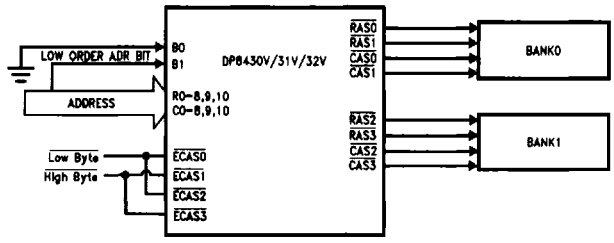

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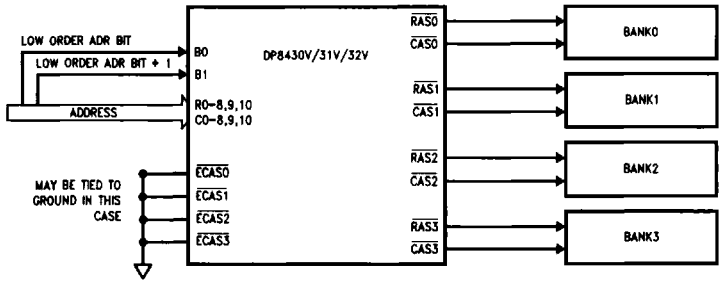
FIGURE 26b. DRAM Array Setup for Address Pipelining with 2 Banks (C6, C5, C4 = 1, 0, 1 or C6, C5, C4 = 0, 0, 1 (Also Allowing Error Scrubbing) during Programming)

7.4 ERROR SCRUBBING

In error scrubbing during refresh, the user selects one, two or four $\overline{RAS}$ and $\overline{CAS}$ outputs per bank. When performing error detection and correction, memory is always accessed as words. Since the $\overline{CAS}$ signals are not used to select individual bytes, the $\overline{ECAS}$ inputs can be tied low as shown in *Figures 27a* and *27b*.



TL/F/11118-41

FIGURE 27a. DRAM Array Setup for 4 Banks Using Error Scrubbing (C6, C5, C4 = 0, 1, 0 during Programming)

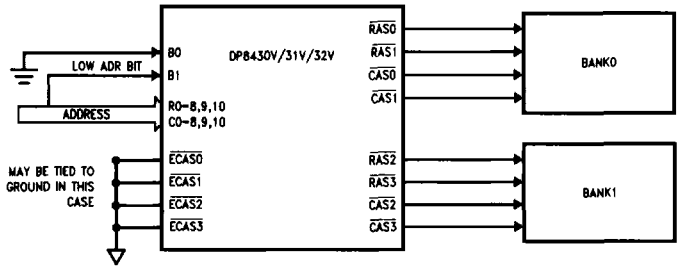


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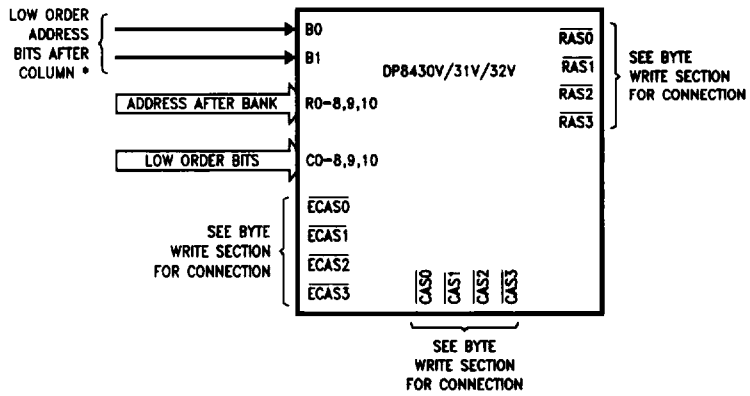
FIGURE 27b. DRAM Array Setup for Error Scrubbing with 2 Banks (C6, C5, C4 = 0, 0, 1 during Programming)

7.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes (Continued)

7.5 PAGE/BURST MODE

In a static column, page or burst mode system, the least significant bits must be tied to the column address in order to ensure that the page/burst accesses are to sequential memory addresses, as shown in *Figure 28.* In a nibble mode system, the least significant bits must be tied to the highest column and row address bits in order to ensure that sequential address bits are the "nibble" bits for nibble mode accesses *(Figure 28).* The $\overline{ECAS}$ inputs may then be toggled with the DP8430V/31V/32V's address latches in fall-through mode, while $\overline{AREQ}$ is asserted. The $\overline{ECAS}$ inputs can also be used to select individual bytes. When using nibble mode DRAMS, the third and fourth address bits can be tied to the bank select inputs to perform memory interleaving. In page or static column modes, the two address bits after the page size can be tied to the bank select inputs to select a new bank if the page size is exceeded.



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*See table below for row, column & bank address bit map. A0, A1 are used for byte addressing in this example.

Addresses	Nibble Mode*	Page Mode/Static Column Mode Page Size			
		256 Bits/Page	512 Bits/Page	1024 Bits/Page	2048 Bits/Page
Column Address	C9,R9 = A2,A3 C0-8 = X	C0-7 = A2-9 C8-10 = X	C0-8 = A2-10 C9,10 = X	C0-9 = A2-11 C10 = X	C0-10 = A2-12
Row Address	X	X	X	X	X
B0	A4	A10	A11	A12	A13
B1	A5	A11	A12	A13	A14

Assume that the least significant address bits are used for byte addressing. Given a 32-bit system A0,A1 would be used for byte addressing.

X = DON'T CARE, the user can do as he pleases.

*Nibble mode values for R and C assume a system using 1 Mbit DRAMs.

FIGURE 28. Page, Static Column, Nibble Mode System

8.0 Test Mode

Staggered refresh in combination with the error scrubbing mode places the DP8430V/31V/32V in test mode. In this mode, the 24-bit refresh counter is divided into a 13-bit and 11-bit counter. During refreshes both counters are incremented to reduce test time.

9.0 DRAM Critical Timing Parameters

The two critical timing parameters, shown in *Figure 29*, that must be met when controlling the access timing to a DRAM are the row address hold time, t_{RAH}, and the column address setup time, t_{ASC}. Since the DP8430V/31V/32V contain a precise internal delay line, the values of these parameters can be selected at programming time. These values will also increase and decrease if DELCLK varies from 2 MHz.

9.1 PROGRAMMABLE VALUES OF t_{RAH} AND t_{ASC}

The DP8430V/31V/32V allow the values of t_{RAH} and t_{ASC} to be selected at programming time. For each parameter, two choices can be selected. t_{RAH}, the row address hold time, is measured from $\overline{RAS}$ asserted to the row address starting to change to the column address. The two choices for t_{RAH} are 15 ns and 25 ns, programmable through address bit C8.

t_{ASC}, the column address setup time, is measured from the column address valid to $\overline{CAS}$ asserted. The two choices for t_{ASC} are 0 ns and 10 ns, programmable through address bit C7.

9.2 CALCULATION OF t_{RAH} AND t_{ASC}

There are two clock inputs to the DP8430V/31V/32V. These two clocks, DELCLK and CLK can either be tied together to the same clock or be tied to different clocks running asynchronously at different frequencies.

The clock input, DELCLK, controls the internal delay line and refresh request clock. DELCLK should be a multiple of 2 MHz. If DELCLK is not a multiple of 2 MHz, t_{RAH} and t_{ASC} will change. The new values of t_{RAH} and t_{ASC} can be calculated by the following formulas:

If t_{RAH} was programmed to equal 15 ns then t_{RAH} = 15*(((DELCLK Divisor)* 2 MHz/(DELCLK Frequency)) − 1) + 15 ns.

If t_{RAH} was programmed to equal 25 ns then t_{RAH} = 25*(((DELCLK Divisor)* 2 MHz/(DELCLK Frequency)) − 1) + 25 ns.

If t_{ASC} was programmed to equal 0 ns then t_{ASC} = 12.5* ((DELCLK Divisor)* 2 MHz/(DELCLK Frequency)) − 12.5 ns.

If t_{ASC} was programmed to equal 10 ns then t_{ASC} = 22.5* ((DELCLK Divisor)* 2 MHz/(DELCLK Frequency)) − 12.5 ns.

Since the values of t_{RAH} and t_{ASC} are increased or decreased, the time to $\overline{CAS}$ asserted will also increase or decrease. These parameters can be adjusted by the following formula:

Delay to $\overline{CAS}$ = Actual Spec. + Actual t_{RAH} − Programmed t_{RAH} + Actual t_{ASC} − Programmed t_{ASC}.

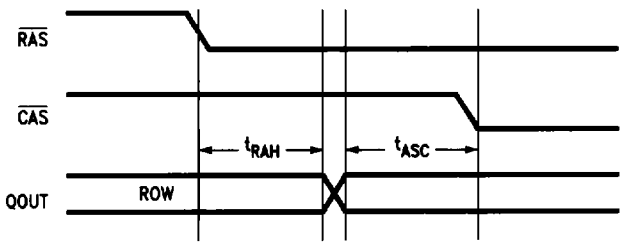

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FIGURE 29. t_{RAH} and t_{ASC}

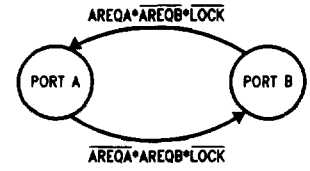
10.0 Dual Accessing (DP8432V)

The DP8432V has all the functions previously described. In addition to those features, the DP8432V also has the capabilities to arbitrate among refresh, Port A and a second port, Port B. This allows two CPUs to access a common DRAM array. DRAM refresh has the highest priority followed by the currently granted port. The ungranted port has the lowest priority. The last granted port will continue to stay granted even after the access has terminated, until an access request is received from the ungranted port (see *Figure 30a*). The dual access configuration assumes that both Port A and Port B are synchronous to the system clock. If they are not synchronous to the system clock they should be externally synchronized (Ex. By running the access requests through several Flip-Flops, see *Figure 32a*).

10.1 PORT B ACCESS MODE

Port B accesses are initiated from a single input, $\overline{AREQB}$. When $\overline{AREQB}$ is asserted, an access request is generated. If GRANTB is asserted and a refresh is not taking place or precharge time is not required, $\overline{RAS}$ will be asserted when $\overline{AREQB}$ is asserted. Once $\overline{AREQB}$ is asserted, it must stay asserted until the access is over. $\overline{AREQB}$ negated, negates $\overline{RAS}$ as shown in *Figure 30b*. Note that if $\overline{ECAS}0 = 1$ during programming the $\overline{CAS}$ outputs may be held asserted (beyond $\overline{RAS}$n negating) by continuing to assert the appropriate $\overline{ECAS}$n inputs (the same as Port A accesses). If Port B is not granted, the access will begin on the first or second positive edge of CLK after GRANTB is asserted (See R0, R1 programming bit definitions) as shown in *Figure 30c*, assuming that Port A is not accessing the DRAM ($\overline{CS}$, $\overline{ADS}$/ALE and $\overline{AREQ}$) and $\overline{RAS}$ precharge for the particular bank has completed. It is important to note that for GRANTB to transition to Port B, Port A must **not** be requesting an access at a rising clock edge (or locked) and Port B must be requesting an access at that rising clock edge. Port A can request an access through $\overline{CS}$ and $\overline{ADS}$/ALE or $\overline{CS}$ and $\overline{AREQ}$. Therefore during an interleaved access where $\overline{CS}$ and $\overline{ADS}$/ALE become asserted before $\overline{AREQ}$ from the previous access is negated, Port A will retain GRANTB = 0 whether $\overline{AREQB}$ is asserted or not.

Since there is no chip select for Port B, $\overline{AREQB}$ must incorporate this signal. This mode of accessing is similar to Mode 1 accessing for Port A.



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Explanation of Terms

AREQA = Chip Selected access request from Port A

AREQB = Chip Selected access request from Port B

LOCK = Externally controlled LOCKing of the Port that is currently GRANTed.

FIGURE 30a. DP8432V Port A/Port B Arbitration State Diagram. This arbitration may take place during the "ACCESS" or "REFRESH" state (see *Figure 13*).

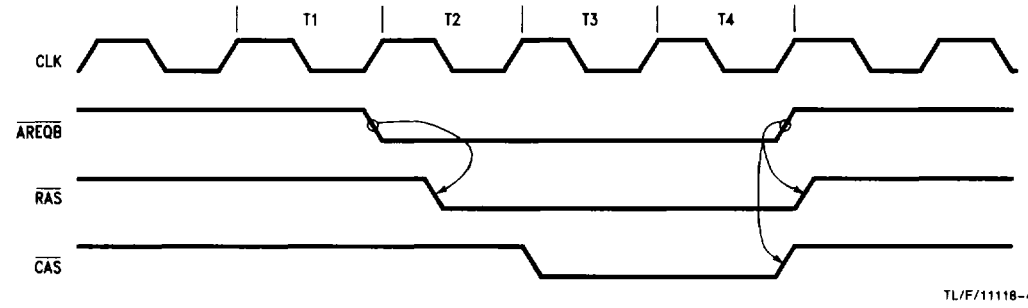

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FIGURE 30b. Access Request for Port B

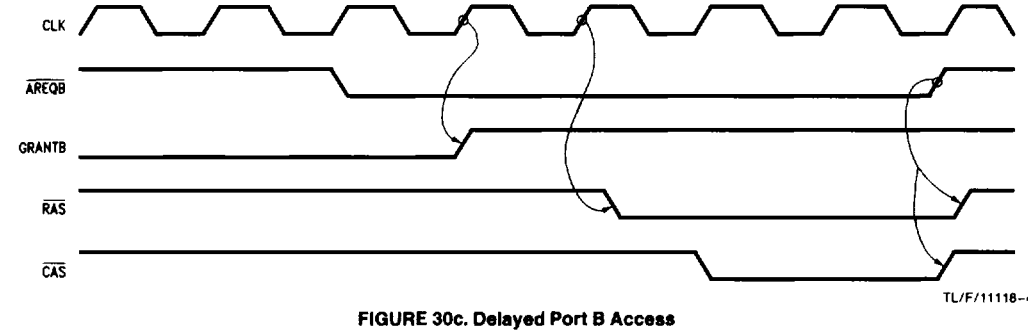

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FIGURE 30c. Delayed Port B Access

10.0 Dual Accessing (DP8432V) (Continued)

10.2 PORT B WAIT STATE SUPPORT

Advanced transfer acknowledge for Port B, $\overline{\text{ATACKB}}$, is used for wait state support for Port B. This output will be asserted when $\overline{\text{RAS}}$ for the Port B access is asserted, as shown in *Figures 31a* and *31b*. Once asserted, this output will stay asserted until $\overline{\text{AREQB}}$ is negated. With external logic, $\overline{\text{ATACKB}}$ can be made to interface to any CPU's wait input as shown in *Figure 31c*.

10.3 COMMON PORT A AND PORT B DUAL PORT FUNCTIONS

An input, $\overline{\text{LOCK}}$, and an output, GRANTB, add additional functionality to the dual port arbitration logic. $\overline{\text{LOCK}}$ allows Port A or Port B to lock out the other port from the DRAM. When a Port is locked out of the DRAM, wait states will be inserted into its access cycle until it is allowed to access memory. GRANTB is used to multiplex the input control signals and addresses to the DP8432V.

10.3.1 GRANTB Output

The output GRANTB determines which port has current access to the DRAM array. GRANTB asserted signifies Port B has access. GRANTB negated signifies Port A has access to the DRAM array.

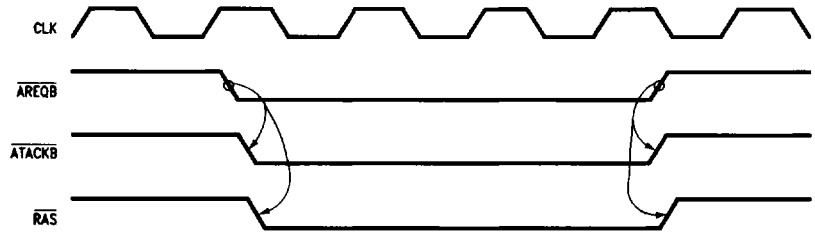

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FIGURE 31a. Non-Delayed Port B Access

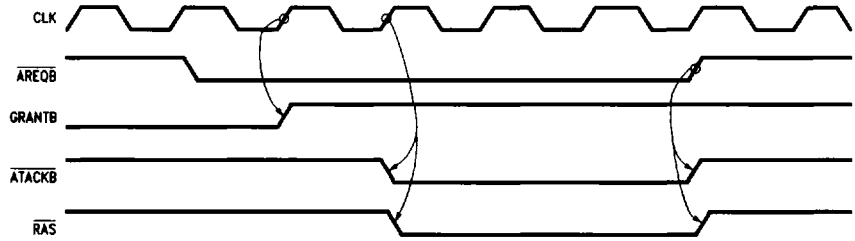

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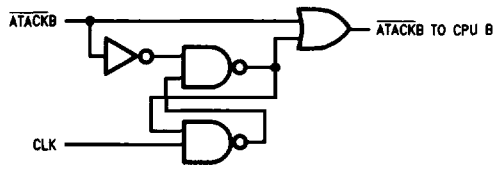
FIGURE 31b. Delayed Port B Access



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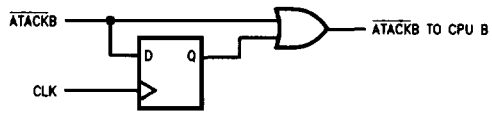
A. Extend $\overline{\text{ATACK}}$ to ½T (½ Clock) after $\overline{\text{RAS}}$ goes low.



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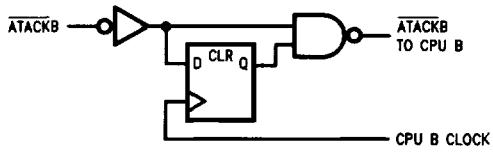
B. Extend $\overline{\text{ATACK}}$ to 1T after $\overline{\text{RAS}}$ goes low.



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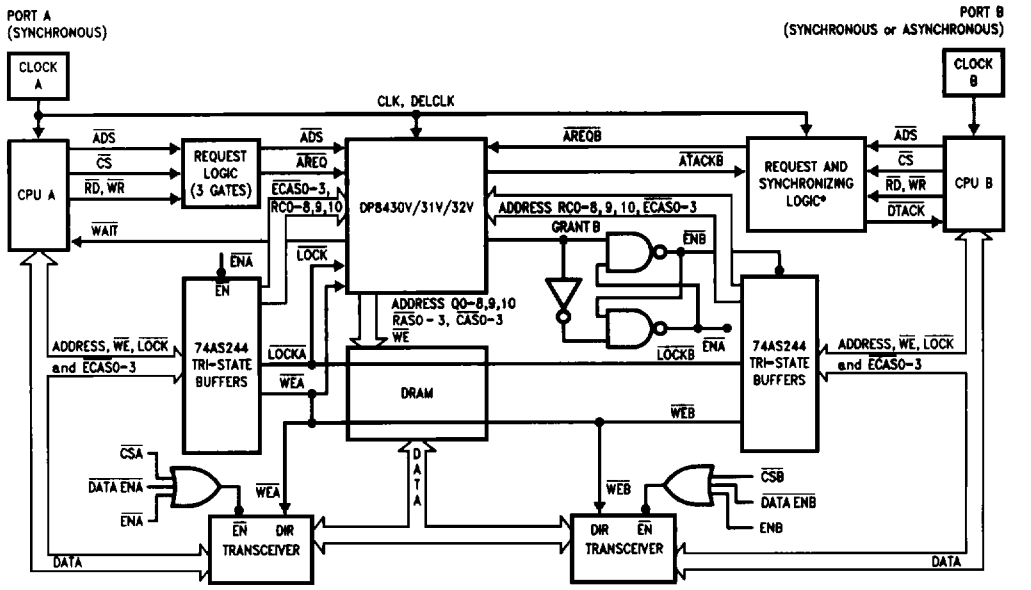
C. Synchronize $\overline{\text{ATACKB}}$ to CPU B Clock. This is useful if CPU B runs asynchronous to the DP8432.

FIGURE 31c. Modifying Wait Logic for Port B

10.0 Dual Accessing (DP8432V) (Continued)

Since the DP8432V has only one set of address inputs, the signal is used, with the addition of buffers, to allow the currently granted port's addresses to reach the DP8432V. The signals which need to be bufferred are R0–10, C0–10, B0–1, $\overline{ECAS0}$–3, $\overline{WE}$, and $\overline{LOCK}$. All other inputs are not common and do not have to be buffered as shown in *Figure 32a*. If a Port, which is not currently granted, tries to access the DRAM array, the GRANTB output will transition from a rising clock edge from $\overline{AREQ}$ or $\overline{AREQB}$ negating and will precede the $\overline{RAS}$ for the access by one or two clock periods. GRANTB will then stay in this state until the other port requests an access and the currently granted port is not accessing the DRAM as shown in *Figure 32b*.



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*If Port B is synchronous the Request Synchronizing logic will not be required.

FIGURE 32a. Dual Accessing with the DP8432V (System Block Diagram)

10.0 Dual Accessing (DP8432V) (Continued)

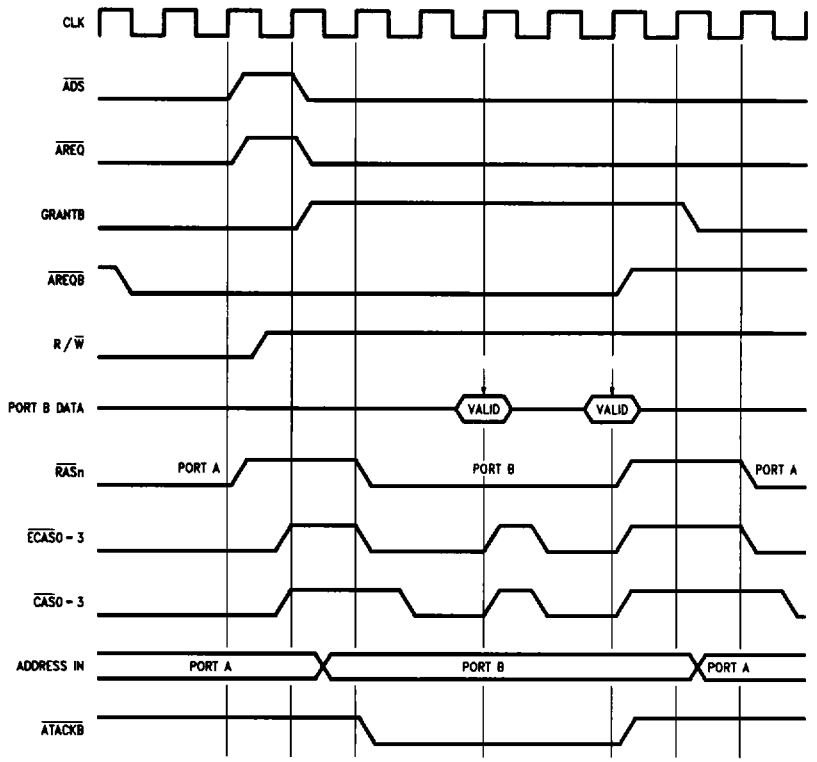

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FIGURE 32b. Wait States during a Port B Access

10.3.2 LOCK Input

When the LOCK input is asserted, the currently granted port can "lock out" the other port through the insertion of wait states to that port's access cycle. LOCK does not disable refreshes, it only keeps GRANTB in the same state even if the other port requests an access, as shown in *Figure 33*. LOCK can be used by either port.

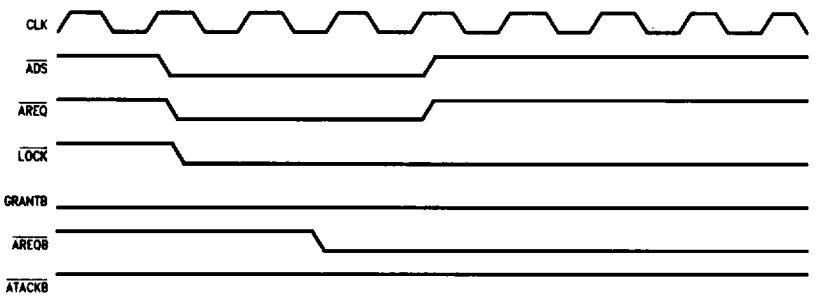

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FIGURE 33. LOCK Function

11.0 Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature under Bias ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C

All Input or Output Voltage
with Respect to GND ..... −0.5V to +7V
Power Dissipation @ 20 MHz 0.5W
ESD Rating 2000V
Temperature Cycle ..... 300 of 0/125°C

12.0 DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage	Tested with a Limited Functional Pattern	2.0		V_{CC} + 0.5	V
V_{IL}	Logical 0 Input Voltage	Tested with a Limited Functional Pattern	−0.5		0.8	V
V_{OH1}	Q and $\overline{WE}$ Outputs	I_{OH} = −10 mA	V_{CC} − 1.0			V
V_{OL1}	Q and $\overline{WE}$ Outputs	I_{OL} = 10 mA			0.5	V
V_{OH2}	All Outputs except Qs, $\overline{WE}$	I_{OH} = −3 mA	V_{CC} − 1.0			V
V_{OL2}	All Outputs except Qs, $\overline{WE}$	I_{OL} = 3 mA			0.5	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or GND	−10		10	μA
$I_{IL\,ML}$	$\overline{ML}$ Input Current (Low)	V_{IN} = GND			200	μA
I_{CC1}	Standby Current	CLK at 12 MHz (V_{IN} = V_{CC} or GND)		6	15	mA
I_{CC1}	Standby Current	CLK at 20 MHz (V_{IN} = V_{CC} or GND)		8	17	mA
I_{CC1}	Standby Current	CLK at 33 MHz (V_{IN} = V_{CC} or GND)		10	20	mA
I_{CC2}	Supply Current	CLK at 12 MHz (Inputs Active) (I_{LOAD} = 25 pF) (V_{IN} = V_{CC} or GND)		30	60	mA
I_{CC2}	Supply Current	CLK at 20 MHz (Inputs Active) (I_{LOAD} = 25 pF) (V_{IN} = V_{CC} or GND)		65	90	mA
I_{CC2}	Supply Current	CLK at 33 MHz (Inputs Active) (I_{LOAD} = 25 pF) (V_{IN} = V_{CC} or GND)		115	150	mA
C_{IN}*	Input Capacitance	f_{IN} at 1 MHz			10	pF

*C_{IN} is not 100% tested.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Input pulse 0V to 3V; $t_R = t_F$ = 2.5 ns. Input reference point on AC measurements is 1.5V. Output reference point is 1.5V.

Note 3: AC production testing is done at 50 pF.

13.0 AC Timing Parameters

Two speed selections are given, the DP8430V/31V/32V-20 and the DP8430V/31V/32V-33. The differences between the two parts are the maximum operating frequencies of the input CLKs and the maximum delay specifications. Low frequency applications may use the "-25" part to gain improved timing.

The AC timing parameters are grouped into sectional numbers as shown below. These numbers also refer to the timing diagrams.

1–36 Common parameters to all modes of operation

50–56 Difference parameters used to calculate;
$\overline{RAS}$ low time,
$\overline{RAS}$ precharge time,
$\overline{CAS}$ high time and
$\overline{CAS}$ low time

100–121 Common dual access parameters used for Port B accesses and inputs and outputs used only in dual accessing

200–212 Refresh parameters

300–315 Mode 0 access parameters used in both single and dual access applications

400–416 Mode 1 access parameters used in both single and dual access applications

450–455 Special Mode 1 access parameters which supersede the 400–416 parameters when dual accessing

500–506 Programming parameters

Unless otherwise stated V_{CC} = 5.0V ±10%, 0 < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:

C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Input pulse 0V to 3V; tR = tF = 2.5 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.4V for High and 0.8V for Low.

Note 3: AC Production testing is done at 50 pF.

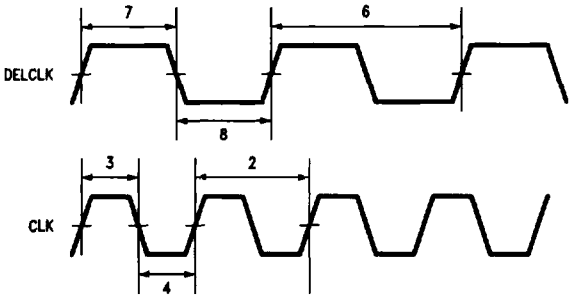

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FIGURE 34. Clock, DELCLK Timing

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:

C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or

C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Number	Symbol	Common Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
1	f_{CLK}	CLK Frequency	0	33	0	33
2	tCLKP	CLK Period	30		30	
3, 4	tCLKPW	CLK Pulse Width	12		12	
5	fDCLK	DELCLK Frequency	12	40	12	40
6	tDCLKP	DELCLK Period	25	83	25	83
7, 8	tDCLKPW	DELCLK Pulse Width	12		12	
9a	tPRASCAS0	$\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 0 ns)	30		30	
9b	tPRASCAS1	$\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 10 ns)	40		40	
9c	tPRASCAS2	($\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 0 ns)	40		40	
9d	tPRASCAS3	($\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 10 ns)	50		50	
10a	tRAH	Row Address Hold Time (tRAH = 15)	15		15	
10b	tRAH	Row Address Hold Time (tRAH = 25)	25		25	
11a	tASC	Column Address Setup Time (tASC = 0)	0		0	
11b	tASC	Column Address Setup Time (tASC = 10)	10		10	
12	tPCKRAS	CLK High to $\overline{RAS}$ Asserted following Precharge		18		22
13	tPARQRAS	$\overline{AREQ}$ Negated to $\overline{RAS}$ Negated		25		29
14	tPENCL	$\overline{ECAS}$0–3 Asserted to $\overline{CAS}$ Asserted		15		22
15	tPENCH	$\overline{ECAS}$0–3 Negated to $\overline{CAS}$ Negated		14		21
16	tPARQCAS	$\overline{AREQ}$ Negated to $\overline{CAS}$ Negated		36		43
17	tPCLKWH	CLK to $\overline{WAIT}$ Negated		25		25
18	tPCLKDL0	CLK to $\overline{DTACK}$ Asserted (Programmed as $\overline{DTACK}$ of 1/2, 1, 1½ or if $\overline{WAITIN}$ is Asserted)		23		23
19	tPEWL	$\overline{ECAS}$ Negated to $\overline{WAIT}$ Asserted during a Burst Access		29		29
20	tSECK	$\overline{ECAS}$ Asserted Setup to CLK High to Recognize the Rising Edge of CLK during a Burst Access	13		13	

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:

C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or

C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Number	Symbol	Common Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
21	tPEDL	$\overline{ECAS}$ Asserted to $\overline{DTACK}$ Asserted during a Burst Access (Programmed as $\overline{DTACK}$0)		29		29
22	tPEDH	$\overline{ECAS}$ Negated to $\overline{DTACK}$ Negated during a Burst Access		30		30
23	tSWCK	$\overline{WAITIN}$ Asserted Setup to CLK	5		5	
24	tPWINWEH	$\overline{WIN}$ Asserted to $\overline{WE}$ Asserted		18		28
25	tPWINWEL	$\overline{WIN}$ Negated to $\overline{WE}$ Negated		18		28
26	tPAQ	Row, Column Address Valid to Q0–8, 9, 10 Valid		20		29
27	tPCINCQ	COLINC Asserted to Q0–8, 9, 10 Incremented		24		33
28	tSCINEN	COLINC Asserted Setup to $\overline{ECAS}$ Asserted to Ensure tASC = 0 ns	14		16	
29a	tSARQCK1	$\overline{AREQ}$, $\overline{AREQB}$ Negated Setup to CLK High with 1 Period of Precharge	25		25	
29b	tSARQCK2	$\overline{AREQ}$, $\overline{AREQB}$ Negated Setup to CLK High with >1 Period of Precharge Programmed	11		11	
30	tPAREQDH	$\overline{AREQ}$ Negated to $\overline{DTACK}$ Negated		20		20
31	tPCKCAS	CLK High to $\overline{CAS}$ Asserted when Delayed by $\overline{WIN}$		21		28
32	tSCADEN	Column Address Setup to $\overline{ECAS}$ Asserted to Guarantee tASC = 0	10		11	
33	tWCINC	COLINC Pulse Width	10		10	
34a	tPCKCL0	CLK High to $\overline{CAS}$ Asserted following Precharge (tRAH = 15 ns, tASC = 0 ns)		65		73
34b	tPCKCL1	CLK High to $\overline{CAS}$ Asserted following Precharge (tRAH = 15 ns, tASC = 10 ns)		75		83
34c	tPCKCL2	CLK High to $\overline{CAS}$ Asserted following Precharge (tRAH = 25 ns, tASC = 0 ns)		75		83
34d	tPCKCL3	CLK High to $\overline{CAS}$ Asserted following Precharge (tRAH = 25 ns, tASC = 10 ns)		85		93
35	tCAH	Column Address Hold Time (Interleave Mode Only)	25		25	
36	tPCQR	$\overline{CAS}$ Asserted to Row Address Valid (Interleave Mode Only)		70		70

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Number	Symbol	Difference Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
50	tD1	($\overline{AREQ}$ or $\overline{AREQB}$ Negated to $\overline{RAS}$ Negated) Minus (CLK High to $\overline{RAS}$ Asserted)		9		9
51	tD2	(CLK High to Refresh $\overline{RAS}$ Negated) Minus (CLK High to $\overline{RAS}$ Asserted)		7		7
52	tD3a	($\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted (Mode 1)) Minus ($\overline{AREQ}$ Negated to $\overline{RAS}$ Negated)		4		4
53	tD3b	(CLK High to $\overline{RAS}$ Asserted (Mode 0)) Minus ($\overline{AREQ}$ Negated to $\overline{RAS}$ Negated)		2		2
54	tD4	($\overline{ECAS}$ Asserted to $\overline{CAS}$ Asserted) Minus ($\overline{ECAS}$ Negated to $\overline{CAS}$ Negated)	−5	5	−5	5
55	tD5	(CLK to Refresh $\overline{RAS}$ Asserted) Minus (CLK to Refresh $\overline{RAS}$ Negated)		4		4
56	tD6	($\overline{AREQ}$ Negated to $\overline{RAS}$ Negated) Minus ($\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted (Mode 1))		5		5

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Number	Symbol	Common Dual Access Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
100	tHCKARQB	$\overline{AREQB}$ Negated Held from CLK High	2		2	
101	tSARQBCK	$\overline{AREQB}$ Asserted Setup to CLK High	5		5	
102	tPAQBRASL	$\overline{AREQB}$ Asserted to $\overline{RAS}$ Asserted		29		33
103	tPAQBRASH	$\overline{AREQB}$ Negated to $\overline{RAS}$ Negated		24		28
105	tPCKRASG	CLK High to $\overline{RAS}$ Asserted for Pending Port B Access		37		41
106	tPAQBATKBL	$\overline{AREQB}$ Asserted to $\overline{ATACKB}$ Asserted		37		37
107	tPCKATKB	CLK High to $\overline{ATACKB}$ Asserted for Pending Access		45		45
108	tPCKGH	CLK High to GRANTB Asserted		28		28
109	tPCKGL	CLK High to GRANTB Negated		26		26
110	tSADDCKG	Row Address Setup to CLK High That Asserts $\overline{RAS}$ following a GRANTB Change to Ensure tASR = 0 ns for Port B	7		11	
111	tSLOCKCK	$\overline{LOCK}$ Asserted Setup to CLK Low to Lock Current Port	4		4	
112	tPAQATKBH	$\overline{AREQ}$ Negated to $\overline{ATACKB}$ Negated		16		16
113	tPAQBCASH	$\overline{AREQB}$ Negated to $\overline{CAS}$ Negated		38		45
114	tSADAQB	Address Valid Setup to $\overline{AREQB}$ Asserted	6		10	
116	tHCKARQG	$\overline{AREQ}$ Negated Held from CLK High	5		5	
117	tWAQB	$\overline{AREQB}$ High Pulse Width to Guarantee tASR = 0 ns	17		19	
118a	tPAQBCAS0	$\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 0 ns)		79		86
118b	tPAQBCAS1	$\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 10 ns)		89		96
118c	tPAQBCAS2	$\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 0 ns)		89		96
118d	tPAQBCAS3	$\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 10 ns)		99		106
120a	tPCKCASG0	CLK High to $\overline{CAS}$ Asserted for Pending Port B Access (tRAH = 15 ns, tASC = 0 ns)		84		91
120b	tPCKCASG1	CLK High to $\overline{CAS}$ Asserted for Pending Port B Access (tRAH = 15 ns, tASC = 10 ns)		94		101
120c	tPCKCASG2	CLK High to $\overline{CAS}$ Asserted for Pending Port B Access (tRAH = 25 ns, tASC = 0 ns)		94		101
120d	tPCKCASG3	CLK High to $\overline{CAS}$ Asserted for Pending Port B Access (tRAH = 25 ns, tASC = 10 ns)		104		111
121	tSBADDCKG	Bank Address Valid Setup to CLK High That Starts $\overline{RAS}$ for Pending Port B Access	5		5	

13.0 AC Timing Parameters (Continued)

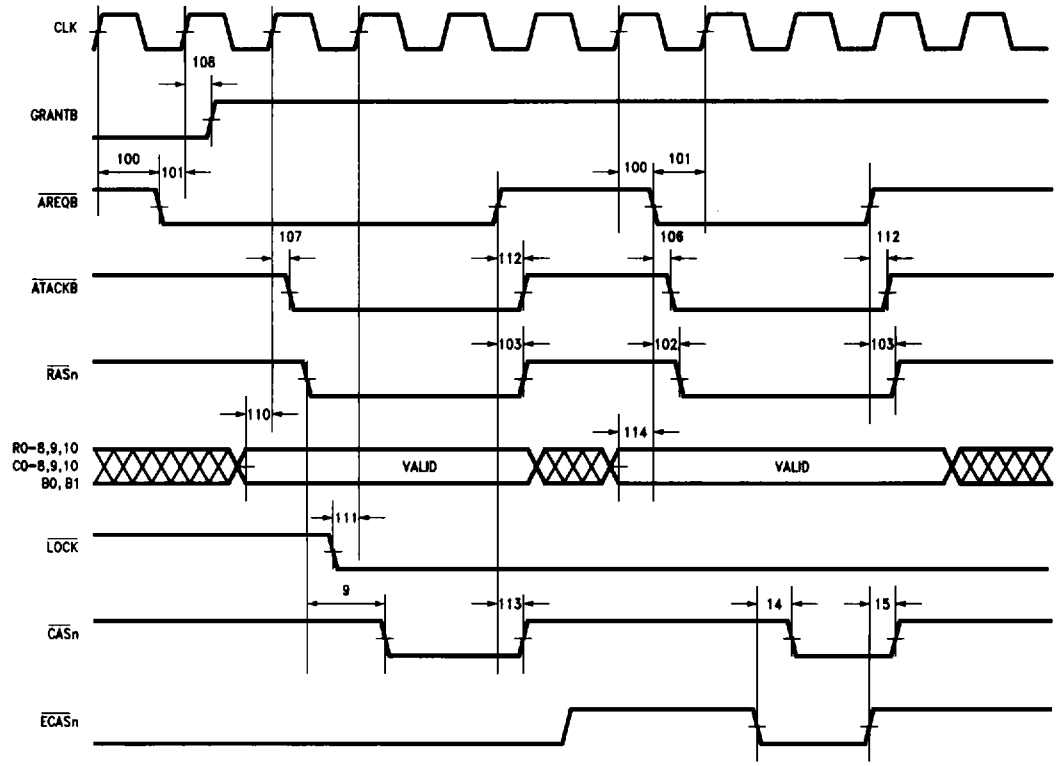

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FIGURE 35. 100: Dual Access Port B

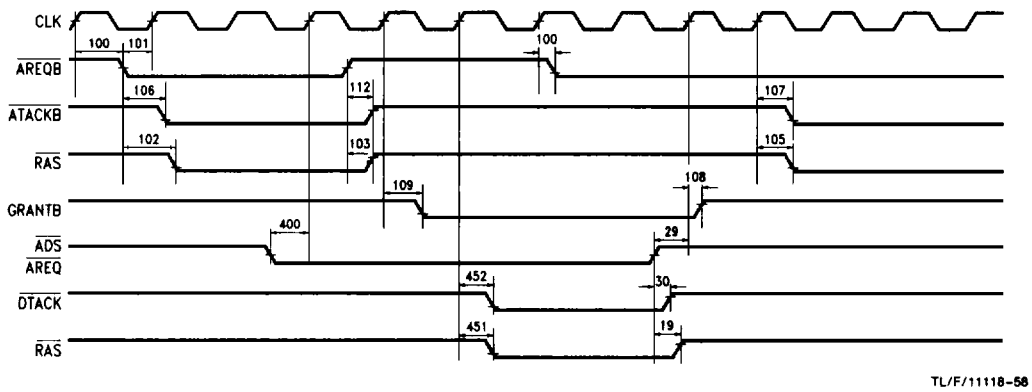

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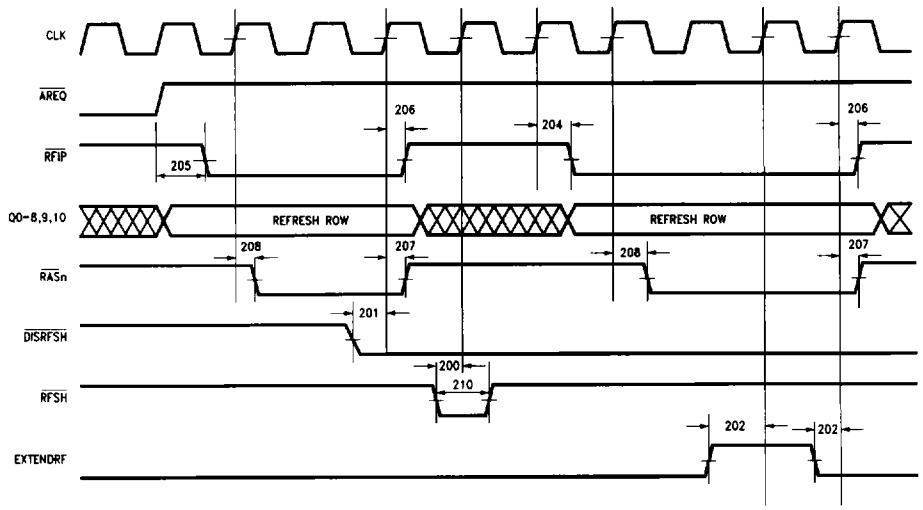
FIGURE 36. 100: Port A and Port B Dual Access

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Number	Symbol	Refresh Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
200	tSRFCK	$\overline{RFSH}$ Asserted Setup to CLK High	16		16	
201	tSDRFCK	$\overline{DISRFSH}$ Asserted Setup to CLK High	16		16	
202	tSXRFCK	EXTENDRF Setup to CLK High	8		8	
204	tPCKRFL	CLK High to $\overline{RFIP}$ Asserted		26		26
205	tPARQRF	$\overline{AREQ}$ Negated to $\overline{RFIP}$ Asserted		38		38
206	tPCKRFH	CLK High to $\overline{RFIP}$ Negated		41		41
207	tPCKRFRASH	CLK High to Refresh $\overline{RAS}$ Negated		26		30
208	tPCKRFRASL	CLK High to Refresh $\overline{RAS}$ Asserted		20		24
209a	tPCKCL0	CLK High to $\overline{CAS}$ Asserted during Error Scrubbing (t_{RAH} = 15 ns, t_{ASC} = 0 ns)		64		73
209b	tPCKCL1	CLK High to $\overline{CAS}$ Asserted during Error Scrubbing (t_{RAH} = 15 ns, t_{ASC} = 10 ns)		74		83
209c	tPCKCL2	CLK High to $\overline{CAS}$ Asserted during Error Scrubbing (t_{RAH} = 25 ns, t_{ASC} = 0 ns)		74		83
209d	tPCKCL3	CLK High to $\overline{CAS}$ Asserted during Error Scrubbing (t_{RAH} = 25 ns, t_{ASC} = 10 ns)		85		94
210	tWRFSH	$\overline{RFSH}$ Pulse Width	9		9	
211	tPCKRQL	CLK High to $\overline{RFRQ}$ Asserted		22		22
212	tPCKRQH	CLK High to $\overline{RFRQ}$ Negated		22		22



TL/F/11118–59

FIGURE 37. 200: Refresh Timing

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Number	Symbol	Mode 0 Access Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
300	tSCSCK	$\overline{CS}$ Asserted to CLK High	8		8	
301a	tSALECKNL	ALE Asserted Setup to CLK High Not Using On-Chip Latches or if Using On-Chip Latches and B0, B1, Are Constant, Only 1 Bank	11		11	
301b	tSALECKL	ALE Asserted Setup to CLK High, if Using On-Chip Latches if B0, B1 Can Change, More Than One Bank	20		20	
302	tWALE	ALE Pulse Width	10		10	
303	tSBADDCK	Bank Address Valid Setup to CLK High	10		10	
304	tSADDCK	Row, Column Valid Setup to CLK High to Guarantee tASR = 0 ns	6		10	
305	tHASRCB	Row, Column, Bank Address Held from ALE Negated (Using On-Chip Latches)	6		6	
306	tSRCBAS	Row, Column, Bank Address Setup to ALE Negated (Using On-Chip Latches)	1		1	
307	tPCKRL	CLK High to $\overline{RAS}$ Asserted		19		23
308a	tPCKCL0	CLK High to $\overline{CAS}$ Asserted (t_{RAH} = 15 ns, t_{ASC} = 0 ns)		65		72
308b	tPCKCL1	CLK High to $\overline{CAS}$ Asserted (t_{RAH} = 15 ns, t_{ASC} = 10 ns)		75		82
308c	tPCKCL2	CLK High to $\overline{CAS}$ Asserted (t_{RAH} = 25 ns, t_{ASC} = 0 ns)		75		82
308d	tPCKCL3	CLK High to $\overline{CAS}$ Asserted (t_{RAH} = 25 ns, t_{ASC} = 10 ns)		85		92
309	tHCKALE	ALE Negated Hold from CLK High	0		0	
310	tSWINCK	$\overline{WIN}$ Asserted Setup to CLK High to Guarantee $\overline{CAS}$ is Delayed	−16		−16	
311	tPCSWL	$\overline{CS}$ Asserted to $\overline{WAIT}$ Asserted		20		20
312	tPCSWH	$\overline{CS}$ Negated to $\overline{WAIT}$ Negated		20		20
313	tPCLKDL1	CLK High to $\overline{DTACK}$ Asserted (Programmed as $\overline{DTACK0}$)		27		27
314	tPALEWL	ALE Asserted to $\overline{WAIT}$ Asserted ($\overline{CS}$ is Already Asserted)		21		21
315		$\overline{AREQ}$ Negated to CLK High That Starts Access $\overline{RAS}$ to Guarantee tASR = 0 ns (Non-Interleaved Mode Only)	27		31	
316	tPCKCV0	CLK High to Column Address Valid (t_{RAH} = 15 ns, t_{ASC} = 0 ns)		58		67
317	tPCKCV1	CLK High to Column Address Valid (t_{RAH} = 25 ns, t_{ASC} = 0 ns)		68		75

13.0 AC Timing Parameters (Continued)

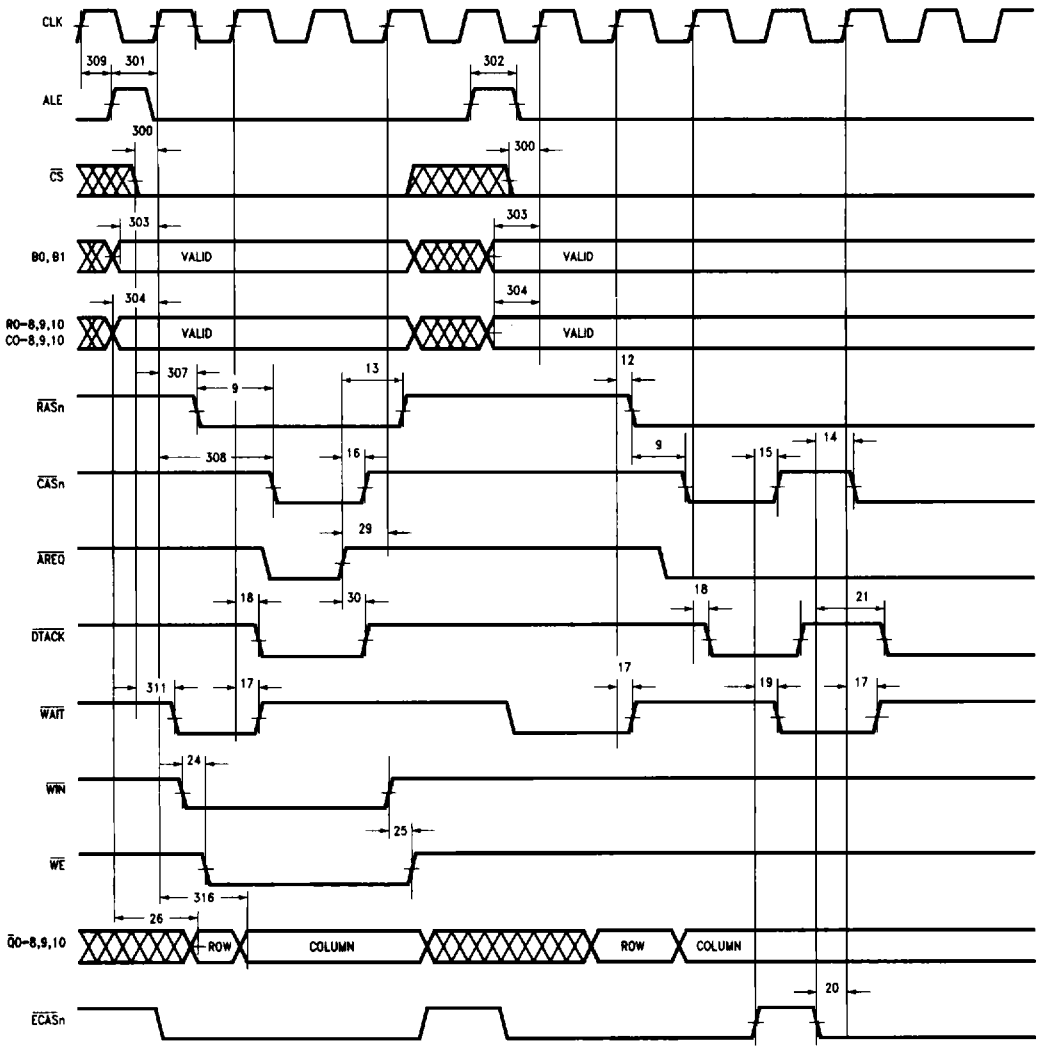


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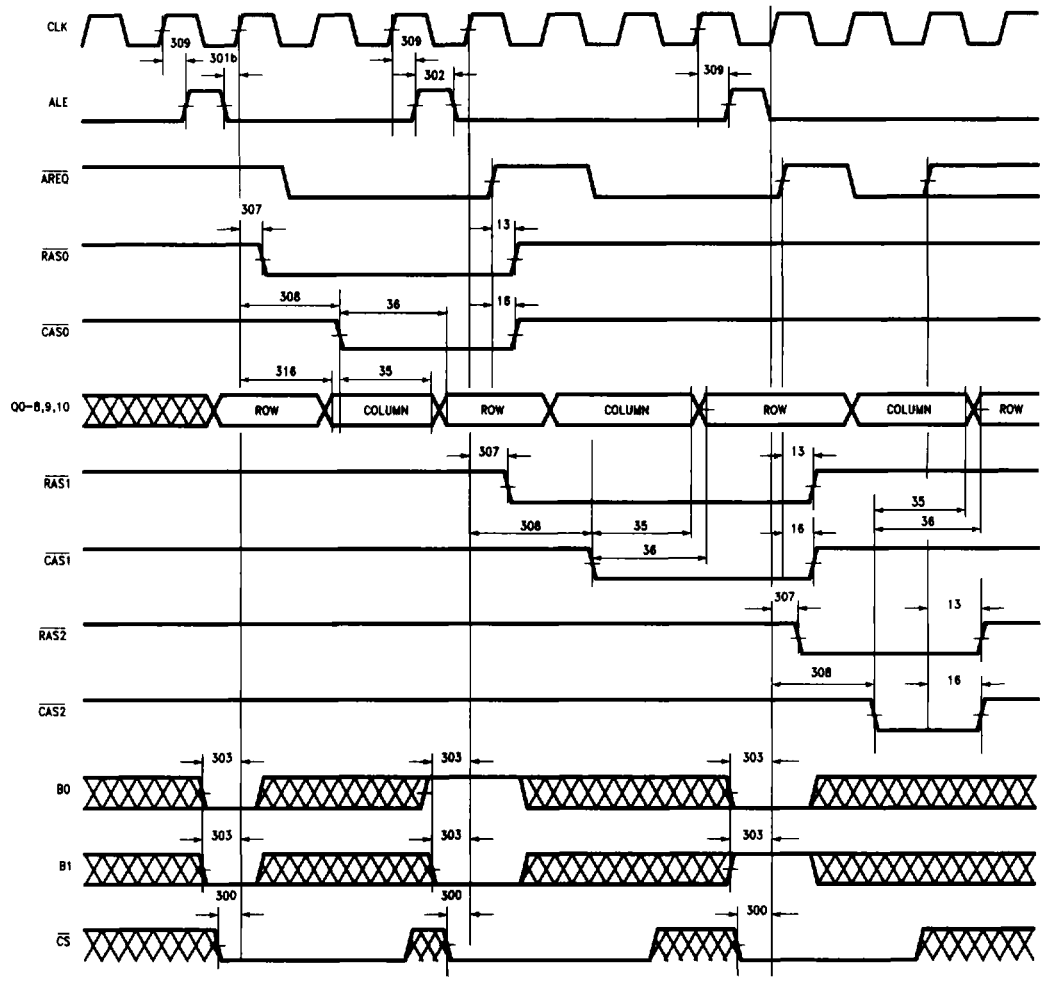
FIGURE 38. 300: Mode 0 Timing

13.0 AC Timing Parameters (Continued)



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(Programmed as C4 = 1, C5 = 1, C6 = 1)

FIGURE 39. 300: Mode 0 Interleaving

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Number	Symbol	Mode 1 Access Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
400a	tSADSCK1	$\overline{ADS}$ Asserted Setup to CLK High	9		9	
400b	tSADSCKW	$\overline{ADS}$ Asserted Setup to CLK (to Guarantee Correct $\overline{WAIT}$ or $\overline{DTACK}$ Output; Doesn't Apply for $\overline{DTACK}$0)	19		19	
401	tSCSADS	$\overline{CS}$ Setup to $\overline{ADS}$ Asserted	4		4	
402	tPADSRL	$\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted		20		24
403a	tPADSCL0	$\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 0 ns)		70		77
403b	tPADSCL1	$\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 10 ns)		80		87
403c	tPADSCL2	$\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 0 ns)		80		87
403d	tPADSCL3	$\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 10 ns)		90		97
404	tSADDADS	Row Address Valid Setup to $\overline{ADS}$ Asserted to Guarantee tASR = 0 ns	6		11	
405	tHCKADS	$\overline{ADS}$ Negated Held from CLK High	0		0	
406	tSWADS	$\overline{WAITIN}$ Asserted Setup to $\overline{ADS}$ Asserted to Guarantee $\overline{DTACK}$0 Is Delayed	0		0	
407	tSBADAS	Bank Address Setup to $\overline{ADS}$ Asserted	6		6	
408	tHASRCB	Row, Column, Bank Address Held from $\overline{ADS}$ Asserted (Using On-Chip Latches)	6		6	
409	tSRCBAS	Row, Column, Bank Address Setup to $\overline{ADS}$ Asserted (Using On-Chip Latches)	1		1	
410	tWADSH	$\overline{ADS}$ Negated Pulse Width	12		17	
411	tPADSD	$\overline{ADS}$ Asserted to $\overline{DTACK}$ Asserted (Programmed as $\overline{DTACK}$0)		29		29
412	tSWINADS	$\overline{WIN}$ Asserted Setup to $\overline{ADS}$ Asserted (to Guarantee $\overline{CAS}$ Delayed during Writes Accesses)	−10		−10	
413	tPADSWL0	$\overline{ADS}$ Asserted to $\overline{WAIT}$ Asserted (Programmed as $\overline{WAIT}$0, Delayed Access)		19		19
414	tPADSWL1	$\overline{ADS}$ Asserted to $\overline{WAIT}$ Asserted (Programmed $\overline{WAIT}$ 1/2 or 1)		22		22
415	tPCLKDL1	CLK High to $\overline{DTACK}$ Asserted (Programmed as $\overline{DTACK}$0, Delayed Access)		27		27
416		$\overline{AREQ}$ Negated to $\overline{ADS}$ Asserted to Guarantee tASR = 0 ns (Non Interleaved Mode Only)	27		29	
417	tPADSCV0	$\overline{ADS}$ Asserted to Column Address Valid (t_{RAH} = 15 ns, t_{ASC} = 0 ns)		51		60

13.0 AC Timing Parameters (Continued)

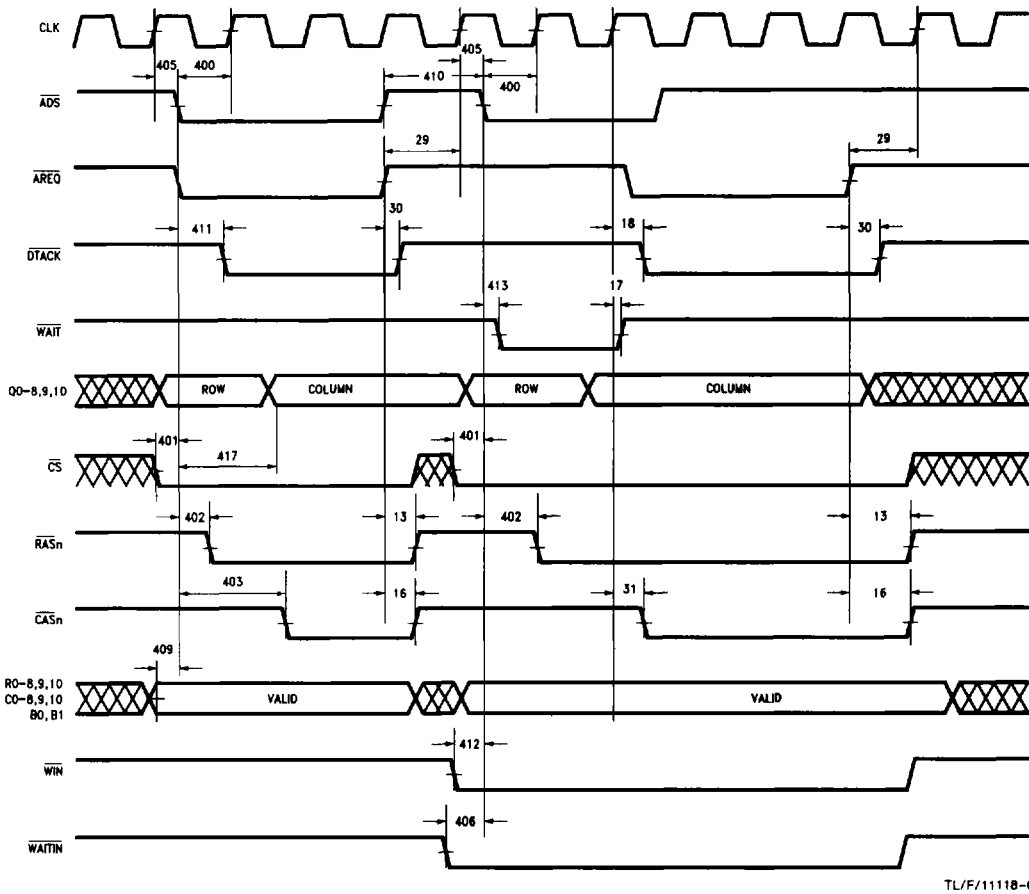

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FIGURE 40. 400: Mode 1 Timing

13.0 AC Timing Parameters (Continued)

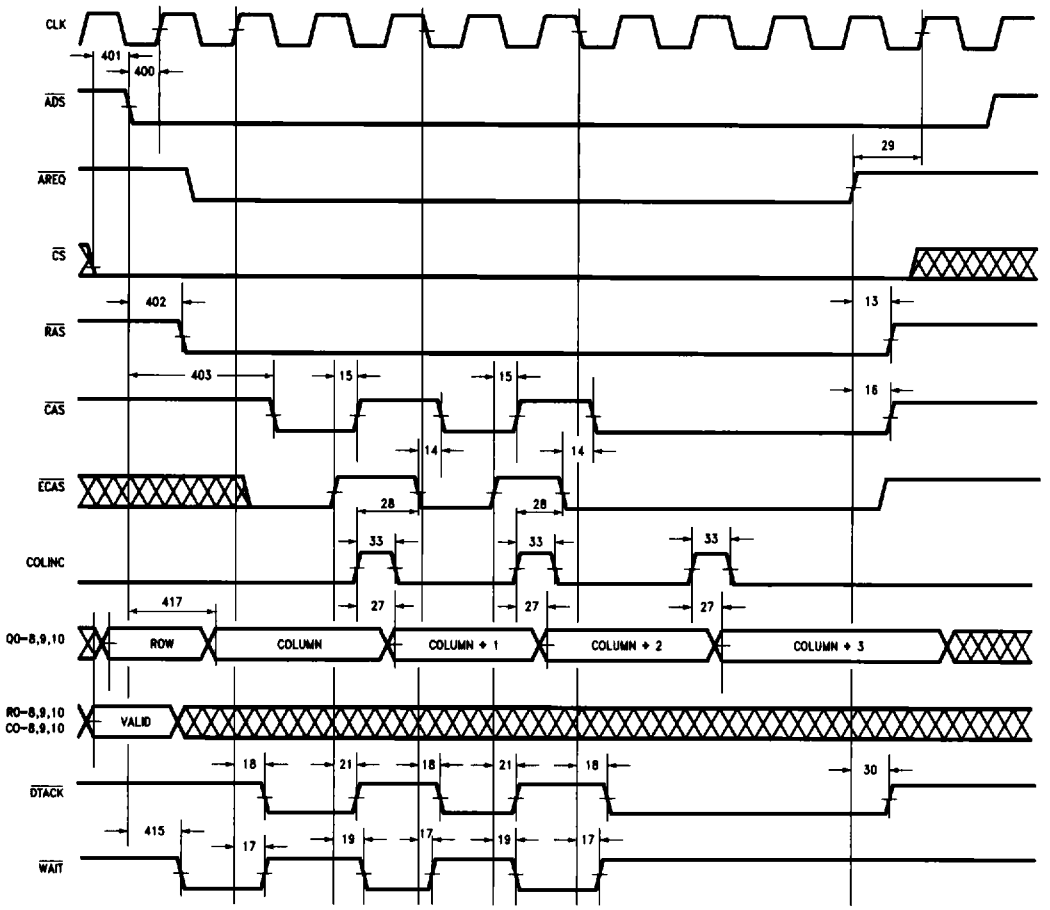

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FIGURE 41. 400: COLINC Page/Static Column Access Timing

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

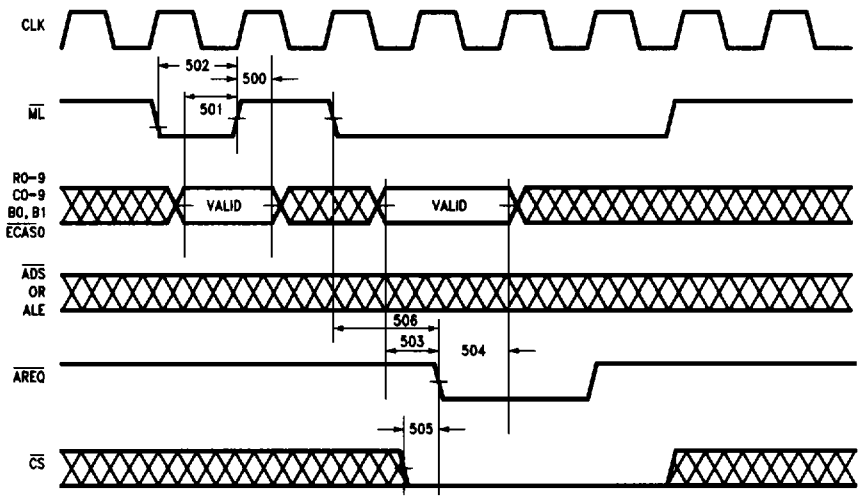
Number	Symbol	Mode 1 Dual Access Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
450	tSADDCKG	Row Address Setup to CLK High That Asserts $\overline{RAS}$ following a GRANTB Port Change to Ensure tASR = 0 ns	10		12	
451	tPCKRASG	CLK High to $\overline{RAS}$ Asserted for Pending Access		30		34
452	tPCLKDL2	CLK to $\overline{DTACK}$ Asserted for Delayed Accesses (Programmed as $\overline{DTACK}$0)		37		37
453a	tPCKCASG0	CLK High to $\overline{CAS}$ Asserted for Pending Access (t_{RAH} = 15 ns, t_{ASC} = 0 ns)		81		88
453b	tPCKCASG1	CLK High to $\overline{CAS}$ Asserted for Pending Access (t_{RAH} = 15 ns, t_{ASC} = 10 ns)		91		98
453c	tPCKCASG2	CLK High to $\overline{CAS}$ Asserted for Pending Access (t_{RAH} = 25 ns, t_{ASC} = 0 ns)		91		98
453d	tPCKCASG3	CLK High to $\overline{CAS}$ Asserted for Pending Access (t_{RAH} = 25 ns, t_{ASC} = 10 ns)		101		108
454	tSBADDCKG	Bank Address Valid Setup to CLK High that Asserts $\overline{RAS}$ for Pending Access	3		3	
455	tSADSCK0	$\overline{ADS}$ Asserted Setup to CLK High	8		8	

13.0 AC Timing Parameters (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 DRAMs per bank, including trace capacitance (Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, 10 and $\overline{WE}$; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, 10 and $\overline{WE}$.

Number	Symbol	Programming Parameter Description	DP8430V/31V/32V-33			
			C_L		C_H	
			Min	Max	Min	Max
500	tHMLADD	Mode Address Held from $\overline{ML}$ Negated	6		6	
501	tSADDML	Mode Address Setup to $\overline{ML}$ Negated	6		6	
502	tWML	$\overline{ML}$ Pulse Width	12		12	
503	tSADAQML	Mode Address Setup to $\overline{AREQ}$ Asserted	0		0	
504	tHADAQML	Mode Address Held from $\overline{AREQ}$ Asserted	30		30	
505	tSCSARQ	$\overline{CS}$ Asserted Setup to $\overline{AREQ}$ Asserted	6		6	
506	tSMLARQ	$\overline{ML}$ Asserted Setup to $\overline{AREQ}$ Asserted	6		6	



TL/F/11118–64

FIGURE 42. 500: Programming

14.0 DP8430V/31V/32V User Hints

1. All inputs to the DP8430V/31V/32V should be tied high, low or the output of some other device.

   Note: One signal is active high. COLINC (EXTNDRF) should be tied low to disable.

2. Each ground on the DP8430V/31V/32V must be decoupled to the closest on-chip supply (V_{CC}) with 0.1 μF ceramic capacitor. This is necessary because these grounds are kept separate inside the DP8430V/31V/32V. The decoupling capacitors should be placed as close as possible with short leads to the ground and supply pins of the DP8430V/31V/32V.
3. The output called "CAP" should have a 0.1 μF capacitor to ground.
4. The DP8430V/31V/32V has 20Ω series damping resistors built into the output drivers of $\overline{RAS}$, $\overline{CAS}$, address and $\overline{WE}$/$\overline{RFRQ}$. Space should be provided for external damping resistors on the printed circuit board (or wire-wrap board) because they may be needed. The value of these damping resistors (if needed) will vary depending upon the output, the capacitance of the load, and the characteristics of the trace as well as the routing of the trace. The value of the damping resistor also may vary between the wire-wrap board and the printed circuit board. To determine the value of the series damping resistor it is recommended to use an oscilloscope and look at the furthest DRAM from the DP8430V/31V/32V. The undershoot of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and the addresses should be kept to less than 0.5V below ground by varying the value of the damping resistor. The damping resistors should be placed as close as possible with short leads to the driver outputs of the DP8430V/31V/32V.
5. The circuit board must have a good V_{CC} and ground plane connection. If the board is wire-wrapped, the V_{CC} and ground pins of the DP8430V/31V/32V, the DRAM associated logic and buffer circuitry must be soldered to the V_{CC} and ground planes.
6. The traces from the DP8430V/31V/32V to the DRAM should be as short as possible.
7. Parameter Changes due to Loading

   All A.C. parameters are specified with the equivalent load capacitances, including traces, of 64 DRAMs organized as 4 banks of 18 DRAMs each. Maximums are based on worst-case conditions. If an output load changes then the A.C. timing parameters associated with that particular output must be changed. For example, if we changed our output load to

   C = 250 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3

   C = 760 pF loads on Q0–9 and $\overline{WE}$

   we would have to modify some parameters (not all calculated here)

   $308a clock to $\overline{CAS}$ asserted

   (t_{RAH} = 15 ns, t_{ASC} = 0 ns)

   A ratio can be used to figure out the timing change per change in capacitance for a particular parameter by using the specifications and capacitances from heavy and light load timing.

$$\text{Ratio} = \frac{\$308a\ \text{w/Heavy Load} - \$308a\ \text{w/Light Load}}{C_H(\overline{CAS}) - C_L(\overline{CAS})}$$

$$= \frac{79\ \text{ns} - 72\ \text{ns}}{125\ \text{pF} - 50\ \text{pF}} = \frac{7\ \text{ns}}{75\ \text{pF}}$$

$$\$308a\ (\text{actual}) = (\text{capacitance difference} \times \text{ratio}) + \$308a\ (\text{specified})$$

$$= (250\ \text{pF} - 125\ \text{pF})\frac{7\ \text{ns}}{75\ \text{pF}} + 79\ \text{ns}$$

$$= 11.7\ \text{ns} + 79\ \text{ns}$$

$$= 90.7\ \text{ns @ 250 pF load}$$