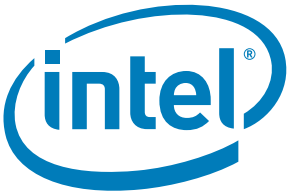
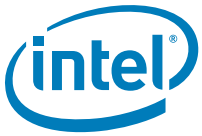


Mobile Intel® 945 Express Chipset Family

Datasheet

June 2008

Document Number: 309219-006



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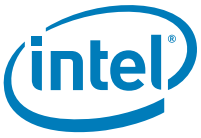

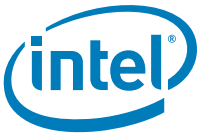

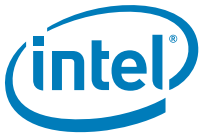

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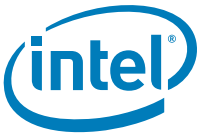

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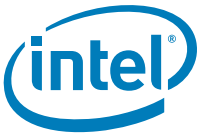

Revision History

Revision Number	Description	Revision Date
-001	Initial release	January 2006
-002	• Added Information on Mobile Intel® 945GMS and 940GML Express Chipsets. and made some minor edits • Removed support for DFGT and HW VLD • In Chapter 1 — in Section 1.1.2 - included support for 4-GB physical memory @ 667 MHz — Updated CPU support information for all (G)MCH's • In Chapter 10 — Updated Section Section 10.5.4.2 — Updated ODT logic in Section Section 10.2.7 • In Chapter 11 — Corrected title of Table 50 — Changed VCCASM to VCCAux under Note 1 of Table 53 and updated filtering requirements	April 2006
-003	• Added information on Mobile Intel® 943GML Express Chipset • Updated Processor Support	November 2006
-004	• Added information on Ultra Mobile Intel® 945GU Express Chipset • Added Spec Update, Revision -007 information	April 2007
-005	• Added information on Mobile Intel® 945GME Express Chipset • Added Section 1.1.10 • Updated Device Identification Information in Table 3 and Section 5.1.2 • Updated Device Identification Information in Table 10 and Section 7.1.2 • Updated Device Identification Information in Table 12 and Section 8.1.2	July 2007
-006	• Chapter 1: Added bullet information on Mobile Intel® 945GSE Express Chipset • Section 1.5: New section on Mobile Intel 945GSE Express Chipset	June 2008

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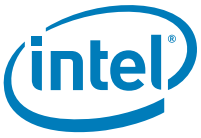
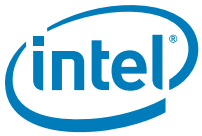




1 Introduction

This document contains specifications for the following chipsets:

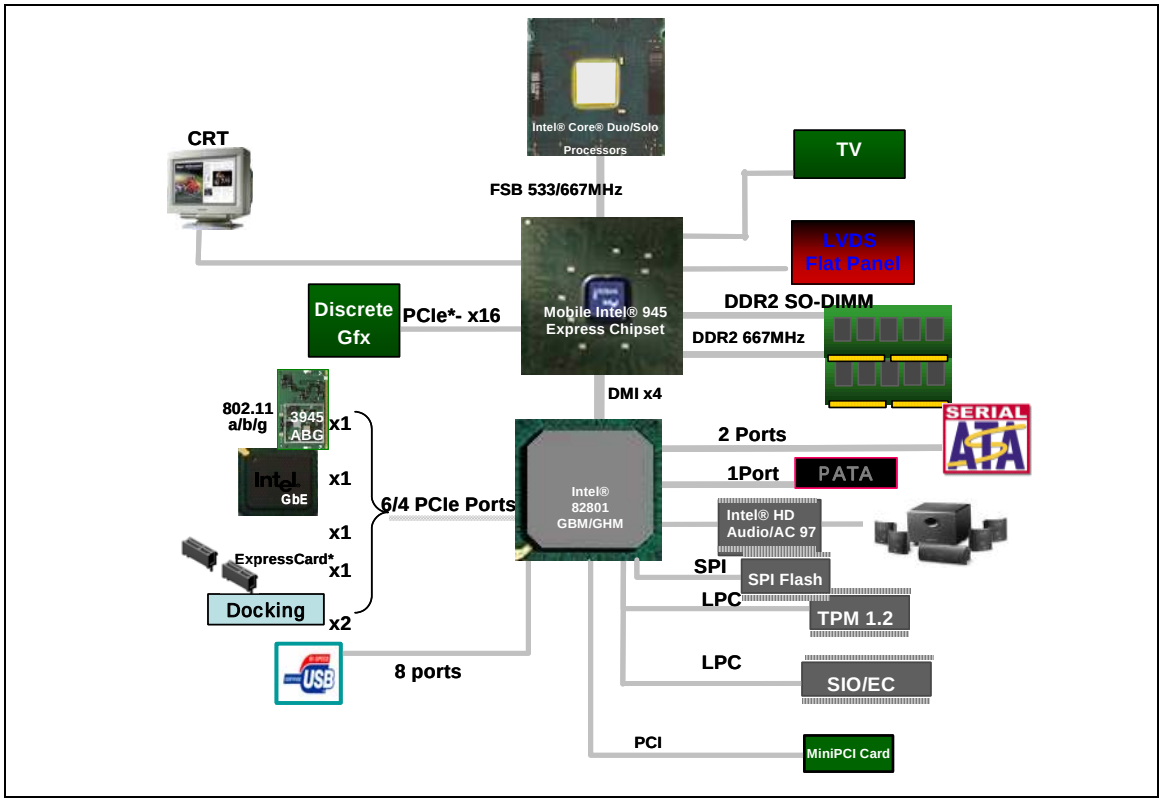
- The Mobile Intel® 945 Express Chipset family for the Intel Centrino Duo Technology.
- The Intel 945GT Express Chipset is designed for use in desktop designs.
- The Intel® 945GU Express Chipset is designed for use with the Intel Processor A100 and A110 in the Intel ultra mobile platform designs.
- The Mobile Intel® 945GSE Express Chipset is designed for use with the Intel® Atom™ Processor N270 in the Netbook Platform 2008 designs.

The Mobile Intel 945GM/945GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets come with the Generation 3.5 Intel Integrated Graphics Engine, and the Intel® Graphics Media Accelerator 950 (Intel® GMA 950), providing enhanced graphics support over the previous generation Graphics and Memory Controller Hubs ((G)MCH's).

The (G)MCH manages the flow of information between the four following primary interfaces:

- FSB
- System Memory Interface
- Graphics Interface
- DMI

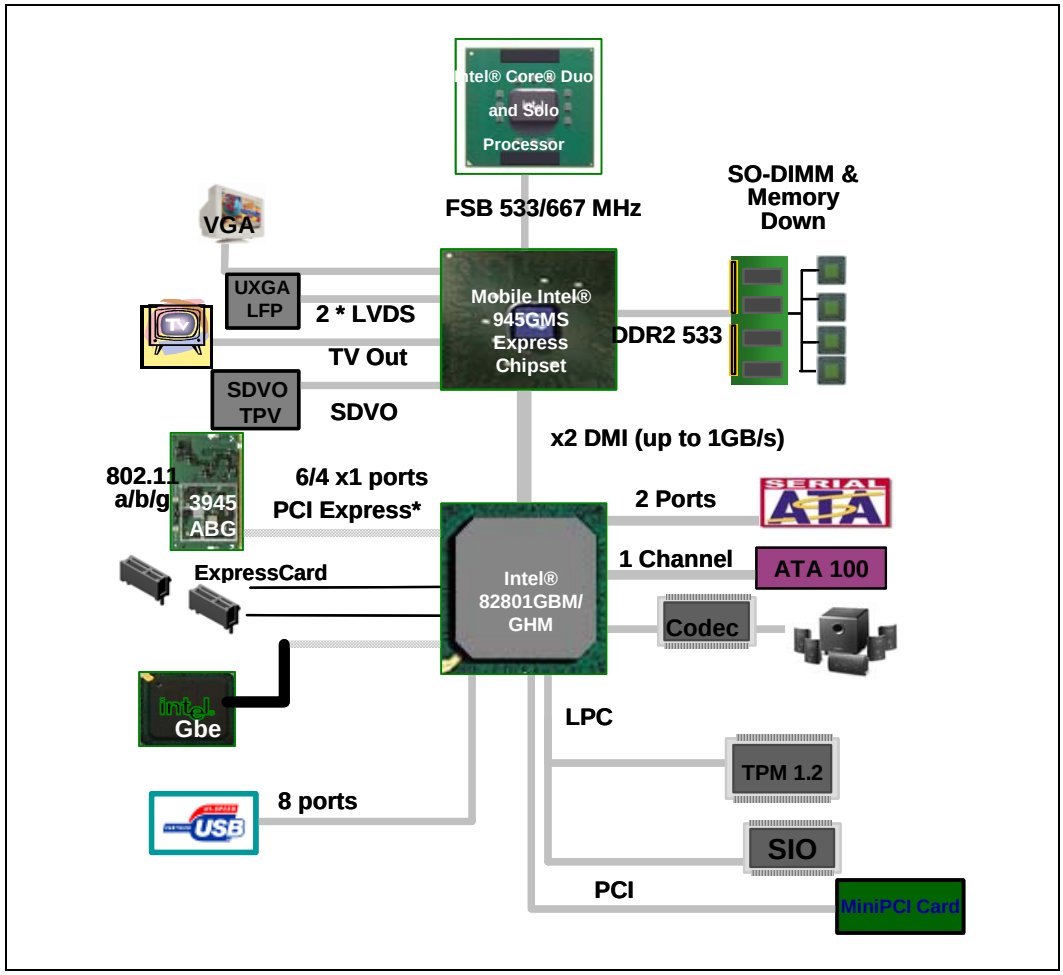
Figure 1. Intel® Centrino® Duo Technology with Mobile Intel® 945 Express Chipset Family (G)MCH



The (G)MCH can also be enabled to support external graphics, using the x16 PCI Express* graphics attach port. When external graphics is enabled, the internal graphics ports are inactive. However, SDVO operation concurrent with PCIe* x1 link is supported.

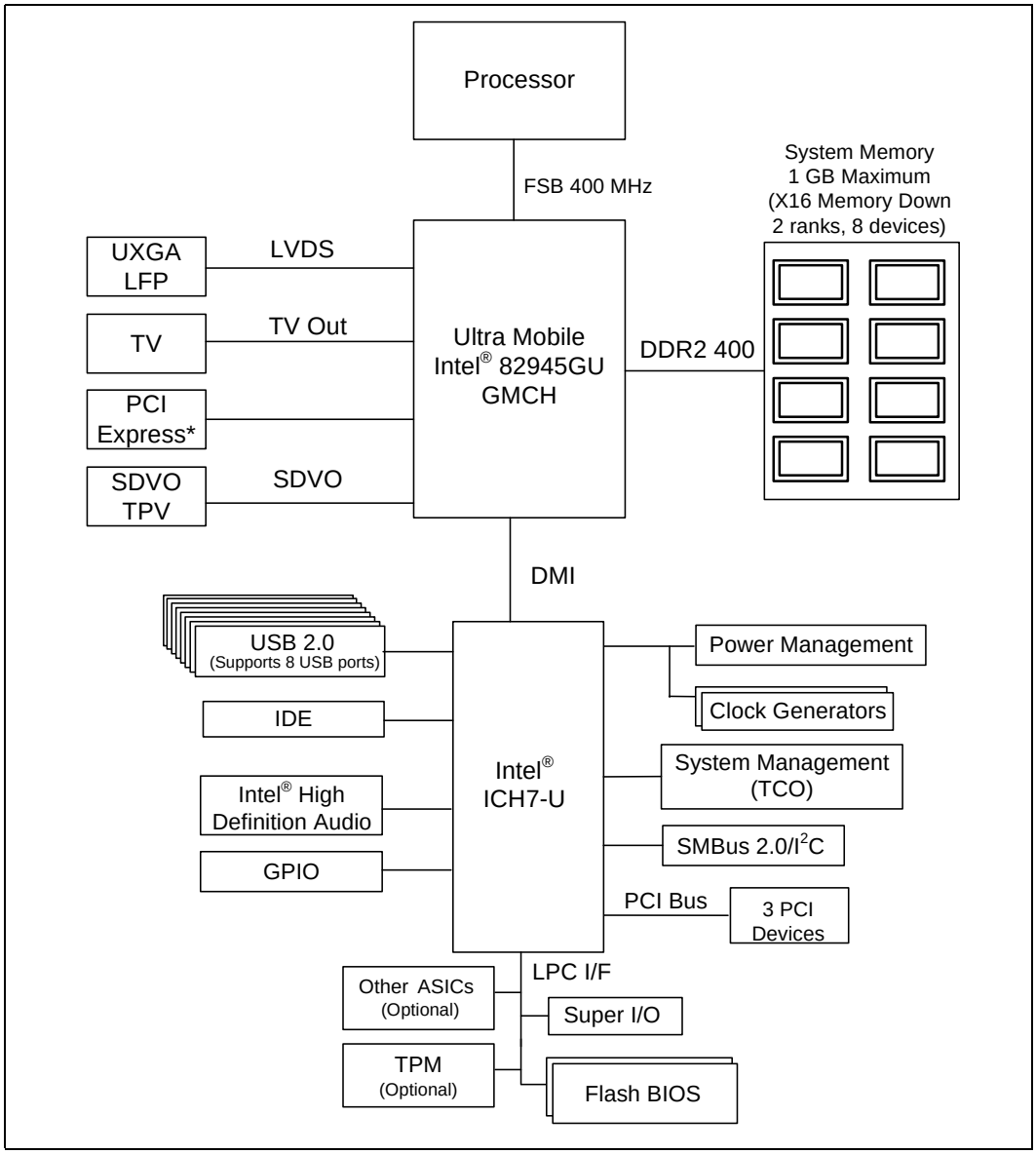
Note: The above diagram is only indicative of the (G)MCH capabilities. Please refer to the feature-sets in the following sections for details on the processor and ICH variants supported by each (G)MCH SKU.

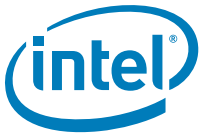
Figure 2. Intel Centrino Duo Technology and Intel Centrino Technology with Mobile Intel® 945GMS Express Chipset



Note: The Mobile Intel 945GMS/GSE Express Chipset may have notes in BROWN font throughout this document. This is to point out differences which are relative to these two chipsets only.

Figure 3. Ultra Mobile Intel® 945GU Express Chipset Example System Diagram





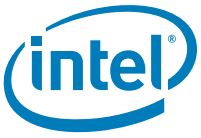
1.1 Mobile Intel® 945GM/GME Express Chipset Feature Support

1.1.1 Processor Support

- Intel® Core™2 Duo mobile processor, Intel® Core™2 Duo mobile processor LV (Low Voltage), Intel® Core™2 Duo mobile processor ULV (Ultra Low Voltage)
- Intel® Core™ Duo processor, Intel® Core™ Duo processor LV (Low Voltage), Intel® Core™ Duo processor ULV (Ultra Low Voltage)
- Intel® Core™ Solo processor ULV
- Intel® Celeron® M processor (Intel Core processor based), Celeron M processor ULV
- 533-MHz and 667-MHz front side bus (FSB) support
- Source synchronous double-pumped (2x) Address
- Source synchronous quad-pumped (4x) Data
- Other key features are:
  - Support for DBI (Data Bus Inversion)
  - Support for MSI (Message Signaled Interrupt)
  - 32-bit interface to address up to 4 GB of memory
  - A 12-deep In-Order Queue to pipeline FSB commands
- AGTL+ bus driver with integrated AGTL termination resistors

1.1.2 System Memory Support

- Supports single-/dual-channel DDR2 SDRAM
- Maximum Memory supported: up to 4 GB at 400, 533 and 667 MHz
- 64-bit wide per channel
- Three Memory Channel Configurations supported:
  - Single-Channel
  - Dual-Channel Symmetric
  - Dual-Channel Asymmetric
- One SO-DIMM connector per channel
- 256-Mb, 512-Mb and 1-Gb memory technologies supported
- Support for x8 and x16 devices
- Support for DDR2 On-Die Termination (ODT)
- Enhanced Addressing support (XOR and Swap)
- Intel® Rapid Memory Power Management (Intel® RMPM)
- Dynamic row power-down
- No support for Fast Chip Select mode
- Support for 2N timings only
- Supports Partial Writes to memory using Data Mask signals (DM)

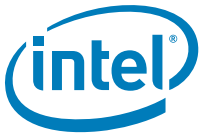


1.1.3 Discrete Graphics using PCI Express*

- One 16-lane (x16) PCI Express port for external PCI Express-based graphics card.
- Compliant to the current *PCI Express* Base Specification* base PCI Express frequency of 2.5 GHz only.
- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8/10 encoding used to transmit data across this interface.
- Maximum theoretical realized bandwidth on interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16.
- 100-MHz differential reference clock (shared by PCI Express Gfx and DMI)
- STP-AGP/AGP_BUSY Protocol equivalent for PCI Express-based attach is via credit-based PCI Express mechanism.
- PCI Express power management support
- L0s, L1, L2/L3 Ready, L3
- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., conventional PCI 2.3 configuration space as a PCI-to-PCI bridge).
- PCI Express Extended Configuration Space. The first 256 bytes of configuration space aliases directly to the PCI compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express Enhanced Addressing Mechanism. Accessing the device configuration space in a flat memory mapped fashion.
- Automatic discovery, negotiation, and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI-X Relaxed ordering)
- Support for peer segment destination write traffic (no peer-to-peer read traffic) in Virtual Channel 0 only.
- APIC and MSI interrupt messaging support. Will send Intel-defined “End Of Interrupt” broadcast message when initiated by the CPU.
- Downstream Lock Cycles (including Split Locks)
- Automatic clock extraction and phase correction at the receiver.

1.1.4 Internal Graphics

- Intel® Gen 3.5 Integrated Graphics Engine
- 250-MHz core render clock and 200 MHz core display clock at 1.05-V core voltage
- Supports TV-Out, LVDS, CRT and SDVO
- Dynamic Video Memory Technology (DVMT 3.0)
- Intel® Display Power Saving Technology 2.0 (Intel® DPST 2.0)
- Intel® Smart 2D Display Technology (Intel® S2DDT)
- Intel® Automatic Display Brightness
- Video Capture via x1 concurrent PCIe port
- Concurrent operation of x1 PCIe and SDVO
- 4x pixel rate HWMC
- Microsoft DirectX* 9.1 operating system
- Intermediate Z in Classic Rendering
- Internal Graphics Display Device States: D0, D1, D3
- Graphics Display Adapter States: D0, D3.



1.1.4.1 Analog CRT

- Integrated 400-MHz RAMDAC
- Analog Monitor Support up to QXGA
- Support for CRT Hot Plug

1.1.4.2 LVDS Interface

- Panel support up to UXGA (1600 x 1200)
- 25-MHz to 112-MHz single-/dual-channel; @18 bpp
  - TFT panel type supported
- Pixel Dithering for 18-bit TFT panel to emulate 24-bpp true color displays
- Panel Fitting. Panning, and Center Mode Supported
- CPIS 1.5 compliant
- Spread spectrum clocking supported
- Panel Power Sequencing support
- Integrated PWM interface for LCD backlight inverter control

1.1.4.3 TV-Out

- Three integrated 10-bit DACS
- MacroVision* support (not supported on Mobile Intel 945GME Express Chipset)
- Overscaling
- NTSC/PAL
- Component, S-Video and Composite Output interfaces
- HDTV support
  - 480p/720p/1080i/1080p

1.1.4.4 SDVO Ports

- Concurrent operation of x1 PCIe with SDVO
- Two SDVO Ports supported
  - SDVO is muxed onto the PCIe pins
  - DVI 1.0 Support for External Digital Monitor
  - Downstream HDCP Support but no Upstream HDCP Support
  - TV/HDTV/DVD Support
  - Display Hot Plug Support
- Supports appropriate external SDVO components (DVI, LVDS, TV-Out)
  - I^2C channel provided for control

1.1.5 ICH Support

- Support for both Intel® 82801GHM and Intel® 82801GBM

1.1.6 DMI

- Chip-to-chip interface between (G)MCH and ICH
- Configurable as x2 or x4 DMI lanes
- DMI lane reversal support
- 2 GB/s (1 GB/s each direction) point-to-point interface to Intel 82801GBM
- 32-bit downstream address
- Direct Media Interface asynchronously coupled to core
- Supports two Virtual Channels for traffic class performance differentiation
- Supports both snooped and non-snooped upstream requests
- Supports isochronous non-snooped traffic
- Supports legacy snooped isochronous traffic
- Supports the following traffic types to or from Intel 82801GBM
  - Peer write traffic between DMI and PCI Express Graphics port
  - DMI-to-DRAM
  - DMI-to-CPU (FSB Interrupts or MSIs only).
  - CPU-to-DMI
  - Messaging in both directions, including Intel Vendor-specific messages
  - Supports Power Management state change messages
  - APIC and MSI interrupt messaging support
  - Supports SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters

1.1.7 Power Management

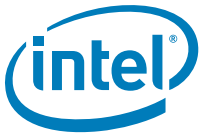
- ACPI S0, S3, S4, S5
- CPU States C0, C1, C2, C3, C4 states
- PCI Express Link States: L0, L0s, L1, L2, L3
- Intel Rapid Memory Power Management
- HSLPCPU# output
- DPWR# support

1.1.8 ISIPP Support

- Yes

1.1.9 Package

- FCBGA
- Ball Count: 1466 balls
- Package Size: 37.5 mm x 37.5 mm
- Ball Pitch: 42-mil x 34-mil pitch



1.1.10 Mobile Intel® 945GME Chipset Feature Support

All features supported by Mobile Intel® 945GM/GME Express Chipset shall be supported by Mobile Intel 945GME Express Chipset unless otherwise noted in the following sections. Additional features are:

1.1.10.1 Analog TV-Out

- No support for MacroVision

1.2 Mobile Intel® 945PM Express Chipset Feature Support

All features supported by the Mobile Intel 945GM/GME Express Chipset shall be supported by the Mobile Intel 945PM Express Chipset unless noted otherwise below. However, the Mobile Intel 945PM Express Chipset does not support Integrated Graphics display. Additional features/differences are also listed here, if applicable.

1.3 Intel® 945GT Express Chipset Feature Support

All features supported by the Mobile Intel 945GM/945GME Express Chipset shall be supported by the Intel 945GT Express Chipset unless otherwise noted. Additional features/differences are also listed here, if applicable.

Note: The Intel 945GT Express Chipset is targeted for use in desktop designs.

1.3.1 Processor Support

- Intel Core Duo processor SV (Standard Voltage)

1.3.2 Internal Graphics

- 400-MHz core render clock and 320-MHz core display clock at 1.5-V core voltage only

1.3.2.1 LVDS Interface

- Dual-channels LVDS interface support: 2 x 18 bpp panel support up to QXGA (2048 x 1536)

1.3.2.2 Analog CRT

- Analog Monitor Support up to QXGA

1.3.3 ISIPP Support

- No

1.4 Mobile Intel® 945 Express Chipset Feature Support

All features supported by Mobile Intel 945GM/945GME Express Chipset shall be supported by Intel 945GMS Express Chipset unless noted otherwise below. However, The Mobile Intel 945GMS Express Chipset does not include support for External Graphics via a PCIe Interface. Additional features/differences are also listed here, if applicable.

1.4.1 Processor Support

- Intel Core 2 Duo mobile processor LV and ULV
- Intel Core Duo processor LV and ULV
- Intel Core Solo processor ULV
- Celeron M processor ULV
- 533-MHz and 667-MHz front side bus (FSB) support

1.4.2 System Memory Support

- Supports single-channel DDR2 SDRAM only
- Maximum Memory supported 2 GB
- Memory Channel Topologies supported:
  - — Single-channel with 1 SO-DIMM only (up to 1 GB)
  - — Single-channel with 1 SO-DIMM (up to 1 GB) and Memory Down (up to 1 GB)
- Support for DDR2 at 400 MHz and 533 MHz

1.4.3 Internal Graphics

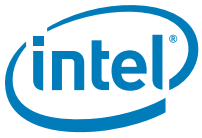
- 166-MHz core render clock and 200 MHz core display clock at 1.05-V core voltage only
- Support for only one SDVO port
- SDVO slot reversal not supported
- Support for dual-channel LVDS resolutions up to UXGA
- Support for CRT resolutions up to QXGA
- TV support for HDTV

1.4.4 DMI

- DMI lane width support for x2 only
- DMI Lane reversal not supported

1.4.5 Package

- FCBGA
- Ball Count: 998 balls
- Package Size: 27 mm x 27 mm
- Ball pitch: 0.8-mm uniform pitch



1.5 Mobile Intel® 945GSE Express Chipset Feature Support

All features supported by Mobile Intel® 945GMS Express Chipset are supported by Mobile Intel 945GSE Express Chipset unless otherwise noted in the following sections. Additional features are list below.

1.5.1 Analog TV-Out

- No support for MacroVision*

1.6 Mobile Intel® 940GML Express Chipset Feature Support

All features supported by Mobile Intel 945GM/945GME Express Chipset shall be supported by Intel 940GML Express Chipset unless noted otherwise below. However, The Mobile 940GML Express Chipset does not include support for External Graphics via a PCIe interface.

1.6.1 Processor Support

- Celeron M processor (Intel Core processor based), Celeron M processor ULV
- 533-MHz FSB support only

1.6.2 System Memory Support

- Maximum Memory supported 2 GB (1 GB per rank)
- Support for DDR2 at 400 MHz and 533 MHz
- No support for Dual-Channel Interleaved mode of operation
- Enhanced Addressing support (Swap only)

1.6.3 Internal Graphics

- 166-MHz render clock
- 200-MHz and 133-MHz display clock at 1.05-V core voltage
- Intel S2DDT not supported
- Automatic Display Brightness

1.6.4 ICH Support

- Support for Intel 82801GBM (base variant of ICH7M) only

1.6.5 Power Management

- Intel Rapid Power Management not supported

1.6.6 ISIPP Support

- No

1.7 Mobile Intel® 943GML Express Chipset Feature Support

All features supported by Mobile Intel 940GMLGM Express Chipset shall be supported by Intel 943GML Express Chipset unless noted otherwise below.

1.7.1 System Memory Support

- Support for Dual-Channel Interleaved mode of operation

1.7.2 Internal Graphics

- 200-MHz Render Clock

1.8 Mobile Intel® 945GU Express Chipset Feature Support

The following sections describe the key differences between the 945GU Express Chipset and the Mobile Intel 945GMS Express Chipset.

1.8.1 Processor Support

- Intel® Processor A100 and A110 on 90 nm Process with 512-KB L2 Cache 400-MHz front side bus (FSB) support

1.8.2 System Memory Support

- Supports single-channel DDR2 SDRAM
- Maximum Memory supported: up to 1 GB at 400 MHz
- 256-Mb, 512-Mb and 1-Gb memory technologies supported
- Support for x16 devices only

1.8.3 x1 PCI Express*

- One single-lane (x1) PCI Express port.
- Hot Plug not supported.

1.8.4 Internal Graphics

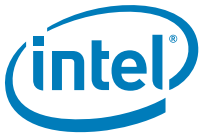
- 133-MHz core render clock and 133-MHz core display clock at 1.05-V core voltage
- CRT Not supported

1.8.5 LVDS Interface

- 25 MHz –112 MHz single channel; @18 bpp
- Panel support up to XGA (1024 x 768) internal and SXGA (1280 x 1024) external

1.8.6 SDVO Ports

- Single SDVO Port supported



1.8.7 ICH Support

- Support for Intel ICH7-U

1.8.8 DMI

- Configurable as x2 DMI lane interface

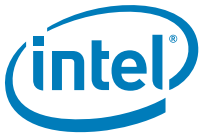
1.8.9 Package

- FCBGA
- Ball Count: 1249 balls
- Package Size: 22 mm x 22 mm
- Ball Pitch: 0.593-mm x 0.893-mm pitch

1.9 Terminology

(Sheet 1 of 2)

Term	Description
AGTL+	Advanced Gunning Transceiver Logic + (AGTL+) bus
Core	The internal base logic in the (G)MCH
CPU	Central Processing Unit
CRT	Cathode Ray Tube
DDR2	A second generation Double Data Rate SDRAM memory technology
DBI	Dynamic Bus inversion
DMI	Direct Media Interface The chip-to-chip interconnect between the Mobile Intel® 945GM/GME/PM/GMS/GSE, 943/940GML and Intel® 945GT Express Chipsets and the Intel® 82801GBM/GHM, is an Intel Proprietary interface. For the Ultra Mobile Intel® 945GU Express Chipset, the chip-to-chip connection is to the 82801GU ICH7-U.
DVI*	Digital Visual Interface is the interface specified by the DDWG (Digital Display Working Group)
FSB	Front Side Bus Connection between (G)MCH and the CPU. Also known as the Host interface
(G)MCH	Graphics Memory Controller Hub
GTL+	Gunning Transceiver Logic + (GTL+) bus
Host	This term is used synonymously with processor
I^2C	Inter-IC (a two wire serial bus created by Philips)
iDCT	Inverse Discrete Cosine Transform
Intel® 82801GBM (ICH7M)	The Intel® I/O Controller Hub component (base variant) that contains the primary PCI interface, LPC interface, USB2, ATA-100, and other I/O functions. It communicates with the (G)MCH over a proprietary interconnect called DMI.
Intel® 82801GHM (ICH7M)	The Digital Home variant of the I/O Controller Hub with support for Intel® Centrino® Duo technology. In addition to the features of the 82801GBM, It includes support for 2 additional PCIe* ports and Intel® ViiV™ technology
Intel® 82801GU (ICH7-U)	The Intel® I/O Controller Hub component that contains the primary PCI interface, LPC interface, USB2, ATA-100, and other I/O functions. It communicates with the Ultra Mobile Intel 945GU Express Chipset over a proprietary interconnect called DMI.
INTx	An interrupt request signal where X stands for interrupts A,B,C and D
LCD	Liquid Crystal Display
LFP	Local Flat Panel
LVDS	Low Voltage Differential Signaling A high-speed, low-power data transmission standard used for display connections to LCD panels.



(Sheet 2 of 2)

Term	Description
NCTF	Non-Critical to Function As a function of Intel's continuous improvement goals, we have identified package level modifications that add to the overall solder joint strength and reliability of our component. Through our research and development, we have concluded that adding non-critical to function (NCTF) solder balls to our packages can improve the overall package-to-board solder joint strength and reliability. Ball locations/signal ID's followed with the suffix of “NCTF” have been designed into the package footprint to enhance the package to board solder joint strength/reliability of this product by absorbing some of the stress introduced by the Characteristic Thermal Expansion (CTE) mismatch of the Die to package interface. It is expected that in some cases, where board stresses are excessive, these balls may crack partially or completely, however, cracks in the NCTF balls will have no impact to our product performance or reliability. Intel has added these balls primarily to serve as stress absorbers.
NTSC	National Television Standards Committee
PAL	Phase Alternate Line
PEG	External Graphics using PCI Express* Architecture A high-speed serial interface whose configuration is software compatible with the existing PCI specifications. The specific PCI Express implementation intended for connecting the (G)MCH to an external graphics controller is an x16 link
PWM	Pulse Width Modulation
Rank	A unit of DRAM corresponding 4 to 8 devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol
SDVO	Serial Digital Video Out (SDVO) Digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS, TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO. For the Mobile Intel 945GM/GME and Intel 945GT Express Chipsets, it will be multiplexed on a portion of the x16 graphics PCI Express interface.
SDVO Device	Third party codec that utilizes SDVO as an input. May have a variety of output formats, including DVI, LVDS, TV-out, etc.
x1	Refers to a Link or Port with one Physical Lane
x8	Refers to a Link or Port with eight Physical Lanes
x16	Refers to a Link or Port with sixteen Physical Lanes
xN	Refers to a Link with “N” Physical Lanes
VLD	Variable Length Decoding
VTT	Front Side Bus Power Supply (VCCP)

1.10 Reference Documents

Document	Document No./Location
Mobile Intel® 945 Express Chipset Family Specification Update	http://www.intel.com/design/mobile/specupdt/309220.htm
Intel® Core™ Duo Processor and Intel® Core™ Solo Processor on 65 nm Process Datasheet	http://www.intel.com/design/mobile/datashts/309221.htm
Intel® Core™ Duo Processor and Intel® Core™ Solo Processor on 65 nm Process Specification Update	http://www.intel.com/design/mobile/specupdt/309222.htm
Intel® I/O Controller Hub 7 (ICH7) Family Datasheet	http://www.intel.com/design/chipsets/datashts/307013.htm
Intel® I/O Controller Hub 7 (ICH7) Family Specification Update	http://www.intel.com/design/chipsets/specupdt/307014.htm
PCI Local Bus Specification 2.3	http://www.pcisig.com
PCI Express Base Specification 1.1*	http://www.pcisig.com
PCI Power Management Interface Specification 1.2	http://www.pcisig.com
VESA Specifications	http://www.vesa.org
Advanced Configuration and Power Management(ACPI) Specification 1.0b, 2.0 and 3.0	http://www.teleport.com/~acpi/
JEDEC Double Data Rate (DDR) SDRAM Specification *JEDEC Double Data Rate 2 (DDR2) SDRAM Specification*	http://www.jedec.com
Intel DDR2 400/533 JEDEC Specification ***Addendum***	www.intel.com/technology/memory/ddr/specs
Intel DDR2 667/800 JEDEC Specification ***Addendum***	www.intel.com/technology/memory/ddr/specs
Intel Developer website link for DDR validation information	http://developer.intel.com/technology/memory/
Intel Developer website link for PCI Express Architecture*	http://www.intel.com/technology/pciexpress/devnet/mobile.htm

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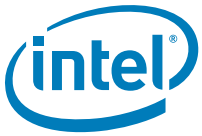


2 Signal Description

This section describes the (G)MCH signals. These signals are arranged in functional groups according to their associated interface. The following notations are used to describe the signal type:

Notations	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. (V_{CCP})
PCI Express*	PCI Express interface signals. These signals are compatible with current *PCI Local Bus Specification* Signaling Environment AC Specifications. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2 V max. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V. Please refer to the *PCI Local Bus Specification*.
CMOS	CMOS buffers. 1.5-V tolerant
HVCMOS	CMOS buffers. 3.3-V tolerant
COD	CMOS Open Drain buffers. 3.3-V tolerant
SSTL-1.8	Stub Series Termination Logic: These are 1.8-V capable buffers. 1.8-V tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.
LVDS	Low Voltage Differential signal interface
Ref	Voltage reference signal

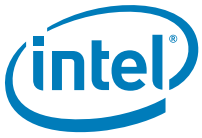
Note: System Address and Data Bus signals are logically inverted signals. The actual values are inverted of what appears on the system bus. This must be considered and the addresses and data bus signals must be inverted inside the (G)MCH. All processor control signals follow normal convention: A 0 indicates an active level (low voltage), and a 1 indicates an active level (high voltage).

2.1 Host Interface

Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the host bus (V_{CCP}).

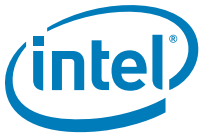
2.1.1 Host Interface Signals

Signal Name	Type	Description
HADS#	I/O AGTL+	**Host Address Strobe:** The system bus owner asserts HADS# to indicate the first of two cycles of a request phase. The (G)MCH can also assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O AGTL+	**Host Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
HBPRI#	O AGTL+	**Host Bus Priority Request:** The (G)MCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O AGTL+	**Host Bus Request 0#:** The (G)MCH pulls the processor bus HBREQ0**#** signal low during HCPURST#. The signal is sampled by the processor on the active-to-inactive transition of HCPURST#. HBREQ0# should be tri-stated after the hold time requirement has been satisfied.
HCPURST#	O AGTL+	**Host CPU Reset:** The CPURST# pin is an output from the (G)MCH. The (G)MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. HCPURST**#** allows the processor to begin execution in a known state.
HDBSY#	I/O AGTL+	**Host Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O AGTL+	**Host Defer:** Signals that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.



Signal Name	Type	Description
HDINV[3:0]#	I/O AGTL+	**Host Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. HDINV# Data Bits HDINV[3]# HD[63:48]# HDINV[2]# HD[47:32]# HDINV[1]# HD[31:16]# HDINV[0]# HD[15:0]#
HDRDY#	I/O AGTL+	**Host Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+ 2X	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The (G)MCH drives HA[31:3]# during snoop cycles on behalf of PCI Express*/Internal Graphics or ICH7M. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+ 2X	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. Strobe Address Bits HADSTB[0]# HA[15:3]#, HREQ[4:0]# HADSTB[1]# HA[31:16]#, HREQ[4:0]#
HD[63:0]#	I/O AGTL+ 4X	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+ 4X	**Host Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0]# and HDINV[3:0]# at the 4x transfer rate. Strobe Data Bits HDSTBP[3]#, HDSTBN[3]# HD[63:48]#, HDINV[3]# HDSTBP[2]#, HDSTBN[2]# HD[47:32]#, HDINV[2]# HDSTBP[1]#, HDSTBN[1]# HD[31:16]#, HDINV[1]# HDSTBP[0]#, HDSTBN[0]# HD[15:00]#, HDINV[0]#
HHIT#	I/O AGTL+	**Host Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.

Signal Name	Type	Description
HHITM#	I/O AGTL+	**Host Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic, i.e., PCI Express graphics access to System Memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+ 2X	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O AGTL+	**Host Response Status:** Indicates the type of response according to the following the table: HRS[2:0]# — Response type 000 — Idle state 001 — Retry response 010 — Deferred response 011 — Reserved (not driven by (G)MCH) 100 — Hard Failure (not driven by (G)MCH) 101 — No data response 110 — Implicit Write back 111 — Normal data response
HDPWR#	I/O AGTL+	**Host Data Power:** Used by (G)MCH to indicate that a data return cycle is pending within 2 HCLK cycles or more. CPU uses this signal during a read-cycle to activate the data input buffers in preparation for HDRDY# and the related data.
HCPUSLP#	O CMOS	**Host CPU Sleep:** When asserted in the Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts.



Signal Name	Type	Description
THERMTRIP#	O AGTL+	Connects between the processor and the ICH7-M. Assertion of THERMTRIP# (Thermal Trip) indicates the (G)MCH junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the (G)MCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the (G)MCH core junction temperature. To protect (G)MCH, its core voltage (Vcc) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RSTIN# is asserted. While the assertion of the RSTIN# signal will deassert THERMTRIP#, if the (G)MCH's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted.

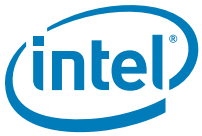
2.1.2 Host Interface Reference and Compensation

Signal Name	Type	Description
HVREF	I A	**Host Reference Voltage:** Reference voltage input for the Data, Address, and Common clock signals of the host AGTL+ interface.
HXRCOMP	I/O A	**Host X RCOMP:** Used to calibrate the host AGTL+ I/O buffers. This signal is powered by the host interface termination rail (V_{CCP}).
HXSCOMP	I/O A	**Host X SCOMP:** Slew rate compensation for the host interface.
HXSWING	I A	**Host X Voltage Swing:** These signals provide reference voltages used by the HXRCOMP circuits.
HYRCOMP	I/O A	**Host Y RCOMP:** Used to calibrate the host AGTL+ I/O buffers.
HYSCOMP	I/O A	**Host Y SCOMP:** Slew rate compensation for the host interface.
HYSWING	I A	**Host Y Voltage Swing:** These signals provide reference voltages used by the HYRCOMP circuitry.

2.2 DDR2 DRAM Interface

2.2.1 DDR2 SDRAM Channel A Interface

Signal Name	Type	Description
SA_DQ[63:0]	I/O SSTL1.8 2x	**Data Bus:** DDR2 Channel A data signal interface to the SDRAM data bus.
SA_DM[7:0]	O SSTL1.8 2X	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM[7:0] for every data byte lane.
SA_DQS[7:0]	I/O SSTL1.8 2x	**Data Strobes:** SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS[7:0]# during read and write transactions.
SA_DQS[7:0]#	I/O SSTL1.8 2x	**Data Strobe Complements:** These are the complementary strobe signals.
SA_MA[13:0]	O SSTL1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. ***Note:*** SA_MA13 is for support of 1-Gb devices.
SA_BS[2:0]	O SSTL1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank.
SA_RAS#	O SSTL1.8	**RAS Control Signal:** Used with SA_CAS# and SA_WE# (along with SM_CS#) to define the SDRAM commands.
SA_CAS#	O SSTL1.8	**CAS Control Signal:** Used with SA_RAS# and SA_WE# (along with SM_CS#) to define the SDRAM commands.
SA_WE#	O SSTL1.8	**Write Enable Control Signal:** Used with SA_RAS# and SA_CAS# (along with SM_CS#) to define the SDRAM commands.
SA_RCVENIN#	I SSTL1.8	**Clock Input:** Used to emulate source-synch clocking for reads. Connects internally to SA_RCVENOUT#. Leave as No Connect.
SA_RCVENOUT#	O SSTL1.8	**Clock Output:** Used to emulate source-synch clocking for reads. Connects internally to SA_RCVENIN#. Leave as No Connect.



2.2.2 DDR2 SDRAM Channel B Interface

Note: The Ultra Mobile Intel 945GU Express Chipset does not support Channel B. These signals are Not on the Ultra Mobile Intel 945GU Express Chipset.

(Sheet 1 of 2)

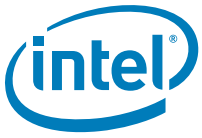
Signal Name	Type	Description
SB_DQ[63:0]	I/O SSTL1.8 2x	**Data Lines:** DDR / DDR2 Channel B data signal interface to the SDRAM data bus. ***Note:*** These signals do not exist on the Mobile Intel® 945GMS/GSE Express Chipset.
SB_DM[7:0]	O SSTL1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane. These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. ***Note:*** These signals do not exist on the Mobile Intel 945GMS/GSE Express Chipset.
SB_DQS[7:0]	I/O SSTL1.8 2x	**Data Strobes:** DDR2: SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS[7:0]# during read and write transactions. ***Note:*** These signals do not exist on the Mobile Intel 945GMS/GSE Express Chipset.
SB_DQS[7:0]#	I/O SSTL1.8 2x	**Data Strobe Complements:** These are the complementary strobe signals. ***Note:*** These signals do not exist on the Mobile Intel 945GMS/GSE Express Chipset.
SB_MA[13:0]	O SSTL1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. ***Note:*** SB_MA13 is for support of 1-Gb devices.
SB_BS[2:0]	O SSTL1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank.
SB_RAS#	O SSTL1.8	**RAS Control Signal:** Used with SB_CAS# and SB_WE# (along with SM_CS#) to define the SDRAM commands.
SB_CAS#	O SSTL1.8	**CAS Control Signal:** Used with SB_RAS# and SB_WE# (along with SM_CS#) to define the SDRAM commands.

(Sheet 2 of 2)

Signal Name	Type	Description
SB_WE#	O SSTL1.8	**Write Enable Control Signal:** Used with SB_RAS# and SB_CAS# (along with SM_CS#) to define the SDRAM commands.
SB_RCVENIN#	I SSTL1.8	**Clock Input:** Used to emulate source-synch clocking for reads. Leave as No Connect. ***Note:*** These signals do not exist on the Mobile Intel 945GMS/GSE Express Chipset.
SB_RCVENOUT#	O SSTL1.8	**Clock Output:** Used to emulate source-synch clocking for reads. Leave as No Connect. ***Note:*** These signals do not exist on the Mobile Intel 945GMS/GSE Express Chipset.

2.2.3 DDR2 Common Signals

Signal Name	Type	Description
SM_CK[3:0]	O SSTL1.8	**SDRAM Differential Clock:** (2 per DIMM) These are the SDRAM Differential Clock signals The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM.
SM_CK[3:0]#	O SSTL1.8	**SDRAM Inverted Differential Clock:** (2 per DIMM) These are the SDRAM Inverted Differential Clock signals.
SM_CS[3:0]#	O SSTL1.8	**Chip Select:** (1 per rank) These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank. ***Note***: SM_CS[3:2] are Not on the Ultra Mobile 945GU Express Chipset.



Signal Name	Type	Description
SM_CKE[3:0]	O SSTL1.8	**Clock Enable:** (1 per rank) SM_CKE[3:0] is used: to initialize the SDRAMs during power-up, to power-down SDRAM ranks, to place all SDRAM ranks into and out of self-refresh during STR. SM_CKE[1:0]: Single-channel mode: Route to SO-DIMM 0 Dual-channel mode: Route to SO-DIMM A SM_CKE[3:2]: Single-channel mode: Route to SO-DIMM 1 Dual-channel mode: Route to SO-DIMM B ***Note**:* SM_CKE[3:2] are Not on the Ultra Mobile 945GU Express Chipset. ***Note**:* Ultra Mobile 945GU Express Chipset only supports memory down. The chipset does not support SO-DIMMs.
SM_ODT[3:0]	O SST1.8	**On Die Termination:** Active Termination Control.

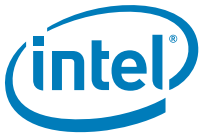
2.2.4 DDR2 SDRAM Reference and Compensation

Signal Name	Type	Description
SM_RCOMPN	I/O A	**System Memory RCOMP N:** Buffer compensation This signal is powered by the System Memory rail. (2.5 V for DDR, 1.8 V for DDR2).
SM_RCOMPP	I/O A	**System Memory RCOMP P:** Buffer compensation This signal is powered by the System Memory rail.
SM_VREF[1:0]	I A	**SDRAM Reference Voltage:** Reference voltage inputs for each DQ, DQS, & RCVENIN#. Also used during ODT RCOMP.
SM_OCDCOMP[1:0]	I A	**On-Die DRAM OCD Driver Compensation:** Can be left as NC. OCD is not supported ***Note**:* These signals are Not on the Ultra Mobile 945GU Express Chipset.

2.3 PCI Express-Based Graphics Interface Signals

Unless otherwise specified, these signals are AC coupled.

Signal Name	Type	Description
EXP_A_RXN[15:0] EXP_A_RXP[15:0]	I PCI Express*	PCI Express Graphics Receive Differential Pair ***Note:*** These signals do not exist on the Mobile Intel® 945GMS/GSE Express Chipset. ***Note***: Only EXP_A_RXN[5, 0] and EXP_A_RXP[5, 0] are on the Ultra Mobile 945GU Express Chipset.
EXP_A_TXN[15:0] EXP_A_TXP[15:0]	O PCI Express	PCI Express Graphics Transmit Differential Pair ***Note:*** These signals do not exist on the Mobile Intel 945GMS/GSE Express Chipset. ***Note***: Only EXP_A_TXN[5, 0] and EXP_A_TXP[5, 0] are on the Ultra Mobile 945GU Express Chipset.
EXP_A_COMPO	I A	PCI Express Graphics Output Current and Resistance Compensation
EXP_A_COMPI	I A	PCI Express Graphics Input Current Compensation



2.3.1 Serial DVO and PCI Express-Based Graphics Signal Mapping

SDVO and PCI Express Interface for Graphics architecture are muxed together (these signals are not available as separate balls on the package).

Note: On the 82945GU (G)MCH the SDVO signals are Not multiplexed.

Table 1. SDVO and PCI Express-Based Graphics Port Signal Mapping

SDVO Mode	PCI Express Mode
SDVOB_RED#	EXP_TXN0
SDVOB_RED	EXP_TXP0
SDVOB_GREEN#	EXP_TXN1
SDVOB_GREEN	EXP_TXP1
SDVOB_BLUE#	EXP_TXN2
SDVOB_BLUE	EXP_TXP2
SDVOB_CLKN	EXP_TXN3
SDVOB_CLKP	EXP_TXP3
SDVOC_RED#	EXP_TXN4
SDVOC_RED	EXP_TXP4
SDVOC_GREEN#	EXP_TXN5
SDVOC_GREEN	EXP_TXP5
SDVOC_BLUE#	EXP_TXN6
SDVOC_BLUE	EXP_TXP6
SDVOC_CLKN	EXP_TXN7
SDVOC_CLKP	EXP_TXP7
SDVO_TVCLKIN#	EXP_RXN0
SDVO_TVCLKIN	EXP_RXP0
SDVOB_INT#	EXP_RXN1
SDVOB_INT	EXP_RXP1
SDVO_FLDSTALL#	EXP_RXN2
SDVO_FLDSTALL	EXP_RXP2
SDVOC_INT#	EXP_RXN5
SDVOC_INT	EXP_RXP5

NOTE:

1. The Mobile Intel 945GMS/GSE Express Chipset employs only the ***SDVO B*** port and associated signals (TVCLKIN, INT and FLDSTALL differential pairs) as highlighted above.
2. The SDVO to PCIe signal mapping shown in the table above is applicable for the **non-reversed SDVO-only mode**. For more details on SDVO mapping for all possible configurations, see Section 10.3.2.2.

2.4 DMI – MCH to ICH Serial Interface

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I PCI Express	**DMI input from ICH:** Direct Media Interface receive differential pair
DMI_TXP[3:0] DMI_TXN[3:0]	O PCI Express	**DMI output to ICH:** Direct Media Interface transmit differential pair

Note: DMI x2 or x4 is supported for Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipsets.

Signal Name	Type	Description
DMI_RXP[1:0] DMI_RXN[1:0]	I PCI Express	**DMI input from ICH:** Direct Media Interface receive differential pair
DMI_TXP[1:0] DMI_TXN[1:0]	O PCI Express	**DMI output to ICH:** Direct Media Interface transmit differential pair

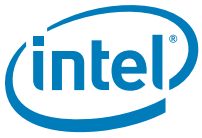
Note: DMI x2 only is supported for the Mobile Intel 945GMS/GSE Express Chipset and Ultra Mobile Intel 945GU Express Chipset.

2.5 Integrated Graphics Interface Signals

2.5.1 CRT DAC SIGNALS

Note: The Ultra Mobile Intel 945GU Express Chipset does not support a CRT interface. Theses signals are Not on the Ultra Mobile Intel 945GU Express Chipset.

Signal Name	Type	Description
CRT_RED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
CRT_RED#	O A	**RED# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
CRT_GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
CRT_GREEN#	O A	**GREEN# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.



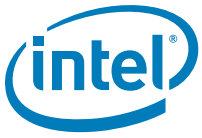
Signal Name	Type	Description
CRT_BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each signal (e.g., 75-Ω resistor on the board, in parallel with a 75-Ω CRT load).
CRT_BLUE#	O A	**BLUE# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
CRT_IREF	O A	**Resistor Set:** Set point resistor for the internal color palette DAC. A 255 Ω, 1% resistor is required between CRT_IREF and motherboard ground.
CRT_HSYNC	O A	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or ìsync interval.
CRT_VSYNC	O A	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable).

2.5.2 Analog TV-out Signals

Signal Name	Type	Description
TVDAC_A	O A	**TVDAC Channel A Output:** TVDAC_A supports the following: **Composite:** CVBS signal **Component:** Chrominance (Pb) analog signal
TVDAC_B	O A	**TVDAC Channel B Output:** TVDAC_B supports the following: **S-Video**: Luminance analog signal **Component**: Luminance (Y) analog signal
TVDAC_C	O A	**TVDAC Channel C Output:** TVDAC_C supports the following: **S-Video**: Chrominance analog signal **Component**: Chrominance (Pr) analog signal
TV_DCONSEL[1:0]	O A	**TV D-connector Select:** Supports 525i, 525p, 750p, 1125i and 1125p ***Note:*** This signal is Not on the Ultra Mobile Intel 945GU Express Chipset.
TV_IRTNA	O A	**Current Return for TVDAC Channel A:** Connect to ground on board
TV_IRTNB	O A	**Current Return for TVDAC Channel B:** Connect to ground on board
TV_IRTNC	O A	**Current Return for TVDAC Channel C:** Connect to ground on board
TV_IREF	O A	**TV Reference Current:** Uses an external resistor of 5 kΩ ±1% to set internal voltage levels

2.5.3 LVDS Signals

Signal Name	Type	Description
LDVS Channel A		
LADATAP[2:0]	O LVDS	Channel A differential data output – positive
LADATAN[2:0]	O LVDS	Channel A differential data output – negative
LA_CLKP	O LVDS	Channel A differential clock output – positive
LA_CLKN	O LVDS	Channel A differential clock output – negative
LDVS Channel B (Not on the Intel® 945GU Express Chipset)		
LBDATAP[2:0]	O LVDS	Channel B differential data output – positive
LBDATAN[2:0]	O LVDS	Channel B differential data output – negative
LB_CLKP	O LVDS	Channel B differential clock output – positive
LB_CLKN	O LVDS	Channel B differential clock output – negative
LFP Panel Power and Backlight Control		
LVDD_EN	O HVCMOS	LVDS panel power enable: Panel power control enable control. This signal is also called VDD_DBL in the CPIS specification and is used to control the VDC source to the panel logic.
LBKLT_EN	O HVCMOS	LVDS backlight enable: Panel backlight enable control. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry. ***Note:*** The accuracy of the PWM duty cycle of L_BKLT_CTL signal for any given value will be **within ±20 ns**.
LBKLT_CTL	O HVCMOS	Panel backlight brightness control: Panel brightness control. This signal is also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal.
LVDS Reference Signals		
LIBG	I/O Ref	LVDS Reference Current. 1.5 kΩ pull-down resistor needed
LVREFH	I Ref	Reserved - Must be connected to ground.
LVDS Reference Signals		
LVREFL	I Ref	Reserved - Must be connected to ground.
LVBG	O A	Reserved - No connect



2.5.4 Serial DVO Interface

All of the pins in this section are multiplexed with the upper eight lanes of the PCI Express interface.

Note: On the Ultra Mobile 945GU Express Chipset the SDVO signals are Not multiplexed.

Note: On the Ultra Mobile 945GU Express Chipset the “B” designator is not used in the signal name. For example, the SDVO clock signal names are SDVO_CLKP and SDVO_CLKN on the 945GU Express Chipset.

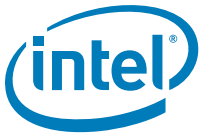
Signal Name	Type	Description
SDVO B Interface		
SDVOB_CLKP	O PCI Express	Serial Digital Video B Clock Multiplexed with EXP_TXP_3
SDVOB_CLKN	O PCI Express	Serial Digital Video B Clock Complement Multiplexed with EXP_TXN_3
SDVOB_RED	O PCI Express	Serial Digital Video B Red Data Multiplexed with EXP_TXP_0
SDVOB_RED#	O PCI Express	Serial Digital Video B Red Data Complement Multiplexed with EXP_TXN_0
SDVOB_GREEN	O PCI Express	Serial Digital Video B Green Data Multiplexed with EXP_TXP_1
SDVOB_GREEN#	O PCI Express	Serial Digital Video B Green Data Complement Multiplexed with EXP_TXN_1
SDVOB_BLUE	O PCI Express	Serial Digital Video B Blue Data Multiplexed with EXP_TXP_2
SDVOB_BLUE#	O PCI Express	Serial Digital Video B Blue Data Complement Multiplexed with EXP_TXN_2
SDVO C Interface		
SDVOC_RED	O PCI Express	Serial Digital Video C Red Data Multiplexed with EXP_TXP_4
SDVOC_RED#	O PCI Express	Serial Digital Video C Red Complement Multiplexed with EXP_TXN_4
SDVOC_GREEN	O PCI Express	Serial Digital Video C Green Multiplexed with EXP_TXP_5
SDVOC_GREEN#	O PCI Express	Serial Digital Video C Green Complement Multiplexed with EXP_TXN_5
SDVOC_BLUE	O PCI Express	Serial Digital Video Channel C Blue Multiplexed with EXP_TXP_6
SDVOC_BLUE#	O PCI Express	Serial Digital Video C Blue Complement Multiplexed with EXP_TXN_6
SDVOC_CLKP	O PCI Express	Serial Digital Video C Clock Multiplexed with EXP_TXP_7

Signal Name	Type	Description
SDVOC_CLKN	O PCI Express	Serial Digital Video C Clock Complement Multiplexed with EXP_TXN_7
SDVO Common Signals		
SDVO_TVCLKIN	I PCI Express	Serial Digital Video TVOUT Synchronization Clock Multiplexed with EXP_RXP_0
SDVO_TVCLKIN#	I PCI Express	Serial Digital Video TV-out Synchronization Clock Complement Multiplexed with EXP_RXN_0
SDVO_FLDSTALL	I PCI Express	Serial Digital Video Field Stall Multiplexed with EXP_RXP_2 ***Note:*** This signal is referred to as SDVO_FLDSTALLP on the Ultra Mobile Intel 945GU Express Chipset.
SDVO_FLDSTALL#	I PCI Express	Serial Digital Video Field Stall Complement Multiplexed with EXP_RXN_2 ***Note***: This signal is referred to as SDVO_FLDSTALLN on the Ultra Mobile Intel 945GU Express Chipset.
SDVOB_INT	I PCI Express	Serial Digital Video Input Interrupt - Port B Multiplexed with EXP_RXP_1
SDVOB_INT#	I PCI Express	Serial Digital Video Input Interrupt Complement - Port B Multiplexed with EXP_RXN_1
SDVOC_INT	I PCI Express	Serial Digital Video Input Interrupt - Port C Multiplexed with EXP_RXP_5
SDVOC_INT#	I PCI Express	Serial Digital Video Input Interrupt Complement - Port C Multiplexed with EXP_RXN_5

Note: The Mobile Intel 945GMS/GSE Express Chipset supports only the signals marked in Brown.

2.5.5 Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	Description
LCTLA_CLK	I/O COD	I^2C Based control signal (Clock) for External SSC clock chip control – optional
LCTLB_DATA	I/O COD	I^2C Based control signal (Data) for External SSC clock chip control – optional
DDCCLK	I/O COD	CRT DDC clock monitor control support ***Note***: This signal is Not on the Ultra Mobile Intel 945GU Express Chipset.
DDCDATA	I/O COD	CRT DDC Data monitor control support ***Note***: This signal is Not on the Ultra Mobile Intel 945GU Express Chipset.
LDDC_CLK	I/O COD	EDID support for flat panel display



Signal Name	Type	Description
LDDC_DATA	I/O COD	EDID support for flat panel display
SDVOCTRL_CLK	I/O COD	I^2C-based control signal (Clock) for SDVO device
SDVOCTRL_DATA	I/O COD	I^2C-based control signal (Data) for SDVO device

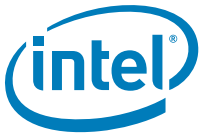
2.6 PLL Signals

Signal Name	Type	Description
CLK_REQ#	O COD	**External Clock Request:** (G)MCH drives CLK_REQ# to control the PCI Express* differential clock input to itself. Not supported with the Intel® 915 Express Chipset family clocking solutions.
HCLKP	I Diff Clk	**Differential Host Clock In:** Differential clock input for the host PLL. This is a low voltage differential signal and runs at the FSB data rate.
HCLKN	I Diff Clk	**Differential Host Clock Input Complement**
GCLKP	I Diff Clk	**Differential PCI Express-Based Graphics / DMI Clock In:** These pins receive a differential 100-MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
GCLKN	I Diff Clk	**Differential PCI Express Based Graphics / DMI Clock In Complement**
DREF_CLKP	I Diff Clk	**Display PLLA Differential Clock In – 96 MHz:** Display PLL Differential Clock In, no SSC support
DREF_CLKN	I Diff Clk	**Display PLLA Differential Clock In Complement:** Display PLL Differential Clock In Complement - no SSC support.
DREF_SSCLKP	I Diff Clk	**Display PLLB Differential Clock In – 100 MHz:** Optional Display PLL Differential Clock In for SSC support. ***Note:*** Differential Clock input for optional SSC support for LVDS display.
DREF_SSCLKN	I Diff Clk	**Display PLLB Differential Clock In Complement:** Optional Display PLL Differential Clock In Complement for SSC support ***Note:*** Differential Clock input for optional SSC support for LVDS display.

2.7 Reset and Miscellaneous Signals

Signal Name	Type	Description
RSTIN#	I HVCMOS	**Reset In:** When asserted this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PLTRST# output of the ICH7M. This input has a Schmitt trigger to avoid spurious resets. This input buffer is 3.3 V tolerant.
PWROK	I HVCMOS	**Power OK:** When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 99 ms and clocks stable for at least 1 µs. Please see Section 10.6.6 for details. This input buffer is 3.3-V tolerant.
H_BSEL [2:0] (CFG[2:0])	I AGTL+	**Host Bus Speed Select:** At the deassertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus. External Pull-ups are required.
CFG[17:3]	I AGTL+	**HW Straps:** CFG [17:3] has internal pull up.
CFG[20:18]	I HVCMOS	**HW Straps:** CFG [20:18] has internal pull down
PM_PM_BM_BUSY#	O HVCMOS	**(G)MCH Integrated Graphics Busy:** Used for PM synchronization with ICH. This signal should be connected to PM_BM_BUSY# of the ICH-M.
PM_EXTTS[1:0]#	I HVCMOS	**External Thermal Sensor Input:** If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling. EXTTS1# can alternately be used to implement fast C4/C4E exit. See Section 10.6.7 for details. This functionality is not available on EXTTS0#.
ICH_SYNC#	O HVCMOS	**ICH Synchronization:** Asserted to synchronize with ICH on faults. ICH_SYNC# must be connected to ICH7M's MCH_SYNC# signal.

Note: Some of the strappings mentioned in the table above do not exist on the Mobile Intel 945GMS/GSE Express Chipset. For more details, please refer to Chapter 12 for strapping definitions.



2.8 Platform Power Planes

Interface	Voltage Level (Typical Operation)	Voltage Range
(G)MCH Core	1.05 V	1.05 V to 1.5 V
DDR 2	1.8 V	1.6 V to 1.89 V
FSB V_{CC} (V_{TT})	1.05 V	1.05 V to 1.284 V
HV Buffers	3.3 V	3.135 V to 3.465 V
CRT DAC ***Note***: This signal Power Plane is Not on the Ultra Mobile Intel 945GU Express Chipset.	2.5 V	2.32 V to 2.625 V
TV DAC	3.3 V	3.135 V to 3.465 V
LVDS Transmitter/Analog	2.5 V	2.375 V to 2.625 V
LVDS Digital	1.5 V	1.425 V to 1.575 V
PCI Express* V_{CC}	1.5 V	1.39 V to 1.575 V
PCI Express Bandgap V_{CC}	2.5 V	2.32 V to 2.625 V
HPLL/DPLL/PCIEPLL	1.5 V	1.39 V to 1.575 V
GPIO	3.3 V	3.135 V to 3.465 V

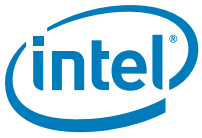
2.9 Power and Ground

(Sheet 1 of 2)

Interface	Ball Name	Description
Host	V_{TT} (V_{CCP})	FSB power supply (1.05 V) - (V_{CCP})
DRAM	V_{CCSM}	System memory power supply (1.8 V)
PCI Express* Based Graphics / DMI	V_{CCA_3GBG}	PCI Express* / DMI band gap power supply (2.5 V)
	V_{SSA_3GBG}	PCI Express / DMI band gap ground
	V_{CCA_HPLL}	Power supply for the host VCO in the host/mem/core PLL (1.5 V)
	V_{CC3G}	PCI Express / DMI Analog power supply (1.5 V)
PLL Analog	V_{CCA_MPLL}	Power supply for the mem VCO in the host/mem/core PLL (1.5 V)
	V_{CCD_HMPLL}	Power Supply for the digital dividers in the HMPLL (1.5 V)
	V_{CCA_3GPLL}	Power supply for the 3GIO PLL (1.5 V)
	V_{CCA_DPLLA}	Display A PLL power supply (1.5 V)
	V_{CCA_DPLLB}	Display B PLL power supply (1.5 V)
High Voltage Interfaces	V_{CCHV}	Power supply for the HV buffers (3.3 V)

(Sheet 2 of 2)

Interface	Ball Name	Description
CRT DAC ***Note***: These signals are Not on the Ultra Mobile Intel 945GU Express Chipset.	V_{CCA_CRTDAC}	Analog power supply for the DAC (2.5 V)
	V_{SSA_CRTDAC}	Analog ground for the DAC
	V_{CC_SYNC}	Power supply for HSYNC/ VSYNC (2.5 V)
LVDS	V_{CCD_LVDS}	Digital power supply (1.5 V)
	V_{CCTX_LVDS}	Data/Clk Tx power supply (2.5 V)
	V_{CCA_LVDS}	LVDS analog power supply (2.5 V)
	V_{SSA_LVDS}	LVDS analog VSS
TVDAC	V_{CCA_TVBG}	TV DAC Band Gap Power (3.3 V)
	V_{SSA_TVBG}	TV DAC Band Gap VSS
	V_{CCD_TVDAC}	Dedicated Power Supply for TVDAC (1.5 V)
	V_{CCDQ_TVDAC}	Power Supply for Digital Quiet TVDAC (1.5 V)
	V_{CCA_TVDACA}	Power Supply for TV Out Channel A (3.3 V)
	V_{CCA_TVDACB}	Power Supply for TV Out Channel B (3.3 V)
	V_{CCA_TVDACC}	Power Supply for TV Out Channel C (3.3 V)
I/O	V_{CC_AUX}	Power Supply for DDR DLLs, DDR IO, FSB HSIO, and FSB IO (1.5 V)
Core	V_{CC}	Core V_{CC} (1.05 V/ 1.5 V)
Ground	V_{SS}	Ground
NCTF	**Non-Critical To Function power signals:** "NCTF" (Non-Critical To Function) have been designed into the package footprint to enhance the Solder Joint Reliability of our products by absorbing some of the stress introduced by the Characteristic Thermal Expansion (CTE) mismatch of the Die to package interface. It is expected that in some cases, these balls may crack partially or completely, however, this will have no impact to our product performance or reliability. Intel has added these balls primarily to serve as sacrificial stress absorbers.	
	V_{CC_NCTF}	NTCF Core V_{CC} (1.05 V/ 1.5 V)
	V_{CCSM_NCTF}	NTCF V_{CC_AUX} power supply 1.5 V
	V_{SS_NCTF}	NTCF Ground



2.10 Reset States and Pull-up / Pull-downs

This section describes the expected states of the (G)MCH I/O buffers during and immediately after the assertion of RSTIN#. This table only refers to the contributions on the interface from the (G)MCH and does not reflect any external influence (such as external pull-up/pull-down resistors or external drivers.

Table 2. Legend

DRIVE	Strong drive to 0 or 1 (to normal value supplied by the core logic if not otherwise stated)
N/A	Value is indeterminate
IN	Input buffer enabled
TRI	Tri-state (Signals are not driven)
PU	Weak internal pull-up
PD	Weak internal pull-down
STRAP	Value is determined by the strap setting

2.10.1 Host Interface Signals

Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the host bus (VTT).

(Sheet 1 of 2)

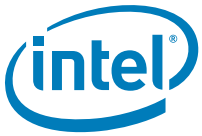
Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
HADS#	I/O AGTL+	PU	PU	PU
HBNR#	I/O AGTL+	PU	PU	PU
HBPRI#	O AGTL+	PU	PU	PU
HBREQ0#	I/O AGTL+	PU	PU	DRIVE 0
HCPURST#	O AGTL+	DRIVE 0	DRIVE 0	DRIVE 0
HDBSY#	I/O AGTL+	PU	PU	PU
HDEFER#	O AGTL+	PU	PU	PU
HDINV[3:0]#	I/O AGTL+	PU	PU	PU
HDRDY#	I/O AGTL+	PU	PU	PU
HA[31:3]#	I/O AGTL+	PU	PU	PU
HADSTB[1:0]#	I/O AGTL+	N/A	PU	N/A
HD[63:2]#	I/O AGTL+	PU	PU	PU

(Sheet 2 of 2)

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
HD[1]#	I/O AGTL+	DRIVE 0	PU	DRIVE 0
HD[0]#	I/O AGTL+	PU	PU	PU
HDSTBP[3:0]#	I/O AGTL+	N/A	PU	N/A
HDSTBN[3:0]#	I/O AGTL+	N/A	PU	N/A
HHIT#	I/O AGTL+	PU	PU	PU
HHITM#	I/O AGTL+	PU	PU	PU
HLOCK#	I/O AGTL+	PU	PU	PU
HREQ[4:0]#	I/O AGTL+	PU	PU	PU
HTRDY#	O AGTL+	PU	PU	PU
HRS[2:0]#	O AGTL+	PU	PU	PU
HDPWR#	O AGTL+	PU	PU	PU
HCPUSLP#	O CMOS	PU	PU	PU
THERMTRIP#	O AGTL+	PU	PU	PU

2.10.2 Host Interface Reference and Compensation

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
HVREF	I A	DRIVE 1	DRIVE 1	DRIVE 1
HXRCOMP	I/O A	PD	PD	PD
HXSCOMP	I/O A	PU	PU	PU
HXSWING	I A	PU	PU	PU
HYRCOMP	I/O A	PU	PU	PD
HYSCOMP	I/O A	PU	PU	PU
HYSWING	I A	PU	PU	PU



2.10.3 DDR2 SDRAM Channel A Interface

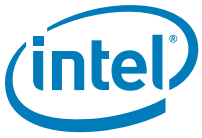
Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
SA_DQ[63:0]	I/O SSTL1.8	TRI	TRI	TRI
SA_DM[7:0]	O SSTL1.8	TRI	TRI	TRI
SA_DQS[7:0]	I/O SSTL1.8	TRI	TRI	TRI
SA_DQS[7:0]#	I/O SSTL1.8	TRI	TRI	TRI
SA_MA[13:0]	O SSTL1.8	TRI	TRI	TRI
SA_BS[2:0]	O SSTL1.8	TRI	TRI	TRI
SA_RAS#	O SSTL1.8	TRI	TRI	TRI
SA_CAS#	O SSTL1.8	TRI	TRI	TRI
SA_WE#	O SSTL1.8	TRI	TRI	TRI
SA_RCVENIN#	I SSTL1.8	TRI	TRI	TRI
SA_RCVENOUT#	O SSTL1.8	TRI	TRI	TRI

2.10.4 DDR2 SDRAM Channel B Interface

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
SB_DQ[63:0]	I/O SSTL1.8	TRI	TRI	TRI
SB_DM[7:0]	O SSTL1.8	TRI	TRI	TRI
SB_DQS[7:0]	I/O SSTL1.8	TRI	TRI	TRI
SB_DQS[7:0]#	I/O SSTL1.8	TRI	TRI	TRI
SB_MA[13:0]	O SSTL1.8	TRI	TRI	TRI
SB_BS[2:0]	O SSTL1.8	TRI	TRI	TRI
SB_RAS#	O SSTL1.8	TRI	TRI	TRI
SB_CAS#	O SSTL1.8	TRI	TRI	TRI
SB_WE#	O SSTL1.8	TRI	TRI	TRI
SB_RCVENIN#	I SSTL1.8	TRI	TRI	TRI
SB_RCVENOUT#	O SSTL1.8	TRI	TRI	TRI

2.10.5 DDR2 Common Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
SM_CK[1:0], SM_CK[3:2]	O SSTL1.8	TRI	TRI	TRI
SM_CK[1:0]#, SM_CK[3:2]#	O SSTL1.8	TRI	TRI	TRI
SM_CS[3:0]#	O SSTL1.8	TRI	TRI	TRI
SM_CKE[3:0]	O SSTL1.8	DRIVE 0	DRIVE 0	DRIVE 0
SM_ODT[3:0]	O SSTL1.8	DRIVE 0	DRIVE 0	DRIVE 0



2.10.6 DDR SDRAM Reference and Compensation

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
SMRCOMPN	I/O A	PU	PU	PU
SMRCOMPP	I/O A	PD	PD	PD
SMVREF[1:0]	I A	TRI	TRI	TRI

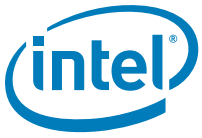
2.10.7 PCI Express-Based Graphics Interface Signals (PCIe x16 Mode)

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
EXP_RXN[15:0]	I PCI Express*	N/A	TRI	TRI
EXP_RXP[15:0]	I PCI Express	N/A	TRI	TRI
EXP_TXN[15:0]	O PCI Express	PD	PD	PU
EXP_TXP[15:0]	O PCI Express	PD	PD	PU
EXP_COMPO	I A	TRI	TRI	TRI
EXP_COMPI	I A	TRI	TRI	TRI

2.10.8 PCI Express-Based Graphics Interface Signals (SDVO Mode)

(Sheet 1 of 2)

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
SDVO C Interface				
SDVOC_RED	O PCI Express*	PU	PU	PU
SDVOC_RED#	O PCI Express	PU	PU	PU
SDVOC_GREEN	O PCI Express	PU	PU	PU
SDVOC_GREEN#	O PCI Express	PU	PU	PU
SDVOC_BLUE	O PCI Express	PU	PU	PU
SDVOC_BLUE#	O PCI Express	PU	PU	PU
SDVOC_CLKP	O PCI Express	PU	PU	PU
SDVOC_CLKN	O PCI Express	PU	PU	PU
SDVOC_INT	I PCI Express	TRI	TRI	TRI
SDVOC_INT#	I PCI Express	TRI	TRI	TRI
SDVO B Interface				
SDVOB_CLKP	O PCI Express	PU	PU	PU
SDVOB_CLKN	O PCI Express	PU	PU	PU
SDVOB_RED	O PCI Express	PU	PU	PU
SDVOB_RED#	O PCI Express	PU	PU	PU
SDVOB_GREEN	O PCI Express	PU	PU	PU
SDVOB_GREEN#	O PCI Express	PU	PU	PU
SDVOB_BLUE	O PCI Express	PU	PU	PU
SDVOB_BLUE#	O PCI Express	PU	PU	PU



(Sheet 2 of 2)

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
SDVOB_INT	I PCI Express	TRI	TRI	TRI
SDVOB_INT#	I PCI Express	TRI	TRI	TRI
SDVO Common Signals				
SDVO_TVCLKIN	I PCI Express	TRI	TRI	TRI
SDVO_TVCLKIN#	I PCI Express	TRI	TRI	TRI
SDVO_FLDSTALL	I PCI Express	TRI	TRI	TRI
SDVO_FLDSTALL#	I PCI Express	TRI	TRI	TRI

2.10.9 DMI

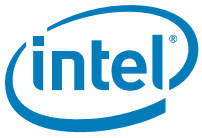
Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
DMI_RXN[3:0]	I PCI Express*	N/A	TRI	TRI
DMI_RXP[3:0]	I PCI Express	N/A	TRI	TRI
DMI_TXN[3:0]	O PCI Express	PU	PU	PU
DMI_TXP[3:0]	O PCI Express	PU	PU	PU

2.10.10 CRT DAC SIGNALS

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
CRT_RED	O A	TRI	TRI	TRI
CRT_RED#	O A	TRI	TRI	TRI
CRT_GREEN	O A	TRI	TRI	TRI
CRT_GREEN#	O A	TRI	TRI	TRI
CRT_BLUE	O A	TRI	TRI	TRI
CRT_BLUE#	O A	TRI	TRI	TRI
CRT_IREF	O A	TRI	TRI	TRI
CRT_HSYNC	O A	TRI	DRIVE 0	TRI
CRT_VSYNC	O A	TRI	DRIVE 0	TRI

2.10.11 Analog TV-out Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
TVDAC_A	O A	TRI	TRI	TRI
TVDAC_B	O A	TRI	TRI	TRI
TVDAC_C	O A	TRI	TRI	TRI
TV_IRTNA	O A	TRI	TRI	TRI
TV_IRTNB	O A	TRI	TRI	TRI
TV_IRTNC	O A	TRI	TRI	TRI
TV_IREF	O A	TRI	TRI	TRI



2.10.12 LVDS Signals

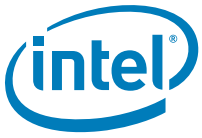
Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
LDVS Channel A				
LADATAP[2:0]	O LVDS	DRIVE 0	DRIVE 0	DRIVE 0
LADATAN[2:0]	O LVDS	DRIVE 0	DRIVE 0	DRIVE 0
LACLKP	O LVDS	DRIVE 0	DRIVE 0	DRIVE 0
LACLKN	O LVDS	DRIVE 0	DRIVE 0	DRIVE 0
LDVS Channel B				
LBDATAP[2:0]	O LVDS	DRIVE 0	DRIVE 0	DRIVE 0
LBDATAN[2:0]	O LVDS	DRIVE 0	DRIVE 0	DRIVE 0
LBCLKP	O LVDS	DRIVE 0	DRIVE 0	DRIVE 0
LBCLKN	O LVDS	DRIVE 0	DRIVE 0	DRIVE 0
LFP Panel Control Signal				
LVDD_EN	O HVCMOS	TRI	DRIVE 0	TRI
LBKLT_EN	O HVCMOS	TRI	DRIVE 0	TRI
LBKLT_CRTL	O HVCMOS	TRI	DRIVE 0	TRI
LVDS Reference Signal				
LVREFH	I Ref	TRI	TRI	TRI
LVREFL	I Ref	TRI	TRI	TRI
LIBG	I / O Ref	TRI	TRI	TRI

2.10.13 Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
LCTLA_CLK	I/O COD	TRI	TRI	PU
LCTLB_DATA	I/O COD	TRI	TRI	PU
CRT_DDCCLK	I/O COD	TRI	TRI	PU
CRT_DDCDATA	I/O COD	TRI	TRI	PU
LDDC_CLK	I/O COD	TRI	TRI	PU
LDDC_DATA	I/O COD	TRI	TRI	PU
SDVOCTRL_CLK	I/O COD	TRI	TRI	DRIVE 0
SDVOCTRL_DATA	I/O COD	DRIVE 1	DRIVE 1	DRIVE 0

2.10.14 PLL Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
HCLKP	I Diff Clk	IN	IN	DRIVE 1
HCLKN	I Diff Clk	IN	IN	DRIVE 0
GCLKP	I Diff Clk	IN	IN	DRIVE 0
GCLKN	I Diff Clk	IN	IN	DRIVE 1
DREF_CLKP	I Diff Clk	IN	IN	DRIVE 1
DREF_CLKN	I Diff Clk	IN	IN	DRIVE 0
DREF_SSCLKP	I Diff Clk	IN	IN	DRIVE 1
DREF_SSCLKN	I Diff Clk	IN	IN	DRIVE 0



2.10.15 Reset and Miscellaneous Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3
RSTIN#	I HVCMOS	DRIVE 0	DRIVE 1	DRIVE 0
PWROK	I HVCMOS	DRIVE 0	DRIVE 1	DRIVE 0
H_BSEL [2:0] (CFG[2:0])	I HVCMOS	PD	STRAP	DRIVE 0
CFG[17:3]	I AGTL+	PD	STRAP	PU
EXT_TS[1:0]#	I HVCMOS	PU	PU	PU
ICH_SYNC#	O HVCMOS	PU	DRIVE 1	TRI

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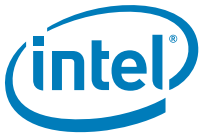

3 (G)MCH Register Description

3.1 Register Terminology

The following table shows the register-related terminology used in this datasheet. For general terminology, refer to the Section 1.9.

(Sheet 1 of 2)

Abbreviation	Definition
RO	**Read Only bit(s).** Writes to these bits have no effect. This may be a status bit or a static value.
RS/WC	**Read Set / Write Clear bit(s).** The first time the bit is read with an enabled byte, it returns the value 0, but a side-effect of the read is that the value changes to 1. Any subsequent reads with enabled bytes return a 1 until a 1 is written to the bit. When the bit is read, but the byte is not enabled, the state of the bit does not change, and the value returned is irrelevant, but will match the state of the bit. When a 0 is written to the bit, there is no effect. When a 1 is written to the bit, its value becomes 0, until the next byte-enabled read. When the bit is written, but the byte is not enabled, there is no effect.
R/W	**Read / Write bit(s).** These bits can be read and written by software. Hardware may only change the state of this bit by reset.
R/WC	**Read / Write Clear bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/WC/S	**Read / Write Clear / Sticky bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to 0 the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express* related bits a cold reset is "Power Good Reset" as defined in the current *PCI Local Bus Specification*).
R/W/B	**Read / Write / Blind bit(s).** These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit.
R/W/K	**Read / Write / Key bit(s).** These bits can be read and written by software. Additionally this bit, when set, prohibits some other bit field(s) from being writable (bit fields become Read Only).
R/W/L	**Read / Write / Lockable bit(s).** These bits can be read and written by software. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writable (bit field becomes Read Only).
R/W/L/K	**Read / Write / Lockable / Key bit(s).** These bits can be read and written by software. Additionally this bit is a Key bit that, when set, prohibits this bit field and/or some other specified bit fields from being writable (bit fields become Read Only).

(Sheet 2 of 2)

Abbreviation	Definition
R/W/S	**Read / Write / Sticky bit(s).** These bits can be read and written by software. Bits are not cleared by “warm” reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the current *PCI Local Bus Specification*).
R/WSC	**Read / Write Self Clear bit(s).** These bits can be read and written by software. When the bit is 1, hardware may clear the bit to 0 based upon internal events, possibly sooner than any subsequent software read could retrieve a 1.
R/WSC/L	**Read / Write Self Clear / Lockable bit(s).** These bits can be read and written by software. When the bit is 1, hardware may clear the bit to 0 based upon internal events, possibly sooner than any subsequent software read could retrieve a 1. Additionally there is a bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writable (bit field becomes Read Only).
R/WC	**Read Write Clear bit(s).** These bits can be read and written by software. However, a write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/WO	**Write Once bit(s).** Once written by software, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	**Write Only.** These bits may be written by software, but will always return 0’s when read. They are used for write side-effects. Any data written to these registers cannot be retrieved.

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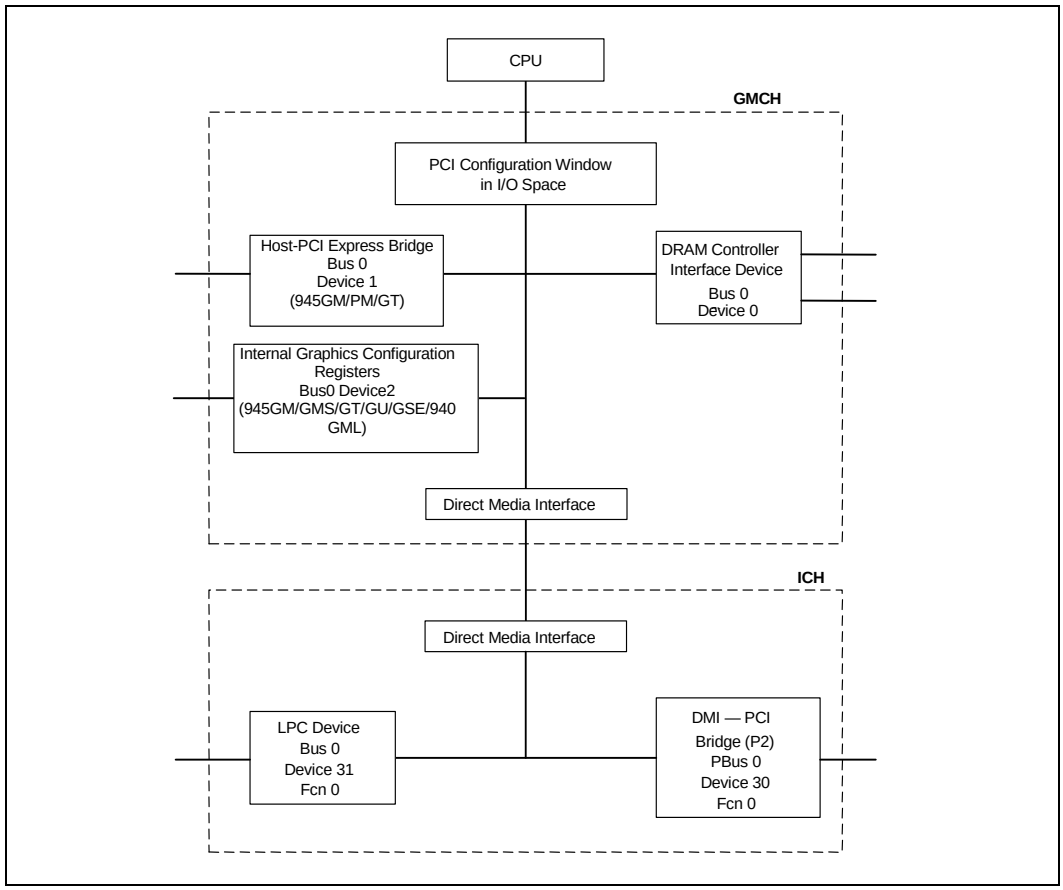
4 (G)MCH Configuration Process and Registers

4.1 Platform Configuration Structure

The DMI physically connects the (G)MCH and the ICH; so, from a configuration standpoint, the DMI is logically PCI Bus 0. As a result, all devices internal to the (G)MCH and the ICH appear to be on PCI Bus 0. The system's primary PCI expansion bus is physically attached to the ICH and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI bus number. The PCI Express Graphics Attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI Bus 0.

Note: That a physical PCI Bus 0 does not exist and that DMI and the internal devices in the (G)MCH and ICH logically constitute PCI Bus 0 to configuration software. This is shown in the following figure.

Figure 4. Conceptual Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset Platform PCI Configuration Diagram



The (G)MCH contains four PCI devices within a single physical component. The configuration registers for the four devices are mapped as devices residing on PCI Bus 0.

Device 0: Host Bridge/DRAM Controller. Logically this appears as a PCI device residing on PCI Bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), configuration for the DMI, and other (G)MCH specific registers.

Device 1: Host-PCI Express Bridge. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI Bus 0 and is compliant with the current *PCI Local Bus Specification*. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.

Device 2: Internal Graphics Control. Logically, this appears as a PCI device residing on PCI Bus 0. Physically, Device 2 contains the configuration registers for 3D, 2D, and display functions.

4.2 Routing Configuration Accesses

The (G)MCH supports two PCI related interfaces: DMI and PCI Express. PCI and PCI Express configuration cycles are selectively routed to one of these interfaces. The (G)MCH is responsible for routing configuration cycles to the proper interface. Configuration cycles to the ICH internal devices and Primary PCI (including downstream devices) are routed to the ICH via DMI. Configuration cycles to both the PCI Express Graphics PCI compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port.

A detailed description of the mechanism for translating CPU I/O bus cycles to configuration cycles is described below.

4.2.1 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based configuration space that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The *PCI Local Bus Specification* defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the CPU. Configuration space is supported by a mapping mechanism implemented within the (G)MCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the (G)MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The (G)MCH is responsible for translating and routing the CPU's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal (G)MCH configuration registers, DMI or PCI Express.

4.2.2 Logical PCI Bus 0 Configuration Mechanism

The (G)MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device. The host-DMI bridge entity within the (G)MCH is hardwired as Device 0 on PCI Bus 0. The host-PCI Express bridge entity within the (G)MCH is hardwired as Device 1 on PCI Bus 0. Device 2 contains the control registers for the Integrated Graphics Controller. The ICH decodes the Type 0 access and generates a configuration access to the selected internal device.

4.2.3 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and falls outside the range claimed by the host-PCI Express bridge (not between the upper bound of the bridge device's SUBORDINATE BUS NUMBER register and the lower bound of the bridge device's SECONDARY BUS NUMBER register), the (G)MCH will generate a Type 1 DMI Configuration Cycle. A[1:0] of the DMI request packet for the Type 1 configuration cycle will be "01". Bits 31:2 of the CONFIG_ADDRESS register will be translated to the A[31:2] field of the DMI request packet of the configuration cycle as shown below. This DMI configuration cycle will be sent over the DMI.

If the cycle is forwarded to the ICH via the DMI, the ICH compares the non-zero Bus Number with the SECONDARY BUS NUMBER and SUBORDINATE BUS NUMBER registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH's devices, the DMI, or a downstream PCI bus.

Figure 5. DMI Type 0 Configuration Address Translation

CONFIG_ADDRESS

31	30:28	27:24	23:16	15:11	10:8	7:2	1	0
1	Re-served	0	**0**	Device Number	Func-tion	Register Number	x	x

DMI Type 0 Configuration Address Extension

31:12	11:8	7:2	1	0
Reserved	Device Number	Func-tion	Register Number	0	**0**

Figure 6. DMI Type 1 Configuration Address Translation

CONFIG_ADDRESS

31	28	27	24	23	16	15	11	10	8	7	2	1	0
1	Re-served		0		**Bus Number**		Device Number		Func-tion		Register Number	x	x

DMI TYPE 1 CONFIGURATION ADDRESS EXTENSION

31	28	27	24	23	16	15	11	10	8	7	2	1	0
Reserved					**Bus Number**		Device Number		Func-tion		Register Number	0	**1**

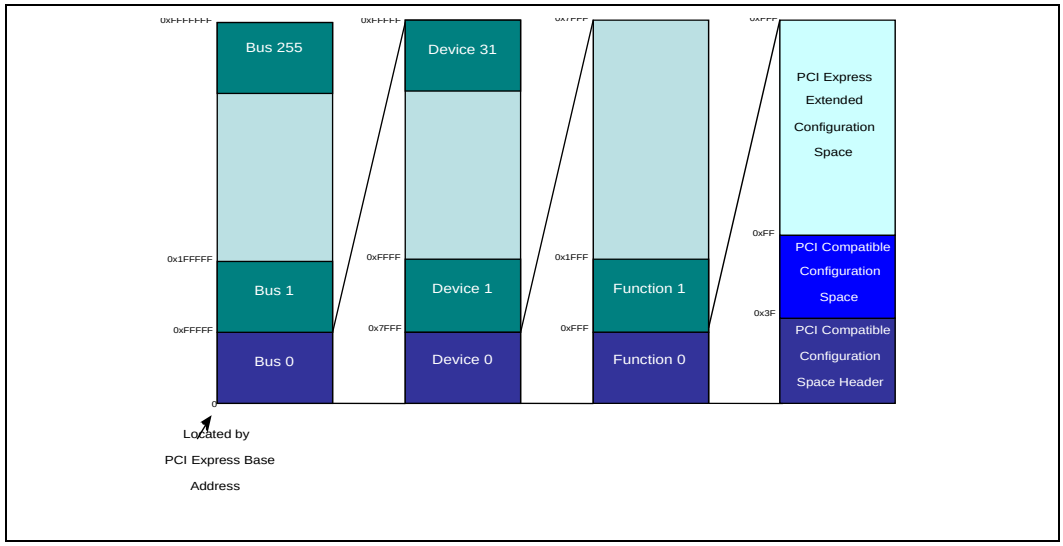
4.2.4 PCI Express Enhanced Configuration Mechanism

PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by the *PCI Local Bus Specification*. PCI Express configuration space is divided into a conventional PCI 2.3-compatible region, which consists of the first 256 bytes of a logical device's configuration space and a PCI Express extended region, which consists of the remaining configuration space.

The PCI-compatible region can be accessed using either the mechanism defined in the previous section or using the enhanced PCI Express configuration access mechanism described in this section. The extended configuration registers may only be accessed using the enhanced PCI Express configuration access mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the dword to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The enhanced PCI Express configuration access mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. PCIEXBAR defines the base address for a 64-, 128-, or 256-MB block of addresses below the top of addressable memory (currently 4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The PCI Express Configuration Transaction Header includes an additional 4 bits (Extended Register Address[3:0]) between the function number and register address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all 0's.

Figure 7. Memory Map to PCI Express Device Configuration Space



As with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

To access this space (steps 1, 2, 3 are done only once by BIOS):

1. Use the PCI-compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 31 of the DEVEN register.
2. Use the PCI-compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register.
3. Calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32 KB) + (function number * 4 KB) + (1 B * offset within the function) = host address).
4. Use a memory write or memory read cycle to the calculated host address to write to or read from that register.

31	28	27	20	19	15	14	12	11	8	7	2	1	0
Base		Bus		Device		Func.		Extended		Register Number		x	x

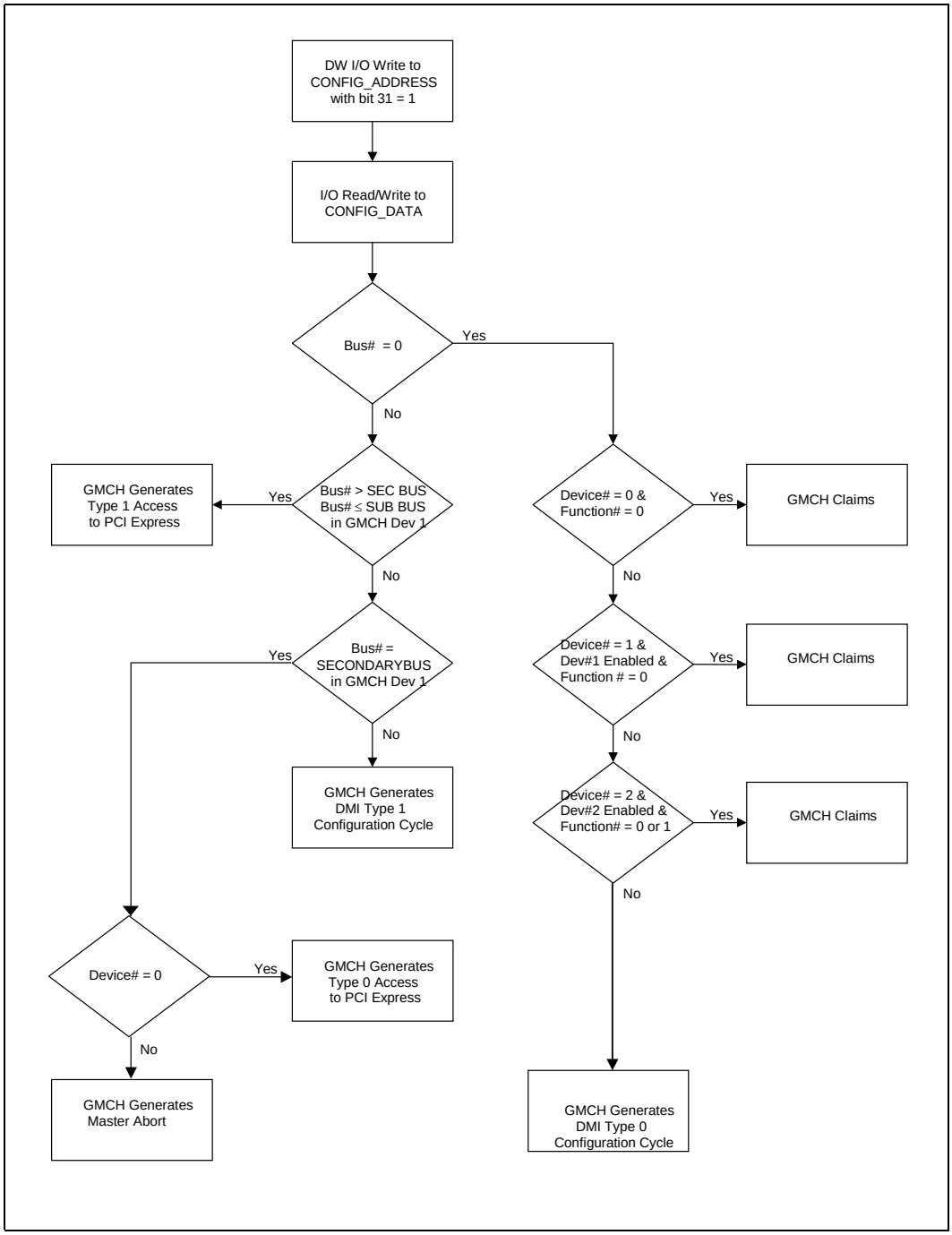
PCI Express configuration writes:

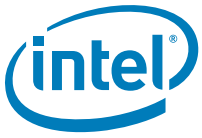
- Internally the host interface unit will translate writes to PCI Express extended configuration space to configurations on the backbone.
- The host interface unit will treat the posted write as a non-posted write internal to the host interface unit.
- Writes to extended space are posted on the FSB, but non-posted on the PEG or DMI pins (i.e., translated to configuration writes).

See the current *PCI Local Bus Specification* for more information on both the conventional PCI 2.3 compatible and PCI Express enhanced configuration mechanism and transaction rules.

4.2.5 (G)MCH Configuration Cycle Flowchart

Figure 8. (G)MCH Configuration Cycle Flowchart





4.3 (G)MCH Register Introduction

The (G)MCH contains two sets of software accessible registers, accessed via the host CPU I/O address space: Control registers and internal configuration registers.

1. Control registers are I/O mapped into the CPU I/O space, which control access to PCI and PCI Express configuration space (see section entitled I/O Mapped registers).
2. Internal configuration registers residing within the (G)MCH are partitioned into four logical device register sets (“logical” since they reside within a single physical device). The first register set is dedicated to host bridge functionality (i.e., DRAM configuration, other chipset operating parameters and optional features). The second register block is dedicated to host-PCI Express bridge functions (controls PCI Express interface configurations and operating parameters). The third register block is for the internal graphics functions.

The (G)MCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the host CPU. The registers that reside within the lower 256 bytes of each device can be accessed as byte, word (16-bit), or dword (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a dword. All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in dword (32-bit) quantities.

Some of the (G)MCH registers described in this section contain reserved bits. These bits are labeled Reserved. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the configuration address register.

In addition to reserved bits within a register, the (G)MCH contains address locations in the configuration space of the host bridge entity that are marked either “Reserved” or “Intel Reserved”. The (G)MCH responds to accesses to “Reserved” address locations by completing the host cycle. When a Reserved register location is read, a 0 value is returned. (Reserved registers can be 8, 16, or 32 bits in size). Writes to Reserved registers have no effect on the (G)MCH. Registers that are marked as Intel Reserved must not be modified by system software. Writes to Intel Reserved registers may cause system failure. Reads from Intel Reserved registers may return a non-zero value.

Upon a Full Reset, the (G)MCH sets its entire set configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the (G)MCH registers accordingly.

4.4 I/O Mapped Registers

The (G)MCH contains two registers that reside in the CPU I/O address space – the Configuration Address (CONFIG_ADDRESS) register and the Configuration Data (CONFIG_DATA) register. The Configuration Address register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

4.4.1 CONFIG_ADDRESS—Configuration Address Register

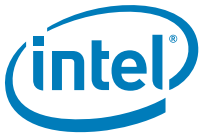
I/O Address: 0CF8h Accessed as a DW

Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DW. A byte or word reference will “pass through” the Configuration Address register and DMI onto the PCI_A bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

(Sheet 1 of 2)

Bit	Access & Default	Description
31	R/W 0b	**Configuration Enable (CFGE):** When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
30:24	RO 00h	**Reserved**
23:16	R/W 00h	**Bus Number:** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus 0 agent. If this is the case and the (G)MCH is not the target (i.e., the device number is >= 3 and not equal to 7), then a DMI Type 0 Configuration Cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by Device 1’s SECONDARY BUS NUMBER or SUBORDINATE BUS NUMBER register, then a DMI Type 1 Configuration Cycle is generated. If the Bus Number is non-zero and matches the value programmed into the SECONDARY BUS NUMBER register of Device 1, a Type 0 PCI Configuration Cycle will be generated on PCI Express-G*. If the Bus Number is non-zero, greater than the value in the SECONDARY BUS NUMBER register of Device 1 and less than or equal to the value programmed into the SUBORDINATE BUS NUMBER register of Device 1 a Type 1 PCI Configuration Cycle will be generated on PCI Express-G. This field is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 Configuration Cycles.
15:11	R/W 00h	**Device Number:** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is “00” the (G)MCH decodes the Device Number field. The (G)MCH is always Device Number 0 for the host bridge entity, Device Number 1 for the host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0,1, 2 or 7 the internal (G)MCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express and DMI Configuration Cycles.



(Sheet 2 of 2)

Bit	Access & Default	Description
10:8	R/W 000b	**Function Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The (G)MCH ignores Configuration Cycles to its internal Devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express and DMI Configuration Cycles.
7:2	R/W 00h	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address register. This field is mapped to byte 7 [7:2] of the request header format for during PCI Express and DMI Configuration Cycles.
1:0	RO 00b	**Reserved**

4.4.2 CONFIG_DATA—Configuration Data Register

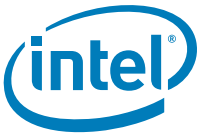
I/O Address: 0CFCh

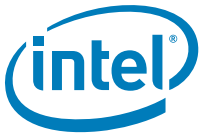
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	R/W 0000 0000 h	**Configuration Data Window (CDW):** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

§





5 Host Bridge Device 0 - Configuration Registers (D0:F0)

Warning: Address locations that are not listed are considered Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

5.1 Device 0 Configuration Registers

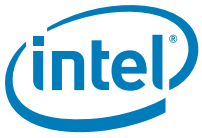
Table 3. Device 0 Configuration Registers (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	0	1	8086h	RO
Device Identification	DID	2	3	27A0h[1] 27ACh[2]	RO
PCI Command	PCICMD	4	5	0006h	R/W; RO
PCI Status	PCISTS	6	7	0090h	R/WC; RO
Revision Identification	RID	8	8	00h	RO
Class Code	CC	9	B	060000h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HDR	E	E	00h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	E0h	RO
Egress Port Base Address	EPBAR	40	43	00000000h	R/W/L; RO
(G)MCH Memory Mapped Register Range Base	MCHBAR	44	47	00000000h	R/W/L; RO
PCI Express* Register Range Base Address	PCIEXBAR	48	4B	E0000000h	R/W/L; RO
MCH-ICH Serial Interconnect Ingress Root Complex	DMIBAR	4C	4F	00000000h	R/W/L; RO
(G)MCH Graphics Control Register (Device 0)	GGC	52	53	0030h	R/W/L; RO
Device Enable	DEVEN	54	57	0000001Bh	R/W/L; RO
Reserved		60	63		
Programmable Attribute Map 0	PAM0	90	90	00h	R/W/L; RO
Programmable Attribute Map 1	PAM1	91	91	00h	R/W/L; RO
Programmable Attribute Map 2	PAM2	92	92	00h	R/W/L; RO

Table 3. Device 0 Configuration Registers (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Programmable Attribute Map 3	PAM3	93	93	00h	R/W/L; RO
Programmable Attribute Map 4	PAM4	94	94	00h	R/W/L; RO
Programmable Attribute Map 5	PAM5	95	95	00h	R/W/L; RO
Programmable Attribute Map 6	PAM6	96	96	00h	R/W/L; RO
Legacy Access Control	LAC	97	97	00h	R/W/L; RO
Reserved		98	9B		
Top of Low Used DRAM Register	TOLUD	9C	9C	08h	R/W/L; RO
System Management RAM Control	SMRAM	9D	9D	02h	R/W/L; RO
Extended System Management RAM Control	ESMRAMC	9E	9E	38h	R/W/L; R/WC; RO
Reserved		A0	A1		
Error Status	ERRSTS	C8	C9	0000h	R/WC; ROR/ WC/S
Error Command	ERRCMD	CA	CB	0000h	R/W; RO
Reserved		CC	CF		
Scratchpad Data	SKPD	DC	DF	00000000h	R/W
Capability Identifier	CAPID0	E0	E8		RO
Reserved		F8	FF		

NOTES:
1. Valid for all Mobile Intel 945 Express Chipsets except for the Mobile Intel 945GME/GSE Express Chipset.
2. Valid for the Mobile Intel 945GME/GSE Express Chipset only.



5.1.1 VID - Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 00-01h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

5.1.2 DID - Device Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 02-03h
Default Value: 27A0h[1]
27ACh[2]
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	27A0h[1] 27ACh[2]	**Device Identification Number (DID):** Identifier assigned to the (G)MCH core/primary PCI device.

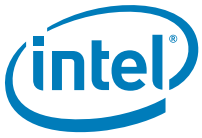
NOTES:
1. Valid for all Mobile Intel 945 Express Chipsets except for the Mobile Intel 945GME/GSE Express Chipset.
2. Valid for the Mobile Intel 945GME/GSE Express Chipset only.

5.1.3 PCICMD - PCI Command

B/D/F/Type: 0/0/0/PCI
Address Offset: 04-05h
Default Value:0006h
Access: R/W; RO
Size: 16 bits

Since MCH Device 0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Access	Default Value	Description
15:10	RO	00h	**Reserved**
9:9	RO	0b	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back write. Since Device 0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect.
8:8	R/W	0b	**SERR Enable (SERRE):** This bit is a global enable bit for Device 0 SERR messaging. The (G)MCH does not have an SERR signal. The (G)MCH communicates the SERR condition by sending an SERR message over (G)MCH ICH Serial Interface (DMI) to the ICH. If this bit is set to a 1, the (G)MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. If SERRE is clear, then the SERR message is not generated by the (G)MCH for Device 0. Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring on their respective devices. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7:7	RO	0b	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6:6	RO	0b	**Parity Error Enable (PERRE):** PERRB is not implemented by the MCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5:5	RO	0b	**VGA Palette Snoop Enable (VGASNOOP):** The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4:4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** The MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3:3	RO	0b	**Special Cycle Enable (SCE):** The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2:2	RO	1b	**Bus Master Enable (BME):** The MCH is always enabled as a master on DMI. This bit is hardwired to a 1. Writes to this bit position have no effect.
1:1	RO	1b	**Memory Access Enable (MAE):** The MCH always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0:0	RO	0b	**I/O Access Enable (IOAE):** This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.



5.1.4 PCISTS - PCI Status

B/D/F/Type: 0/0/0/PCI
Address Offset: 06-07h
Default Value: 0090h
Access: R/WC; RO
Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since MCH Device 0 does not physically reside on PCI_A, many of the bits are not implemented.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:15	RO	0b	**Detected Parity Error (DPE):** The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14:14	R/WC	0b	**Signaled System Error (SSE):** This bit is set to 1 when the MCH Device 0 generates an SERR message over DMI for any enabled Device 0 error condition or. Device 0 error conditions are enabled in the PCICMD and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS or ERRSTS registers. Software clears this bit by writing a 1 to it.
13:13	R/WC	0b	**Received Unsupported Request (RURS):** This bit is set when the MCH generates a DMI request that receives a Unsupported request completion. Software clears this bit by writing a 1 to it.
12:12	R/WC	0b	**Received Completion Abort Status (RCAS):** This bit is set when the MCH generates a DMI request that receives a completion abort. Software clears this bit by writing a 1 to it.
11:11	RO	0b	**Signaled Target Abort Status (STAS):** The MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	RO	00b	**DEVSEL Timing (DEVT):** These bits are hardwired to 00. Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the MCH.
8:8	RO	0b	**Master Data Parity Error Detected (DPD):** PERR signaling and messaging are not implemented by the MCH therefore this bit is hardwired to 0. Writes to this bit position have no effect.
7:7	RO	1b	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the MCH.

(Sheet 2 of 2)

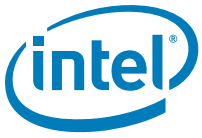
Bit	Access	Default Value	Description
6:5	RO	00b	**Reserved**
4:4	RO	1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the AGP Capability standard register resides.
3:0	RO	0h	**Reserved**

5.1.5 RID - Revision Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH Device 0.

Bit	Access	Default Value	Description
7:0	RO	02h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. For the A-0 Stepping, this value is 00h.



5.1.6 CC - Class Code

B/D/F/Type: 0/0/0/PCI
Address Offset: 09-0Bh
Default Value: 060000h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access	Default Value	Description
23:16	RO	06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the MCH. This code has the value 06h, indicating a bridge device.
15:8	RO	00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of bridge into which the MCH falls. The code is 00h indicating a host bridge.
7:0	RO	00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

5.1.7 MLT - Master Latency Timer

B/D/F/Type: 0/0/0/PCI
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the MCH is not a PCI master. Therefore this register is not implemented.

Bit	Access	Default Value	Description
7:0	RO	00h	**Reserved**

5.1.8 HDR - Header Type

B/D/F/Type: 0/0/0/PCI
Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

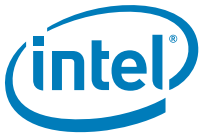
Bit	Access	Default Value	Description
7:0	RO	00h	**PCI Header (HDR):** This field always returns 0 to indicate that the MCH is a single function device with standard header layout. Reads and writes to this location have no effect.

5.1.9 SVID - Subsystem Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2C-2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access	Default Value	Description
15:0	R/WO	0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.



5.1.10 PAGE BREAKSID - Subsystem Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2E-2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access	Default Value	Description
15:0	R/WO	0000h	**Subsystem ID (SUBID):** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

5.1.11 CAPPTR - Capabilities Pointer

B/D/F/Type: 0/0/0/PCI
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access	Default Value	Description
7:0	RO	E0h	**Pointer to the Offset of the First Capability ID Register Block:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

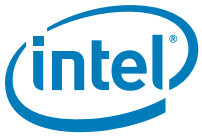
5.1.12 EPBAR - Egress Port Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 40-43h
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This is the base address for the Egress Port Root Complex MMIO configuration space. This window of addresses contains the Egress Port Root Complex register set for the PCI Express Hierarchy associated with the MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any conventional PCI 2.3-compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to bit[0] of this register.

Bit	Access	Default Value	Description
31:12	R/W/L	00000h	**Egress Port RCRB Base Address:** This field corresponds to bits 31 to 12 of the base address Egress port RCRB MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the Egress Port RCRB and associated registers.
11:1	RO	000h	**Reserved**
0	R/W/L	0b	**EPBAR Enable (EPBAREN):** 0: EPBAR is disabled and does not claim memory. 1: EPBAR memory mapped accesses are claimed and decoded appropriately.



5.1.13 MCHBAR - (G)MCH Memory Mapped Register Range Base

B/D/F/Type: 0/0/0/PCI

Address Offset: 44-47h

Default Value: 00000000h

Access: R/W/L; RO

Size: 32 bits

This is the base address for the MCH MMIO Configuration space. There is no physical memory within this 16-KB window that can be addressed. The 16 KB reserved by this register does not alias to any conventional PCI 2.3-compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to bit[0] of this register.

Bit	Access	Default Value	Description
31:14	R/W/L	00000h	**(G)MCH Memory Map Base Address:** This field corresponds to bits 31 to 14 of the base address MCHBAR configuration space. BIOS will program this register resulting in a base address for a 16-KB block of contiguous memory address space. This register ensures that a naturally aligned 16-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the MCH register set.
13:1	RO	0000h	**Reserved**
0	R/W/L	0b	**MCHBAR Enable (MCHBAREN):** 0: MCHBAR is disabled and does not claim any memory. 1: MCHBAR memory mapped accesses are claimed and decoded appropriately.

5.1.14 PCIEXBAR - PCI Express Register Range Base Address

B/D/F/Type:	0/0/0/PCI
Address Offset:	48-4Bh
Default Value:	E0000000h
Access:	R/W/L; RO
Size:	32 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express hierarchy associated with the (G)MCH. There is no actual physical memory within this address range (64 MB, 128 MB, or 256 MB) window that can be addressed. Each PCI Express hierarchy requires a PCI Express BASE register. The (G)MCH supports one PCI Express hierarchy.

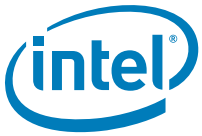
The address range reserved by this register does not alias to any conventional PCI 2.3-compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to bit[0] of this register.

The PCI Express Base Address [bits 15:12] must never be set to 0Fh because this would result in PCI Express configuration space overlapping the HSEG space required for the Intel® Pentium® 4 processor to respond to interrupts and system management events. The PCI Express Base Address cannot be below the address written to the top of low usable dram register (TOLUD).

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31:28	R/W/L	1110b	**PCI Express* Base Address:** This field corresponds to bits 31 to 28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a 256-MB block of contiguous memory address space. Having control of those particular 4 bits insures that this base address will be on a 256-MB boundary, above the lowest 256 MB and still within total addressable memory space, currently 4 GB. Configuration software will read this register to determine where the 256-MB range of addresses resides for this particular host bridge. The address used to access the PCI Express configuration space for a specific device can be determined as follows: *PCI Express Base Address + Bus Number * 1 MB + Device Number * 32 KB + Function Number * 4 KB* The address used to access the PCI Express configuration space for **Device 1** in this component would be as follows. *PCI Express Base Address + 0 * 1 MB + 1 * 32 KB + 0 * 4 KB =* **PCI Express Base Address + 32 KB**. ***Note:*** This address is at the beginning of the 4-KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.



(Sheet 2 of 2)

Bit	Access	Default Value	Description
27	R/W/L	0b	**128-MB Address Mask:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
26	R/W/L	0b	**64-MB Base Address Mask:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
25:3	RO	000000h	**Reserved**
2:1	R/W/L	00b	**Length:** This field describes the length of this region - Enhanced Configuration Space Region/Buses Decoded 00: 256 MB (Buses 0-255). Bits 31:28 are decoded in the PCI Express Base Address field. 01: 128 MB (Buses 0-127). Bits 31:27 are decoded in the PCI Express Base Address field. 10: 64 MB (Buses 0-63). Bits 31:26 are decoded in the PCI Express Base Address field. 11: Reserved
0	R/W/L	0b	**PCIEXBAR Enable (PCIEXBAREN):** 0: PCIEXBAR register is disabled. Memories read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR register bits 31:28 are R/W with no functionality behind them. 1: The PCIEXBAR register is enabled. Memories read and write transactions whose address bits 31:28 match PCIEXBAR 31:28 will be translated to configuration reads and writes within the (G)MCH. These translation cycles are routed as shown in the tables above.

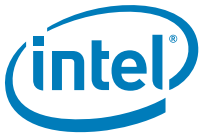
5.1.15 DMIBAR - MCH-ICH Serial Interconnect Ingress Root Complex

B/D/F/Type: 0/0/0/PCI
Address Offset: 4C-4Fh
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This is the base address for the DMI Root Complex MMIO configuration space. This window of addresses contains the DMI Root Complex register set for the PCI Express Hierarchy associated with the MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any conventional PCI 2.3-compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to bit[0] of this register.

Bit	Access	Default Value	Description
31:12	R/W/L	00000h	**DMI Root Complex MMIO Register Set Base Address:** This field corresponds to bits 31 to 12 of the base address DMI RCRB MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the DMI RCRB registers.
11:1	RO	000h	**Reserved**
0	R/W/L	0b	**DMIBAR Enable (DMIBAREN):** 0: DMIBAR is disabled and does not claim any memory. 1: DMIBAR memory mapped accesses are claimed and decoded appropriately.



5.1.16 GGC - (G)MCH Graphics Control (Device 0)

B/D/F/Type: 0/0/0/PCI
Address Offset: 52-53h
Default Value: 0030h
Access: R/W/L; RO
Size: 16 bits

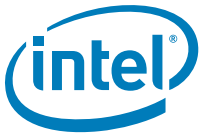
Bit	Access	Default Value	Description
15:7	RO	00000000 0b	**Reserved**
6:4	R/W/L	011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. *Stolen Memory Bases is located between (TOLUD - SMSize) to TOUD.* 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0. Class Code register is 80. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. Others = Reserved ***Note:***This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.
3:2	RO	00b	**Reserved**
1	R/W/L	0b	**IGD VGA Disable (IVD)** 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80. 0: Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.
0	RO	0b	**Reserved**

5.1.17 DEVEN - Device Enable

B/D/F/Type: 0/0/0/PCI
Address Offset: 54-57h
Default Value: 0000001Bh
Access: R/W/L; RO
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the MCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access	Default Value	Description
31:5	RO	000000h	**Reserved**
4	R/W/L	1b	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden. 1: Bus 0 Device 2 Function 1 is enabled and visible.
3	R/W/L	1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden 1: Bus 0 Device 2 Function 0 is enabled and visible
2	RO	0b	**Reserved**
1	R/W/L	1b	**PCI Express* Graphics Port Enable (D1EN):** 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by SDVO presence HW strap and SDVO/PCIe concurrent HW strap.
0	RO	1b	**Host Bridge:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.



5.1.18 PAM0 - Programmable Attribute Map 0

B/D/F/Type:	0/0/0/PCI
Address Offset:	90h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h-0FFFFFh.

The MCH allows programmable memory attributes on 13 legacy memory segments of various sizes in the 640-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE = 1, the CPU read accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.

WE - Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM register controls two regions, typically 16 KB in size.

Accesses to the entire PAM region (000C_0000h to 000F_FFFFh) from DMI and PCI Express Graphics Attach low priority will be forwarded to main memory. The PAM read enable and write enable bits are not functional for these accesses. In other words, a full set of PAM decode/attribute logic is not being implemented. Also note that the MCH may hang if a PCI Express Graphics Attach or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM). For these reasons the following critical restriction is placed on the programming of the PAM regions:

At the time that a DMI or PCI Express Graphics Attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

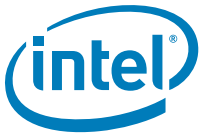
Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0F0000h-0FFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0F0000h to 0FFFFFh. 00:DRAM Disabled: All accesses are directed to DMI. 01:Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10:Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11:Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0	RO	0h	**Reserved**

5.1.19 PAM1 - Programmable Attribute Map 1

B/D/F/Type: 0/0/0/PCI
Address Offset: 91h
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h-0C7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0C4000h-0C7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000h to 0C7FFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**



Bit	Access	Default Value	Description
1:0	R/W/L	00b	**0C0000h-0C3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.20 PAM2 - Programmable Attribute Map 2

B/D/F/Type: 0/0/0/PCI
Address Offset: 92h
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h-0CFFFFh.

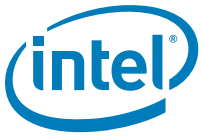
Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0CC000h-0CCFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0CC000h to 0CCFFFh. 00:DRAM Disabled: Accesses are directed to DMI. 01:Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10:Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11:Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0C8000h-0CBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.21 PAM3 - Programmable Attribute Map 3

B/D/F/Type: 0/0/0/PCI
Address Offset: 93h
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h-0D7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0D4000h-0D7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0D0000-0D3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000 to 0D3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.



5.1.22 PAM4 - Programmable Attribute Map 4

B/D/F/Type:	0/0/0/PCI
Address Offset:	94h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h-0DFFFFh.

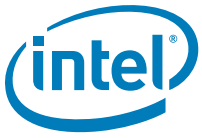
Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0DC000h-0DFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0D8000h-0DBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.23 PAM5 - Programmable Attribute Map 5

B/D/F/Type: 0/0/0/PCI
Address Offset: 95h
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h-0E7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0E4000h-0E7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0E0000h-0E3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.



5.1.24 PAM6 - Programmable Attribute Map 6

B/D/F/Type: 0/0/0/PCI
Address Offset: 96h
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h-0EFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0EC000h-0EFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0E8000h-0EBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

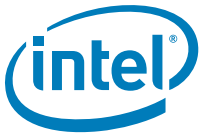
5.1.25 LAC - Legacy Access Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 97h
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15-16 MB.

Bit	Access	Default Value	Description
7	R/W/L	0b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies “behind” this space is not remapped. 0: No memory hole. 1: Memory hole from 15 MB to 16 MB.
6:1	RO	00h	**Reserved**
0	R/W	0b	**MDA Present (MDAP):** This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if Device 1's VGA Enable bit is not set. If Device 1's VGA enable bit is not set, then accesses to IO address range 03BCh-03BFh are forwarded to DMI. If the VGA enable bit is set and MDA is not present, then accesses to IO address range 03BCh-03BFh are forwarded to PCI Express-G* if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to DMI. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh (including ISA address aliases, A[15:10] are not used in decode). Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to DMI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA:

VAGEN	MDAP	Description
0	0	All references to MDA and VGA space are routed to HI
0	1	Illegal Combination
1	0	All VGA and MDA references are routed to PCI Express Graphics Attach
1	1	All VGA references are routed to PCI Express Graphics Attach.MDA references are routed to HI.



5.1.26 TOLUD - Top of Low Used DRAM Register

B/D/F/Type: 0/0/0/PCI

Address Offset: 9Ch

Default Value: 08h

Access: R/W/L; RO

Size: 8 bits

This 8-bit register defines the Top of Usable Dram. Graphics Stolen Memory and TSEG are within dram space defined under TOLUD. From the top of low used dram, (G)MCH claims 1 to 64 MBs of DRAM for internal graphics if enabled and 1, 2 or 8 MBs of DRAM for TSEG if enabled.

Note: Even if the OS does not need any PCI space, TOLUD can only be programmed to FFh. This ensures that addresses within 128 MB below 4 GB that are reserved for APIC.

Bit	Access	Default Value	Description
7:3	R/W/L	01h	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31 to 27 of an address one byte above the maximum DRAM memory that is usable by the operating system. Address bits [31:27] programmed to a “01h” implies a minimum memory size of 128 MBs. Configuration software must set this value to the smaller of the following 2 choices - maximum amount memory in the system - Minimum address allocated for PCI memory. Address bits 26:0 are assumed to be 000_0000h for the purposes of address comparison. The host interface positively decodes an address towards dram if the incoming address is less than that value programmed in this register. This register must **not** be set to 0000 0 b. The Top of Usable DRAM is the lowest address above both Graphics Stolen memory and TSEG. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD and further decrements by TSEG size to determine base of TSEG.
2:0	RO	00b	**Reserved**

5.1.27 SMRAM - System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Dh
Default Value: 02h
Access: R/W/L; RO
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access	Default Value	Description
7	RO	0b	**Reserved**
6	R/W/L	0b	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	R/W	0b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	R/W/L	0b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, GMS, TOLUD, TSEG_SZ, and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	R/W/L	0b	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the sections on SMM for more details. Once D_LCK is set, this bit becomes read only.

Bit	Access	Default Value	Description
2:0	RO	010b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the MCH supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.

5.1.28 ESMRAMC - Extended System Management RAM Control

B/D/F/Type: 0/0/0/PCI

Address Offset: 9Eh

Default Value: 38h

Access: R/W/L; R/WC; RO

Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Note: When Extended SMRAM is used, the maximum amount of DRAM accessible is limited to 256 MB.

(Sheet 1 of 2)

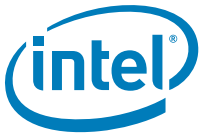
Bit	Access	Default Value	Description
7	R/W/L	0b	**Enable High SMRAM (H_SMRAME):** Controls the SMM memory space location (i.e., above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	R/WC	0b	**Invalid SMRAM Access (E_SMERR):** This bit is set when CPU has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO	1b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the MCH.
4	RO	1b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the MCH.

(Sheet 2 of 2)

Bit	Access	Default Value	Description
3	RO	1b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the MCH.
2:1	R/W/L	00b	**TSEG Size (TSEG_SZ):** Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled. **00** - 1-MB TSEG (TOLUD: Graphics Stolen Memory Size - 1 M) to (TOLUD - Graphics Stolen Memory Size). **01** - 2-MB Tseg (TOLUD: Graphics Stolen Memory Size - 2 M) to (TOLUD - Graphics Stolen Memory Size). **10** - 8-MB Tseg (TOLUD: Graphics Stolen Memory Size - 8 M) to (TOLUD - Graphics Stolen Memory Size). **11** - Reserved _LCK has been set, these bits become read only.
0	R/W/L	0b	**TSEG Enable (T_EN):** Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Once D_LCK is set, this bit becomes read only.

5.1.29 TOM - Top Of Memory

B/D/F/Type: 0/0/0/PCI
Address Offset: A0-A1h
Default Value: 0001h
Access: R/W/L; RO
Size: 16 bits



5.1.30 ERRSTS - Error Status

B/D/F/Type: 0/0/0/PCI

Address Offset: C8-C9h

Default Value: 0000h

Access: R/WC; ROR/WC/S

Size: 16 bits

This register is used to report various error conditions via the SERR messaging mechanism. An SERR message is generated on a 0-to-1 transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

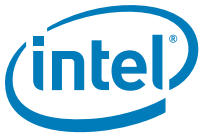
Bit	Access	Default Value	Description
15	RO	0b	**Reserved**
14	RO	0b	**Reserved**
13	RO	0b	**Reserved**
12	R/WC	0b	**(G)MCH Software Generated Event for SMI:** This indicates the source of the SMI was a Device 2 Software Event.
11	R/WC	0b	**(G)MCH Thermal Sensor Event for SMI/SCI/SERR:** Indicates that a (G)MCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, Smi command and Sci command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.
10	RO	0b	**Reserved**
9	R/WC	0b	**LOCK to Non-DRAM Memory Flag (LCKF):** When this bit is set to 1, the MCH has detected a lock operation to memory space that did not map into DRAM.
8	R/WC	0b	**Received Refresh Timeout Flag (RRTOF):** This bit is set when 1024 memory core refreshes are enqueued.
7	R/WC	0b	**DRAM Throttle Flag (DTF):** 1:Indicates that a DRAM Throttling condition occurred. 0:Software has cleared this flag since the most recent throttling event
6:0	R/WC	00h	**Reserved**

5.1.31 ERRCMD - Error Command

B/D/F/Type: 0/0/0/PCI
Address Offset: CA-CBh
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This register controls the MCH responses to various system errors. Since the MCH does not have an SERRB signal, SERR messages are passed from the MCH to the ICH over DMI. When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Access	Default Value	Description
15:13	RO	000b	**Reserved**
12	RO	0b	**Reserved**
11	R/W	0b	**SERR on (G)MCH Thermal Sensor Event (TSESERR):** 1: The MCH generates a SERR DMI special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0: Reporting of this condition via SERR messaging is disabled.
10	RO	0b	**Reserved**
9	R/W	0b	**SERR on LOCK to non-DRAM Memory (LCKERR):** 1: The MCH will generate a DMI SERR special cycle whenever a CPU lock cycle is detected that does not hit DRAM. 0: Reporting of this condition via SERR messaging is disabled.
8	R/W	0b	**SERR on DRAM Refresh Timeout (DRTOERR):** 1: The (G)MCH generates an SERR DMI special cycle when a DRAM Refresh timeout occurs. 0: Reporting of this condition via SERR messaging is disabled.
7	R/W	0b	**SERR on DRAM Throttle Condition (DTCERR):** 1: The (G)MCH generates an SERR DMI special cycle when a DRAM Read or Write Throttle condition occurs. 0: Reporting of this condition via SERR messaging is disabled.
6:0	RO	00h	**Reserved**



5.1.32 SKPD - Scratchpad Data

B/D/F/Type: 0/0/0/PCI
Address Offset: DC-DFh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access	Default Value	Description
31:0	R/W	00000000h	**Scratchpad Data:** 1 dword of data storage.

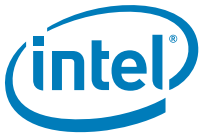
5.1.33 CAPID0 - Capability Identifier

B/D/F/Type: 0/0/0/PCI
Address Offset: E0-E8h
Default Value:
Access: RO
Size: 72 bits

This register identifies the capabilities of the chipset

Bit	Access	Default Value	Description
71:64	RO	08h	**Reserved**
63	RO	0b	**Reserved**
62:60	RO	000b	**(G)MCH Software Capability ID:** Used to communicate Graphics SKU information to the Graphics Driver software, which is then used by the driver to configure itself accordingly. This setting has no direct effect on hardware. 001: Mobile Intel® 945GM/GME Express Chipset 010: Mobile Intel® 945GMS/GU/GSE Express Chipset 110: Mobile Intel® 943/940GML Express Chipset 011: Mobile Intel® 945PM Express Chipset 101: Intel® 945GT Express Chipset Others: Reserved
59:54	RO		**Reserved**
53	RO	0b	**Integrated TVout Capable:** 0: (G)MCH capable of Integrated TV out. (Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset) 1: (G)MCH not capable of Integrated TV out. (Mobile Intel 945PM Express Chipset)
52	RO	0b	**Reserved**

Bit	Access	Default Value	Description
51:48	RO	0h	**Reserved**
47:44	RO	0h	**Reserved**
43:41	RO	000b	**Render Core Frequency Capability:** 000: 400-MHz operation (Intel 945GT Express Chipset) 010: 250-MHz operation (Mobile Intel 945GM/GME/GMS/GSE Express Chipset) 100: 166 MHz operation (Mobile Intel 943/940GML/GU Express Chipset) Others: Reserved ***Note:*** *Mobile Intel 945GMS/GSE Express Chipset render clock capability is set to 250 MHz but SW must program the render frequency to supported values, i.e., 166 MHz* ***Note:*** *Ultra Mobile Intel 945GU Express Chipset render clock capability is set to 250 MHz but SW must program the render frequency to supported values, i.e., 133 MHz*
40	RO	0b	**Reserved**
39	RO	0b	**Serial Digital Video Out Capable:** 0: (G)MCH capable of serial digital video output. (Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset) 1: (G)MCH not capable of serial digital video output. (Mobile Intel 945PM Express Chipset)
38	RO	0b	**Internal Graphics Capable:** 0: There is a graphics engine within this (G)MCH. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the (G)MCH. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI-to-PCI bridge control register in Device 1 (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the (G)MCH Control register). Graphics Memory is pre-allocated above TSEG Memory. (Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset) 1: There is no graphics engine within this (G)MCH. (Mobile Intel 945PM Express Chipset)
37:36	RO	00b	**Reserved**
35	RO	0b	**Concurrent PCI-E and SDVO Disable:** Controls whether concurrent use of PCI-E Graphics Port and SDVO is allowed. 0: Concurrent PCIe and SDVO is allowed. 1: Concurrent PCIe and SDVO is not allowed. PCIe functionality on the Externa GFX port is disabled if SDVO is present. Forces concurrent PCIe/SDVO strap deasserted if SDVO present strap is sampled asserted.



Bit	Access	Default Value	Description
34:32	RO	N/A	**DDR2 Frequency Capability:** 010:(G)MCH capable of up to DDR2-667 011:(G)MCH capable of up to DDR2-533 100:(G)MCH capable of DDR2-400 Others: Reserved This field controls which values may be written to the Memory Frequency Select field 6:4 of the Clocking Configuration register (MCHBAR Offset C00h). Any attempt to write an unsupported value will be ignored.
31:29	RO	N/A	**FSB Capability:** 011:(G)MCH capable of up to FSB 667 100: (G)MCH capable of up to FSB 533 Others: Reserved These values are determined by the BSEL [2:0] frequency straps. Any unsupported straps will render the (G)MCH host interface inoperable.
28	RO	0b	**Reserved**
27:24	RO	1h	**CAPID Version:** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO	09h	**CAPID Length:** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO	00h	**Next Capability Pointer:** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO	09h	**CAP_ID:** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

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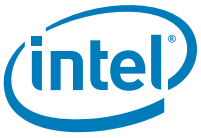
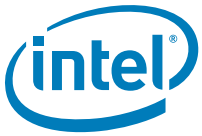




6 Device 0 Memory Mapped I/O Register

Note: All accesses to the memory mapped registers must be made as a single dword (4 bytes) or less. Access must be aligned on a natural boundary.

6.1 Device 0 Memory Mapped I/O Registers

A variety of timing and control registers have been moved to MMR space of Device 0 due to space constraints.

To simplify the read/write logic to the SRAM, BIOS is required to write and read 32-bit aligned dwords. The SRAM includes a separate Write Enable for every dword.

The BIOS read/write cycles are performed in a memory mapped IO range that is setup for this purpose in the PCI configuration space, via standard PCI range scheme.

6.2 Device 0 MCHBAR Chipset Control Registers

Table 4. Device 0 MCHBAR Chipset Control Registers (Sheet 1 of 6)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		00	39		
Front Side Bus Power Management Control 3	FSBPMC3	40	43	00000000h	R/W; RO
Front Side Bus Power Management Control 4	FSBPMC4	44	47	00000000h	R/W; RO
FSB Snoop Control	FSBSNPCTL	48	4B	80800000h	R/W; RO
Reserved		4C	8F		
CPU Sleep Timing Control	SLPCTL	90	93	00005055h	R/W; RO
Channel 0 DRAM Rank Boundary 0	C0DRB0	100	100	00h	R/W
Channel 0 DRAM Rank Boundary 1	C0DRB1	101	101	00h	R/W
Channel 0 DRAM Rank Boundary 2	C0DRB2	102	102	00h	R/W
Channel 0 DRAM Rank Boundary 3	C0DRB3	103	103	00h	R/W
Reserved		104	107		
Channel 0 DRAM Rank 0,1 Attribute	C0DRA0	108	108	00h	R/W; RO
Channel 0 DRAM Rank 2,3 Attribute	C0DRA2	109	109	00h	R/W; RO
Reserved		109	10B		
Channel 0 DRAM Clock Disable	C0DCLKDIS	10C	10C	00h	R/W; RO
Reserved		10D	10D		

Table 4. Device 0 MCHBAR Chipset Control Registers (Sheet 2 of 6)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Channel 0 DRAM Bank Architecture	C0BNKARC	10E	10F	0000h	R/W; RO
Channel 0 DRAM Timing Register 0	C0DRT0	110	113	B96038F8h	R/W; RO
Channel 0 DRAM Timing Register 1	C0DRT1	114	117	02607122h	R/W; RO
Channel 0 DRAM Timing Register 2	C0DRT2	118	11B	800003FFh	R/W; RO
Reserved		11C	11F		
Channel 0 DRAM Controller Mode 0	C0DRC0	120	123	40000802h	R/W; RO
Channel 0 DRAM Controller Mode 1	C0DRC1	124	127	00000000h	R/W; RO
Channel 0 DRAM Controller Mode 2	C0DRC2	128	12B	00000000h	R/W; RO
Reserved		12C	12F		
Channel 0 Adaptive Idle Timer Control	C0AIT	130	137	0000000000000000h	R/W; RO
Reserved		138	139		
Channel 0 (G)MCH Throttling Event Weights.	C0GTEW	140	143	00000000h	R/W/L
Channel 0 (G)MCH Throttling Control	C0GTC	144	147	00000000h	R/W/L; RO
Channel 0 Dram Rank Throttling Passive Event	C0DTPEW	148	14F	0000000000000000h	R/W/L; RO
Channel 0 Dram Rank Throttling Active Event	C0DTAEW	150	157	0000000000000000h	R/W/L
Channel 0 Dram Throttling Control	C0DTC	158	15B	00000000h	R/W/L; RO
Reserved		15C	163		
Channel 0 DRAM Maintenance Control	C0DMC	164	167	00000020h	R/W; RO
Channel 0 ODT Control	C0ODT	168	16F	0002879822049200h	R/W; RO
Channel 1 DRAM Rank Boundary Address 0	C1DRB0	180	180	00h	R/W
Channel 1 DRAM Rank Boundary Address 1	C1DRB1	181	181	00h	R/W
Reserved		182	187		
Channel 1 DRAM Rank 0,1 Attribute	C1DRA0	188	188	00h	R/W; RO
Reserved		189	18B		
Channel 1 DRAM Clock Disable	C1DCLKDIS	18C	18C	00h	R/W; RO
Reserved		18D	18D		
Channel 1 DRAM Bank Architecture	C1BNKARC	18E	18F	0000h	R/W; RO
Channel 1 DRAM Timing Register 0	C1DRT0	190	193	B96038F8h	R/W; RO

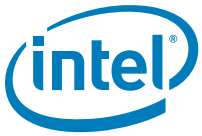


Table 4. Device 0 MCHBAR Chipset Control Registers (Sheet 3 of 6)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Channel 1 DRAM Timing Register 1	C1DRT1	194	197	02607122h	R/W; RO
Channel 1 DRAM Timing Register 2	C1DRT2	198	19B	800003FFh	R/W; RO
Reserved		19C	19F		
Channel 1 DRAM Controller Mode 0	C1DRC0	1A0	1A3	40000802h	R/W; RO
Channel 1 DRAM Controller Mode 1	C1DRC1	1A4	1A7	00000000h	R/W; RO
Channel 1 DRAM Controller Mode 2	C1DRC2	1A8	1AB	00000000h	R/W; RO
Reserved		1AC	1AF		
Channel 1 Adaptive Idle Timer Control	C1AIT	1B0	1B7	0000000000000000h	R/W; RO
Reserved		1B8	1BF		
Channel 1 (G)MCH Throttling Event Weights.	C1GTEW	1C0	1C3	00000000h	R/W/L
Channel 1 (G)MCH Throttling Control	C1GTC	1C4	1C7	00000000h	R/W/L; RO
Channel 1 Dram Rank Throttling Passive Event	C1DTPEW	1C8	1CF	0000000000000000h	R/W/L; RO
Channel 1 Dram Rank Throttling Active Event	C1DTAEW	1D0	1D7	0000000000000000h	R/W/L
Channel 1 Dram Throttling Control	C1DTC	1D8	1DB	00000000h	R/W/L; RO
Reserved		1DC	1E3		
Channel 1DRAM Maintenance Control	C1DMC	1E4	1E7	00000020h	R/W; RO
Reserved		1E8	1FF		
DRAM Channel Control	DCC	200	203	00000000h	R/W; RO
Reserved		204	217		
Write Cache Control	WCC	218	21B	A4000000h	R/W; RO
Reserved		21C	21F		
Main Memory Arbiter Control_0	MMARB0	220	223	00000264h	R/W; RO
Main Memory Arbiter Control_1	MMARB1	224	227	00000000h	R/W; RO
Reserved		228	22F		
SB Test Register	SBTEST	230	233	34020000h	R/W; RO
Reserved		234	283		
On Die Termination Control	ODTC	284	287	00000000h	
Reserved		288	2BF		
System Memory VREF Control	SMVREFC	2A0	2A0	08h	R/W/L; RO

Table 4. Device 0 MCHBAR Chipset Control Registers (Sheet 4 of 6)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		2A1	2AB		
DQS Master Timing	DQSMT	2F4	2F5	0007h	R/W/L
Reserved		2F6	2F7		
RCVENOUTB Master Timing	RCVENMT	2F8	2FB	0000070Fh	R/W/L; RO
Reserved		2FC	33F		
Channel 0 WL0 RCVENOUT Slave Timing	C0WL0REOST	340	340	00h	R/W/L; RO
Channel 0 WL1 RCVENOUT Slave Timing	C0WL1REOST	341	341	00h	R/W/L; RO
Channel 0 WL2 RCVENOUT Slave Timing	C0WL2REOST	342	342	00h	R/W/L; RO
Channel 0 WL3 RCVENOUT Slave Timing	C0WL3REOST	343	343	00h	R/W/L; RO
Reserved		344	35F		
Write DLL Bypass Mode Control	WDLLBYPMODE	360	361	0000h	R/W/L; RO
Reserved		362	36B		
Channel 0 WDLL/Clock Macro Clock Control	C0WDLLCMC	36C	36F	000000FFh	R/W/L; RO
Reserved		370	37B		
Channel 0 Half Clock Timing Control	C0HCTC	37C	37C	00h	R/W/L; RO
Reserved		37D	3BF		
Channel 1 WL0 RCVENOUT Slave Timing	C1WL0REOST	3C0	3C0	00h	R/W/L; RO
Channel 1 WL1 RCVENOUT Slave Timing	C1WL1REOST	3C1	3C1	00h	R/W/L; RO
Channel 1 WL2 RCVENOUT Slave Timing	C1WL2REOST	3C2	3C2	00h	R/W/L; RO
Channel 1 WL3 RCVENOUT Slave Timing	C1WL3REOST	3C3	3C3	00h	R/W/L; RO
Channel 1 WL0 RCVENOUT Slave Timing	C1WL0REOST	3C0	3C0	00h	R/W/L; RO
Reserved		3C1			
C1WDLLCMC - Channel 1 WDLL/ Clock Macro Clock Control		3EC	3EF	0000009Fh	R/W/L; RO
Reserved		3F0	3FB		
Channel 1 Half Clock Timing Control	C1HCTC	3FC	3FC	00h	R/W/L; RO
Reserved		3FD	3FF		

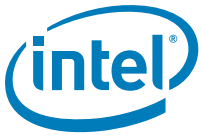


Table 4. Device 0 MCHBAR Chipset Control Registers (Sheet 5 of 6)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Global/System Memory RCOMP Control	GBRCOMPCTL	400	403		R/W/L; RO
Reserved		404	40B		
Channel 0 DRAM Width	C0DRAMW	40C	40D	0000h	R/W/L; RO
Reserved		40E	40F		
Group 1 Strength Control	G1SC	410	410	44h	R/W/L
Reserved		411	417		
Group 2 Strength Control	G2SC	418	418	44h	R/W/L
Reserved		419	41A		
Group 3 Strength Control	G3SC	420	420	44h	R/W/L
Reserved		421	427		
Group 4 Strength Control	G4SC	428	428	44h	R/W/L
Reserved		429	42A		
Group 5 Strength Control	G5SC	430	430	44h	R/W/L
Reserved		431	437		
Group 6 Strength Control	G6SC	438	438	44h	R/W/L
Reserved		439	48B		
Channel 1 DRAM Width	C1DRAMW	48C	48D	0000h	R/W/L; RO
Reserved		48E	48F		
Group 7 Strength Control	G7SC	490	490	44h	R/W/L
Reserved		491	497		
Group 8 Strength Control	G8SC	498	498	44h	R/W/L
Reserved		499	49F		
Group 1 Slew Rate Pull-up Table	G1SRPUT	500	51F		R/W/L; RO
Group 1 Slew Rate Pull-down Table	G1SRPDT	520	53F		R/W/L; RO
Group 2 Slew Rate Pull-up Table	G2SRPUT	540	55F		R/W/L; RO
Group 2 Slew Rate Pull-down Table	G2SRPDT	560	57F		R/W/L; RO
Group 3 Slew Rate Pull-up Table	G3SRPUT	580	59F		R/W/L; RO
Group 3 Slew Rate Pull-up Table	G3SRPDT	5A0	5BF		R/W/L; RO
Group 4 Slew Rate Pull-up Table	G4SRPUT	5C0	5DF		R/W/L; RO
Group 4 Slew Rate Pull-up Table	G4SRPDT	5E0	5FF		R/W/L; RO
Group 5 Slew Rate Pull-up Table	G5SRPUT	600	61F		R/W/L; RO

Table 4. Device 0 MCHBAR Chipset Control Registers (Sheet 6 of 6)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Group 5 Slew Rate Pull-down Table	G5SRPDT	620	63F		R/W/L; RO
Group 6 Slew Rate Pull-up Table	G6SRPUT	640	65F		R/W/L; RO
Group 6 Slew Rate Pull-down Table	G6SRPDT	660	67F		R/W/L; RO
Group 7 Slew Rate Pull-up Table	G7SRPUT	680	69F		R/W/L; RO
Group 7 Slew Rate Pull-down Table	G7SRPDT	6A0	6BF		R/W/L; RO
Group 8 Slew Rate Pull-up Table	G8SRPUT	6C0	6DF		R/W/L; RO
Group 8 Slew Rate Pull-down Table	G8SRPDT	6E0	6FF		R/W/L; RO
Memory Interface Power Management Control 3	MIPMC3	BD8	BDB	00000000h	R/W/L; RO
Unit Power Management Control 4	UPMC4	C30	C33	00000000h	R/W;mi

6.2.1 FSBPMC3 Front Side Bus Power Management Control 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 40-43h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

6.2.2 FSBPMC4 Front Side Bus Power Management Control 4

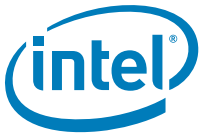
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 44-47h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

6.2.3 FSBSNPCTL- FSB Snoop Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 48-4Bh
Default Value: 00000000h

6.2.4 SLPCTL – CPU Sleep Timing Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 90-93h
Default Value: 00005055h
Access: R/W; RO
Size: 32 bits



6.2.5 C0DRB0 - Channel 0 DRAM Rank Boundary 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 100h
Default Value: 00h
Access: R/W
Size: 8 bits

The DRAM rank boundary register defines the upper boundary address of each DRAM rank with a granularity of 128 MB (256 Mbit, x16 devices). Each rank has its own single-byte DRB register. These registers are used to determine which chip select will be active for a given address.

Channel and Rank Map:

ch0 rank0	100h
ch0 rank1:	101h
ch0 rank2:	102h
ch0 rank3	103h
104h to 107h	Reserved
ch1 rank0:	180h
ch1 rank1:	181h

In all modes, if a DIMM is single sided, it appears as a populated rank and an empty rank. A DRB must be programmed appropriately for each.

Each rank is represented by a byte. Each byte has the following format:

Bit	Access	Default Value	Description
7:0	R/W	00h	**Channel 0 DRAM Rank Boundary Address:** This 8-bit value defines the upper and lower addresses for each DRAM rank. Bits 6:2 are compared against Address 31:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0's. Bit 7 may be programmed to a 1 in the highest DRB (DRB3) if 4 GBs of memory is present.

6.2.6 C0DRB1 - Channel 0 DRAM Rank Boundary 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 101h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

6.2.7 C0DRB2 - Channel 0 DRAM Rank Boundary 1

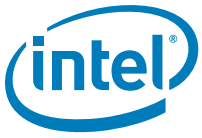
B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	102h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

6.2.8 C0DRB3 - Channel 0 DRAM Rank Boundary 1

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	103h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.



6.2.9 C0DRA0 - Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 108h
Default Value: 00h
Access: R/W; RO
Size: 8 bits

The DRAM rank attribute registers define the page sizes to be used when accessing different ranks. These registers should be left with their default value (all 0's) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks.

Channel and Rank Map:

Ch0 Rank 0,1: 108h
Ch0 Rank 2,3: 109h

Bit	Access	Default Value	Description
7:7	RO	0b	**Reserved**
6:4	R/W	000b	**Channel 0 DRAM Odd Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated 001: Reserved 010: 4 KB 011: 8 KB 100: 16 KB Others: Reserved
3:3	RO	0b	**Reserved**
2:0	R/W	000b	**Channel 0 DRAM Even Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated 001: Reserved 010: 4 KB 011: 8 KB 100: 16 KB Others: Reserved

6.2.10 C0DRA2 - Channel 0 DRAM Rank 2,3 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 109h
Default Value: 00h
Access: R/W; RO
Size: 8 bits

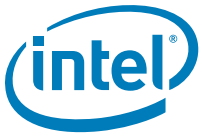
Bit	Access	Default Value	Description
7:7	RO	0b	**Reserved**
6:4	R/W	000b	**Channel 0 DRAM Odd Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated 001: Reserved 010: 4 KB 011: 8 KB 100: 16 KB Others: Reserved
3:3	RO	0b	**Reserved**
2:0	R/W	000b	**Channel 0 DRAM Even Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated 001: Reserved 010: 4 KB 011: 8 KB 100: 16 KB Others: Reserved

6.2.11 C0DCLKDIS - Channel 0 DRAM Clock Disable

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 10Ch
Default Value: 00h
Access: R/W; RO
Size: 8 bits

This register can be used to disable the System Memory Clock signals to each SO-DIMM slot, which can significantly reduce EMI and Power concerns for clocks that go to unpopulated SO-DIMMs. Clocks should be enabled based on whether or not a slot is populated.

Since there are multiple clock signals assigned to each rank of a DIMM, it is important to clarify exactly which rank width field affects which clock signal.



Channel	Rank Clocks	Affected
0	0 or 1	SM_CK[1:0] / SM_CK#[1:0]
1	0 or 1	SM_CK[3:2] / SM_CK#[3:2] ***Note**:* These signals are Not on the Ultra Mobile 945GU Express Chipset.

Bit	Access	Default Value	Description
7:4	RO	0h	**Reserved**
3	R/W	0b	**DIMM Clock Gate Enable Pair 3:** 0: Tri-state the corresponding clock pair 1: Enable the corresponding clock pair
2	R/W	0b	**DIMM Clock Gate Enable Pair 2:** 0: Tri-state the corresponding clock pair 1: Enable the corresponding clock pair
1	R/W	0b	**DIMM Clock Gate Enable Pair 1:** 0: Tri-state the corresponding clock pair 1: Enable the corresponding clock pair
0	R/W	0b	**DIMM Clock Gate Enable Pair 0:** 0: Tri-state the corresponding clock pair 1: Enable the corresponding clock pair

6.2.12 C0BNKARC - Channel 0 DRAM Bank Architecture

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 10E-10Fh
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This register is used to program the bank architecture for each rank.

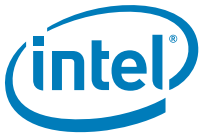
Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7:6	R/W	00b	**Rank 3 Bank Architecture:** 00: 4 Bank 01: 8 Bank 1X: Reserved

Bit	Access	Default Value	Description
5:4	R/W	00b	**Rank 2 Bank Architecture:** 00: 4 Bank 01: 8 Bank 1X: Reserved
3:2	R/W	00b	**Rank 1 Bank Architecture:** 00: 4 Bank 01: 8 Bank 1X: Reserved
1:0	R/W	00b	**Rank 0 Bank Architecture:** 00: 4 Bank 01: 8 Bank 1X: Reserved

6.2.13 C0DRT0 - Channel 0 DRAM Timing Register 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 110-113h
Default Value: B96038F8h
Access: R/W; RO
Size: 32 bits

This 32-bit register defines the timing parameters for all devices in this channel. The BIOS programs this register with the “least common denominator” values for each channel after reading configuration registers of each device in each channel.

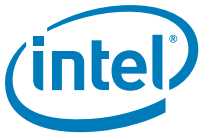


(Sheet 1 of 4)

Bit	Access	Default Value	Description
31:28	R/W	Bh	**Back-to-Back Write to Precharge Command Spacing (Same Bank):** This field determines the number of clocks between write command and a subsequent precharge command to the same bank. The minimum number of clocks is calculated based on this formula for DDR2: **DDR2: CL - 1 + BL/2 + t WR** 0h to 3h: Reserved 4h to Fh: Allowed Write Recovery time (tWR). Write recovery time is a standard DDR2 timing parameter that determines minimum time between a write command and a subsequent precharge command to the same bank. This parameter is programmable on DDR2 DIMMs and the value used above must match the largest delay programmed in any DIMM in the system. Minimum recommended values are documented below: tWR (on CK) 3 Clocks: DDR2 400 4 Clocks: DDR2 533 5 Clocks: DDR2 667
27:24	R/W	9h	**Back-to-Back Write to Read Command Spacing (Same Rank):** This field determines the number of clocks between write command and a subsequent read command to the same rank. The minimum number of clocks is calculated based on this formula: **DDR2: CL - 1 + BL/2 + t WTR** 0h - 5h: Reserved 6h - Ch: Allowed Dh - Fh: Reserved Write to Read Command delay (tWTR). The tWTR is a standard DDR2 timing parameter and is used to time a RD command after a WR command to the same row. Following are the values used for tWTR 2 Clocks – DDR2 400 or DDR2 533 3 Clocks – DDR2 667

(Sheet 2 of 4)

Bit	Access	Default Value	Description
23:22	R/W	01b	**Back-to-Back Write-Read Command Spacing (Different Rank):** This field determines the number of turnaround clocks on the data bus that needs to be inserted between write command and a subsequent read command. The minimum spacing of commands is calculated based on the formula: **DDR2 = BL/2 + TA - 1** (*Derived from*: DDR2 = BL/2 + TA (wr-rd) + WL - CL which gives DDR2 = BL/2 + TA + CL - 1 - CL) BL is the burst length which is 8 TA is the required write to read DQ turnaround on the bus. Can be set to 1,2, or 3 CK using this register CL is CAS Latency **Encoding** — **BL8 CMD Spacing** 00 — 6 01 — 5 10 — 4 11 — Reserved

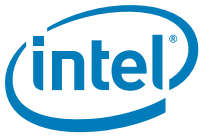


(Sheet 3 of 4)

<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>Description</th></tr>
<tr><td>21:20</td><td>R/W</td><td>10b</td><td>
Back-to-Back Read-Write Command Spacing:
This field determines the number of turnaround clocks between the read command and a subsequent write command.
The minimum spacing of commands is calculated based on the formula:
DDR2 = BL/2 + TA + 1
(
This is derived as follows:
DDR2 = CL + BL/2 + TA (wr-rd) - WL
DDR2 = CL + BL/2 + TA - CL + 1
)
BL is the burst length and is set to 8
TA is the required read to write DQ turnaround on the bus. Can be set to 1,2,3, 4 CK
CL is CAS Latency
<table>
<tr><th>Encoding</th><th>BL4 CMD Spacing</th><th>BL8 CMD Spacing</th></tr>
<tr><td>00</td><td>7</td><td>9</td></tr>
<tr><td>01</td><td>6</td><td>8</td></tr>
<tr><td>10</td><td>5</td><td>7</td></tr>
<tr><td>11</td><td>4</td><td>6</td></tr>
</table>
The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest DIMM is large.
</td></tr>
<tr><td>19:18</td><td>R/W</td><td>00b</td><td>
Back-to-Back Write Command Spacing:
This field controls the turnaround time on the DQ bus for WR-WR sequence to different ranks in one channel.
The minimum spacing of commands is calculated based on the formula
DDR2 = BL/2 + TA
Encoding Turnaround BL8 CMD Spacing
00 2 turnaround clocks on DQ 6
01 1 turnaround clocks on DQ 5
10 0 turnaround clocks on DQ 4
11 Reserved
The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest DIMM is large.
</td></tr>
<tr><td>17:17</td><td>RO</td><td>0b</td><td>Reserved</td></tr>
</table>

(Sheet 4 of 4)

Bit	Access	Default Value	Description
16:16	R/W	0b	**Back-to-Back Read Command Spacing (Different Rank):** This field controls the turnaround time on the DQ bus for Rd-RD sequence to different ranks in one channel. The minimum spacing of commands is calculated based on the formula: **DDR2 = BL/2 + TA** **Encoding — Turnaround — BL8 CMD Spacing** 0 — 2 turnaround clocks on DQ — 6 1 — 1 turnaround clocks on DQ — 5 The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest DIMM is large.
15:11	R/W	07h	**Memory Clock portion of Read Delay (tRD_Mclks):** tRD is the number of memory clocks from CS# assert to H_DRDY# assertion on the FSB. The following tRD_Mclks values are supported: 00000 – 00010: Reserved 00011: 3 mclks 00100: 4 mclks 00101: 5 mclks 00110: 6 mclks 00111: 7 mclks (DDR2 400) 01000 to 11111: Reserved
10:9	RO	00b	**Reserved**
8:4	R/W	0Fh	**Write Auto Precharge to Activate (Same bank) (WRAP2ACTSB):** This field determines the clock spacing between write command with Auto precharge and a subsequent Activate command to the same bank. The minimum spacing is calculated based on this formula **DDR2 = CL -1 + BL/2 + tWR + tRP** 00h to 03h:Reserved 04h to 15h:Allowed 16h to 1Fh:Reserved tWR is a DRAM Parameter
3:0	R/W	8h	**Read Auto Precharge to Activate (Same bank) (RDAP2ACTSB):** This field determines the clock spacing between a read command with Auto precharge and a subsequent Activate command to the same bank. 0h: to 2h: Reserved 3h: to Ch: Allowed Dh: to Fh: Reserved



6.2.14 C0DRT1 - Channel 0 DRAM Timing Register 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 114-117h
Default Value: 02607122h
Access: R/W; RO
Size: 32 bits

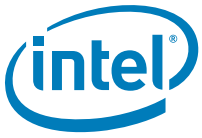
(Sheet 1 of 3)

Bit	Access	Default Value	Description
31:30	R/W	00b	**Reserved**
29:28	R/W	00b	**Read to Precharge (tRTP):** These bits control the number of clocks that are inserted between a read command to a row precharge command to the same rank. Encoding tRTP 00: BL/2 (DDR2 - 400, 533) 01: BL/2+1 (DDR2 - 667) 10: Reserved 11: Reserved
27:24	R/W	2h	**Reserved**
23:19	R/W	0Ch	**Activate to Precharge Delay (tRAS):** This bit controls the number of DRAM clocks for tRAS. Minimum recommendations are beside their corresponding encodings. 00h - 03h: Reserved 04h- 12h: Four to Eighteen clocks respectively 19h - 1Fh: Reserved Recommended values: 8: DDR2 400 C: DDR2 533 F: DDR2 667
18	R/W	0b	**Precharge to Precharge Delay:** Control Pre to Pre delay between the different banks of the same rank. 0 = 1 Clock 1 = 2 Clock
17	RW	0b	**Reserved**
16	R/W	0b	**Pre-All to Activate Delay (tRPALL):** This is applicable only to 8-bank architectures. Must be set to 1 if any rank is populated with 8-bank device technology. 0: tRPALL = tRP 1: tRPALL = tRP + 1

(Sheet 2 of 3)

<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>Description</th></tr>
<tr><td>15:10</td><td>R/W</td><td>1Ch</td><td>Refresh Cycle Time (tRFC):
Refresh cycle time is measured from a Refresh command (REF) until the first Activate command (ACT) to the same rank, required to perform a read or write.

For DDR2, tRFC needs to follow the values recommended in the table below:
<table><tr><th>Parameter</th><th>Symbol</th><th>256 Mb</th><th>512 Mb</th><th>1 Gb</th></tr><tr><td>Refresh to Active/Refresh command time</td><td>tRFC</td><td>75</td><td>105</td><td>127.5</td></tr><tr><td>DDR2-400</td><td>5</td><td>15</td><td>21</td><td>26</td></tr><tr><td>DDR2-533</td><td>4</td><td>20</td><td>28</td><td>34</td></tr><tr><td>DDR2-677</td><td>3</td><td>25</td><td>35</td><td>43</td></tr></table></td></tr>
<tr><td>9:8</td><td>R/W</td><td>01b</td><td>CASB Latency (tCL):
This value is programmable on DDR2 DIMMs. The value programmed here must match the CAS Latency of every DDR2 DIMM in the system.
<table><tr><th>Encoding</th><th>DDR2 CL</th></tr><tr><td>00</td><td>5 (Validated for DDR2 667 MHz)</td></tr><tr><td>01</td><td>4 (Validated for DDR2 533 MHz)</td></tr><tr><td>10</td><td>3 (Validated for DDR2 400 MHz)</td></tr><tr><td>11</td><td>6</td></tr></table>Note: The timings validated by Intel for each DDR2 frequency are indicated above.</td></tr>
<tr><td>7</td><td>RO</td><td>0b</td><td>Reserved</td></tr>
</table>



(Sheet 3 of 3)

<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>Description</th></tr>
<tr><td>6:4</td><td>R/W</td><td>010b</td><td>DRAM RASB to CASB Delay (tRCD):
This bit controls the number of clocks inserted between a row activate command and a read or write command to that row.

<table>
<tr><th>Encoding</th><th>tRCD</th></tr>
<tr><td>000</td><td>2 DRAM Clocks</td></tr>
<tr><td>001</td><td>3 DRAM Clocks (Validated for DDR2 400 MHz)</td></tr>
<tr><td>010</td><td>4 DRAM Clocks (Validated for DDR2 533 MHz)</td></tr>
<tr><td>011</td><td>5 DRAM Clocks (Validated for DDR2 667 MHz)</td></tr>
<tr><td>100</td><td>6 DRAM Clocks</td></tr>
<tr><td>101-111</td><td>Reserved</td></tr>
</table>
Note: The timings validated by Intel for each DDR2 frequency are indicated above.</td></tr>
<tr><td>3</td><td>RO</td><td>0b</td><td>Reserved</td></tr>
<tr><td>2:0</td><td>R/W</td><td>010b</td><td>DRAM RASB Precharge (tRP):
This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank.

<table>
<tr><th>Encoding</th><th>tRP</th></tr>
<tr><td>000</td><td>2 DRAM Clocks</td></tr>
<tr><td>001</td><td>3 DRAM Clocks (Validated for DDR2 400 MHz)</td></tr>
<tr><td>010</td><td>4 DRAM Clocks (Validated for DDR2 533 MHz)</td></tr>
<tr><td>011</td><td>5 DRAM Clocks (Validated for DDR2 667 MHz)</td></tr>
<tr><td>100</td><td>6 DRAM Clocks</td></tr>
<tr><td>101</td><td>7 DRAM Clocks</td></tr>
<tr><td>110-111</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Below is the validation matrix for tCL, tRCD and tRP in table format.

	tCL (CLK Periods)	tRCD (CLK Periods)	tRP (CLK Periods)
400 MHz	3	3	3
533 MHz	4	4	4
667 MHz	5	5	5

6.2.15 C0DRT2 - Channel 0 DRAM Timing Register 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 118-11Bh
Default Value: 800003FFh
Access: R/W; RO
Size: 32 bits

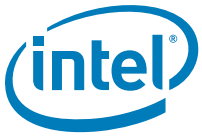
Bit	Access	Default Value	Description
31:30	R/W	10b	**CKE Deassert Duration:** 00 = 1 Mcclk 01 = Reserved 10 = 3 Mcclk (DDR 2) 11 = Reserved **Must be set to 10 for DDR2**
29:18	RO	000h	**Reserved**
17:16	R/W	00b	**Reserved**
15:11	RO	00h	**Reserved**
10:8	R/W	011b	**Reserved**
7:0	R/W	111b	**Reserved**

6.2.16 C0DRC0 - Channel 0 DRAM Controller Mode 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 120-123h
Default Value: 40000802h
Access: R/W; RO
Size: 32 bits

(Sheet 1 of 4)

Bit	Access	Default Value	Description
31:30	RO	01b	**Reserved**
29	R/W	0b	**Initialization Complete (IC):** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28	R/W	0b	**Reserved**
27:24	R/W	0h	**Active SDRAM Ranks:** Implementations may use this field to limit the maximum number of SDRAM ranks that may be active at once. 0000: All ranks allowed to be in the active state 0001: One Rank 0010: Two Ranks Others: Reserved

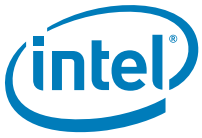


(Sheet 2 of 4)

Bit	Access	Default Value	Description
23:16	R/W	000h	**Reserved**
15	R/W	0b	**CMD Pin Dual Copy Enable:** In a Single-channel mode, the CMD pins (MA, BS, RAS, CAS, WE) on both channels are driven and are physical copies of each other. Setting this bit enables the CMD pins on channel B. Having the additional copy of CMD pins helps reduce loading on these pins, since in a two DIMM system, each copy can be hooked up to one DIMM. In a single DIMM system, the second copy can be disabled to eliminate unnecessary toggling of these pins. If this bit needs to be set, BIOS should do that before memory initialization sequence. This bit should not be set in a dual-channel system.
14	R/W	0b	**Reserved**
13:12	R/W	00b	**Reserved**
11	RO	1b	**Reserved**
10:8	R/W	000b	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000 to 001: Reserved 010: Refresh enabled. Refresh interval 7.8 µs Other: Reserved
7	RO	0b	**Reserved**

(Sheet 3 of 4)

Bit	Access	Default Value	Description
6:4	R/W	000b	**Mode Select (SMS):** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. **000**: Post Reset state – When the (G)MCH exits reset (power-up or otherwise), the mode select field is cleared to 000. During any reset sequence, while power is applied and reset is active, the (G)MCH deasserts all DRAM CLK and CKE signals. After internal reset is deasserted, DRAM CLK and CKE signals remain deasserted until this field is written to a value different than "000". On this event, DRAM CLKs are enabled and all CKE signals remain deasserted for a minimum of 35 ns before CKE signals are asserted. During suspend, (G)MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, (G)MCH will be reset – which will clear this bit field to "000" and maintain DRAM CLK and CKE signals deasserted. After internal reset is deasserted, DRAM CLK and CKE signals remain deasserted until this field is written to a value different than "000". On this event, DRAM CLKs are enabled and CKE signals remain deasserted for a minimum of 35 ns before CKE signals are asserted. During entry to other low power states (C3, S1), (G)MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, (G)MCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. **001:** NOP Command Enable – All CPU cycles to DRAM result in a NOP command on the DRAM interface. **010:** All Banks Pre-charge Enable – All CPU cycles to DRAM result in an "all banks precharge" command on the DRAM interface. **011:** Mode Register Set Enable – All CPU cycles to DRAM result in a "mode register" set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. Host address lines [12:3] are mapped to MA[9:0], and HA[13] is mapped to MA[11]. MA[10] must be set to enable DQSB strobe complements. For the remaining bit fields, refer to the JEDEC spec for DDR2 details. **100-101**: Reserved **110:** CBR Refresh Enable – In this mode all CPU cycles to DRAM Result in a CBR cycle on the DRAM interface **111:** Normal operation



(Sheet 4 of 4)

Bit	Access	Default Value	Description
3	RO	0b	**Reserved**
2	R/W	0b	**Burst Length (BL):** The burst length is the number of QWORDS returned by a DIMM per read command, when not interrupted. This bit is used to select the DRAM controller's Burst Length Operation mode. It must be set to match to the behavior of the DIMM. 0: Reserved 1: Burst Length of 8
1:0	RO	10b	**DRAM Type (DT):** Used to select between supported SDRAM types. 10: Second Revision Dual Data Rate (DDR2) SDRAM Other: Reserved

6.2.17 C0DRC1 - Channel 0 DRAM Controller Mode 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 124-127h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

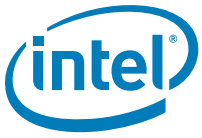
Bit	Access	Default Value	Description
31:20	R/W	0000h	**Reserved**
19:16	R/W	0	**CKE Tri-state Enable Per Rank:** Bit 19 corresponds to rank 3 Bit 18 corresponds to rank 2 Bit 16 corresponds to rank 0 Bit 17 corresponds to rank 1 0 = CKE is not tri-stated. 1 = CKE is tri-stated. This is set only if the rank is physically not populated.
15:13	R/W	000b	**Reserved**
12	R/W	0b	**CS# Tri-state Enable:** When set to a 1, the DRAM controller will tri-state CS# when the corresponding CKE is deasserted. 0: Address Tri-state Disabled 1: Address Tri-state Enabled
11	R/W	0b	**Address Tri-state Enable:** When set to a 1, the DRAM controller will tri-state the MA, CMD, and CS# (CS# if lines only when all CKEs are deasserted. CKEs deassert based on Idle timer or max rank count control.) 0: Address Tri-state Disabled 1: Address Tri-state Enabled

Bit	Access	Default Value	Description
10:9	R/W	00b	**Reserved**
8	R/W	1b	**DRAM Channel IO-Buffers Activate:** This bit is cleared to 0 during reset and remains inactive until it is set to 1 by BIOS. While 0, the DRAM controller core logic forces the state of the IO-buffers in this channel to “reset” or “preset”, depending on the specific buffer type. While 1, the DRAM controller core logic enables the DRAM IO-buffers in this channel to operate normally.
7:0	R/W	00h	**Reserved**

6.2.18 C0DRC2 - Channel 0 DRAM Controller Mode 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 128-12Bh
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
31:28	RO	0h	**Reserved**
27:24	R/W	00b	**Dram ODT Tristate Enable Per Rank:** Bit 27 corresponds to rank 3 Bit 26 corresponds to rank 2 Bit 24 corresponds to rank 0 Bit 25 corresponds to rank 1 0 = ODT is not tri-stated. 1 = ODT is tri-stated. This is set only if the rank is physically not populated.
23:13	RO	000h	**Reserved**
12	R/W	0b	**Reserved**
11:9	RO	000b	**Reserved**
8:2	R/W	00h	**Reserved**
1:0	RO	00b	**Reserved**



6.2.19 C0AIT - Channel 0 Adaptive Idle Timer Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	130-137h
Default Value:	0000000000000000h
Access:	R/W; RO
Size:	64 bits

This register controls Characteristics of Adaptive Idle Timer Mechanism.

6.2.20 C0GTEW - Channel 0 (G)MCH Throttling Event Weight

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	140-143h
Default Value:	00000000h
Access:	R/W/L
Size:	32 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length considerations. It is also possible for BIOS to take into account loading variations caused by different memory types and population of ranks.

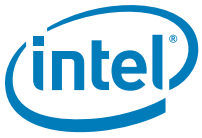
Bit	Access	Default Value	Description
31:24	R/W/L	00h	**Read Weight:** This value is input to the filter if in a given clock there is a valid read command being issued on the memory bus.
23:16	R/W/L	00h	**Write Weight:** This value is input to the filter if in a given clock there is a valid write command being issued on the memory bus.
15:8	R/W/L	00h	**Command Weight:** This value is input to the filter if in a given clock there is a valid command other than a read or a write being issued on the memory bus.
7:0	R/W/L	00h	**Idle Weight:** This value is input to the filter if in a given clock there is no command being issued on the memory bus. If command and address are tristated a value of 0 is input to the filter. If command and address are under reduced drive strength this value is divided by 2 and input to the filter.

6.2.21 C0GTC - Channel 0 (G)MCH Throttling Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 144-147h
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks.

Bit	Access	Default Value	Description
31:31	R/W/L	0b	**(G)MCH Throttle Lock (GTLOCK):** This bit secures the (G)MCH throttling control registers GTEW and GTC. This bit defaults to 0. Once a 1 is written to this bit, all of the configuration register bits are read-only.
30:30	RO	0b	**Reserved**
29:29	R/W/L	0b	**Reserved**
28:25	RO	0h	**Reserved**
24:22	R/W/L	000b	**Reserved**
21:21	R/W/L	0b	**(G)MCH Bandwidth-Based Throttling Enable:** 0 = Bandwidth Threshold (WAB) is not used for throttling. 1 = Bandwidth Threshold (WAB) is used for throttling. If both bandwidth-based and thermal sensor-based throttling modes are on when the thermal sensor trips, the thermal threshold is used for throttling.
20:20	R/W/L	0b	**(G)MCH Thermal Sensor Trip Enable:** 0 = (G)MCH throttling is not initiated when the (G)MCH thermal sensor trips. 1 = (G)MCH throttling is initiated when the (G)MCH thermal sensor trips and the filter output is equal to or exceeds thermal threshold WAT.
19:19	RO	0b	**Reserved**
18:16	R/W/L	000b	**Reserved**
15:8	R/W/L	00h	**WAB:** Threshold allowed per clock for bandwidth based throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.
7:0	R/W/L	00h	**WAT:** Threshold allowed per clock during thermal sensor enabled throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.



6.2.22 C0DTPEW - Channel 0 Dram Rank Throttling Passive Event Weights

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 148-14Fh
Default Value: 0000000000000000h
Access: R/W/L; RO
Size: 64 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length considerations. It is also possible for BIOS to take into account loading variations caused by different memory types and population of ranks. All bits in this register can be locked by the DTLOCK bit in the C0DTC register.

Bit	Access	Default Value	Description
63:48	RO	0000h	**Reserved**
47:40	R/W/L	00h	**Additive Weight for ODT:** This value is added to the total weight of a rank if ODT on that rank is asserted. Note that this value should reflect whether the DRAM modules have been programmed for 75- or 150-Ω termination.
39:32	R/W/L	00h	**Weight for Any Open Page during Active (WAOPDA):** This value is input to the filter if, during the present clock, the corresponding rank has any pages open and is not in power down. The value programmed here is IDD3N from the JEDEC.
31:24	R/W/L	00h	**All Banks Precharge Active (ABPA):** This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged but is not in power down. The value programmed here is IDD2N from the JEDEC spec.
23:16	R/W/L	00h	**Weight for Any Open Page during Power Down (WAOPDPD):** This value is input to the filter if, during the present clock, the corresponding rank is in power down with pages open. The value programmed here is IDD3P from the JEDEC.
15:8	R/W/L	00h	**All Banks Precharge Power Down (ABPPD):** This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged and is powered down. The value programmed here is IDD2P from the JEDEC spec.
7:0	R/W/L	00h	**Self Refresh:** This value is input to the filter if in a clock the corresponding rank is in self refresh.

6.2.23 C0DTAEW - Channel 0 Dram Rank Throttling Active Event Weights

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 150-157h
Default Value: 0000000000000000h
Access: R/W/L
Size: 64 bits

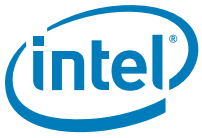
This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length considerations. It is also possible for BIOS to take into account loading variations caused by different memory types and population of ranks. The (G)MCH sends a command to the selected DRAM (via CS# assertion). Based on the command type, one of the weights specified in this register is added to the weight specified in the previous register, which is then input to the filter.

Bit	Access	Default Value	Description
63:56	R/W/L	00h	**Read with AP**
55:48	R/W/L	00h	**Write with AP**
47:40	R/W/L	00h	**Read**
39:32	R/W/L	00h	**Write**
31:24	R/W/L	00h	**Precharge - All**
23:16	R/W/L	00h	**Precharge**
15:8	R/W/L	00h	**Activate**
7:0	R/W/L	00h	**Refresh**

6.2.24 C0DTC - Channel 0 Dram Throttling Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 158-15Bh
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This register is for Programmable Event weights that are inputs into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length, 1N/2N rule considerations. It is also possible for bios to take into account type loading variations of memory caused as a function of memory types and population of ranks.



Bit	Access	Default Value	Description
31	R/L	0b	**Dram Throttle Lock (DTLOCK):** This bit secures the Dram throttling control registers DT*EW and DTC. This bit defaults to 0. Once a 1 is written to this bit, all of the configuration register bits are read-only.
30	RO	0b	**Reserved**
29	R/W/L	0b	**Reserved**
28:25	RO	0h	**Reserved**
24:22	R/W/L	000b	**Reserved**
21	R/W/L	0b	**(G)MCH Bandwidth-Based Throttling Enable:** 0 = Bandwidth Threshold (WAB) is not used for throttling. 1 = Bandwidth Threshold (WAB) is used for throttling. If both bandwidth-based and thermal sensor-based throttling modes are on and the thermal sensor trips, thermal threshold is used for throttling.
20	R/W/L	0b	**(G)MCH Thermal Sensor Trip Enable:** 0 = (G)MCH throttling is not initiated when the (G)MCH thermal sensor trips. 1 = (G)MCH throttling is initiated when the (G)MCH thermal sensor trips and the filter output is equal to or exceeds thermal threshold WAT.
19	RO	0b	**Reserved**
18:16	R/W/L	000b	**Time Constant:** 000: 2^28 Clocks 001: 2^29 Clocks 010: 2^30 Clocks 011: 2^31 Clocks 1XX: Reserved
15:8	R/W/L	00h	**WAB:** Threshold allowed per clock for bandwidth based throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.
7:0	R/W/L	00h	**WAT:** Threshold allowed per clock during for thermal sensor enabled throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.

6.2.25 C0DMC - Channel 0 DRAM Maintenance Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 164-167h
Default Value: 00000020h
Access: R/W; RO
Size: 32 bits

The register fields allow control of DRAM and MCH ODT.

6.2.26 C0ODT - Channel 0 ODT Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	168-16Fh
Default Value:	0002879822049200h
Access:	R/W; RO
Size:	64 bits

The register fields allow control of DRAM and MCH ODT.

6.2.27 C1DRB0 - Channel 1 DRAM Rank Boundary Address 0

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	180h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

6.2.28 C1DRB1 - Channel 1 DRAM Rank Boundary Address 1

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	181h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

6.2.29 C1DRA0 - Channel 1 DRAM Rank 0,1 Attribute

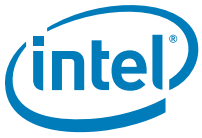
B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	188h
Default Value:	00h
Access:	R/W; RO
Size:	8 bits

The operation of this register is detailed in the description for register C0DRA0.

6.2.30 C1DCLKDIS - Channel 1 DRAM Clock Disable

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	18Ch
Default Value:	00h
Access:	R/W; RO
Size:	8 bits

The operation of this resister is detailed in the description for register C0DCLKDIS.



6.2.31 C1BNKARC - Channel 1 DRAM Bank Architecture

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	18E-18Fh
Default Value:	0000h
Access:	R/W; RO
Size:	16 bits

The operation of this register is detailed in the description for register C0BNKARC.

6.2.32 C1DRT0 - Channel 1 DRAM Timing Register 0

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	190-193h
Default Value:	B96038F8h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT0.

6.2.33 C1DRT1 - Channel 1 DRAM Timing Register 1

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	194-197h
Default Value:	02607122h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT1.

6.2.34 C1DRT2 - Channel 1 DRAM Timing Register 2

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	198-19Bh
Default Value:	800003FFh
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT2.

6.2.35 C1DRC0 - Channel 1 DRAM Controller Mode 0

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1A0-1A3h
Default Value:	40000802h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRC0.

6.2.36 C1DRC1 - Channel 1 DRAM Controller Mode 1

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1A4-1A7h
Default Value:	00000000h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRC1.

6.2.37 C1DRC2 - Channel 1 DRAM Controller Mode 2

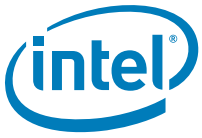
B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1A8-1ABh
Default Value:	00000000h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRC2.

6.2.38 C1AIT - Channel 1 Adaptive Idle Timer Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1B0-1B7h
Default Value:	0000000000000000h
Access:	R/W; RO
Size:	64 bits

This register controls Characteristics of Adaptive Idle Timer Mechanism.



6.2.39 C1GTEW - Channel 1 (G)MCH Throttling Event Weights

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1C0-1C3h
Default Value:	00000000h
Access:	R/W/L
Size:	32 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length considerations. It is also possible for BIOS to take into account loading variations caused by different memory types and population of ranks.

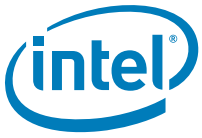
Bit	Access	Default Value	Description
31:24	R/W/L	00h	**Read Weight:** This value is input to the filter if in a given clock there is a valid read command being issued on the memory bus.
23:16	R/W/L	00h	**Write Weight:** This value is input to the filter if in a given clock there is a valid write command being issued on the memory bus.
15:8	R/W/L	00h	**Command Weight:** This value is input to the filter if in a given clock there is a valid command other than a read or a write being issued on the memory bus.
7:0	R/W/L	00h	**Idle Weight:** This value is input to the filter if in a given clock there is no command being issued on the memory bus.

6.2.40 C1GTC - Channel 1 (G)MCH Throttling Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1C4-1C7h
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length, 1N/2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks.

Bit	Access	Default Value	Description
31:31	R/W/L	0b	**(G)MCH Throttle Lock (GTLOCK):** This bit secures the (G)MCH throttling control registers GTEW and GTC. This bit defaults to 0. Once a 1 is written to this bit, all of the configuration register bits are read-only.
30:30	RO	0b	**Reserved**
29:29	R/W/L	0b	**Reserved**
28:25	RO	0h	**Reserved**
24:22	R/W/L	000b	**Reserved**
21:21	R/W/L	0b	**(G)MCH Bandwidth Based Throttling Enable:** 0 = Bandwidth Threshold (WAB) is not used for throttling. 1 = Bandwidth Threshold (WAB) is used for throttling. If both Bandwidth based and thermal sensor based throttling modes are on when the thermal sensor trips, the Thermal threshold is used for throttling.
20:20	R/W/L	0b	**(G)MCH Thermal Sensor Trip Enable:** 0 = (G)MCH throttling is not initiated when the (G)MCH thermal sensor trips. 1 = (G)MCH throttling is initiated when the (G)MCH thermal sensor trips and the Filter output is equal to or exceeds thermal threshold WAT.
19:19	RO	0b	**Reserved**
18:16	R/W/L	000b	**Reserved**
15:8	R/W/L	00h	**WAB:** Threshold allowed per clock for bandwidth based throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.
7:0	R/W/L	00h	**WAT:** Threshold allowed per clock during thermal sensor enabled throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.



6.2.41 C1DTPEW - Channel 1 DRAM Rank Throttling Passive Event Weights

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1C8-1CFh
Default Value: 0000000000000000h
Access: R/W/L; RO
Size: 64 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length considerations. It is also possible for BIOS to take into account loading variations caused by different memory types and population of ranks. All bits in this register can be locked by the DTLOCK bit in the C0DTC register.

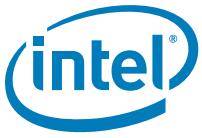
Bit	Access	Default Value	Description
63:48	RO	0000h	**Reserved**
47:40	R/W/L	00h	**Additive Weight for ODT:** This value is added to the total weight of a rank if ODT on that rank is asserted. Note that this value should reflect whether the DRAM modules have been programmed for 75- or 150-Ω termination.
39:32	R/W/L	00h	**Weight for Any Open Page during Active (WAOPDA):** This value is input to the filter if, during the present clock, the corresponding rank has any pages open and is not in power down. The value programmed here is IDD3N from the JEDEC.
31:24	R/W/L	00h	**All Banks Precharge Active (ABPA):** This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged but is not in power down. The value programmed here is IDD2N from the JEDEC spec.
23:16	R/W/L	00h	**Weight for Any Open Page during Power Down (WAOPDPD):** This value is input to the filter if, during the present clock, the corresponding rank is in power down with pages open. The value programmed here is IDD3P from the JEDEC.
15:8	R/W/L	00h	**All Banks Precharge Power Down (ABPPD):** This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged and is powered down. The value programmed here is IDD2P from the JEDEC spec.
7:0	R/W/L	00h	**Self Refresh:** This value is input to the filter if in a clock the corresponding rank is in self refresh.

6.2.42 C1DTAEW - Channel 1 DRAM Rank Throttling Active Event Weights

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1D0-1D7h
Default Value: 0000000000000000h
Access: R/W/L
Size: 64 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length considerations. It is also possible for BIOS to take into account loading variations caused by different memory types and population of ranks. The (G)MCH sends a command to the selected DRAM (via CS# assertion). Based on the command type, one of the weights specified in this register is added to the weight specified in the previous register, which is then input to the filter.

Bit	Access	Default Value	Description
63:56	R/W/L	00h	**Read with AP**
55:48	R/W/L	00h	**Write with AP**
47:40	R/W/L	00h	**Read**
39:32	R/W/L	00h	**Write**
31:24	R/W/L	00h	**Precharge - All**
23:16	R/W/L	00h	**Precharge**
15:8	R/W/L	00h	**Activate**
7:0	R/W/L	00h	**Refresh**



6.2.43 C1DTO - Channel 1 Throttling Observation

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1DC-1DFh
Default Value: 000000_xxxx__xxxx_h
Access: R/W; RO
Size: 32 bits

This register enables observation of the state of the throttling mechanism and current measured bandwidth information.

Bit	Access	Default Value	Description
31:20	RO	000h	**Reserved**
19:19	RO	0b	**Reserved**
18:16	R/W	000b	**Filter Average Selector:** 000 = (G)MCH Filter Average 001 = Rank 0 Filter Average 010 = Rank 1 Filter Average 011-111 = Reserved
15:8	RO	00h	**Selected Filter Average**
7:0	RO	N/A	**(G)MCH and DRAM Throttling Control Signals**

6.2.44 C1DTC - Channel 1 DRAM Throttling Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1D8-1DBh
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

The operation of this register is detailed in the description for register C0DTC.

6.2.45 C1DMC - Channel 1 DRAM Maintenance Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1E4-1E7h
Default Value: 00000020h
Access: R/W; RO
Size: 32 bits

The register fields allow control of DRAM and MCH ODT.

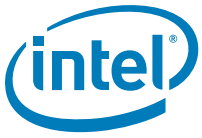
6.2.46 DCC - DRAM Channel Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 200-203h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

This register controls how the DRAM channels work together. It affects how the CxDRB registers are interpreted and allows them to steer transactions to the correct channel.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31:29	RO	000b	**Reserved**
28:24	R/W	00h	**Reserved**
23:23	RO	0b	**Reserved**
22:21	R/W	00b	**Bank Select for EMRS Commands:** 00:Bank 1 (BS[2:0] = 001), EMRS(1) 01:Bank 2 (BS[2:0] = 010), EMRS(2) 10:Bank 3 (BS[2:0] = 011), EMRS(3) 11:Reserved
20	R/W	0b	**Independent Dual-Channel IC/SMS Enable:** 0: IC and SMS controls in DCC register control both system memory channels. 1: IC and SMS bits in C0/1DRC0 register control each system memory channel independently.
19	R/W	0b	**Initialization Complete (IC):** See register description in C0DRC0[29]
18:16	R/W	000b	**Mode Select (SMS):** See register description in C0DRC0[6:4]
15:14	R/W	00b	**Reserved**
13:11	RO	000b	**Reserved**
10:10	R/W	0b	**Channel XOR Disable:** 0: Channel XOR Randomization is enabled. 1: Channel XOR Randomization is disabled
9:9	R/W	0b	**Channel XOR Bit:** 0: Reserved 1: Bit 17 will be XOR'd with the Channel Select bit



(Sheet 2 of 2)

Bit	Access	Default Value	Description
8:3	RO	0b	**Reserved**
2:2	R/W	0b	**Single-Channel Selector (SCS):** When in Single-channel mode, this is the populated channel. 0: Channel 0 1: Channel 1
1:0	R/W	00b	**DRAM Addressing Mode Control (DAMC):** 00: Single-Channel 01: Dual-Channel Asymmetric (Stacked) 10: Dual-Channel Interleaved 11: Reserved

6.2.47 WCC - Write Cache Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 218-21Bh
Default Value: A4000000h
Access: R/W; RO
Size: 32 bits

6.2.48 MMARB0 - Main Memory Arbiter Control_0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 220-223h
Default Value: 00000264h
BIOS Optimal Default 0h
Access: R/W; RO
Size: 32 bits

6.2.49 MMARB1 - Main Memory Arbiter Control_1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 224-227h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

6.2.50 SBTEST - SB Test Register

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 230-233h
Default Value: 34020000h
Access: R/W; RO
Size: 32 bits

6.2.51 ODTC - On Die Termination Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 284-287h
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

6.2.52 SMVREFC - System Memory VREF Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 2A0h
Default Value: 08h
Access: R/W/L; RO
Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	**Reserved**
6	R/W/L	0b	**Differential Receive Strobe Control:** 0: Disabled 1: Enabled
5:4	RO	00b	**Reserved**
3:0	R/W/L	8h	**Reserved**

6.2.53 DQSMT - DQS Master Timing

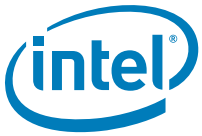
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 2F4-2F5h
Default Value: 0007h
Access: R/W/L
Size: 16 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.54 RCVENMT - RCVENOUTB Master Timing

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 2F8-2FBh
Default Value: 0000070Fh
Access: R/W/L; RO
Size: 32 bits

This register contains the margining controls and status indicators for the RCVENOUTB signals in both channels. This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).



6.2.55 C0WL0REOST - Channel 0 WL0 RCVENOUT Slave Timing

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	340h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.56 C0WL1REOST - Channel 0 WL1 RCVENOUT Slave Timing

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	341h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.57 C0WL2REOST - Channel 0 WL2 RCVENOUT Slave Timing

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	342h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.58 C0WL3REOST - Channel 0 WL3 RCVENOUT Slave Timing

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	343h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.59 WDLLBYPMODE - Write DLL Bypass Mode Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 360-361h
Default Value: 0000h
Access: R/W/L; RO
Size: 16 bits

This register controls WDLL functional and bypass modes for all the buffer types.

6.2.60 C0WDLLCMC - Channel 0 WDLL/Clock Macro Clock Control

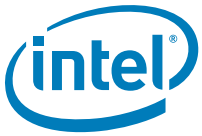
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 36C-36Fh
Default Value: 000000FFh
Access: R/W/L; RO
Size: 32 bits

This register controls WDLL and Macro Clock Control.

6.2.61 C0HCTC - Channel 0 Half Clock Timing Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 37Ch
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

Bit	Access	Default Value	Description
7:6	R/W/L	00b	**Reserved**
5	RO	0b	**Reserved**
4	R/W/L	0b	**Clock Half Clock Push Out for DIMM1:** 0: No Push-out. 1: 0.5 system memory clock push-out.
3	R/W/L	0b	**Control Half Clock Push Out for DIMM1:** 0: No Push-out. 1: 0.5 system memory clock push-out. Setting both CTLQCPI1 and CTLQCPO1 is undefined.
2	R/W/L	0b	**Control Half Clock Push Out for DIMM0:** 0: No Push-out. 1: 0.5 system memory clock push-out. Setting both CTLQCPI0 and CTLQCPO0 is undefined.
1	R/W/L	0b	**Command Half Clock Push Out:** 0: No Push-out. 1: 0.5 system memory clock push-out.
0	R/W/L	0b	**Data Half Clock Push Out:** 0: No Push-out. 1: 0.5 system memory clock push-out.



6.2.62 C1WL0REOST - Channel 1 WL0 RCVENOUT Slave Timing

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	3C0h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.63 C1WL1REOST - Channel 1 WL1 RCVENOUT Slave Timing

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	3C1h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.64 C1WL2REOST - Channel 1 WL2 RCVENOUT Slave Timing

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	3C2h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.65 C1WL3REOST - Channel 1 WL3 RCVENOUT Slave Timing

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	3C3h
Default Value:	00h
Access:	R/W/L; RO
Size:	8 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.66 C1WDLLCMC - Channel 1 WDLL/Clock Macro Clock Control

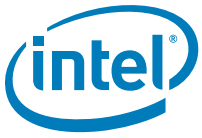
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 3EC-3EFh
Default Value: 0000009Fh
Access: R/W/L; RO
Size: 32 bits

This register controls WDLL and Macro Clock Control.

6.2.67 C1HCTC - Channel 1 Half Clock Timing Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 3FCh
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	**Reserved**
6	R/W/L	0b	**Reserved**
5	RO	0b	**Reserved**
4	R/W/L	0b	**Clock Half Clock Push Out:** 0: No Push-out. 1: 0.5 system memory clock push-out.
3	R/W/L	0b	**Control Half Clock Push Out for DIMM1:** 0: No Push-out. 1: 0.5 system memory clock push-out. Setting both CTLQCPI1 and CTLQCPO1 is undefined.
2	R/W/L	0b	**Control Half Clock Push Out for DIMM0:** 0: No Push-out. 1: 0.5 system memory clock push-out. Setting both CTLQCPI0 and CTLQCPO0 is undefined.
1	R/W/L	0b	**Command Half Clock Push Out:** 0: No Push-out. 1: 0.5 system memory clock push-out.
0	R/W/L	0b	**Data Half Clock Push Out:** 0: No Push-out. 1: 0.5 system memory clock push-out.



6.2.67.1 GBRCOMPCTL - Global/System Memory RCOMP Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 400-403h
Default Value:
Access: R/W/L; RO
Size: 32 bits

This register controls the Global and System Memory RCOMP feature.

Bit	Access	Default Value	Description
31	R/W/L	0b	**Global RCOMP Lock Bit:** Once this bit is set, any further writes to all MCHBAR-IO and MCHBAR-DRAMIO registers will be ignored.
30:24	R/W/L	0h	**Reserved**
23	R/W/L	1b	**Global Periodic RCOMP Disable:** 0: Enable Periodic RCOMP 1: Disable Periodic RCOMP
24	R/W/L	0b	**Reserved**
23:12	R/W/L	000h	**Reserved**
11	R/W/L	0b	**Reserved**
8	R/W/L	0b	**Initial SM RCOMP Enable:** This bit is set after BIOS completed all SM RCOMP required registers.
7:1	RO		**Reserved**
0	R/W/L	0b	**SM RCOMP Digital Filter Enable:** 0 = Disable Digital Filter 1 = Digital Filter Enable

6.2.68 C0DRAMW - Channel 0 DRAM Width

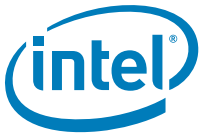
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 40C-40Dh
Default Value: 0000h
Access: R/W/L; RO
Size: 16 bits

This register determines the width of SDRAM devices populated in each rank of memory in this channel.

Bit	Access	Default Value	Description
15:8	RO	00b	**Reserved**
7:6	R/W/L	00b	**Rank 3 Width:** Width of devices in rank 1 00:16-bit wide devices or unpopulated 01:8-bit wide devices 10:Reserved 11:Reserved
5:4	R/W/L	00b	**Rank 2 Width:** Width of devices in rank 0 00:16-bit wide devices or unpopulated 01:8-bit wide devices 10:Reserved 11:Reserved
3:2	R/W/L	00b	**Rank 1 Width:** Width of devices in rank 1 (first DIMM, second side) 00:16-bit wide devices or unpopulated 01:8-bit wide devices 10:Reserved 11:Reserved
1:0	R/W/L	00b	**Rank 0 Width:** Width of devices in rank 0 (first DIMM, first side) 00:16-bit wide devices or unpopulated 01:8-bit wide devices 10:Reserved 11:Reserved

6.2.69 G1SC - Group 1 Strength Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 410h
Default Value: 44h
Access: R/W/L
Size: 8 bits



6.2.70 G2SC - Group 2 Strength Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	418h
Default Value:	44h
Access:	R/W/L
Size:	8 bits

6.2.71 G3SC - Group 3 Strength Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	420h
Default Value:	44h
Access:	R/W/L
Size:	8 bits

6.2.72 G4SC - Group 4 Strength Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	428h
Default Value:	44h
Access:	R/W/L
Size:	8 bits

6.2.73 G5SC - Group 5 Strength Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	430h
Default Value:	44h
Access:	R/W/L
Size:	8 bits

6.2.74 G6SC - Group 6 Strength Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	438h
Default Value:	44h
Access:	R/W/L
Size:	8 bits

6.2.75 C1DRAMW - Channel 1 DRAM Width

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 48C-48Dh
Default Value: 0000h
Access: R/W/L; RO
Size: 16 bits

This register determines the width of SDRAM devices populated in each rank of memory in this channel.

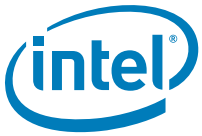
Bit	Access	Default Value	Description
15:8	RO	00b	**Reserved**
7:6	R/W/L	00b	**Reserved**
5:4	R/W/L	00b	**Reserved**
3:2	R/W/L	00b	**Rank 1 Width:** Width of devices in rank 1 (first DIMM, second side) 00:16-bit wide devices or unpopulated 01:8-bit wide devices 10:Reserved 11:Reserved
1:0	R/W/L	00b	**Rank 0 Width:** Width of devices in rank 0 (first DIMM, first side) 00:16-bit wide devices or unpopulated 01:8-bit wide devices 10:Reserved 11:Reserved

6.2.76 G7SC - Group 7 Strength Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 490h
Default Value: 44h
Access: R/W/L
Size: 8 bits

6.2.77 G8SC - Group 8 Strength Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 498h
Default Value: 44h
Access: R/W/L
Size: 8 bits



6.2.78 G1SRPUT - Group 1 Slew Rate Pull-up Table

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	500-51Fh
Default Value:	
Access:	R/W/L; RO
Size:	256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.79 G1SRPDT - Group 1 Slew Rate Pull-Down Table

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	520-53Fh
Default Value:	
Access:	R/W/L; RO
Size:	256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.80 G2SRPUT - Group 2 Slew Rate Pull-up Table

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	540-55Fh
Default Value:	
Access:	R/W/L; RO
Size:	256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.81 G2SRPDT - Group 2 Slew Rate Pull-Down Table

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	560-57Fh
Default Value:	
Access:	R/W/L; RO
Size:	256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.82 G3SRPUT - Group 3 Slew Rate Pull-up Table

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 580-59Fh
Default Value:
Access: R/W/L; RO
Size: 256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.83 G3SRPDT - Group 3 Slew Rate Pull-Down Table

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 5A0-5BFh
Default Value:
Access: R/W/L; RO
Size: 256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.84 G4SRPUT - Group 4 Slew Rate Pull-up Table

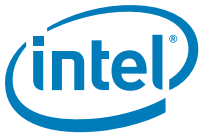
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 5C0-5DFh
Default Value:
Access: R/W/L; RO
Size: 256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.85 G4SRPDT - Group 4 Slew Rate Pull-Down Table

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 5E0-5FFh
Default Value:
Access: R/W/L; RO
Size: 256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).



6.2.86 G5SRPUT - Group 5 Slew Rate Pull-up Table

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	600-61Fh
Default Value:	
Access:	R/W/L; RO
Size:	256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.87 G5SRPDT - Group 5 Slew Rate Pull-Down Table

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	620-63Fh
Default Value:	
Access:	R/W/L; RO
Size:	256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.88 G6SRPUT - Group 6 Slew Rate Pull-up Table

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	640-65Fh
Default Value:	
Access:	R/W/L; RO
Size:	256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.89 G6SRPDT - Group 6 Slew Rate Pull-Down Table

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	660-67Fh
Default Value:	
Access:	R/W/L; RO
Size:	256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.90 G7SRPUT - Group 7 Slew Rate Pull-up Table

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 680-69Fh
Default Value:
Access: R/W/L; RO
Size: 256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.91 G7SRPDT - Group 7 Slew Rate Pull-Down Table

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 6A0-6BFh
Default Value:
Access: R/W/L; RO
Size: 256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.92 G8SRPUT - Group 8 Slew Rate Pull-up Table

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 6C0-6DFh
Default Value:
Access: R/W/L; RO
Size: 256 bits

This register can be locked by the Global RCOMP Lock bit (GBRCOMPCTL[31]).

6.2.93 G8SRPDT - Group 8 Slew Rate Pull-Down Table

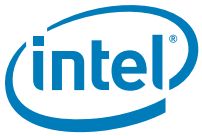
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 6E0-6FFh
Default Value:
Access: R/W/L; RO
Size: 256 bits

6.2.94 MIPMC3– Memory Interface Power Management Control 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: BD8-BDBh
Default Value: 00000000h
BIOS Optimal Default 0h
Access: R/W/L; RO
Size: 32 bits

6.2.95 UPMC4 – Unit Power Management Control 4

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C30-C33h
Default Value: 00000000h
Access: R/W
Size: 32 bits



6.3 Device 0 MCHBAR Clock Controls

Table 5. Device 0 MCHBAR Clock Controls

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Clocking Configuration	CLKCFG	C00	C03	0001000xxx0xxxh	R/W; R/W/L; RO
Reserved		C04	C13		
Unit Power Management Control 1	UPMC1	C14	C15	0323h	R/W; RO
CP Unit Control	CPCTL	C16	C17	0080h	R/W; RO;
Reserved		C18	C1B		
Sticky Scratchpad Data	SSKPD	C1C	C1D	0000h	R/W/S;
Reserved		C1E	C1F		
Unit Power Management Control 2	UPMC2	C20	C21	0001h	R/W; RO
Reserved		C22	C33		
Host-Graphics Interface Power Management Control 1	HGIPMC1	C34	C37	00000000h	R/W; RO
Host-Graphics Interface Power Management Control 2	HGIPMC2	C38	C3B	00000000h	R/W
Reserved		C3C	C43		

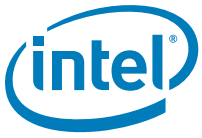
6.3.1 CLKCFG - Clocking Configuration

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C00-C03h
Default Value: 000100_0xxx__0xxx_h
Access: R/W; R/W/L; RO
Size: 32 bits

Bit	Access	Default Value	Description
31	R/W	0b	**Reserved**
30:28	RO	000b	**Reserved**
27:18	R/W	000h	**Reserved**
17	RO	0b	**Reserved**
16:14	R/W	100b	**Reserved**
13	RO	0b	**Reserved**
12	R/W/L	0b	**Reserved**
11:8	R/W	0h	**Reserved**
7:7	R/W/L	0h	**Reserved**
6:4	RO	N/A	**Memory Frequency Select:** 010 = 400 011 = 533 100 = 667 Others = Reserved
3:3	RO	0b	**Reserved**
2:0	RO	N/A	**FSB Frequency Select:** Reflects the State of BSEL pins froms the Processor. BSEL(2:0) selects the FSB frequency as defined below. 000: FSB400 001: FSB533 011: FSB667 Others: Reserved Attempts to strap values to unsupported frequencies will shut down the host PLL.

6.3.2 UPMC1 - Unit Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C14-C15h
Default Value: 0323h
Access: R/W; RO
Size: 16 bits



6.3.3 CPCTL - CPunit Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C16-C17h
Default Value: 0080h
Access: R/W; RO
Size: 16 bits

6.3.4 SSKPD - Sticky Scratchpad Data

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C1C-C1Dh
Default Value: 0000h
Access: R/W/S;
Size: 16 bits

This register holds 16 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers. This register is reset on POWEROK.

Bit	Access	Default Value	Description
15:0	R/W/S	0000h	**Scratchpad Data:** 1 WORD of data storage.

6.3.5 UPMC2 - Unit Power Management Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C20-C21h
Default Value: 0001h
Access: R/W; RO
Size: 16 bits

6.3.6 HGIPMC1 - Host-Graphics Interface Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C34-C37h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

6.3.7 HGIPMC2 - Host-Graphics Interface Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C38-C3Bh
Default Value: 00000000h
Access: R/W
Size: 32 bits

6.4 Device 0 MCHBAR Thermal Management Controls

Note: The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets have two internal thermal sensors. The set of registers from MCHBAR Offset C88h to C9F correspond to Thermal Sensor 1 and the set of registers from MCHBAR Offset CD8 to CE6 correspond to Thermal Sensor 2 respectively.

Table 6. Device 0 MCHBAR Thermal Management Controls (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Thermal Sensor Control 1-1	TSC1	C88	C88	00h	R/W/L
Reserved		C89	C89		
Thermal Sensor Status1	TSS1	C8A	C8A	00h	RO
Thermometer Read 1	TR1	C8B	C8B	FFh	RO
Thermal Sensor Temperature Trip Point 1-1	TSTTP1-1	C8C	C8F	00000000h	R/W/L; RO
Reserved		C90	C91		
Thermal Calibration Offset 1	TCO1	C92	C92	00h	R/WO; R/W/L
Reserved		C93	C93		
Hardware Throttle Control 1	THERM1-1	C94	C94	00h	R/W/L; ROR/WO
Reserved		C95	C95		
TCO Fuses 1	TCOF1	C96	C96	_0xxx__xxxx_h	RS/WC; RO
Reserved		C97	C99		
Thermal Interrupt Status 1	TIS1	C9A	C9B	0000h	R/WC; RO
Thermal Sensor Temperature Trip Point 1-2	TSTTP1-2	C9C	C9F	00000000h	R/WO; R/W/L; RO
Reserved		CA0	CCF		
In Use Bits	IUB	CD0	CD3	00000000h	RO; RS/WC;
Reserved		CD4	CD7		
Thermal Sensor Control 0-1	TSC0-1	CD8	CD8	00h	R/W/L
Reserved		CD9	CD9		
Thermal Sensor Status 0	TSS0	CDA	CDA	00h	RO
Thermometer Read 0	TR0	CDB	CDB	FFh	RO
Thermal Sensor Temperature Trip Point Register 0-1	TSTTP0-1	CDC	CDF	00000000h	R/W/L; RO
Thermal Calibration Offset 0	TCO0	CE2	CE2	00h	R/WO; R/W/L
Reserved		CE3	CE3		
Hardware Throttle Control	THERM0-1	CE4	CE4	00h	R/W/L; ROR/WO
Reserved		CE5	CE5		

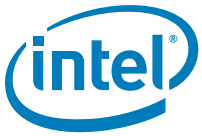


Table 6. Device 0 MCHBAR Thermal Management Controls (Sheet 2 of 2)

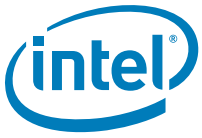
Register Name	Register Symbol	Register Start	Register End	Default Value	Access
TCO Fuses 0	TCOF0	CE6	CE6	_0xxx__xxxx_h	RS/WC; RO
Thermal Interrupt Status	TIS0	CEA	CEB	0000h	R/WC; RO
Thermal Sensor Temperature Trip Point Register	TSTTP0-2	CEC	CEF	00000000h	R/WO; R/W/L; RO
Thermal Error Command	TERRCMD	CF0	CF0	00h	R/W; RO
Thermal SMI Command	TSMICMD	CF1	CF1	00h	R/W; RO
Thermal SCI Command	TSCICMD	CF2	CF2	00h	R/W; RO
Thermal INTR Command	TINTRCMD	CF3	CF3	00h	R/W; RO
External Thermal Sensor Control and Status	EXTTSCS	CFF	CFF	00h	R/WO; R/W/L; RO
Reserved		CFF	E07		
DFT_STRAP1	DFT	E08	E0B	_0xxx__xx0x__xxxx__xxxx__xxxx__xxxx__xxxx__xxxx_h	RO;

6.4.1 TSC1 - Thermal Sensor Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C88h
Default Value: 00h
Access: R/W/L
Size: 8 bits

This register controls the operation of the internal thermal sensor located in the memory hot spot.

Bit	Access	Default Value	Description
7:7	R/W/L	0b	**Thermal Sensor Enable (TSE):** This bit enables power to the thermal sensor. Lockable via TCO bit 7. 0 = Disabled 1 = Enabled
6:6	R/W	0b	**Reserved**
5:2	R/W	0000b	**Digital Hysteresis Amount (DHA):** This bit determines whether no offset, 1 LSB, 2... 15 is used for hysteresis for the trip points. 0001 = 1 TR value added to each trip temperature when tripped 0010 = 2 TR values added to each trip temperature when tripped ... 0110 ~3.0°C (Recommended setting) ... 1110= 14 TR value added to each trip temperature when tripped 1111 = 15 TR values added to each trip temperature when tripped ***Note:*** TR = Temperature Read
1:1	R/W/L	0b	**Reserved**
0:0	N/A	0b	**In Use (IU):** Software semaphore bit. After a full MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. Writing a 0 to this bit has no effect.



6.4.2 TSS1 - Thermal Sensor Status1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C8Ah
Default Value: 00h
Access: RO
Size: 8 bits

This read only register provides trip point information and status of the thermal sensor.

Bit	Access	Default Value	Description
7:7	RO	0b	**Catastrophic Trip Indicator (CTI):** A 1 indicates that the internal thermal sensor temperature is above the catastrophic setting.
6:6	RO	0b	**Hot Trip Indicator (HTI):** A 1 indicates that the internal thermal sensor temperature is above the hot setting.
5:5	RO	0b	**Aux0 Trip Indicator (A0TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux0 setting.
4:4	RO	0b	**Thermometer Mode Output Valid:** 1: Thermometer mode is able to converge to a temperature and that the TR register is reporting a reasonable estimate of the thermal sensor temperature. 0: indicates the Thermometer mode is off, or that temperature is out of range, or that the TR register is being looked at before a temperature conversion has had time to complete.
3:3	RO	0b	**Aux1 Trip Indicator (A1TI):** 1: Internal thermal sensor temperature is above the Aux1 setting.
2:2	RO	0b	**Reserved**
1:1	RO	0b	**Reserved**
0:0	RO	0b	**Reserved**

6.4.3 TR1 - Thermometer Read1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C8Bh
Default Value: FFh
Access: RO
Size: 8 bits

This register generally provides the calibrated current temperature from the thermometer circuit when the Thermometer mode is enabled.

Bit	Access	Default Value	Description
7:0	RO	FFh	**Thermometer Reading (TR):** Provides the current counter value. The current counter value corresponds to thermal sensor temperature if TSS [Thermometer mode Output Valid] = 1. This register has a straight binary encoding that will range from 0 to FFh.

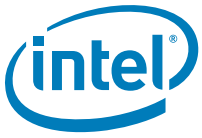
6.4.4 TSTTP1 - Thermal Sensor Temperature Trip Point 1-1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C8C-C8Fh
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This register:

- Sets the target values for some of the trip points in thermometer mode. See also TST [Direct DAC Connect Test Enable].
- Reports the relative thermal sensor temperature. See also TSTTP1-2

Bit	Access	Default Value	Description
31:24	RO	00h	**Relative Temperature (RELT):** HTPS-TR. In Thermometer mode, the RELT field of this register reports the relative temperature of the thermal sensor. Provides a two's complement value of the thermal sensor relative to the Hot trip point. Temperature above the Hot trip point will be positive. See also TSS [Thermometer mode Output Valid] In the Analog mode, the RELT field reports HTPS value.
23:16	R/W/L	00h	**Aux0 Trip Point Setting (A0TPS):** Sets the target for the Aux0 trip point. Lockable by TSTTP2-1 [31].
15:8	R/W/L	00h	**Hot Trip Point Setting (HTPS):** Sets the target value for the Hot trip point. Lockable via TCO bit 7.
7:0	R/W/L	00h	**Catastrophic Trip Point Setting (CTPS):** Sets the target for the Catastrophic trip point. Lockable via TCO bit 7.



6.4.5 TCO1 - Thermal Calibration Offset1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C92h
Default Value: _0xxx__xxxx_h
Access: R/WO; R/W/L
Size: 8 bits

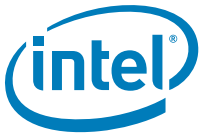
Bit	Access	Default Value	Description
7:7	R/WO	0b	**Lock bit for Catastrophic (LBC):** This bit, when written to a 1, locks the Catastrophic programming interface, including bits 7:0 of this register and bits 7:0 of TSTTP1[15-0], bits 1,7 of TSC 1 and 0 to 3 of TSC 2, and bits 0,7 of TST. This bit may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.
6:0	R/W/L	00h	**Calibration Offset (CO):** This field contains the current calibration offset for the Thermal Sensor DAC inputs. The calibration offset is a twos complement signed number which is added to the temperature counter value to help generate the final value going to the thermal sensor DAC. This field is Read/Write and can be modified by Software unless locked by setting bit 7 of this register. The fuses cannot be programmed via this register. Once this register has been overwritten by software, the values of the TCO fuses can be read using the Therm3 register. ***Note:*** For TCO operation, if TST [Direct DAC Test Enable] = 1, the values in this field are sent directly to Bank B. While this is a seven-bit field, the 7th bit is sign extended to 9 bits for TCO operation.

Register Field Value	Signed Value
00h to 3Fh	00h to 3Fh
41h to 7fh	-3Fh to -1h

6.4.6 THERM1-1 - Hardware Throttle Control 1-1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C94h
Default Value: 00h
Access: R/W/L; ROR/WO
Size: 8 bits

Bit	Access	Default Value	Description
7:7	R/W/L	0b	**Internal Thermal Hardware Throttling Enable Bit (ITHTE):** This bit is a master enable for internal thermal sensor-based hardware throttling 0 Hardware actions via the internal thermal sensor are disabled. 1 Hardware actions via the internal thermal sensor are enabled.
6:5	RO	00b	**Reserved**
4:4	R/W/L	0b	**Throttling Zone Selection (TZS):** This bit determines what temperature zones will enable automatic throttling. This register applies to internal thermal sensor throttling. Lockable by bit0 of this register. See also the throttling registers in PCI configuration space Device 0 which is used to enable or disable throttling 0 = Reserved 1 = Hot and Catastrophic.
3:3	R/W/L	0b	**Halt on Catastrophic (HOC):** When this bit is set, THRMTRIP# is asserted on catastrophic trip to bring the platform down. A system reboot is required to bring the system out of a halt from the thermal sensor. Once the Catastrophic trip point is reached, THRMTRIP# will stay asserted even if the catastrophic trip deasserts before the platform is shut down.
2:2	R/W/L	0b	**Reserved**
1:1	R/W/L	0b	**Reserved**
0:0	R/WO	0b	**Reserved**



6.4.7 TCOF1 – TCO Fuses 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C96h
Default Value: _0xxx__xxxx_h
Access: RS/WC; RO
Size: 8 bits

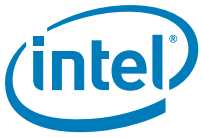
This register indicates the fuse settings for the TCO register. TCO has 7 bits, which are set by fuses when trimmed.

Bit	Access	Default Value	Description
7:7	RS/WC	0b	**INUSE_STS:** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. Writing a 0 to this bit has no effect.
6:0	RO	N/A	**TCO Fuses:** This 7-bit field gives the value of the trimming fuses for TCO. The register always reports the settings of all 7 thermal fuses. ***Note:*** While this is a 7-bit field, the 7th bit is sign extended to 9 bits for TCO operation. **Register Field Value** / **Binary Value** 00h to 3Fh / 0 0000 0000 to 0 0011 1111 41h to 7fh / 1 1100 0001 to 1 1111 1111

6.4.8 TIS1 - Thermal Interrupt Status 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C9A-C9Bh
Default Value: 0000h
Access: R/WC; RO
Size: 16 bits

Bit	Access	Default Value	Description
15:10	RO	00h	**Reserved**
9:9	R/WC	0b	**Was Catastrophic Thermal Sensor Interrupt Event:** 1 = Indicates that a Catastrophic Thermal Sensor trip based on a higher to lower temperature transition through the trip point occurred in the past 0 = No trip for this event, software must write a 1 to clear this status bit.
8:8	R/WC	0b	**Was Hot Thermal Sensor Interrupt Event:** 1 = Indicates that a Hot Thermal Sensor trip based on a higher to lower temperature transition through the trip point occurred in the past 0 = No trip for this event Software must write a 1 to clear this status bit.
7:7	R/WC	0b	**Was Aux0 Thermal Sensor Interrupt Event:** 1 = Indicates that an Aux Thermal Sensor trip based on a higher to lower temperature transition through the trip point occurred in the past 0 = No trip for this event, software must write a 1 to clear this status bit.
6:6	R/WC	0b	**Was Aux1 Thermal Sensor Interrupt Event:** 1 = Indicates that an Aux1 Thermal Sensor trip based on a higher to lower temperature transition through the trip point occurred in the past 0 = No trip for this event, software must write a 1 to clear this status bit.
5:5	R/WC	0b	**Reserved**
4:4	R/WC	0b	**Catastrophic Thermal Sensor Interrupt Event:** 1 = Indicates that a Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. 0 = No trip for this event, software must write a 1 to clear this status bit.
3:3	R/WC	0b	**Hot Thermal Sensor Interrupt Event:** 1 = Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. 0 = No trip for this event, software must write a 1 to clear this status bit.`



Bit	Access	Default Value	Description
2:2	R/WC	0b	**Aux0 Thermal Sensor Interrupt Event:** 1 = Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. 0 = No trip for this event, software must write a 1 to clear this status bit.
1:1	R/WC	0b	**Aux1 Thermal Sensor Interrupt Event:** 1 = Indicates that an Aux1 Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. 0 = No trip for this event, software must write a 1 to clear this status bit.
0:0	R/WC	0b	**Reserved**

6.4.9 TSTTP1-2 – Thermal Sensor Temperature Trip Point 1-2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C9C-C9Fh
Default Value: 00000000h
Access: R/WO; R/W/L; RO
Size: 32 bits

This register sets the target values for some of the trip points in the Thermometer mode. See also TSTTP1.

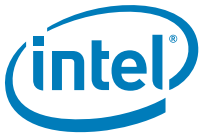
Bit	Access	Default Value	Description
31:31	R/WO	0b	**Lock Bit for Aux0, Aux1 Trip Points:** This bit, when written to a 1, locks the Aux x trip point settings. This lock is reversible. The reversing procedure is: following sequence must be done in order without any other configuration cycles in-between: write testtp2 04C1C202 write testtp2x 04C1C202 write testtp2x 04C1C202 write testtp2 04C1C202 It is expected that the Aux x trip point settings can be changed dynamically when this lock is not set.
30:16	RO	0000h	**Reserved**
15:8	R/W/L	00h	**Reserved**
7:0	R/W/L	00h	**Aux1 Trip Point Setting (A1TPS):** Sets the target value for the Aux1 trip point. Lockable by TSTTP2-1 [31].

6.4.10 IUB - In Use Bits

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CD0-CD3h
Default Value: 00000000h
Access: RO; RS/WC;
Size: 32 bits

Semaphore bits available for software.

Bit	Access	Default Value	Description
31:25	RO	00h	**Reserved:** Must remain hardwired to all 0's to avoid potential resource lockout.
24:24	RS/WC	0b	**In Use Bit 3 (IU3):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it. Writing a 0 to this bit has no effect.
23:17	RO	00h	**Reserved:** Must remain hardwired to all 0's to avoid potential resource lockout.
16:16	RS/WC	0b	**In Use Bit 2 (IU2):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it. Writing a 0 to this bit has no effect.
15:9	RO	00h	**Reserved:** Must remain hardwired to all 0's to avoid potential resource lockout.



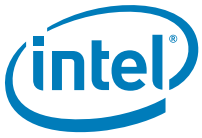
Bit	Access	Default Value	Description
8:8	RS/WC	0b	**In Use Bit 1 (IU1):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it. Writing a 0 to this bit has no effect.
7:1	RO	00h	**Reserved:** Must remain hardwired to all 0's to avoid potential resource lockout.
0:0	RS/WC	0b	**In Use Bit 0 (IU0):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it. Writing a 0 to this bit has no effect.

6.4.11 TSC0-1 - Thermal Sensor Control 0-1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CD8h
Default Value: 00h
Access: R/W/L
Size: 8 bits

This register controls the operation of the internal thermal sensor located in the memory hot spot.

Bit	Access	Default Value	Description
7:7	R/W/L	0b	**Thermal Sensor Enable (TSE):** This bit enables power to the thermal sensor. Lockable via TCO bit 7. 0 = Disabled 1 = Enabled
6:6	R/W	0b	Reserved
5:2	R/W	0000b	**Digital Hysteresis Amount (DHA):** This bit determines whether no offset, 1 LSB, 2... 15 is used for hysteresis for the trip points. 0001 = 1 TR value added to each trip temperature when tripped 0010 = 2 TR values added to each trip temperature when tripped ... 0110 ~3.0°C (Recommended setting) ... 1110= 14 TR value added to each trip temperature when tripped 1111 = 15 TR values added to each trip temperature when tripped ***Note:*** TR = Temperature Read
1:1	R/W/L	0b	**Reserved**
0:0	N/A	0b	**In Use (IU):** Software semaphore bit. After a full MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. Writing a 0 to this bit has no effect.



6.4.12 TSS0 - Thermal Sensor Status0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CDAh
Default Value: 00h
Access: RO
Size: 8 bits

This read only register provides trip point information and status of the thermal sensor.

Bit	Access	Default Value	Description
7:7	RO	0b	**Catastrophic Trip Indicator (CTI):** A 1 indicates that the internal thermal sensor temperature is above the catastrophic setting.
6:6	RO	0b	**Hot Trip Indicator (HTI):** A 1 indicates that the internal thermal sensor temperature is above the hot setting.
5:5	RO	0b	**Aux0 Trip Indicator (A0TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux0 setting.
4:4	RO	0b	**Thermometer Mode Output Valid:** 1: Thermometer mode is able to converge to a temperature and that the TR register is reporting a reasonable estimate of the thermal sensor temperature. 0: indicates the Thermometer mode is off, or that temperature is out of range, or that the TR register is being looked at before a temperature conversion has had time to complete.
3:3	RO	0b	**Aux1 Trip Indicator (A1TI):** 1: Internal thermal sensor temperature is above the Aux1 setting.
2:2	RO	0b	**Reserved**
1:1	RO	0b	**Reserved**
0:0	RO	0b	**Reserved**

6.4.13 TR0 - Thermometer Read 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CDBh
Default Value: FFh
Access: RO
Size: 8 bits

This register generally provides the calibrated current temperature from the thermometer circuit when the Thermometer mode is enabled. See the temperature tables for the temperature calculations.

Bit	Access	Default Value	Description
7:0	RO	FFh	**Thermometer Reading (TR):** Provides the current counter value. The current counter value corresponds to thermal sensor temperature if TSS[Thermometer mode Output Valid] = 1. This register has a straight binary encoding that will range from 0 to FFh.

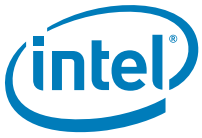
6.4.14 TSTTP0-1 - Thermal Sensor Temperature Trip Point Register 0-1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CDC-CDFh
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This register:

- Sets the target values for some of the trip points in thermometer mode. See also TST [Direct DAC Connect Test Enable].
- Reports the relative thermal sensor temperature. See also TSTTP0-2

Bit	Access	Default Value	Description
31:24	RO	00h	**Relative Temperature (RELT):** HTPS-TR. In Thermometer mode, the RELT field of this register reports the relative temperature of the thermal sensor. Provides a two's complement value of the thermal sensor relative to the Hot trip point. Temperature above the Hot trip point will be positive. See also TSS[Thermometer mode Output Valid] In the Analog mode, the RELT field reports HTPS value.
23:16	R/W/L	00h	**Aux0 Trip Point Setting (A0TPS):** Sets the target for the Aux0 trip point Lockable by TSTTP2-0 [31].



Bit	Access	Default Value	Description
15:8	R/W/L	00h	**Hot Trip Point Setting (HTPS):** Sets the target value for the Hot trip point. Lockable via TCO bit 7.
7:0	R/W/L	00h	**Catastrophic Trip Point Setting (CTPS):** Sets the target for the Catastrophic trip point. See also TST [Direct DAC Connect Test Enable]. Lockable via TCO bit 7.

6.4.15 TCO0 - Thermal Calibration Offset0

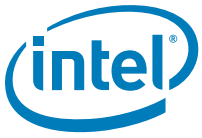
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CE2h
Default Value: _0xxx__xxxx_h
Access: R/WO; R/W/L
Size: 8 bits

Bit	Access	Default Value	Description
7:7	R/WO	0b	**Lock bit for Catastrophic (LBC):** This bit, when written to a 1, locks the Catastrophic programming interface, including bits 7:0 of this register and bits 7:0 of TSTTP1-0 [15-0], bits 1,7 of TSC 1 and 0 to 3 of TSC 2, and bits 0,7 of TST. This bit may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.
6:0	R/W/L	00h	**Calibration Offset (CO):** This field contains the current calibration offset for the Thermal Sensor DAC inputs. The calibration offset is a twos complement signed number which is added to the temperature counter value to help generate the final value going to the thermal sensor DAC. This field is Read/Write and can be modified by Software unless locked by setting bit 7 of this register. The fuses cannot be programmed via this register. Once this register has been overwritten by software, the values of the TCO fuses can be read using the Therm3 register. ***Note:*** For TCO operation, if TST [Direct DAC Test Enable] = 1, the values in this field are sent directly to Bank B. While this is a seven-bit field, the 7th bit is sign extended to 9 bits for TCO operation. Register Field Value: 00h to 3Fh — Signed Value: 00h to 3Fh Register Field Value: 41h to 7fh — Signed Value: -3Fh to -1h

6.4.16 THERM0-1 - Hardware Throttle Control 0-1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CE4h
Default Value: 00h
Access: R/W/L; ROR/WO
Size: 8 bits

Bit	Access	Default Value	Description
7:7	R/W/L	0b	**Internal Thermal Hardware Throttling Enable Bit (ITHTE):** This bit is a master enable for internal thermal sensor-based hardware throttling 0 Hardware actions via the internal thermal sensor are disabled. 1 Hardware actions via the internal thermal sensor are enabled.
6:5	RO	00b	**Reserved**
4:4	R/W/L	0b	**Throttling Zone Selection (TZS):** This bit determines what temperature zones will enable automatic throttling. This register applies to internal thermal sensor throttling. Lockable by bit0 of this register. See also the throttling registers in PCI configuration space Device 0 which is used to enable or disable throttling 0 = Reserved 1 = Hot and Catastrophic.
3:3	R/W/L	0b	**Halt on Catastrophic (HOC):** When this bit is set, THRMTRIP# is asserted on catastrophic trip to bring the platform down. A system reboot is required to bring the system out of a halt from the thermal sensor. Once the Catastrophic trip point is reached, THRMTRIP# will stay asserted even if the catastrophic trip deasserts before the platform is shut down.
2:2	R/W/L	0b	**Reserved**
1:1	R/W/L	0b	**Reserved**
0:0	R/WO	0b	**Reserved**



6.4.17 TCOF0 – TCO Fuses 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CE6h
Default Value: _0xxx__xxxx_h
Access: RS/WC; RO
Size: 8 bits

This register indicates the fuse settings for the TCO register. TCO has 7 bits, which are set by fuses when trimmed.

Bit	Access	Default Value	Description
7:7	RS/WC	0b	**INUSE_STS:** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. Writing a 0 to this bit has no effect.
6:0	RO	N/A	**TCO Fuses:** This 7 bit field gives the value of the trimming fuses for TCO. The register always reports the settings of all 7 thermal fuses. ***Note:*** While this is a 7-bit field, the 7th bit is sign extended to 9 bits for TCO operation. Register Field Value: 00h to 3Fh — Binary Value: 0 0000 0000 to 0 0011 1111 Register Field Value: 41h to 7fh — Binary Value: 1 1100 0001 to 1 1111 1111

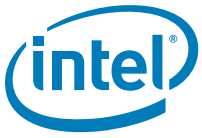
6.4.18 TIS 0- Thermal Interrupt Status 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CEA-CEBh
Default Value: 0000h
Access: R/WC; RO
Size: 16 bits

This register is used to report which specific error condition resulted in the D2F0 or D2F1 ERRSTS[Thermal Sensor event for SMI/SCI/SERR] or memory mapped IIR Thermal Event. SOFTWARE can examine the current state of the thermal zones by examining the TSS. Software can distinguish internal or external Trip Event by examining TSS.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:10	RO	00h	**Reserved**
9:9	R/WC	0b	**Was Catastrophic Thermal Sensor Interrupt Event:** 1 = Indicates that a Catastrophic Thermal Sensor trip based on a higher to lower temperature transition through the trip point occurred in the past 0 = No trip for this event, software must write a 1 to clear this status bit.
8:8	R/WC	0b	**Was Hot Thermal Sensor Interrupt Event:** 1 = Indicates that a Hot Thermal Sensor trip based on a higher to lower temperature transition through the trip point occurred in the past 0 = No trip for this event Software must write a 1 to clear this status bit.
7:7	R/WC	0b	**Was Aux0 Thermal Sensor Interrupt Event:** 1 = Indicates that an Aux Thermal Sensor trip based on a higher to lower temperature transition through the trip point occurred in the past 0 = No trip for this event, software must write a 1 to clear this status bit.
6:6	R/WC	0b	**Was Aux1 Thermal Sensor Interrupt Event:** 1 = Indicates that an Aux1 Thermal Sensor trip based on a higher to lower temperature transition through the trip point occurred in the past 0 = No trip for this event, software must write a 1 to clear this status bit.
5:5	R/WC	0b	**Reserved**
4:4	R/WC	0b	**Catastrophic Thermal Sensor Interrupt Event:** 1 = Indicates that a Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. 0 = No trip for this event, software must write a 1 to clear this status bit.



(Sheet 2 of 2)

Bit	Access	Default Value	Description
3:3	R/WC	0b	**Hot Thermal Sensor Interrupt Event:** 1 = Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. 0 = No trip for this event, software must write a 1 to clear this status bit.
2:2	R/WC	0b	**Aux0 Thermal Sensor Interrupt Event:** 1 = Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. 0 = No trip for this event, software must write a 1 to clear this status bit.
1:1	R/WC	0b	**Aux1 Thermal Sensor Interrupt Event:** 1 = Indicates that an Aux1 Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. 0 = No trip for this event, software must write a 1 to clear this status bit.
0:0	R/WC	0b	**Reserved**

6.4.19 TSTTP0-2 - Thermal Sensor Temperature Trip Point Register 0-2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CEC-CEFh
Default Value: 00000000h
Access: R/WO; R/W/L; RO
Size: 32 bits

This register sets the target values for some of the trip points in the Thermometer mode. See also TSTTP1.

Bit	Access	Default Value	Description
31:31	R/WO	0b	**Lock Bit for Aux0, Aux1 Trip Points:** This bit, when written to a 1, locks the Aux x trip point settings. This lock is reversible. The reversing procedure is: following sequence must be done in order without any other configuration cycles in-between write 04C1C202 to TSTTP0-2 write 04C1C202 to TSTTP1-2 write 04C1C202 to TSTTP1-2 write 04C1C202 to TSTTP1-2 It is expected that the Aux x trip point settings can be changed dynamically when this lock is not set.
30:16	RO	0000h	**Reserved**

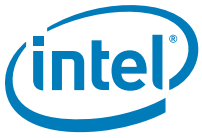
Bit	Access	Default Value	Description
15:8	R/W/L	00h	**Reserved**
7:0	R/W/L	00h	**Aux1 Trip Point Setting (A1TPS):** Sets the target value for the Aux1 trip point. Lockable by TSTTP2-0[31].

6.4.20 TERRCMD - Thermal Error Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CF0h
Default Value: 00h
Access: R/W; RO
Size: 8 bits

This register select which errors are generate a SERR DMI interface special cycle, as enabled by ERRCMD [SERR Thermal Sensor event].The SERR and SCI must not be enabled at the same time for the thermal sensor event.

Bit	Access	Default Value	Description
7:5	RO	0h	**Reserved**
4:4	R/W	0b	**Reserved**
3:3	R/W	0b	**SERR on Aux1 Thermal SensorEvent:** 1 = Enable 0 = Disable
2:2	R/W	0b	**SERR on Catastrophic Thermal Sensor Event:** 1 =Enable 0 = Disable
1:1	R/W	0b	**SERR on Hot Thermal Sensor Event:** 1 = Enable 0 = Disable
0:0	R/W	0b	**SERR on Aux0 Thermal Sensor Event:** 1 = Enable 0 = Disable



6.4.21 TSMICMD - Thermal SMI Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CF1h
Default Value: 00h
Access: R/W; RO
Size: 8 bits

This register selects specific errors to generate a SMI DMI cycle, as enabled by the SMI Error Command register[SMI on Thermal Sensor Trip].

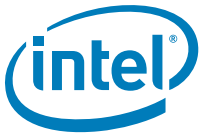
Bit	Access	Default Value	Description
7:5	RO	0h	**Reserved**
4:4	R/W	0b	**Reserved**
3:3	R/W	0b	**SMI on Aux1 Thermal Sensor Trip:** 1 = Enable 0 = Disable
2:2	R/W	0b	**SMI on Catastrophic Thermal Sensor Trip:** 1 = Enable 0 = Disable
1:1	R/W	0b	**SMI on Hot Thermal Sensor Trip:** 1 = Enable 0 = Disable
0:0	R/W	0b	**SMI on Aux0 Thermal Sensor Trip:** 1 = Enable 0 = Disable

6.4.22 TSCICMD - Thermal SCI Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CF2h
Default Value: 00h
Access: R/W; RO
Size: 8 bits

This register selects specific errors to generate a SCI DMI cycle, as enabled by the SCI Error Command register [SCI on Thermal Sensor Trip].The SCI and SERR must not be enabled at the same time for the thermal sensor event.

Bit	Access	Default Value	Description
7:5	RO	0h	**Reserved**
4:4	R/W	0b	**Reserved**
3:3	R/W	0b	**SCI on Aux1 Thermal Sensor Trip:** 1 = Enable 0 = Disable
2:2	R/W	0b	**SCI on Catastrophic Thermal Sensor Trip:** 1 = Enable 0 = Disable
1:1	R/W	0b	**SCI on Hot Thermal Sensor Trip:** 1 = Enable 0 = Disable
0:0	R/W	0b	**SCI on Aux0 Thermal Sensor Trip:** 1 = Enable 0 = Disable



6.4.23 TINTRCMD - Thermal INTR Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CF3h
Default Value: 00h
Access: R/W; RO
Size: 8 bits

This register selects specific errors to generate an INT DMI cycle.

Bit	Access	Default Value	Description
7:5	RO	0h	**Reserved**
4:4	R/W	0b	**Reserved**
3:3	R/W	0b	**INTR on Aux1 Thermal Sensor Trip:** 1 = An INTR DMI cycle is generated by (G)MCH
2:2	R/W	0b	**INTR on Catastrophic Thermal Sensor Trip:** 1 = An INTR DMI cycle is generated by (G)MCH
1:1	R/W	0b	**INTR on Hot Thermal Sensor Trip:** 1 = An INTR DMI cycle is generated by (G)MCH
0:0	R/W	0b	**INTR on Aux0 Thermal Sensor Trip:** 1 = An INTR DMI cycle is generated by (G)MCH

6.4.24 EXTTSCS - External Thermal Sensor Control and Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CFFh
Default Value: 00h
Access: R/WO; R/W/L; RO
Size: 8 bits

(Sheet 1 of 2)

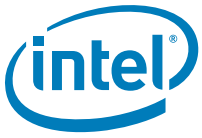
Bit	Access	Default Value	Description
7:7	R/WO	0b	**External Sensor Enable:** Setting this bit to 1 locks the lockable bits in this register. This bit may only be set to a 0 by a hardware reset. Once locked, writing a 0 to bit has no effect. If both internal sensor throttling and external write sensor throttling are enabled, either can initiate throttling. 0 = External Sensor input is disabled. 1 = External Sensor input is enabled.
6:6	R/W/L	0b	**Throttling Type Select (TTS):** Lockable by EXTTSCS [External Sensor Enable]. If External Thermal Sensor Enable = 1, then 0 = DRAM throttling based on the settings in the Device 0 MCHBAR Dram Throttling Control register 1 = (G)MCH throttling, based on the settings in the Device 0 MCHBAR

(Sheet 2 of 2)

Bit	Access	Default Value	Description
5:5	R/W/L	0b	**EXTTS1 Action Select (AS1):** Lockable by EXTTSCS [External Sensor Enable].If External Thermal Sensor Enable = 1, then 0 = The external sensor trip functions same as a Thermometer mode hot trip 1 = The external sensor trip functions as an Thermometer mode aux0 trip ***Note:*** This bit is N/A when Fast C4/C4E exit is enabled.
4:4	R/W/L	0b	**EXTTS0 Action Select (AS0):** Lockable by EXTTSCS [External Sensor Enable]. If External Thermal Sensor Enable = 1, then 0 = The external sensor trip functions same as a Thermometer mode catastrophic trip 1 = The external sensor trip functions same as a Thermometer mode hot trip The above functionality will not be supported when Aux0 trip on EXTTS0# is enabled.
3:3	RO	0b	**EXTTS0 Trip Indicator (S0TI):** A 1 indicates that an externally monitored temperature is exceeding the programmed setting of an external thermal sensor.
2:2	RO	0b	**EXTTS1 Trip Indicator (S1TI):** A 1 indicates that an externally monitored temperature is exceeding the programmed setting of an external thermal sensor. ***Note:*** This bit is N/A when Fast C4/C4e exit is enabled.
1:1	RO	0b	**Reserved**
0:0	R/W	0b	**External Thermal Sensor Signals Routing Control 0:** Route all external sensor signals to affect internal thermal sensor x registers, as appropriate. 1: Route all external sensor signals to affect thermal sensor not x registers, as appropriate

6.4.25 DFT_STRAP1 – DFT Register

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: E08-E0Bh
Default Value:
_0xxx__xx0x__xxxx__xxxx__xxxx__xxxx__xxxx__xxxx_h
Access: RO
Size: 32 bits



6.5 Device 0 MCHBAR ACPI Power Management Controls

Table 7. Device 0 MCHBAR ACPI Power Management Control Registers

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
C2 to C3 Transition Timer	C2C3TT	F00	F03	00000000h	R/W; RO
C3 to C4 Transition Timer	C3C4TT	F04	F07	00000000h	R/W; RO
Memory Interface Power Management Control 4	MIPMC4	F08	F09	0000h	R/W; RO
Memory Interface Power Management Control 5	MIPMC5	F0A	F0B	0000h	R/W; RO
Memory Interface Power Management Control 6	MIPMC6	F0C	F0D	0000h	R/W; RO
Memory Interface Power Management Control 7	MIPMC7	F0E	F0E	00h	R/W
Reserved		F0F	F0F		
Power Management Configuration	PMCFG	F10	F13	00040000h	R/W; RO
Self-Refresh Channel Status	SLFRCS	F14	F17	00000000h	R/WC; RO
Reserved		F18	fAF		
Graphics Interface Power Management Control 1	GIPMC1	FB0	FB3	00000000h	R/W; RO
Reserved		FB4	FB7		
Front Side Bus Power Management Control 1	FSBPMC1	FB8	FBB	00000000h	R/W; RO
Reserved		FBC	FBF		
Unit Power Management Control Register 3	UPMC3	FC0	FC3	00000000h	R/W; RO
Reserved		FC4	FFB		
ECO Bits	ECO	FFC	FFF	00000000h	R/W; RO

6.5.1 Power Management Mode Support Options

The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets have added the capability to support C state power management modes. This allows the option to support CPU PM from either the (G)MCH or ICH7M. Both cannot be implemented at the same time. Below summarizes the difference between supporting CPU states from (G)MCH.

6.5.1.1 (G)MCH CPU PM State Support (Enhanced)

- HCPUSLP# controlled by (G)MCH
- HCPUSLP# asserted in C2, C3 and C4
- PM_BM_BUSY# is not used

6.5.2 C2C3TT - C2 to C3 Transition Timer

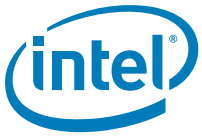
B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F00-F03h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
31:19	RO	0000h	**Reserved**
18:7	R/W	000h	**C2 to C3 Transition Timer (C2C3TT):** Dual purpose timer in 128-core clock granularity Number of core clocks to wait between last snoop from PEG or DMI to a request for C3 being issued. 000 = 128 host clocks FFF = 524288 host clocks MSI's, for the purpose of this register, are handled as snoops
6:0	RO	00h	**Reserved**

6.5.3 C3C4TT - C3 to C4 Transition Timer

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F04-F07h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
31:19	RO	0000h	**Reserved**
18:7	R/W	000h	**C3 to C4 Transition Time:** 128-core clock granularity Number of core clocks to wait between last snoop from PEG or DMI to a request for C4 being issued. 000 = 128 host clocks FFF = 524288 host clocks MSI's, for the purpose of this register, are handled as snoops
6:0	RO	00h	**Reserved**



6.5.4 MIPMC4 - Memory Interface Power Management Control 4

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	F08-F09h
Default Value:	0000h
Access:	R/W; RO
Size:	16 bits

6.5.5 MIPMC5 - Memory Interface Power Management Control 5

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	F0A-F0Bh
Default Value:	0000h
Access:	R/W; RO
Size:	16 bits

6.5.6 MIPMC6 - Memory Interface Power Management Control 6

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	F0C-F0Dh
Default Value:	0000h
Access:	R/W; RO
Size:	16 bits

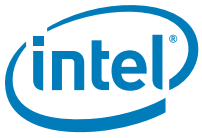
6.5.7 MIPMC7 - Memory Interface Power Management Control 7

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	F0Eh
Default Value:	00h
Access:	R/W
Size:	8 bits

6.5.8 PMCFG - Power Management Configuration

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F10-F13h
Default Value: 00040000h
BIOS Optimal Default 0h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
31	R/W	0b	**Reserved**
30	RO	0b	**Reserved**
29:5	RO; R/W	0b	**Reserved**
4	R/W	0b	**Enhanced Power Management Features Enable:** 0 = Reserved 1 = Enable (G)MCH will use the snoop timers for determining the proper time for allowing a power management mode transition that was requested by ACPI software PM_BM_BUSY# is never asserted The allowed behavior in this mode may be restricted by the Enhanced Power Management Mode and the Enhanced Power Management Snoop-detect Behavior fields
3	RO	0b	**Reserved**
2	R/W	0b	**Reserved**
1:0	R/W	00b	**Enhanced Power Management Mode:** This field is ignored if the Enhanced Power Management Features Enable bit is clear **00** = All enhanced power management functions allowed **01** = Disable the C2 to C3 snoop timer based transition. Never go past C2. **10** = Disable the C3 to C4 snoop timer based transition. Never go past C3. **11** = Reserved Recommended Setting = 00 Field is ignored if the Enhanced Power Management Features Enable = 0



6.5.9 SLFRCS - Self-Refresh Channel Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F14-F17h
Default Value: 00000000h
Access: R/WC; RO
Size: 32 bits

This register is reset by PWROK only.

Bit	Access	Default Value	Description
31:2	RO	00000000h	**Reserved**
1	R/WC	0b	**Channel 1 in Self-refresh:** Set by power management hardware after Channel 1 is placed in self refresh as a result of a Power State or a Reset Warn sequence, Cleared by Power management hardware before starting Channel 1 self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel 1 not guaranteed to be in self-refresh. 1 = Channel 1 in self-refresh.
0	R/WC	0b	**Channel 0 in Self-refresh:** Set by power management hardware after Channel 0 is placed in self refresh as a result of a Power State or a Reset Warn sequence, Cleared by Power management hardware before starting Channel 0 self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel 0 not guaranteed to be in self-refresh. 1 = Channel 0 in self-refresh.

6.5.10 GIPMC1 - Graphics Interface Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: FB0-FB3h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

6.5.11 FSBPMC1 - Front Side Bus Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: FB8-FBBh
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

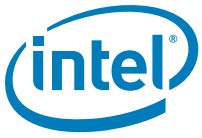
6.5.12 UPMC3 Unit Power Management Control 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: FC0-FC3h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

6.5.13 ECO - ECO Bits

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: FFC-FFFh
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
32:19	R/W; RO	0000000000b	**Reserved**
18	R/W	0b	**Aux0 Trip Remapping:** 1: Aux0 trip for DRAM refresh rate will come from EXTTS0 0: Aux0 trip for DRAM refresh rate will come from EXTTS1 ***Note:*** This register should only be set to 1 if Fast C4/C4e exit has been enabled.
17	R/W; RO	0b	**Reserved**
16	R/W	0h	**Fast C4/C4E Exit Enable:** 1 = Enable Fast C4/C4E Exit. (This bit should be used only if the required implementation exists in hardware; see Section 10.6.7) 0 = Normal Operation (EXTTS1# will be used for thermal throttling)
15:0	RO	0000h	**Reserved**



6.6 DMI RCRB

This section describes the mapped registers for the DMI. The DMIBAR register, described in Section 5.1.15, provides the base address for these registers.

This Root Complex Register Block (RCRB) controls the (G)MCH-ICH7-M serial interconnect. An RCRB is required for configuration and control of elements that are located internal to a root complex that are not directly associated with a PCI Express device. The base address of this space is programmed in DMIBAR in Device 0 configuration space.

Note: All RCRB register spaces needs to remain organized as they are here. The VC capabilities (or at least the first PCI Express Extended Capability) must begin at the 0h offset of the 4-K area pointed to by the associated BAR. This is a *PCI Local Bus Specification* requirement.

Table 8. DMI RCB (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
DMI Virtual Channel Enhanced Capability	DMIVCECH	0	3	04010002h	RO
DMI Port VC Capability Register 1	DMIPVCCAP1	4	7	00000001h	RO; R/WO
DMI Port VC Capability Register 2	DMIPVCCAP2	8	B	00000001h	RO
DMI Port VC Control	DMIPVCCTL	C	D	0000h	R/W; RO
Reserved		E	F		
DMI VC0 Resource Capability	DMIVC0RCAP	10	13	00000001h	RO
DMI VC0 Resource Control	DMIVC0RCTL0	14	17	800000FFh	R/W; RO
Reserved		18	19		
DMI VC0 Resource Status	DMIVC0RSTS	1A	1B	0002h	RO
DMI VC1 Resource Capability	DMIVC1RCAP	1C	1F	00008001h	RO
DMI VC1 Resource Control	DMIVC1RCTL1	20	23	01000000h	R/W; RO
Reserved		24	25		
DMI VC1 Resource Status	DMIVC1RSTS	26	27	0002h	RO
Reserved		28	57		
DMI Link Entry 1 Address	DMILE1A	58	5F	0000000000000000h	R/WO; RO
DMI Link Entry 2 Description	DMILE2D	60	63	00000000h	R/WO; RO
Reserved		64	67		
DMI Link Entry 2 Address	DMILE2A	68	6F	0000000000000000h	R/WO; RO
Reserved		70	83		
DMI Link Capabilities	DMILCAP	84	87	00012C41h	R/WO; RO

Table 8. DMI RCB (Sheet 2 of 2)

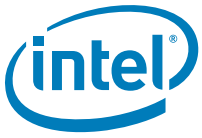
Register Name	Register Symbol	Register Start	Register End	Default Value	Access
DMI Link Control	DMILCTL	88	89	0000h	R/W; RO
DMI Link Status	DMILSTS	8A	8B	0001h	RO
Reserved		8C	EF		
DMI Control 1	DMICTL1	F0	F3	00010000h	R/W; RO; R/W/SC;
Reserved		F4	FB		
DMI Control 2	DMICTL2	FC	FF	00000000h	R/W;
Reserved		100	EB3		
DMI DRC configuration	DMIDRCCFG	EB4	EB7	81010000h	R/W; RO;

6.6.1 DMIVCECH - DMI Virtual Channel Enhanced Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 0-3h
Default Value: 04010002h
Access: RO
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

Bit	Access	Default Value	Description
31:20	RO	040h	**Pointer to Next Capability (PNC):** This field contains the offset to the next PCI Express* capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	RO	1h	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliance with the current *PCI Local Bus Specification.*
15:0	RO	0002h	**Extended Capability ID (ECID):** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.



6.6.2 DMIPVCCAP1 - DMI Port VC Capability Register 1

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 4-7h
Default Value: 00000001h
Access: R/WO; RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	0000000h	**Reserved**
6:4	RO	000b	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3:3	RO	0b	**Reserved**
2:0	R/WO	001b	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel is not included in this count.

6.6.3 DMIPVCCAP2 - DMI Port VC Capability Register 2

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 8-Bh
Default Value: 00000001h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	**Reserved**
23:8	RO	0000h	**Reserved**
7:0	RO	01h	**VC Arbitration Capability (VCAC):** Indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority and VC0 is the lowest priority.

6.6.4 DMIPVCCTL - DMI Port VC Control

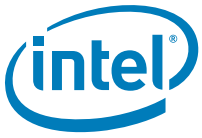
B/D/F/Type: 0/0/0/DMIBAR
Address Offset: C-Dh
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	**Reserved**
3:1	R/W	000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled. 000: Hardware fixed arbitration scheme - e.g., Round Robin Others: Reserved See the current *PCI Local Bus Specification* for more details.
0	RO	0b	**Reserved**

6.6.5 DMIVC0RCAP - DMI VC0 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 10-13h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	00h	**Reserved**
23	RO	0b	**Reserved**
22:16	RO	00h	**Reserved**
15	RO	0b	**Reject Snoop Transactions (REJSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	**Reserved**
7:0	RO	01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.



6.6.6 DMIVC0RCTL0 - DMI VC0 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 14-17h
Default Value: 800000FFh
Access: R/W; RO
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

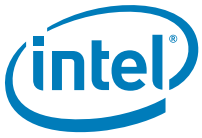
Bit	Access	Default Value	Description
31:31	RO	1b	**Virtual Channel 0 Enable (VC0E):** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	**Reserved**
26:24	RO	000b	**Virtual Channel 0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	RO	0h	**Reserved**
19:17	R/W	000b	**Port Arbitration Select (PAS):** Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only bit 0 of that field is asserted. This field will always be programmed to 1.
16:8	RO	000h	**Reserved**
7:1	R/W	7Fh	**Traffic Class / Virtual Channel 0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given link.
0	RO	1b	**Traffic Class 0 / Virtual Channel 0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

6.6.7 DMIVC0RSTS - DMI VC0 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1A-1Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1:1	RO	1b	**Virtual Channel 0 Negotiation Pending (VC0NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. BIOS Requirement: Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a link.
0:0	RO	0b	**Reserved**



6.6.8 DMIVC1RCAP - DMI VC1 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1C-1Fh
Default Value: 00008001h
Access: RO
Size: 32 bits

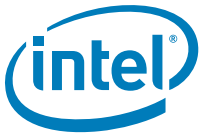
Bit	Access	Default Value	Description
31:24	RO	00h	**Reserved**
23:23	RO	0b	**Reserved**
22:16	RO	00h	**Reserved**
15:15	RO	1b	**Reject Snoop Transactions (REJSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	**Reserved**
7:0	RO	01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

6.6.9 DMIVC1RCTL1 - DMI VC1 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 20-23h
Default Value: 01000000h
Access: R/W; RO
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access	Default Value	Description
31	R/W	0b	**Virtual Channel 1 Enable (VC1E):** 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express* port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. BIOS Requirement: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a link before re-enabling the Virtual Channel.
30:27	RO	0h	**Reserved**
26:24	R/W	001b	**Virtual Channel 1 ID (VC1ID):** Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20	RO	0h	**Reserved**
19:17	R/W	000b	**Port Arbitration Select (PAS):** Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.



Bit	Access	Default Value	Description
16:8	RO	000h	**Reserved**
7:1	R/W	00h	**Traffic Class / Virtual Channel 1 Map (TCVC1M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given link.
0	RO	0b	**Traffic Class 0 / Virtual Channel 1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.

6.6.10 DMIVC1RSTS - DMI VC1 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 26-27h
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1:1	RO	1b	**Virtual Channel 1 Negotiation Pending (VC1NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a link.
0:0	RO	0b	**Reserved**

6.6.11 DMILE2A - DMI Link Entry 2 Address

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 68-6Fh
Default Value: 0000000000000000h
Access: R/WO; RO
Size: 64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

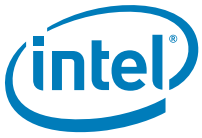
Bit	Access	Default Value	Description
63:32	RO	00000000h	**Reserved**
31:12	R/WO	00000h	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	000h	**Reserved**

6.6.12 DMILCAP - DMI Link Capabilities

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 84-87h
Default Value: 00012C41h
Access: R/WO; RO
Size: 32 bits

This register indicates DMI specific capabilities.

Bit	Access	Default Value	Description
31:18	RO	0000h	**Reserved**
17:15	R/WO	010b	**L1 Exit Latency (L1SELAT):** Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 µs to less than 4 µs. 000:Less than 1 µs 001:1 µs to less than 2 µs 010:2 µs to less than 4 µs 011:4 µs to less than 8 µs 100:8 µs to less than 16 µs 101:16 µs to less than 32 µs 110:32 µs-64 µs 111:More than 64 µs Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.



Bit	Access	Default Value	Description
14:12	R/WO	010b	**L0s Exit Latency (L0SELAT):** Indicates the length of time this Port requires to complete the transition from L0s to L0. 000:Less than 64 ns 001:64 ns to less than 128 ns 010:128 ns to less than 256 ns 011:256 ns to less than 512 ns 100:512 ns to less than 1 µs 101:1 µs to less than 2 µs 110:2 µs-4 µs 111:More than 4 µs
11:10	RO	11b	**Active State Link PM Support (ASLPMS):** L0s & L1 entry supported.
9:4	RO	04h	**Max Link Width (MLW):** Indicates the maximum number of lanes supported for this link.
3:0	RO	1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

6.6.13 DMILCTL - DMI Link Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 88-89h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This register allows control of DMI.

Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	R/W	0b	**Extended Synch (EXTSYNC):** 0: Standard Fast Training Sequence (FTS). 1: Forces extended transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP Ordered Set prior to entering L0, and the transmission of 1024 TS1 ordered sets in the RecoveryRcvrLock state prior to entering the RecoveryRcvrCfg state. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6:2	RO	00h	**Reserved**

Bit	Access	Default Value	Description
1:0	R/W	00b	**Active State Power Management Support (ASPMS):** Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: Reserved 11: L0s and L1 Entry Supported

6.6.14 DMILSTS - DMI Link Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 8A-8Bh
Default Value: 0001h
Access: RO
Size: 16 bits

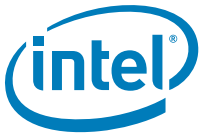
This register indicates DMI status.

Bit	Access	Default Value	Description
15:10	RO	00h	**Reserved**
9:4	RO	00h	**Negotiated Width (NWID):** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 00h:Reserved 01h:Reserved 02h:X2 04h:X4 All other encodings are reserved.
3:0	RO	1h	**Negotiated Speed (NSPD):** Indicates negotiated link speed. 1h: 2.5 Gb/s All other encodings are reserved.

6.6.15 DMICTL1 – DMI Control 1

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: F0-F3h
Default Value: 00010000h
Access: R/W; RO; R/W/SC;
Size: 32 bits

This register must be accessed with DWORD granularity and not with BYTE granularity.



6.6.16 DMICTL2– DMI Control 2

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	FC-FFh
Default Value:	00000000h
Access:	R/W
Size:	32 bits

6.6.17 DMIDRCCFG - DMI DRC Configuration

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	EB4-EB7h
Default Value:	81010000h
Access:	R/W; RO
Size:	32 bits

6.7 Egress Port (EP) RCRB

This Root Complex Register Block (RCRB) controls the port arbitration that is based on the current *PCI Local Bus Specification*. Port arbitration is done for all PCI Express-based isochronous requests (always on Virtual Channel 1) before being submitted to the main memory arbiter. The base address of this space is programmed in EPBAR in Device 0 configuration space.

6.7.1 EP Register Summary

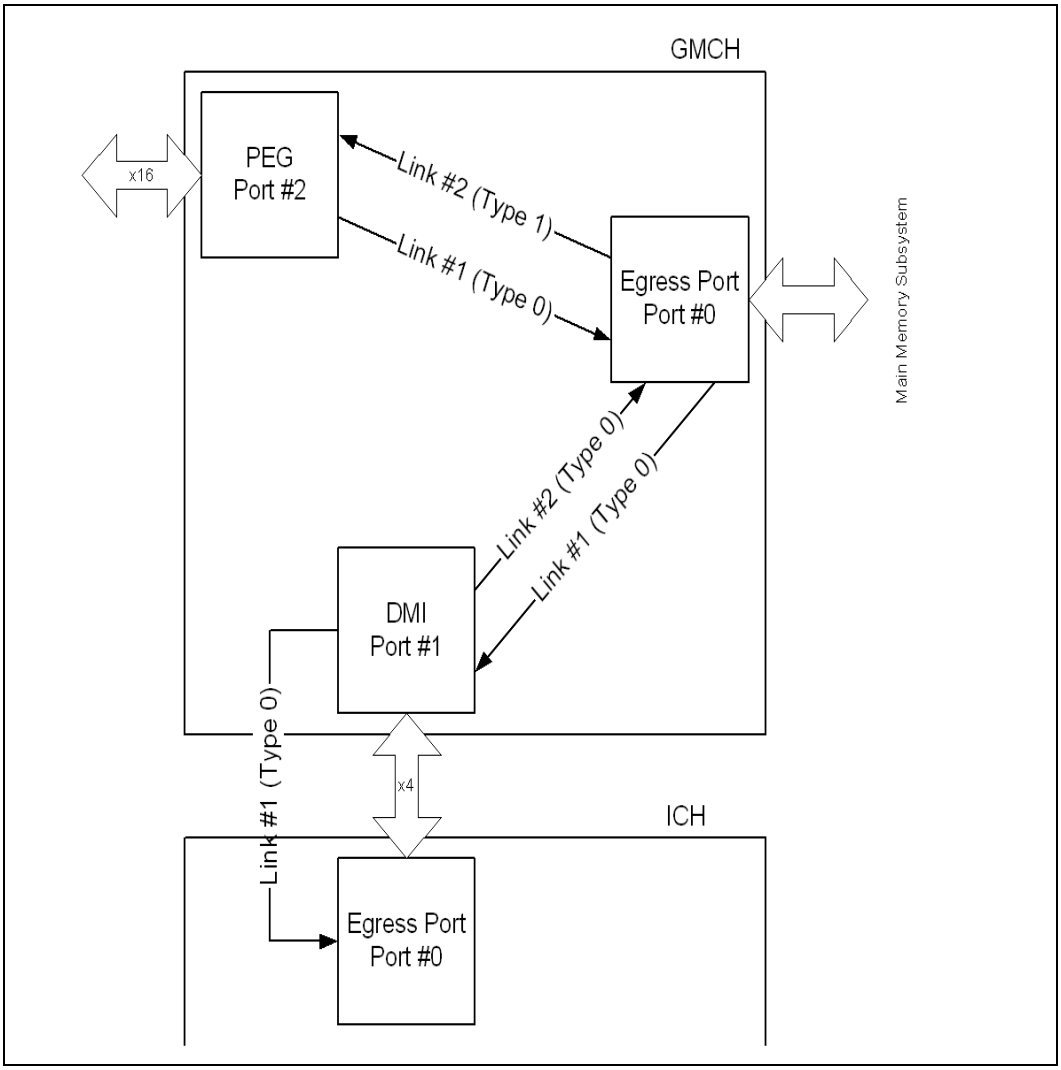
Table 9. EP Register Summary (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		0	3		
EP Port VC Capability Register 1	EPPVCCAP1	4	7	00000401h	R/WO; RO
EP Port VC Capability Register 2	EPPVCCAP2	8	B	00000001h	RO
EP VC 0 Resource Capability	EPVC0RCAP	10	13	00000001h	RO
EP VC 0 Resource Control	EPVC0RCTL	14	17	800000FFh	R/W; RO;
EP VC 0 Resource Status	EPVC0RSTS	1A	1B	0000H	RO
EP VC 1 Resource Capability	EPVC1RCAP	1C	1F	10008010h	R/WO; RO
EP VC 1 Resource Control	EPVC1RCTL	20	23	01080000h	R/W; RO; R/W/SC;
EP VC 1 Resource Status	EPVC1RSTS	26	27	0000h	RO;
EP VC 1 Maximum Number of Time Slots	EPVC1MTS	28	2B	04050609h	R/W;
EP VC 1 Isoch Slot Time	EPVC1IST	38	3F	0000000000000000h	R/W;
Reserved		40	43		

Table 9. EP Register Summary (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
EP Element Self Description	EPESD	44	47	00000201h	R/WO; RO
Reserved		48	4F		
EP Link Entry 1 Description	EPLE1D	50	53	01000000h	R/WO; RO
Reserved		54	57		
EP Link Entry 1 Address	EPLE1A	58	5F	0000000000000000h	R/WO; RO
EP Link Entry 2 Description	EPLE2D	60	63	02000002h	R/WO; RO
Reserved		64	67		
EP Link Entry 2 Address	EPLE2A	68	6F	0000000000008000h	RO
Reserved		70	9F		
Port Arbitration Table	PORTARB	100	11F	00000000000000000000000000000000000000000000000000000000000000000000000000000000h	R/W;
Reserved		120	FFF		

Figure 9. Link Declaration Topology



6.7.2 EPPVCCAP1 - EP Port VC Capability Register 1

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 4-7h
Default Value: 00000401h
Access: R/WO; RO
Size: 32 bits

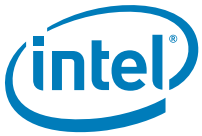
Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:12	RO	00000h	**Reserved**
11:8	RO	04h	**Reserved**
7:3	RO	0h	**Reserved**
2:0	R/WO	001b	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

6.7.3 EPPVCCAP2 - EP Port VC Capability Register 2

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 8-Bh
Default Value: 00000001h
Access: RO;
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.



6.7.4 EPVC0RCAP - EP VC 0 Resource Capability

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 10-13h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	00h	**Reserved**
23	RO	0b	**Reserved**
22:16	RO	00h	**Reserved**
15	RO	0b	**Reject Snoop Transactions (RSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	**Reserved**
7:0	RO	01h	**Port Arbitration Capability (PAC):** Indicates types of Port Arbitration supported by this VC0 resource.

6.7.5 EPVC0RCTL - EP VC 0 Resource Control

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 14-17h
Default Value: 800000FFh
Access: R/W; RO
Size: 32 bits

Controls the resources associated with Egress Port Virtual Channel 0.

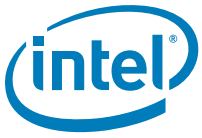
Bit	Access	Default Value	Description
31	RO	1b	**VC0 Enable:** For VC0 this is hardwired to 1 and read only.
30:27	RO	0h	**Reserved**
26:24	RO	000b	**VC0 ID:** For VC0 this is hardwired to 0 and read only.
23:20	RO	0h	**Reserved**
19:17	RO	000b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service.
16:8	RO	000h	**Reserved**
7:1	R/W	7Fh	**TC/VC0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource.
0	RO	1b	**Reserved**

6.7.6 EPVC0RSTS - EP VC 0 Resource Status

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 1A-1Bh
Default Value: 0000h
Access: RO
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1	RO	0b	**VC0 Negotiation Pending (VC0NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a link.
0	RO	0b	**Reserved**



6.7.7 EPVC1RCAP - EP VC 1 Resource Capability

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 1C-1Fh
Default Value: 10008010h
Access: R/WO; RO
Size: 32 bits

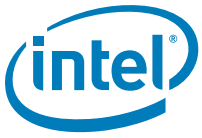
Bit	Access	Default Value	Description
31:24	RO	10h	**Reserved**
23	RO	0b	**Reserved**
22:16	R/WO	00h	**Reserved**
15:15	RO	1b	**Reject Snoop Transactions (RSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	**Reserved**
7:0	RO	10h	**Port Arbitration Capability (PAC):** Indicates types of Port Arbitration supported by this VC1 resource.

6.7.8 EPVC1RCTL - EP VC 1 Resource Control

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 20-23h
Default Value: 01080000h
Access: R/W; RO; R/W/SC;
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access	Default Value	Description
31	R/W	0b	**VC1 Enable (VC1E):** Upon Read after negotiation: 0: Virtual Channel is disabled. 1: Virtual Channel is enabled.
30:27	RO	0h	**Reserved**
26:24	R/W	001b	**VC1 ID (VC1ID):** Assigns a VC ID to the VC resource. Assigned value must be non-zero.
23:20	RO	0h	**Reserved**
19:17	R/W	100b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service.
16	R/W/SC	0b	**Reserved**
15:8	RO	00h	**Reserved**
7:1	R/W	00h	**TC/VC1 Map (TCVC1M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource.
0:0	RO	0b	**TC0/VC1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.



6.7.9 EPVC1RSTS - EP VC 1 Resource Status

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 26-27h
Default Value: 0000h
Access: RO
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1	RO	0b	**VC1 Negotiation Pending (VC1NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a link.
0	RO	0b	**Reserved**

6.7.10 EPVC1MTS - EP VC 1 Maximum Number of Time Slots

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 28-2Bh
Default Value: 04050609h
Access: R/W
Size: 32 bits

The fields in this register reflects the maximum number of time slots supported by the (G)MCH for various configurations.

6.7.11 EPVC1IST - EP VC 1 Isoch Slot Time

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 38-3Fh
Default Value: 0000000000000000h
Access: R/W
Size: 64 bits

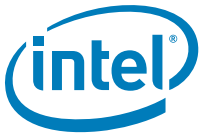
This register reflects the number of common host clocks per time slot.

6.7.12 EPESD - EP Element Self Description

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 44-47h
Default Value: 00000201h
Access: R/WO; RO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
31:24	RO	00h	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00 h indicates to configuration software that this is the default egress port.
23:16	R/WO	00h	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO	02h	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PEG and DMI).
7:4	RO	0h	**Reserved**
3:0	RO	1h	**Element Type (ET):** Indicates the type of the Root Complex Element. Value of h represents a port to system memory.



6.7.13 EPLE1D - EP Link Entry 1 Description

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 50-53h
Default Value: 01000000h
Access: R/WO; RO
Size: 32 bits

This register is the first part of a Link Entry which declares an internal link to another Root Complex Element.

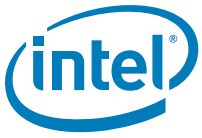
Bit	Access	Default Value	Description
31:24	RO	01h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2	RO	0000h	**Reserved**
1	RO	0b	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

6.7.14 EPLE1A - EP Link Entry 1 Address

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 58-5Fh
Default Value: 0000000000000000h
Access: R/WO; RO
Size: 64 bits

This register is the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	**Reserved**
31:12	R/WO	00000h	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0	RO	000h	**Reserved**



6.7.15 EPLE2D - EP Link Entry 2 Description

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 60-63h
Default Value: 02000002h
Access: R/WO; RO
Size: 32 bits

This register is the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	02h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (PEG). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2	RO	0000h	**Reserved**
1	RO	1b	**Link Type (LTYP):** Indicates that the link points to configuration space of the integrated device which controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	R/WO	0b	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

6.7.16 EPLE2A - EP Link Entry 2 Address

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 68-6Fh
Default Value: 0000000000008000h
Access: RO
Size: 64 bits

This register is the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:28	RO	0000000 00h	**Reserved**
27:20	RO	00h	**Bus Number (BUSN):**
19:15	RO	00001b	**Device Number (DEVN):** Target for this link is PCI Express x16 port (Device 1).
14:12	RO	000b	**Function Number (FUNN):**
11:0	RO	000h	**Reserved**

6.7.17 PORTARB - Port Arbitration Table

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 100-11Fh
Default Value : 00000000000000000000000000000000 00000000000000000000000000000000h
Access: R/W
Size: 256 bits

The port arbitration table register is a read-write register array used to store the arbitration table for Port Arbitration of the Egress Port VC resource.

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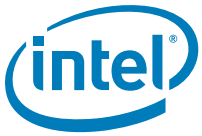


7 PCI Express Graphics Device 1 Configuration Registers (D1:F0)

Device 1 contains the controls associated with the x16 root port that is the intended attach point for external graphics. It is typically referred to as PEG (PCI Express Graphics) port. It also functions as the virtual PCI-to-PCI bridge that was previously associated with AGP.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express* Base Specification* defines two types of reserved bits:

- Reserved and Preserved: Reserved for future RW implementations; software must preserve value read for writes to bits.
- Reserved and 0: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and 0, all bits marked as Reserved are part of the Reserved and Preserved type which has historically been the typical definition for Reserved.

Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first disable the link, then program the registers, then re-enable the link (which will cause a full-retrain with the new settings).

7.1 PEG Device 1 Function 0 Configuration Register Summary

Table 10. PEG Device 1 Function 0 Configuration Register Summary (Sheet 1 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID1	0	1	8086h	RO
Device Identification	DID1	2	3	27A1h[1] 27ADh[2]	RO
PCI Command	PCICMD1	4	5	0000h	R/W; RO
PCI Status	PCISTS1	6	7	0010h	R/WC; RO
Revision Identification	RID1	8	8	00h	RO
Class Code	CC1	9	B	060400h	RO
Cache Line Size	CL1	C	C	00h	R/W
Header Type	HDR1	E	E	01h	RO
Primary Bus Number	PBUSN1	18	18	00h	RO
Secondary Bus Number	SBUSN1	19	19	00h	R/W
Subordinate Bus Number	SUBUSN1	1A	1A	00h	R/W

Table 10. PEG Device 1 Function 0 Configuration Register Summary (Sheet 2 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
I/O Base Address	IOBASE1	1C	1C	F0h	R/W; RO
I/O Limit Address	IOLIMIT1	1D	1D	00h	R/W; RO
Secondary Status	SSTS1	1E	1F	0000h	R/WC; RO
Memory Base Address	MBASE1	20	21	FFF0h	R/W; RO
Memory Limit Address	MLIMIT1	22	23	0000h	R/W; RO
Prefetchable Memory Base Address	PMBASE1	24	25	FFF1h	R/W; RO
Prefetchable Memory Limit Address	PMLIMIT1	26	27	0001h	R/W; RO
Reserved		28	2B		
Reserved		2C	2F		
Capabilities Pointer	CAPPTR1	34	34	88h	RO
Interrupt Line	INTRLINE1	3C	3C	00h	R/W
Interrupt Pin	INTRPIN1	3D	3D	01h	RO
Bridge Control	BCTRL1	3E	3F	0000h	R/W; RO
Reserved		7F	7F		
Power Management Capabilities	PM_CAPID1	80	83	C8029001h	RO
Power Management Control/Status	PM_CS1	84	87	00000000h	RO; R/W/S;
Subsystem ID and Vendor ID Capabilities	SS_CAPID	88	8B	0000800Dh	RO
Subsystem ID and Subsystem Vendor ID	SS	8C	8F	00008086h	R/WO
Message Signaled Interrupts Capability ID	MSI_CAPID	90	91	A005h	RO
Message Control	MC	92	93	0000h	R/W; RO
Message Address	MA	94	97	00000000h	R/W; RO
Message Data	MD	98	99	0000h	R/W
PCI Express-G* Capability List	PEG_CAPL	A0	A1	0010h	RO
PCI Express-G Capabilities	PEG_CAP	A2	A3	0141h	R/WO; RO
Device Capabilities	DCAP	A4	A7	00000000h	RO
Device Control	DCTL	A8	A9	0000h	R/W; RO
Device Status	DSTS	AA	AB	0000h	R/WC; RO
Link Capabilities	LCAP	AC	AF	02014D01h	R/WO; RO
Link Control	LCTL	B0	B1	0000h	R/W; ROR/W/ SC;

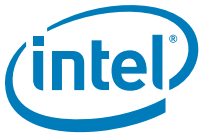


Table 10. PEG Device 1 Function 0 Configuration Register Summary (Sheet 3 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Link Status	LSTS	B2	B3	1001h	RO
Slot Capabilities	SLOTCAP	B4	B7	00000000h	R/WO; RO
Slot Control	SLOTCTL	B8	B9	01C0h	R/W; RO
Slot Status	SLOTSTS	BA	BB	00_0s00_0h	R/WC; RO
Root Control	RCTL	BC	BD	0000h	R/W; RO
Root Status	RSTS	C0	C3	00000000h	R/WC; RO
PCI Express-G Legacy Control	PEGLC	EC	EF	00000000h	R/W; RO
PEG Control 1	PEGCTL1	F0	F3	00010000h	RO;R/W
Reserved		F4	E7F		
PEG Timing Configuration	PEGTCFG	E80	E83	08080488h	R/WC; RO;

NOTES:
1. Valid for all Mobile Intel 945 Express Chipsets except for the Mobile Intel 945GME/GSE Express Chipset.
2. Valid for the Mobile Intel 945GME/GSE Express Chipset only.

7.1.1 VID1 - Vendor Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 00-01h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

7.1.2 DID1 - Device Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 02-03h
Default Value: 27A1h[1]
27ADh[2]
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	27A1h[1] 27ADh[2]	**Device Identification Number (DID1):** Identifier assigned to the (G)MCH Device 1 (virtual PCI-to-PCI bridge, PCI Express* Graphics port).

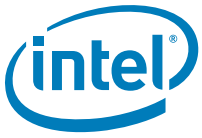
NOTES:
1. Valid for all Mobile Intel 945 Express Chipsets except for the Mobile Intel 945GME/GSE Express Chipset.
2. Valid for the Mobile Intel 945GME/GSE Express Chipset only.

7.1.3 PCICMD1 - PCI Command

B/D/F/Type: 0/1/0/PCI
Address Offset: 04-05h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

(Sheet 1 of 3)

Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10	R/W	0b	**INTA Assertion Disable (INTAAD):** 0: This device is permitted to generate INTA interrupt messages. 1: This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be deasserted when this bit is set. Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD assert and deassert messages.
9	RO	0b	**Fast Back-to-Back Enable (FB2B):** Not Applicable or Implemented. Hardwired to 0.



(Sheet 2 of 3)

Bit	Access	Default Value	Description
8	R/W	0b	**SERR Message Enable (SERRE1):** Controls Device 1 SERR messaging. The (G)MCH communicates the SERRB condition by sending an SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control register. 0: The SERR message is generated by the (G)MCH for Device 1 only under conditions enabled individually through the Device Control register. 1: The (G)MCH is enabled to generate SERR messages which will be sent to the ICH for specific Device 1 error conditions generated/detected on the primary side of the virtual PCI-to-PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS1 register.
7	RO	0b	**Reserved**
6	R/W	0b	**Parity Error Enable (PERRE):** Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0: Master Data Parity Error bit in PCI Status register **cannot** be set. 1: Master Data Parity Error bit in PCI Status register **can** be set.
5	RO	0b	**VGA Palette Snoop (VGAPS):** Not Applicable or Implemented. Hardwired to 0.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Not Applicable or Implemented. Hardwired to 0.
3	RO	0b	**Special Cycle Enable (SCE):** Not Applicable or Implemented. Hardwired to 0.
2	R/W	0b	**Bus Master Enable (BME):** Controls the ability of the PEG port to forward Memory and IO Read/Write Requests in the upstream direction. 0: This device is prevented from making memory or IO requests to its primary bus. According to the *PCI Local Bus Specification*, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address 0 with byte enables deasserted. Reads will be forwarded to memory address 0 and will return Unsupported Request status (or Master abort) in its completion packet. 1: This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available. This bit does not affect forwarding of completions from the primary interface to the secondary interface.

(Sheet 3 of 3)

Bit	Access	Default Value	Description
1	R/W	0b	**Memory Access Enable (MAE):** 0: All of Device 1's memory space is disabled. 1: Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W	0b	**IO Access Enable (IOAE):** 0: All of Device 1's I/O space is disabled. 1: Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

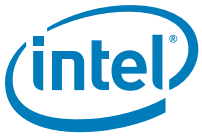
7.1.4 PCISTS1 - PCI Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 06-07h
Default Value: 0010h
Access: R/WC; RO
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the “virtual” host-PCI Express bridge embedded within the (G)MCH.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Not Applicable or Implemented. Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device (error forwarding is not supported).
14	R/WC	0b	**Signaled System Error (SSE):** This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO	0b	**Received Master Abort Status (RMAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO	0b	**Received Target Abort Status (RTAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO	0b	**Signaled Target Abort Status (STAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO	00b	**DEVSELB Timing (DEVT):** This device is not the subtractive decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.



(Sheet 2 of 2)

Bit	Access	Default Value	Description
8	RO	0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PEG's virtual PCI-to-PCI bridge is integrated with the MCH functionality there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The *PCI Local Bus Specification* defines it as a R/WC, but for our implementation an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO	0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	**Reserved**
5	RO	0b	**66/60 MHz Capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4	RO	1b	**Capabilities List (CAPL):** Indicates that a capabilities list is present. Hardwired to 1.
3	RO	0b	**INTA Status (INTAS):** Indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and deassert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit. Note that INTA emulation interrupts received across the link are not reflected in this bit.
2:0	RO	000b	**Reserved**

7.1.5 RID1 - Revision Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH Device 1. These bits are read only and writes to this register have no effect.

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision Identification Number (RID1):** This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. For the A-0 Stepping, this value is 00h.

7.1.6 CC1 - Class Code

B/D/F/Type: 0/1/0/PCI
Address Offset: 9-Bh
Default Value: 060400h
Access: RO
Size: 24 bits

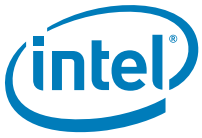
This register identifies the basic function of the device, a more specific sub-class, and a register- specific programming interface.

Bit	Access	Default Value	Description
23:16	RO	06h	**Base Class Code (BCC):** Indicates the base class code for this device. This code has the value 06h, indicating a bridge device.
15:8	RO	04h	**Sub-Class Code (SUBCC):** Indicates the sub-class code for this device. The code is 04h indicating a PCI-to-PCI bridge.
7:0	RO	00h	**Programming Interface (PI):** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

7.1.7 CL1 - Cache Line Size

B/D/F/Type: 0/1/0/PCI
Address Offset: 0Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access	Default Value	Description
7:0	R/W	00h	**Cache Line Size (Scratch Pad):** Implemented by PCI Express* devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.



7.1.8 HDR1 - Header Type

B/D/F/Type: 0/1/0/PCI
Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access	Default Value	Description
7:0	RO	01h	**Header Type Register (HDR):** Returns 01 to indicate that this is a single function device with bridge header layout.

7.1.9 PBUSN1 - Primary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this “virtual” host-PCI Express bridge is connected to PCI Bus 0.

Bit	Access	Default Value	Description
7:0	RO	00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since Device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

7.1.10 SBUSN1 - Secondary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 19h
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the “virtual” bridge, i.e., to PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

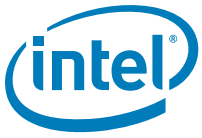
Bit	Access	Default Value	Description
7:0	R/W	00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express-G*.

7.1.11 SUBUSN1 - Subordinate Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Bit	Access	Default Value	Description
7:0	R/W	00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the Device 1 bridge. When only a single PCI device resides on the PCI Express-G segment, this register will contain the same value as the SBUSN1 register.



7.1.12 IOBASE1 - I/O Base Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	1Ch
Default Value:	F0h
Access:	R/W; RO
Size:	8 bits

This register controls the CPU to PCI Express-G I/O access routing based on the following formula:

IO_BASE <= address <= IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Access	Default Value	Description
7:4	R/W	Fh	**I/O Address Base (IOBASE):** Corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express-G*. BIOS must not set this register to 00h otherwise 0CF8h/0CFCh accesses will be forwarded to the PCI Express hierarchy associated with this device.
3:0	RO	0h	**Reserved**

7.1.13 IOLIMIT1 - I/O Limit Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	1Dh
Default Value:	00h
Access:	R/W; RO
Size:	8 bits

This register controls the CPU to PCI Express-G I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

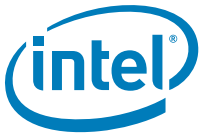
Bit	Access	Default Value	Description
7:4	R/W	0h	**I/O Address Limit (IOLIMIT):** Corresponds to A[15:12] of the I/O address limit of Device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0	RO	0h	**Reserved**

7.1.14 SSTS1 - Secondary Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 1E-1Fh
Default Value: 0000h
Access: R/WC; RO
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express-G side) of the “virtual” PCI-to-PCI bridge embedded within (G)MCH.

Bit	Access	Default Value	Description
15	R/WC	0b	**Detected Parity Error (DPE):** When set indicates that the MCH received across the link (upstream) a Posted Write Data Poisoned TLP (EP=1).
14	R/WC	0b	**Received System Error (RSE):** This bit is set when the secondary side receives an ERR_FATAL or ERR_NONFATAL message due to an error detected by the secondary side, and the SERR Enable bit in the Bridge Control register is 1.
13	R/WC	0b	**Received Master Abort (RMA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	R/WC	0b	**Received Target Abort (RTA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO	0b	**Signaled Target Abort (STA):** Not Applicable or Implemented. Hardwired to 0. The (G)MCH does not generate Target Aborts (the (G)MCH will never complete a request using the Completer Abort Completion status).
10:9	RO	00b	**DEVSELB Timing (DEVT):** Not Applicable or Implemented. Hardwired to 0.
8	R/WC	0b	**Master Data Parity Error (SMDPE):** When set indicates that the MCH received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO	0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	**Reserved**
5	RO	0b	**66/60 MHz Capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4:0	RO	00h	**Reserved**



7.1.15 MBASE1 - Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 20-21h
Default Value: FFF0h
Access: R/W; RO
Size: 16 bits

This register controls the CPU to PCI Express-G non-prefetchable memory access routing based on the following formula:

MEMORY_BASE <= address <= MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return 0's when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access	Default Value	Description
15:4	R/W	FFFh	**Memory Address Base (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express-G*.
3:0	RO	0h	**Reserved**

7.1.16 MLIMIT1 - Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 22-23h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This register controls the CPU to PCI Express-G non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return 0's when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express-G address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved CPU-PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges, i.e., prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the (G)MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Access	Default Value	Description
15:4	R/W	000h	**Memory Address Limit (MLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express-G*.
3:0	RO	0h	**Reserved**

7.1.17 PMBASE1 - Prefetchable Memory Base Address

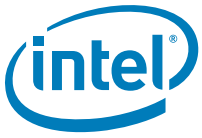
B/D/F/Type: 0/1/0/PCI
Address Offset: 24-25h
Default Value: FFF1h
Access: R/W; RO
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE <= address <= PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 32-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access	Default Value	Description
15:4	R/W	FFFh	**Prefetchable Memory Base Address (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express-G*.
3:0	RO	0h	**Reserved**



7.1.18 PMLIMIT1 - Prefetchable Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 26-27h
Default Value: 0001h
Access: R/W; RO
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE <= address <= PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 32-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the CPU perspective.

Bit	Access	Default Value	Description
15:4	R/W	000h	**Prefetchable Memory Address Limit (PMLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express-G*.
3:0	RO	0h	**Reserved**

7.1.19 CAPPTR1 - Capabilities Pointer

B/D/F/Type: 0/1/0/PCI
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access	Default Value	Description
7:0	RO	88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

7.1.20 INTRLINE1 - Interrupt Line

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value; rather it is used by device drivers and operating systems to determine priority and vector information.

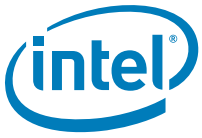
Bit	Access	Default Value	Description
7:0	R/W	00h	**Interrupt Connection (INTCON):** Used to communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this device's interrupt pin is connected.

7.1.21 INTRPIN1 - Interrupt Pin

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access	Default Value	Description
7:0	RO	01h	**Interrupt Pin (INTPIN):** As a single function device, the PCI Express* device specifies INTA as its interrupt pin. 01h=INTA.



7.1.22 BCTRL1 - Bridge Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 3E-3Fh
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

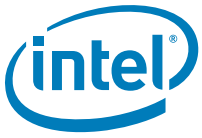
This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express-G) as well as some bits that affect the overall behavior of the "virtual" host-PCI Express bridge embedded within (G)MCH, e.g., VGA compatible address ranges mapping.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:12	RO	0h	**Reserved**
11	RO	0b	**Discard Timer SERR Enable (DTSERRE):** Not Applicable or Implemented. Hardwired to 0.
10	RO	0b	**Discard Timer Status (DTSTS):** Not Applicable or Implemented. Hardwired to 0.
9	RO	0b	**Secondary Discard Timer (SDT):** Not Applicable or Implemented. Hardwired to 0.
8	RO	0b	**Primary Discard Timer (PDT):** Not Applicable or Implemented. Hardwired to 0.
7	RO	0b	**Fast Back-to-Back Enable (FB2BEN):** Not Applicable or Implemented. Hardwired to 0.
6	R/W	0b	**Secondary Bus Reset (SRESET):** Setting this bit triggers a hot reset on the corresponding PCI Express* Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0, L0s, or L1 states.
5	RO	0b	**Master Abort Mode (MAMODE):** When acting as a master, unclaimed reads that experience a master abort returns all 1's and any writes that experience a master abort completes normally and the data is thrown away. Hardwired to 0.
4	R/W	0b	**VGA 16-bit Decode (VGA16D):** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0: Execute 10-bit address decodes on VGA I/O accesses. 1: Execute 16-bit address decodes on VGA I/O accesses.
3	R/W	0b	**VGA Enable (VGAEN):** Controls the routing of CPU initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in Device 0, offset 97h[0].

(Sheet 2 of 2)

Bit	Access	Default Value	Description
2	R/W	0b	**ISA Enable (ISAEN):** Needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the (G)MCH to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0: All addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions will be mapped to PCI Express-G*. 1: (G)MCH will not forward to PCI Express-G any I/O transactions addressing the last 768 bytes in each 1-KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express-G these cycles will be forwarded to DMI where they can be subtractively or positively claimed by the ISA bridge.
1	R/W	0b	**SERR Enable (SERREN):** 0: No forwarding of error messages from secondary side to primary side that could result in an SERR. 1: ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	R/W	0b	**Parity Error Response Enable (PEREN):** Controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the MCH receives across the link (upstream) a Read Data Completion Poisoned TLP 0: Master Data Parity Error bit in Secondary Status register **cannot** be set. 1: Master Data Parity Error bit in Secondary Status register **can** be set.



7.1.23 PM_CAPID1 - Power Management Capabilities

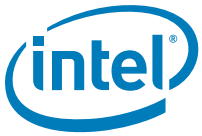
B/D/F/Type: 0/1/0/PCI
Address Offset: 80-83h
Default Value: C8029001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:27	RO	19h	**PME Support (PMES):** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot & D3cold. This device is not required to do anything to support D3hot & D3cold; it simply must report that those states are supported. Refer to the current *PCI Power Management Specification* for encoding explanation and other power management details.
26:26	RO	0b	**D2 Power State Support (D2PSS):** Hardwired to 0 to indicate that the D2 power management state is **not** supported.
25:25	RO	0b	**D1 Power State Support (D1PSS):** Hardwired to 0 to indicate that the D1 power management state is **not** supported.
24:22	RO	000b	**Auxiliary Current (AUXC):** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21:21	RO	0b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is **not** required before generic class device driver is to use it.
20:20	RO	0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19:19	RO	0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate this device does **not** support PMEB generation.
18:16	RO	010b	**PCI PM CAP Version (PCIPMCV):** Hardwired to 02h to indicate there are 4 bytes of power management registers implemented and that this device complies with the current *PCI Power Management Interface Specification*.
15:8	RO	90h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, then the next item in the capabilities list is the PCI Express capability at A0h.
7:0	RO	01h	**Capability ID (CID):** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

7.1.24 PM_CS1 - Power Management Control/Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 84-87h
Default Value: 00000000h
Access: ROR/W/S;
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:15	RO	0b	**PME Status (PMESTS):** Indicates that this device does not support PMEB generation from D3cold.
14:13	RO	00b	**Data Scale (DSCALE):** Indicates that this device does not support the power management data register.
12:9	RO	0h	**Data Select (DSEL):** Indicates that this device does not support the power management data register.
8	R/W/S	0b	**PME Enable (PMEE):** Indicates that this device does not generate PMEB assertion from any D-state. 0: PMEB generation not possible from any D State 1: PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2	RO	00h	**Reserved**



Bit	Access	Default Value	Description
1:0	R/W	00b	**Power State (PS):** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00: D0 01: D1 (Not supported in this device) 10: D2 (Not supported in this device) 11: D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional. When the Power State is other than D0, the bridge will Master Abort (i.e., not claim) any downstream cycles (with exception of type 0 configuration cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the MCH logs as Master Aborts in Device 0 PCISTS[13] There is no additional hardware functionality required to support these Power States.

7.1.25 SS_CAPID - Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 88-8Bh
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides.

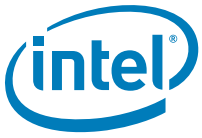
Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:8	RO	80h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO	0Dh	**Capability ID (CID):** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI bridge.

7.1.26 SS - Subsystem ID and Subsystem Vendor ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 8C-8Fh
Default Value: 00008086h
Access: R/WO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and hardware reset.

Bit	Access	Default Value	Description
31:16	R/WO	0000h	**Subsystem ID (SSID):** Identifies the particular subsystem and is assigned by the vendor.
15:0	R/WO	8086h	**Subsystem Vendor ID (SSVID):** Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.



7.1.27 MSI_CAPID - Message Signaled Interrupts Capability ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 90-91h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

The reporting of the existence of this capability can be disabled by setting MSICH (CAPL[0] @ 7Fh). In that case walking this linked list will skip this capability and instead go directly from the PCI PM capability to the PCI Express capability.

Bit	Access	Default Value	Description
15:8	RO	A0h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Express* capability.
7:0	RO	05h	**Capability ID (CID):** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

7.1.28 MC - Message Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 92-93h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

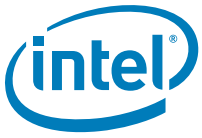
Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	RO	0b	**64-bit Address Capable (64AC):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32-b/4-GB limit.

Bit	Access	Default Value	Description
6:4	R/W	000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO	000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. Value:Number of Messages Requested 000: 1 All of the following are reserved in this implementation: 001: 2 010: 4 011: 8 100: 16 101: 32 110: Reserved 111: Reserved
0	R/W	0b	**MSI Enable (MSIEN):** Controls the ability of this device to generate MSIs. 0:MSI will not be generated. 1:MSI will be generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

7.1.29 MA - Message Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 94-97h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
31:2	R/W	00000000h	**Message Address (MA):** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	**Force Dword Align (FDWA):** Hardwired to 0 so that addresses assigned by system software are always aligned on a dword address boundary.



7.1.30 MD - Message Data

B/D/F/Type: 0/1/0/PCI
Address Offset: 98-99h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/W	0000h	**Message Data (MD):** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

7.1.31 PEG_CAPL - PCI Express-G Capability List

B/D/F/Type: 0/1/0/PCI
Address Offset: A0-A1h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

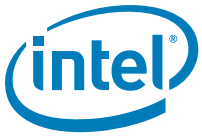
Bit	Access	Default Value	Description
15:8	RO	00h	**Pointer to Next Capability (PNC):** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express* specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO	10h	**Capability ID (CID):** Identifies this linked list item (capability structure) as being for PCI Express registers.

7.1.32 PEG_CAP - PCI Express-G Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A2-A3h
Default Value: 0141h
Access: R/WO; RO
Size: 16 bits

This register defines the PCI Express device capabilities.

Bit	Access	Default Value	Description
15:14	RO	00b	**Reserved**
13:9	RO	00h	**Interrupt Message Number (IMN):** Not Applicable or Implemented. Hardwired to 0.
8	R/WO	1b	**Slot Implemented (SI):** 0: The PCI Express* Link associated with this port is connected to an integrated component or is disabled. 1: The PCI Express Link associated with this port is connected to a slot. *BIOS Requirement: This field must be initialized appropriately if a slot connection is not implemented.*
7:4	RO	4h	**Device/Port Type (DPT):** Hardwired to 4h to indicate root port of PCI Express Root Complex.
3:0	RO	1h	**PCI Express Capability Version (PCIECV):** Hardwired to 1 as it is the first version.

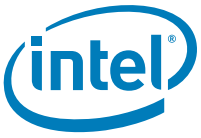


7.1.33 DCAP - Device Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A4-A7h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register defines the PCI Express device capabilities.

Bit	Access	Default Value	Description
31:6	RO	0000000h	**Reserved**
5:5	RO	0b	**Extended Tag Field Supported (ETFS):** Hardwired to indicate support for 5-bit tags as a requestor.
4:3	RO	00b	**Phantom Functions Supported (PFS):** Not Applicable or Implemented. Hardwired to 0.
2:0	RO	000b	**Max Payload Size (MPS):** Hardwired to indicate 128B max supported payload for Transaction Layer Packets (TLP).



7.1.34 DCTL - Device Control

B/D/F/Type: 0/1/0/PCI
Address Offset: A8-A9h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

Provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command register.

Bit	Access	Default Value	Description
15:12	RO	0h	**Reserved**
11:11	RO	0b	**Reserved**
10:8	RO	000b	**Reserved**
7:5	R/W	000b	**Max Payload Size (MPS):** 000:128B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. All other encodings are reserved. Hardware will actually ignore this field. It is writeable only to support compliance testing.
4	RO	0b	**Reserved**
3	R/W	0b	**Unsupported Request Reporting Enable (URRE):** When set, Unsupported Requests will be reported. Reporting of error messages received by Root Port is controlled exclusively by Root Control register.
2	R/W	0b	**Fatal Error Reporting Enable (FERE):** When set fatal errors will be reported. For a Root Port, the reporting of fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	R/W	0b	**Non-Fatal Error Reporting Enable (NFERE):** When set non-fatal errors will be reported. For a Root Port, the reporting of non-fatal errors is internal to the root. No external ERR_NONFATAL message is generated. Uncorrectable errors can result in degraded performance.
0	R/W	0b	**Correctable Error Reporting Enable (CERE):** When set correctable errors will be reported. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_CORR message is generated.

7.1.35 DSTS - Device Status

B/D/F/Type: 0/1/0/PCI
Address Offset: AA-ABh
Default Value: 0000h
Access: R/WC; RO
Size: 16 bits

This register reflects status corresponding to controls in the Device Control register.

The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

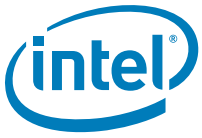
Bit	Access	Default Value	Description
15:6	RO	000h	**Reserved**
5	RO	0b	**Transactions Pending (TP):** 0: All pending transactions (including completions for any outstanding non-posted requests on any used Virtual Channel) have been completed. 1: Indicates that the device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4	RO	0b	**Reserved**
3	R/WC	0b	**Unsupported Request Detected (URD):** When set this bit indicates that the Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported.
2	R/WC	0b	**Fatal Error Detected (FED):** When set this bit indicates that fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
1	R/WC	0b	**Non-Fatal Error Detected (NFED):** When set this bit indicates that non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
0	R/WC	0b	**Correctable Error Detected (CED):** When set this bit indicates that correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.

7.1.36 LCAP - Link Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: AC-AFh
Default Value: 02014D01h
Access: R/WO; RO
Size: 32 bits

This register indicates PCI Express device specific capabilities.

Bit	Access	Default Value	Description
31:24	RO	02h	**Port Number (PN):** Indicates the PCI Express* port number for the given PCI Express link. Matches the value in Element Self Description[31:24].
23:18	RO	00h	**Reserved**
17:15	R/WO	010b	**L1 Exit Latency (L1ELAT):** Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 µs to less than 4 µs. *BIOS Requirement: If this field is required to be any value other than the default, BIOS must initialize it accordingly.* Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	RO	100b	**L0s Exit Latency (L0SELAT):** Indicates the length of time this Port requires to complete the transition from L0s to L0. 000:Less than 64 ns 001:64 ns to less than 128 ns 010:128 ns to less than 256 ns 011:256 ns to less than 512 ns 100:512 ns to less than 1 µs 101:1 µs to less than 2 µs 110:2 µs - 4 µs 111:More than 4 µs The actual value of this field depends on the common Clock Configuration bit (LCTL[6]) and the Common and Non-Common clock L0s Exit Latency values in PEGL0SLAT (Offset 224h).
11:10	R/WO	11b	**Active State Link PM Support (ASLPMS):** BIOS Requirement: Desktop chipsets do not support ASPM L1, so BIOS should program this field to "01".
9:4	RO	10h	**Max Link Width (MLW):** Indicates the maximum number of lanes supported for this link.
3:0	RO	1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.



7.1.37 LCTL - Link Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B0-B1h
Default Value: 0000h
Access: R/W; ROR/W/SC
Size: 16 bits

This register allows control of PCI Express link.

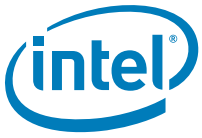
Bit	Access	Default Value	Description
15:8	RO	000h	**Reserved**
7	R/W	0b	**Reserved**
6	R/W	0b	**Common Clock Configuration (CCC):** 0: Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1: Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. The state of this bit affects the L0s Exit Latency reported in LCAP[14:12] and the N_FTS value advertised during link training. See PEGL0SLAT at offset 224h.
5	R/W/SC	0b	**Retrain Link (RL):** 0: Normal operation. 1: Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
4	R/W	0b	**Link Disable (LD):** 0: Normal operation 1: Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 1 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO	0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 bytes.
2	RO	0b	**Reserved**
1:0	R/W	00b	**Active State PM (ASPM):** Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: Reserved 11: L0s and L1 Entry Supported

7.1.38 LSTS - Link Status

B/D/F/Type: 0/1/0/PCI
Address Offset: B2-B3h
Default Value: 1001h
Access: RO
Size: 16 bits

This register indicates PCI Express link status.

Bit	Access	Default Value	Description
15:13	RO	000b	**Reserved**
12	RO	1b	**Slot Clock Configuration (SCC):** 0: The device uses an independent clock irrespective of the presence of a reference on the connector. 1: The device uses the same physical reference clock that the platform provides on the connector.
11	RO	0b	**Link Training (LTRN):** Indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO	0b	**Training Error (TE):** This bit is set by hardware upon detection of unsuccessful training of the Link to the L0 Link state.
9:4	RO	00h	**Negotiated Width (NW):** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 01h: X1 10h: X16 All other encodings are reserved.
3:0	RO	1h	**Negotiated Speed (NS):** Indicates negotiated link speed. 1h:2.5 Gb/s All other encodings are reserved.



7.1.39 SLOTCAP - Slot Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: B4-B7h
Default Value: 00000000h
Access: R/WO; RO
Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

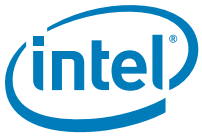
Bit	Access	Default Value	Description
31:19	R/WO	0000h	**Physical Slot Number (PSN):** Indicates the physical slot number attached to this Port. *BIOS Requirement: This field must be initialized by BIOS to a value that assigns a slot number that is globally unique within the chassis.*
18:17	RO	00b	**Reserved**
16:15	R/WO	00b	**Slot Power Limit Scale (SPLS):** Specifies the scale used for the Slot Power Limit Value. 00: 1.0x 01: 0.1x 10: 0.01x 11: 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	R/WO	00h	**Slot Power Limit Value (SPLV):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	R/WO	0b	**Hot Plug Capable (HPC):** Indicates that this slot is capable of supporting Hot Plug operations.
5	R/WO	0b	**Hot Plug Surprise (HPS):** Indicates that a device present in this slot might be removed from the system without any prior notification.
4	R/WO	0b	**Power Indicator Present (PIP):** Indicates that a Power Indicator is implemented on the chassis for this slot.
3	R/WO	0b	**Attention Indicator Present (AIP):** Indicates that an Attention Indicator is implemented on the chassis for this slot.
2	RO	0b	**Reserved**
1	RO	0b	**Reserve**
0	R/WO	0b	**Attention Button Present (ABP):** Indicates that an Attention Button is implemented on the chassis for this slot. The Attention Button allows the user to request Hot Plug operations.

7.1.40 SLOTCTL - Slot Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B8-B9h
Default Value: 01C0h
Access: R/W; RO
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10:10	R/W	0b	**Reserved**
9:8	R/W	01b	**Power Indicator Control (PIC):** Reads to this register return the current state of the Power Indicator. Writes to this register set the Power Indicator and cause the Port to send the appropriate POWER_INDICATOR_* messages. 00: Reserved 01: On 10: Blink 11: Off
7:6	R/W	11b	**Attention Indicator Control (AIC):** Reads to this register return the current state of the Attention Indicator. Writes to this register set the Attention Indicator and cause the Port to send the appropriate ATTENTION_INDICATOR_* messages. 00: Reserved 01: On 10: Blink 11: Off
5	R/W	0b	**Hot Plug Interrupt Enable (HPIE):** When set enables generation of hot plug interrupt on enabled Hot Plug events.
4	R/W	0b	**Command Completed Interrupt Enable (CCI):** When set enables the generation of hot plug interrupt when a command is completed by the Hot Plug controller.
3	R/W	0b	**Presence Detect Changed Enable (PDCE):** When set enables the generation of Hot Plug interrupt or wakeup message on a presence detect changed event.
2	RO	0b	**Reserved**
1	RO	0b	**Reserved**
0	R/W	0b	**Attention Button Pressed Enable (ABPE):** When set enables the generation of Hot Plug interrupt or wakeup message on an attention button pressed event.



7.1.41 SLOTSTS - Slot Status

B/D/F/Type: 0/1/0/PCI
Address Offset: BA-BBh
Default Value: 00_0s00_0h
Access: R/WC; RO
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

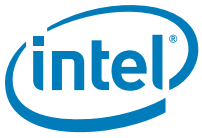
Bit	Access	Default Value	Description
15:7	RO	000h	**Reserved**
6	RO	Strap	**Presence Detect State (PDS):** Indicates the presence of a card in the slot. 0: Slot Empty 1: Card Present in slot.
5	RO	0b	**Reserved**
4	R/WC	0b	**Command Completed (CC):** Set when the hot plug controller completes an issued command. This field applies only to commands/writes issued by software to control the Attention Indicator or Power Indicator. The command completed bit will be set when a slot control register write has occurred and all appropriate indicator messages associated with that slot control register write have been sent. A command completed interrupt will only be sent when enabled and the command completed bit transitions from 0 to 1. Software must wait for confirmation of command completion (notification via Command Completed interrupt or polling Command Completed field) before issuing the next command. However, if the Command Completed register is not set 1 second after the command is issued, the host software is allowed to repeat the command or to issue the next command. It is a programming error if software issues a write before the controller has completed processing of the previous command and before the 1-second time limit has expired.
3	R/WC	0b	**Presence Detect Changed (PDC):** Set when a Presence Detect change is detected. This corresponds to an edge on the signal that corresponds to bit 6 of this register (Presence Detect State).
2	RO	0b	**Reserved**
1	RO	0b	**Reserved**
0	R/WC	0b	**Attention Button Pressed (ABP):** Set when the Attention Button is pressed.

7.1.42 RCTL - Root Control

B/D/F/Type: 0/1/0/PCI
Address Offset: BC-BDh
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command register.

Bit	Access	Default Value	Description
15:4	RO	000h	**Reserved**
3	R/W	0b	**PME Interrupt Enable (PMEIE):** 0: No interrupts are generated as a result of receiving PME messages. 1: Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status register. A PME interrupt is also generated if the PME Status bit of the Root Status register is set when this bit is set from a cleared state.
2	R/W	0b	**System Error on Fatal Error Enable (SEFEE):** Controls the Root Complex's response to fatal errors. 0: No SERR generated on receipt of fatal error. 1: Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	R/W	0b	**System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE):** Controls the Root Complex's response to non-fatal errors. 0: No SERR generated on receipt of non-fatal error. 1: Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W	0b	**System Error on Correctable Error Enable (SECEE):** Controls the Root Complex's response to correctable errors. 0: No SERR generated on receipt of correctable error. 1: Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.



7.1.43 RSTS - Root Status

B/D/F/Type: 0/1/0/PCI
Address Offset: C0-C3h
Default Value: 00000000h
Access: R/WC; RO
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access	Default Value	Description
31:18	RO	0000h	**Reserved**
17	RO	0b	**PME Pending (PMEP):** Indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	R/WC	0b	**PME Status (PMES):** Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO	0000h	**PME Requestor ID (PMERID):** Indicates the PCI requestor ID of the last PME requestor.

7.1.44 PEGLC - PCI Express-G Legacy Control

B/D/F/Type: 0/1/0/PCI
Address Offset: EC-EFh
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

This register controls functionality that is needed by Legacy (non-PCI Express aware) OS's during run time.

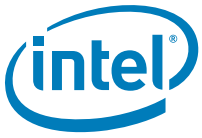
Bit	Access	Default Value	Description
31:3	RO	00000000h	**Reserved**
2	R/W	0b	**PME GPE Enable (PMEGPE):** 0: Do not generate GPE PME message when PME is received. 1: Generate a GPE PME message when PME is received (Assert_PMEGPE and deassert_PMEGPE messages on DMI). This enables the MCH to support PMEs on the PEG port under legacy OSs.
1	R/W	0b	**Hot Plug GPE Enable (HPGPE):** 0: Do not generate GPE Hot Plug message when Hot Plug event is received. 1: Generate a GPE Hot Plug message when Hot Plug Event is received (Assert_HPGPE and deassert_HPGPE messages on DMI). This enables the MCH to support Hot Plug on the PEG port under legacy OSs.
0	R/W	0b	**General Message GPE Enable (GENGPE):** 0: Do not forward received GPE assert/deassert messages. 1: Forward received GPE assert/deassert messages. These general GPE message can be received via the PEG port from an external Intel® device (i.e., PxH) and will be subsequently forwarded to the ICH (via Assert_GPE and deassert_GPE messages on DMI). For example, PxH might send this message if a PCI Express* device is hot plugged into a PxH downstream port.

7.1.45 PEGCTL1 – PEG Control 1

B/D/F/Type: 0/1/0/PCI
Address Offset: F0-F3h
Default Value: 00010000h
Access: R/W; RO
Size: 32 bits
This register must be accessed with DWORD granularity and not with BYTE granularity.

7.1.46 PEGTCFG – PEG Timing Configuration

B/D/F/Type: 0/1/0/MMR
Address Offset: E80-E83h
Default Value: 08080488h
Access: R/WC; RO
Size: 32 bits



7.2 PCI Express Device 1 Extended Configuration Registers

Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Table 11. PCI Express Device 1 Extended Configuration Registers

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Virtual Channel Enhanced Capability Header	VCECH	100	103	14010002h	RO
Port VC Capability Register 1	PVCCAP1	104	107	00000001h	R/WO; RO
Port VC Capability Register 2	PVCCAP2	108	10B	00000001h	RO
Port VC Control	PVCCTL	10C	10D	0000h	R/W; RO
Reserved		10E	10F		
VC0 Resource Capability	VC0RCAP	110	113	00000000h	RO
VC0 Resource Control	VC0RCTL	114	117	800000FFh	R/W; RO
Reserved		118	119		
VC0 Resource Status	VC0RSTS	11A	11B	0002h	RO
Reserved		11C	13F		
Root Complex Link Declaration Enhanced	RCLDECH	140	143	00010005h	RO
Element Self Description	ESD	144	147	02000100h	R/WO; RO
Reserved		148	14F		
Link Entry 1 Description	LE1D	150	153	00000000h	R/WO; RO
Reserved		154	157		
Link Entry 1 Address	LE1A	158	15F	0000000000000000h	R/WO; RO
Reserved		160	217		
PCI Express-G* Configuration	PEGCFG	200	203	00201F6Eh	R/W; ROR/W/SC;
PCI Express-G Timeout Control	PEGTC	204	207	00000CF4h	R/W; RO;
PCI Express-G Countdown Control	PEGCC	208	20B	000034B0h	R/W; RO;
PCI Express-G Sequence Status	PEGSSTS	218	21F	0000000000000FFFh	RO
Reserved		220	FFF		

7.2.1 VCECH - Virtual Channel Enhanced Capability Header

B/D/F/Type: 0/1/0/MMR
Address Offset: 100-103h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities.

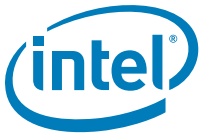
Bit	Access	Default Value	Description
31:20	RO	140h	**Pointer to Next Capability (PNC):** The Link Declaration Capability is the next in the PCI Express* extended capabilities list.
19:16	RO	1h	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliances with the current *PCI Local Bus Specification.*
15:0	RO	0002h	**Extended Capability ID (ECID):** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

7.2.2 PVCCAP1 - Port VC Capability Register 1

B/D/F/Type: 0/1/0/MMR
Address Offset: 104-107h
Default Value: 00000001h
Access: R/WO; RO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	0000000h	**Reserved**
6:4	RO	000b	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	**Reserved**
2:0	R/WO	001b	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.



7.2.3 PVCCAP2 - Port VC Capability Register 2

B/D/F/Type: 0/1/0/MMR
Address Offset: 108-10Bh
Default Value: 00000001h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	**VC Arbitration Table Offset (VCATO):** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8	RO	0000h	**Reserved**
7:0	RO	01h	**VC Arbitration Capability (VCAC):** Indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority. VC0 is the lowest priority.

7.2.4 PVCCTL - Port VC Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 10C-10Dh
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	**Reserved**
3:1	R/W	000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 001b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field can not be modified when more than one VC in the LPVC group is enabled.
0	RO	0b	**Reserved**

7.2.5 VC0RCAP - VC0 Resource Capability

B/D/F/Type: 0/1/0/MMR
Address Offset: 110-113h
Default Value: 00000000h
Access: RO
Size: 32 bits

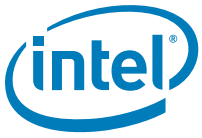
Bit	Access	Default Value	Description
31:16	RO	00h	**Reserved**
15:15	RO	0b	**Reject Snoop Transactions (RSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0	RO	0000h	**Reserved**

7.2.6 VC0RCTL - VC0 Resource Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 114-117h
Default Value: 800000FFh
Access: R/W; RO
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	**VC0 Enable (VC0E):** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	**Reserved**
26:24	RO	000b	**VC0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:8	RO	0000h	**Reserved**
7:1	R/W	7Fh	**TC/VC0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	**TC0/VC0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.



7.2.7 VC0RSTS - VC0 Resource Status

B/D/F/Type: 0/1/0/MMR
Address Offset: 11A-11Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1:1	RO	1b	**VC0 Negotiation Pending (VC0NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	**Reserved**

7.2.8 RCLDECH - Root Complex Link Declaration Enhanced

B/D/F/Type: 0/1/0/MMR
Address Offset: 140-143h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PEG) to other elements of the root complex component to which it belongs. See the current *PCI Local Bus Specification* for link/topology declaration requirements.

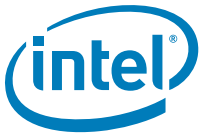
Bit	Access	Default Value	Description
31:20	RO	000h	**Pointer to Next Capability (PNC):** This is the last capability in the PCI Express* extended capabilities list
19:16	RO	1h	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification.
15:0	RO	0005h	**Extended Capability ID (ECID):** Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability. See corresponding Egress Port Link Declaration Capability registers for diagram of Link Declaration Topology.

7.2.9 ESD - Element Self Description

B/D/F/Type: 0/1/0/MMR
Address Offset: 144-147h
Default Value: 02000100h
Access: R/WO; RO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
31:24	RO	02h	**Port Number (PN):** Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	R/WO	00h	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element. **BIOS Requirement**: Must be initialized according to guidelines in the *PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)*.
15:8	RO	01h	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as we don't report any peer-to-peer capabilities in our topology).
7:4	RO	0h	**Reserved**
3:0	RO	0h	**Element Type (ET):** Indicates the type of the Root Complex Element. Value of 0 h represents a root port.



7.2.10 LE1D - Link Entry 1 Description

B/D/F/Type: 0/1/0/MMR
Address Offset: 150-153h
Default Value: 00000000h
Access: R/WO; RO
Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	00h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. **BIOS Requirement**: Must be initialized according to guidelines in the *PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).*
15:2	RO	0000h	**Reserved**
1	RO	0b	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

7.2.11 LE1A - Link Entry 1 Address

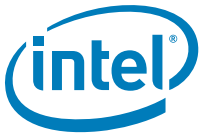
B/D/F/Type: 0/1/0/MMR
Address Offset: 158-15Fh
Default Value: 0000000000000000h
Access: R/WO; RO
Size: 64 bits

This register is the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	**Reserved**
31:12	R/WO	00000h	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	000h	**Reserved**

7.2.12 PEGTC - PCI Express-G Timeout Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 204-207h
Default Value: 00000CF4h
Access: R/W; RO
Size: 32 bits



7.2.13 PEGCC - PCI Express-G Countdown Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 208-20Bh
Default Value: 000034B0h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
31:24	R/W	00h	**Reserved**
23:22	R/W	00b	**Reserved**
21:20	R/W	10b	**L0s Entry Policy (L0SEP):** 00: Standard L0s 01: Ultra Aggressive L0s Entry 10: Aggressive L0s Entry 11: Reserved (undefined behavior) ***Note:*** These bits can be updated by BIOS during run time
19	RO	0b	**Reserved**
18:11	R/W	06h	**Reserved**
10:0	R/W	4B0h	**Reserved**

7.2.14 PEGSTS - PCI Express-G Status

B/D/F/Type: 0/1/0/MMR
Address Offset: 214-217h
Default Value: 0000FFFFh
Access: RO
Size: 32 bits

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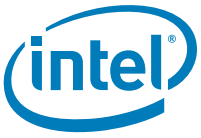
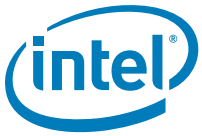




8 Internal Graphics Device 2 Configuration Register (D2:F0-F1)

Note: This section is not applicable for the Mobile Intel 945PM Express Chipset variant.

Device 2 contains registers for the internal graphics functions. The table below lists the PCI configuration registers in order of ascending offset address.

Function 0 can be VGA compatible or not, this is selected through bit 1 of GGC register (Device 0, offset 52h).

The following sections describe Device 2 PCI configuration registers only.

8.1 Device 2 Function 0 PCI Configuration Register Details

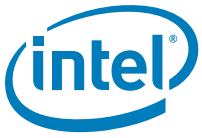
Table 12. Device 2: Function 0 Configuration Registers (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	0	1	8086h	RO
Device Identification	DID2	2	3	27A2h[1] 27AEh[2]	RO
PCI Command	PCICMD2	4	5	0000h	R/W; RO
PCI Status	PCISTS2	6	7	0090h	R/WC; RO
Revision Identification	RID2	8	8	00h	RO
Class Code	CC	9	B	030000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT2	D	D	00h	RO
Header Type	HDR2	E	E	80h	RO
Reserved		F	F		
Memory Mapped Range Address	MMADR	10	13	00000000h	R/W; RO;
I/O Base Address	IOBAR	14	17	00000001h	R/W; RO
Graphics Memory Range Address	GMADR	18	1B	00000008h	R/W; ROR/W/L;
Graphics Translation Table Range Address	GTTADR	1C	1F	00000000h	R/W; R/W/L; RO
Subsystem Vendor Identification	SVID2	2C	2D	0000h	R/WO
Subsystem Identification	SID2	2E	2F	0000h	R/WO

Table 12. Device 2: Function 0 Configuration Registers (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Video BIOS ROM Base Address	ROMADR	30	33	00000000h	RO
Capabilities Pointer	CAPPTR	34	34	90h	RO
Interrupt Line	INTRLINE	3C	3C	00h	R/W;
Interrupt Pin	INTRPIN	3D	3D	01h	RO
Minimum Grant	MINGNT	3E	3E	00h	RO
Maximum Latency	MAXLAT	3F	3F	00h	RO
Mirror of Dev0 Capability Pointer	MCAPPTR	44	44	48h	RO
Reserved		48	50		
Mirror of Dev0 (G)MCH Graphics Control	MGGC	52	53	0030h	RO
Mirror of Dev0 DEVEN	MDEVENdev 0F0	54	57	0000001Bh	RO
Reserved		58	5B		
Base of Stolen Memory	BSM	5C	5F	07800000h	RO
Reserved		60	61		
Multi Size Aperture Control	MSAC	62	62	01h	R/W; RO
Reserved		63	7E		
Capabilities List Control	CAPL	7F	7F	00h	R/W; RO
Reserved		80	BF		
Graphics Debug Reset	GDRST	C0	C0	00h	R/W; RO
Unit Power Management Control 4	UPMC4	C1	C2	0000h	RO; R/W;
Reserved		C2	CF		
Power Management Capabilities ID	PMCAPID	D0	D1	0001h	RO
Power Management Capabilities	PMCAP	D2	D3	0022h	RO
Power Management Control/Status	PMCS	D4	D5	0000h	R/W; RO
Software SMI	SWSMI	E0	E1	0000h	R/WO; R/WC
System Display Event Register	ASLE	E4	E7		R/W;
Reserved		E8	FB		
Graphics Clock Frequency Control	GCFC	F0	F1	0000h	R/W; RO;
ASL Storage	ASLS	FC	FF	00000000h	R/W

NOTES:
1. Valid for all Mobile Intel 945 Express Chipsets except for the Mobile Intel 945GME/GSE Express Chipset.
2. Valid for the Mobile Intel 945GME/GSE Express Chipset only.



8.1.1 VID2 - Vendor Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 0-1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

8.1.2 DID2 - Device Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2-3h
Default Value: 27A2h[1]
27AEh[2]
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	27A2h[1] 27AEh[2]	**Device Identification Number (DID):** Identifier assigned to the (G)MCH core/primary PCI device.

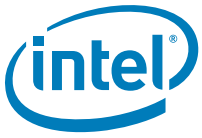
NOTES:
1. Valid for all Mobile Intel 945 Express Chipsets except for the Mobile Intel 945GME/GSE Express Chipset.
2. Valid for the Mobile Intel 945GME/GSE Express Chipset only.

8.1.3 PCICMD2 - PCI Command

B/D/F/Type: 0/2/0/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD register in the IGD disables the IGD PCI-compliant master accesses to main memory.

Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10	R/W	0b	**Interrupt Disable:** This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	RO	0b	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO	0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO	0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO	0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W	0b	**Bus Master Enable (BME):** 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI-compliant master.
1	R/W	0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0: Disable 1: Enable
0	R/W	0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0: Disable 1: Enable



8.1.4 PCISTS2 - PCI Status

B/D/F/Type: 0/2/0/PCI
Address Offset: 6-7h
Default Value: 0090h
Access: R/WC; RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI-compliant master abort and PCI-compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO	0b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO	0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO	0b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO	0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to 00.
8	RO	0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO	1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO	0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO	0b	**66-MHz PCI Capable (66C):** N/A - Hardwired to 0.

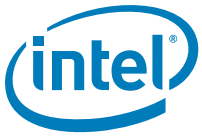
Bit	Access	Default Value	Description
4	RO	1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	R/WC	0b	**Interrupt Status:** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit is set by Hardware and Software must write a 1 to clear it.
2:0	RO	000b	**Reserved**

8.1.5 RID2 - Revision Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number for Device 2 Functions 0 and 1

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH.



8.1.6 CC - Class Code

B/D/F/Type: 0/2/0/PCI
Address Offset: 9-Bh
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	Description
23:16	RO	03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. This code has the value 03h, indicating a Display Controller.
15:8	RO	00h	**Sub-Class Code (SUBCC):** Based on Device 0 GGC-GMS bits and GGC-IVD bits. 00h:VGA compatible 80h:Non VGA (GMS = “000” or IVD = “1”)
7:0	RO	00h	**Programming Interface (PI):** 00h:Hardwired as a Display controller.

8.1.7 CLS - Cache Line Size

B/D/F/Type: 0/2/0/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access	Default Value	Description
7:0	RO	00h	**Cache Line Size (CLS):** This field is hardwired to 0’s. The IGD as a PCI-compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

8.1.8 MLT2 - Master Latency Timer

B/D/F/Type: 0/2/0/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

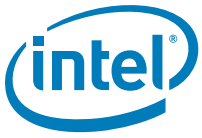
Bit	Access	Default Value	Description
7:0	RO	00h	**Master Latency Timer Count Value:** Hardwired to 0's.

8.1.9 HDR2 - Header Type

B/D/F/Type: 0/2/0/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	Description
7:7	RO	1b	**Multi Function Status (MFunc):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the MFunc bit is also set.
6:0	RO	00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.



8.1.10 MMADR - Memory Mapped Range Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 10-13h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Access	Default Value	Description
31:19	R/W	0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:19].
18:4	RO	0000h	**Address Mask:** Hardwired to 0's to indicate 512-KB address range.
3	RO	0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO	00b	**Memory Type:** Hardwired to 0's to indicate 32-bit address.
0	RO	0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

8.1.11 IOBAR - I/O Base Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 14-17h
Default Value: 00000001h
Access: R/W; RO
Size: 32 bits

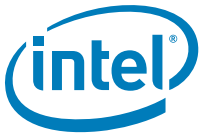
This register provides the Base offset of the I/O registers within Device 2. Bits [15:3] are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits [2:1] are fixed and return 0; bit 0 is hardwired to a 1 indicating that 8 bytes of I/O space are decoded.

Access to the 8 bytes of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device 2 is turned off or if internal graphics is disabled.

Note: Access to this IO BAR is independent of VGA functionality within Device 2. This mechanism is available only through Function 0 of Device 2 and is not duplicated in Function 1.

If an access to this IO bar is allowed, then the (G)MCH claims all 8-, 16- or 32-bit IO cycles from the CPU that falls within the 8B claimed.

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:3	R/W	0000h	**IO Base Address:** Set by the OS, these bits correspond to address signals [15:3].
2:1	RO	00b	**Memory Type:** Hardwired to 0's to indicate 32-bit address.
0	RO	1b	**Memory / IO Space:** Hardwired to 1 to indicate IO space.



8.1.12 GMADR - Graphics Memory Range Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 18-1Bh
Default Value: 00000008h
Access: R/W; ROR/W/L;
Size: 32 bits

IGD graphics memory base address is specified in this register.

Bit	Access	Default Value	Description
31:28	R/W	000b	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:28].
27:4	RO	000000h	**Address Mask:** Hardwired to 0's to indicate at least 256-MB address range
3	RO	1b	**Prefetchable Memory:** Hardwired to 1 to enable prefetching
2:1	RO	00b	**Memory Type:** Hardwired to 0 to indicate 32-bit address.
0	RO	0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

8.1.13 GTTADR - Graphics Translation Table Range Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 1C-1Fh
Default Value: 00000000h
Access: R/W; R/W/L; RO
Size: 32 bits

This register requests allocation for Graphics Translation Table Range. The allocation is for 256 KB and the base address is defined by bits [31:18].

Bit	Access	Default Value	Description
31:18	R/W	0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:18].
17:4	RO	0000h	**Address Mask:** Hardwired to 0's to indicate at least 256-KB address range.
3	RO	0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO	00b	**Memory Type:** Hardwired to 0's to indicate 32-bit address.
0	RO	0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

8.1.14 SVID2 - Subsystem Vendor Identification

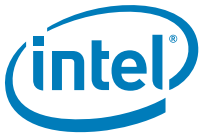
B/D/F/Type: 0/2/0/PCI
Address Offset: 2C-2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/WO	0000h	**Subsystem Vendor ID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read-Only. This register can only be cleared by a Reset.

8.1.15 SID2 - Subsystem Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2E-2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/WO	0000h	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read-Only. This register can only be cleared by a Reset.



8.1.16 ROMADR - Video BIOS ROM Base Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 30-33h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Access	Default Value	Description
31:18	RO	0000h	**ROM Base Address:** Hardwired to 0's.
17:11	RO	00h	**Address Mask:** Hardwired to 0's to indicate 256-KB address range.
10:1	RO	000h	**Reserved:** Hardwired to 0's.
0	RO	0b	**ROM BIOS Enable:** 0 = ROM not accessible.

8.1.17 CAPPTR - Capabilities Pointer

B/D/F/Type: 0/2/0/PCI
Address Offset: 34h
Default Value: 90h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	90h	**Capabilities Pointer Value:** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List which is the MSI Capabilities ID register at address 90h or the Power Management Capabilities ID registers at address D0h. The value is determined by CAPL[0]

8.1.18 INTRLINE - Interrupt Line

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access	Default Value	Description
7:0	R/W	00h	**Interrupt Connection:** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to.

8.1.19 INTRPIN - Interrupt Pin

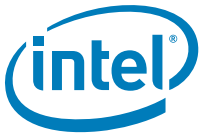
B/D/F/Type: 0/2/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	01h	**Interrupt Pin:** As a single function device, the IGD specifies INTA# as its interrupt pin. 01h:INTA#.

8.1.20 MINGNT - Minimum Grant

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Minimum Grant Value:** The IGD does not burst as a PCI-compliant master.



8.1.21 MAXLAT - Maximum Latency

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Maximum Latency Value:** The IGD has no specific requirements for how often it needs to access the PCI bus.

8.1.22 MCAPPTR - Mirror of Dev0 Capability Pointer

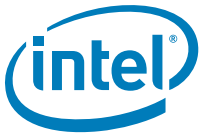
B/D/F/Type: 0/2/0/PCI
Address Offset: 44h
Default Value: 48h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	48h	**Capabilities Pointer Value:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

8.1.23 MGGC - Mirror of Dev0 (G)MCH Graphics Control

B/D/F/Type: 0/2/0/PCI
Address Offset: 52-53h
Default Value: 0030h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:7	RO	000h	**Reserved**
6:4	RO	011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Stolen Memory Bases is located between (TOLUD - SMSize) to TOUD. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0. Class Code register is 80. 001 = DVMT (UMA) mode, 1MB of memory pre-allocated for frame buffer. 011 = DVMT (UMA) mode, 8MB of memory pre-allocated for frame buffer. All Others = Reserved ***Note:***This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.
3:2	RO	00b	**Reserved:**
1	RO	0b	**IGD VGA Disable (IVD):** 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80. 0: Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.
0	RO	0b	**Reserved**



8.1.24 MDEVENdev0F0 - Mirror of Dev0 DEVEN

B/D/F/Type: 0/2/0/PCI
Address Offset: 54-57h
Default Value: 0000001Bh
Access: RO
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the MCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access	Default Value	Description
31:8	RO	000000h	**Reserved**
7	RO	0b	**Reserved**
6:5	RO	00b	**Reserved**
4	RO	1b	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden 1: Bus 0 Device 2 Function 1 is enabled and visible If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit.
3	RO	1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden 1: Bus 0 Device 2 Function 0 is enabled and visible
2	RO	0b	**Reserved**
1	RO	1b	**PCI Express* Graphics Port Enable (D1EN):** 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by the device capabilities, SDVO presence HW strap and SDVO/PCIe concurrent HW strap. Device 1 is disabled on Reset if the SDVO present strap is sampled high and the SDVO/PCIe concurrent strap is sampled low.
0	RO	1b	**Host Bridge:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

8.1.25 BSM - Base of Stolen Memory

B/D/F/Type: 0/2/0/PCI
Address Offset: 5C-5Fh
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, (G)MCH claims 1 to 64 MBs of DRAM for internal graphics if enabled.

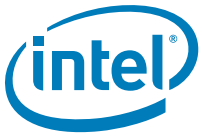
Bit	Access	Default Value	Description
31:20	RO	078h	**Base of Stolen Memory (BSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. The host interface determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanations.
19:0	RO	00000h	**Reserved**

8.1.26 MSAC - Multi Size Aperture Control

B/D/F/Type: 0/2/0/PCI
Address Offset: 62h
Default Value: 10h
Access: R/W; RO
Size: 8 bits

This register determines the size of the graphics memory aperture in Function 0 and in the un-trusted space. By default, the aperture size is 256 MB. Only the system BIOS will write this register based on pre-boot address allocation efforts, but the graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.

Bit	Access	Default Value	Description
7:4	R/W	0h	**Scratch Bits Only**
3:2	RO	00b	**Reserved**
1:0	R/W	10b	**Untrusted Aperture Size (LHSAS):** 00: Reserved 01: Reserved 10: 256 MB. Bit 28 is read-write and bit 27 of GMADR is read-only limiting the address space to 256 MB. The untrusted GTT is 256 KB. 11: Reserved



8.1.27 CAPL - Capabilities List Control

B/D/F/Type: 0/2/0/PCI
Address Offset: 7Fh
Default Value: 00h
Access: R/W; RO
Size: 8 bits

This register allows BIOS to hide capabilities that are part of the Device 2 PCI Capabilities Linked List. By setting the appropriate bits, certain capabilities will be "skipped" during a later phase of system initialization.

Bit	Access	Default Value	Description
7:1	RO	00h	**Reserved**
0	R/W	0b	**MSI Capability Hidden (MSICH):** 0: MSI Capability at 90h is included in list. 1: MSI Capability is **not** included in list. Power Management Capability ID's (D0h) pointer is the next capability.

8.1.28 GDRST - Graphics Debug Reset

B/D/F/Type: 0/2/0/PCI
Address Offset: C0h
Default Value: 00h
Access: R/W; RO
Size: 8 bits

Bit	Access	Default Value	Description
7:2	RO	00h	**Reserved**
1	RO	0b	**Graphics Reset Status:** 0: Graphics subsystem not in Reset. 1: Graphics Subsystem in Reset as a result of Graphics Debug Reset. This bit gets is set to a 1 when Graphics debug reset bit is set to a 1 and the Graphics hardware has completed the debug reset sequence and all Graphics assets are in reset. This bit is cleared when Graphics Debug Reset bit is set to a 0.

Bit	Access	Default Value	Description
0	R/W	0b	**Graphics Debug Reset:** 1 = Assert display and render domain reset 0 = Deassert display and render domain reset Render and Display clock domain resets should be asserted for at least 20 µs. Once this bit is set to a 1 all GFX core MMIO registers are returned to power on default state. All Ring buffer pointers are reset, command stream fetches are dropped and ongoing render pipeline processing is halted, state machines and State Variables returned to power on default state, Display and overlay engines are halted (garbage on screen). VGA memory is not available, Store dwords, interrupts are not guaranteed to be completed. Device 2 IO registers are not available. Device 2 configuration registers are available when Graphics debug reset is asserted.

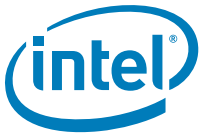
8.1.29 Unit Power Management Control4- UPMC4

B/D/F/Type: 0/2/0/PCI
Address Offset: C1-C2h
Default Value: 0000h
Access: RO; R/W;
Size: 16 bits

8.1.30 PMCAPID - Power Management Capabilities ID

B/D/F/Type: 0/2/0/PCI
Address Offset: D0-D1h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**NEXT_PTR:** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO	01h	**CAP_ID:** SIG defines this ID is 01h for power management.



8.1.31 PMCAP - Power Management Capabilities

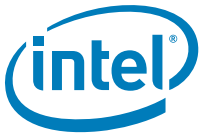
B/D/F/Type: 0/2/0/PCI
Address Offset: D2-D3h
Default Value: 0022h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	**PME Support:** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO	0b	**D2:** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO	0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO	000b	**Reserved**
5	RO	1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO	0b	**Auxiliary Power Source:** Hardwired to 0.
3	RO	0b	**PME Clock:** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO	010b	**Version:** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with the current *PCI Power Management Interface Specification*.

8.1.32 PMCS - Power Management Control/Status

B/D/F/Type: 0/2/0/PCI
Address Offset: D4-D5h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO	00b	**Reserved**
12:9	RO	0h	**Reserved**
8	RO	0b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO	00h	**Reserved**
1:0	R/W	00b	**PowerState:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the graphics controller specification. Bits[1:0]Power state 00 D0Default 01 D1Not Supported 10 D2Not Supported 11 D3



8.1.33 SWSMI - Software SMI

B/D/F/Type: 0/2/0/PCI
Address Offset: E0-E1h
Default Value: 0000h
Access: R/WO; R/WC
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2F0address E0h-E1h must be reserved for this register.

Bit	Access	Default Value	Description
15:8	R/WO	00h	**SW Scratch Bits**
7:1	R/W	00h	**Software Flag:** Used to indicate caller and SMI function desired, as well as return result
0	R/WC	0b	**(G)MCH Software SMI Event:** When Set this bit will trigger an SMI. Software must write a 0 to clear this bit

8.1.34 ASLE - System Display Event Register

B/D/F/Type: 0/2/0/PCI
Address Offset: E4-E7h
Default Value:
Access: R/W
Size: 32 bits

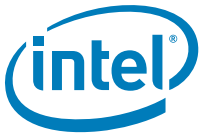
The exact use of these bytes including whether they are addressed as bytes, words, or as a dword, is not pre-determined but subject to change by driver and System BIOS teams (acting in unison).

Bit	Access	Default Value	Description
31:24	R/W	N/A	**ASLE Scratch Trigger3:** When written, this scratch byte triggers an interrupt when IEF bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	R/W	N/A	**ASLE Scratch Trigger2:** When written, this scratch byte triggers an interrupt when IEF bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	R/W	N/A	**ASLE Scratch Trigger 1:** When written, this scratch byte triggers an interrupt when IEF bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	R/W	N/A	**ASLE Scratch Trigger 0:** When written, this scratch byte triggers an interrupt when IEF bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

8.1.35 GCFC - Graphics Clock Frequency Control

B/D/F/Type: 0/2/0/PCI
Address Offset: F0-F1h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

Note: The values indicated in this register are applicable only for the Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset. This register is a “Don’t Care” for the Mobile Intel 945PM Express Chipset.



Bit	Access	Default Value	Description
15:14	R/W	0b	**Reserved**
14	R/W	0b	**Reserved**
13	R/W	0b	**Reserved**
12	R/W	0b	**Reserved**
11	R/W	0b	**Core Render Clock Disable:** 0: crclk enabled 1: crclk disabled
10	R/W	0b	**Reserved**
9	R/W	0b	**Core Display Clock Disable:** 0:cdclk is running 1:cdclk is gated
8	R/W	0b	**Reserved**
7	R/W	0b	**Core Display Low Frequency Enable:** 0 = Do not use low frequency target (>=133 MHz) for Display Clock. 1 = Use low frequency target (>=133 MHz) for Display Clock (Mobile Intel® 943/940GML/945GU Express Chipset). ***Note:*** For Ultra Mobile Intel 945GU Express Chipset, this bit must be set to 1.
6:4	R/W	000b	**Graphics Core Display Clock Select:** Software programs this register; however updates are controlled by Render core clock capability settings for each variant. 000 => 200 MHz (Mobile Intel® 945GM/GME/GMS/GU/GSE & 943/940GML Express Chipset) 100 => 320 MHz (Intel® 945GT Express Chipset) Others: Reserved
3	RO	0b	**Reserved**
2:0	R/W	000b	**Graphics Core Render Clock Select:** Software programs this register; however updates are controlled by Render core clock capability settings for each variant. 000 => 166 MHz (Mobile Intel 945GMS/GU/GSE & 943/940GML Express Chipset) 001 => 200 MHz (Mobile Intel 943GML Express Chipset) 011 => 250 MHz (Mobile Intel 945GM/GME Express Chipset) 101 => 400 MHz (Intel 945GT Express Chipset) Others = Reserved

8.1.36 ASLS - ASL Storage

B/D/F/Type: 0/2/0/PCI
Address Offset: FC-FFh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This SW scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access	Default Value	Description
31:0	R/W	00000000h	RW according to a software controlled usage to support device switching

8.2 Device 2 Function 1 PCI Configuration Registers

Table 13. Device 2 Function 1 PCI Configuration Registers Summary Table (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	0	1	8086h	RO
Device Identification	DID2	2	3	27A6h	RO
PCI Command	PCICMD2	4	5	0000h	R/W; RO
PCI Status	PCISTS2	6	7	0090h	RO
Revision Identification	RID2	8	8	00h	RO
Class Code Register	CC	9	B	038000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT2	D	D	00h	RO
Header Type	HDR2	E	E	80h	RO
Reserved		F	F		
Memory Mapped Range Address	MMADR	10	13	00000000h	R/W; RO
Subsystem Vendor Identification	SVID2	2C	2D	0000h	RO
Subsystem Identification	SID2	2E	2F	0000h	RO
Video BIOS ROM Base Address	ROMADR	30	33	00000000h	RO
Capabilities Pointer	CAPPOINT	34	34	D0h	RO
Minimum Grant	MINGNT	3E	3E	00h	RO

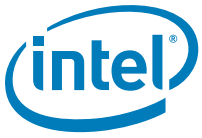


Table 13. Device 2 Function 1 PCI Configuration Registers Summary Table (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Maximum Latency	MAXLAT	3F	3F	00h	RO
Mirror of Dev0 Capability Pointer	MCAPPTR	44	44	48h	RO
Reserved		48	50		
Mirror of Dev0 (G)MCH Graphics Control	MGGC	52	53	0030h	RO
Mirror of Dev0 DEVEN	MDEVENdev0F0	54	57	0000001Bh	RO
Reserved		58	5B		
Base of Stolen Memory	BSM	5C	5F	07800000h	RO
Reserved		60	C2		
Power Management Capabilities ID	PMCAPID	D0	D1	0001h	RO
Power Management Capabilities	PMCAP	D2	D3	0022h	RO
Power Management Control/Status	PMCS	D4	D5	0000h	R/W; RO
Software SMI	SWSMI	E0	E1	0000h	R/WO; R/WC
Reserved		E2	F3		
Legacy Backlight Brightness	LBB	F4	F7	00000000h	R/W
Reserved		F8	FB		
ASL Storage	ASLS	FC	FF	00000000h	R/W

8.2.1 VID2 - Vendor Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 0-1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

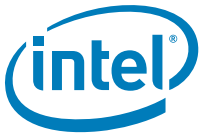
Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

8.2.2 DID2 - Device Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2-3h
Default Value: 27A6h
Access: RO
Size: 16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID is necessary for allowing distinct Plug and Play enumeration of Function 1 when both Function 0 and Function 1 have the same class code.

Bit	Access	Default Value	Description
15:0	RO	27A6h	**Device Identification Number (DID):** This is a 16-bit value assigned to the (G)MCH Graphic device Function 1.



8.2.3 PCICMD2 - PCI Command

B/D/F/Type: 0/2/1/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD register in the IGD disables the IGD PCI-compliant master accesses to main memory.

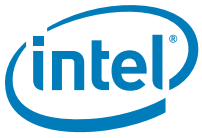
Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10:10	RO	0b	**Reserved**
9	RO	0b	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO	0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO	0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO	0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	**VGA Palette Snoop Enable (VGASNOOP):** This bit is hardwired to 0 to disable snooping.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W	0b	**Bus Master Enable (BME):** Set to 1 to enable the IGD to function as a PCI-compliant master. Set to 0 to disable IGD bus mastering.
1	R/W	0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0: Disable 1: Enable
0	R/W	0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0: Disable 1: Enable

8.2.4 PCISTS2 - PCI Status

B/D/F/Type: 0/2/1/PCI
Address Offset: 6-7h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI-compliant master abort and PCI-compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO	0b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO	0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO	0b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO	0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	**DEVSEL Timing (DEVT):** Not applicable. These bits are hardwired to 00.
8	RO	0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO	1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO	0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO	0b	**66-MHz PCI Capable (66C):** Not applicable. Hardwired to 0.
4	RO	1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO	0b	**Interrupt Status:** Hardwired to 0.
2:0	RO	0h	**Reserved**



8.2.5 RID2 - Revision Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number for Device 2 Functions 0 and 1.

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. For the A-0 Stepping, this value is 00h.

8.2.6 CC - Class Code Register

B/D/F/Type: 0/2/1/PCI
Address Offset: 9-Bh
Default Value: 038000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	Description
23:16	RO	03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. This code has the value 03h, indicating a Display Controller.
15:8	RO	80h	**Sub-Class Code (SUBCC):** 80h:Non VGA
7:0	RO	00h	**Programming Interface (PI):** 00h:Hardwired as a Display controller.

8.2.7 CLS - Cache Line Size

B/D/F/Type: 0/2/1/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

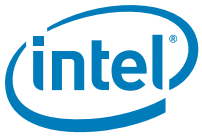
Bit	Access	Default Value	Description
7:0	RO	00h	**Cache Line Size (CLS):** This field is hardwired to 0's. The IGD as a PCI-compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

8.2.8 MLT2 - Master Latency Timer

B/D/F/Type: 0/2/1/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access	Default Value	Description
7:0	RO	00h	**Master Latency Timer Count Value:** Hardwired to 0's.



8.2.9 HDR2 - Header Type

B/D/F/Type: 0/2/1/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	Description
7	RO	1b	**Multi Function Status (MFunc):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the MFunc bit is also set.
6:0	RO	00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

8.2.10 MMADR - Memory Mapped Range Address

B/D/F/Type: 0/2/1/PCI
Address Offset: 10-13h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Access	Default Value	Description
31:19	R/W	0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:19].
18:4	RO	0000h	**Address Mask:** Hardwired to 0's to indicate 512-KB address range.
3	RO	0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO	00b	**Memory Type:** Hardwired to 0's to indicate 32-bit address.
0	RO	0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

8.2.11 SVID2 - Subsystem Vendor Identification

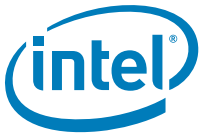
B/D/F/Type: 0/2/1/PCI
Address Offset: 2C-2Dh
Default Value: 0000h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	0000h	**Subsystem Vendor ID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

8.2.12 SID2 - Subsystem Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2E-2Fh
Default Value: 0000h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	0000h	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.



8.2.13 ROMADR - Video BIOS ROM Base Address

B/D/F/Type: 0/2/1/PCI
Address Offset: 30-33h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Access	Default Value	Description
31:18	RO	0000h	**ROM Base Address:** Hardwired to 0.
17:11	RO	00h	**Address Mask:** Hardwired to 0's to indicate 256-KB address range.
10:1	RO	000h	**Reserve**
0:0	RO	0b	**ROM BIOS Enable:** 0 = ROM not accessible.

8.2.14 CAPPOINT - Capabilities Pointer

B/D/F/Type: 0/2/1/PCI
Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	D0h	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List which is the Power Management Capabilities ID registers at address D0h.

8.2.15 MINGNT - Minimum Grant

B/D/F/Type: 0/2/1/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Minimum Grant Value:** The IGD does not burst as a PCI-compliant master.

8.2.16 MAXLAT - Maximum Latency

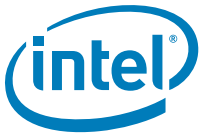
B/D/F/Type: 0/2/1/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Maximum Latency Value:** The IGD has no specific requirements for how often it needs to access the PCI bus.

8.2.17 MCAPPTR - Mirror of Dev0 Capability Pointer

B/D/F/Type: 0/2/1/PCI
Address Offset: 44h
Default Value: 48h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	48h	**Capabilities Pointer Value:** In this case the first capability is the product-specific Capability Identifier (CAPID0).



8.2.18 MGGC - Mirror of Dev0 (G)MCH Graphics Control

B/D/F/Type: 0/2/1/PCI
Address Offset: 52-53h
Default Value: 0030h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:7	RO	0000000 00b	**Reserved**
6:4	RO	011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Stolen Memory Bases is located between (TOLUD - SMSize) to TOUD. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (memory and IO), and the Sub-Class Code field within Device 2 Function 0. Class Code register is 80. 001 = DVMT (UMA) mode, 1MB of memory pre-allocated for frame buffer. 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.
3:2	RO	00b	**Reserved**
1	RO	0b	**IGD VGA Disable (IVD):** 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80. 0: Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.
0	RO	0b	**Reserved**

8.2.19 MDEVENdev0F0 - Mirror of Dev0 DEVEN

B/D/F/Type: 0/2/1/PCI
Address Offset: 54-57h
Default Value: 0000001Bh
Access: RO
Size: 32 bits

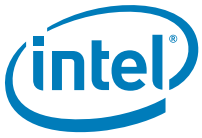
This register allows for enabling/disabling of PCI devices and functions that are within the MCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access	Default Value	Description
31:7	RO	0000000h	**Reserved**
4	RO	1b	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden. 1: Bus 0 Device 2 Function 1 is enabled and visible.
3	RO	1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden. 1: Bus 0 Device 2 Function 0 is enabled and visible.
2	RO	0b	**Reserved**
1	RO	1b	**PCI Express Graphics Port Enable (D1EN):** 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by the device capabilities, SDVO presence HW strap and SDVO/PCIe concurrent HW strap. Device 1 is Disabled on Reset if {the SDVO present strap is sampled high and the SDVO/PCIe concurrent strap is sampled low}.
0	RO	1b	**Host Bridge:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

8.2.20 SSRW - Software Scratch Read Write

B/D/F/Type: 0/2/1/PCI
Address Offset: 58-5Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:0	RO	00000000h	**Reserved**



8.2.21 BSM - Base of Stolen Memory

B/D/F/Type: 0/2/1/PCI
Address Offset: 5C-5Fh
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, (G)MCH claims 1 to 64 MBs of DRAM for internal graphics if enabled.

Bit	Access	Default Value	Description
31:20	RO	078h	**Base of Stolen Memory (BSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. The host interface determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanations.
19:0	RO	00000h	**Reserved**

8.2.22 PMCAPID - Power Management Capabilities ID

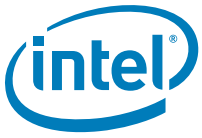
B/D/F/Type: 0/2/1/PCI
Address Offset: D0-D1h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**NEXT_PTR:** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO	01h	**CAP_ID:** SIG defines this ID is 01h for power management.

8.2.23 PMCAP - Power Management Capabilities

B/D/F/Type: 0/2/1/PCI
Address Offset: D2-D3h
Default Value: 0022h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	**PME Support:** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO	0b	**D2:** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO	0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO	000b	**Reserved**
5	RO	1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO	0b	**Auxiliary Power Source:** Hardwired to 0.
3	RO	0b	**PME Clock:** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO	010b	**Version:** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with the current *PCI Power Management Interface Specification.*



8.2.24 PMCS - Power Management Control/Status

B/D/F/Type: 0/2/1/PCI
Address Offset: D4-D5h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

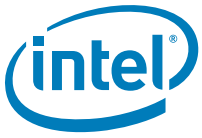
Bit	Access	Default Value	Description
15	RO	0b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9	RO	00h	**Reserved**
8	RO	0b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO	00h	**Reserved**
1:0	R/W	00b	**PowerState:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. **Bits[1:0] Power state** 00 D0 Default 01 D1 Not Supported 10 D2 Not Supported 11 D3

8.2.25 SWSMI - Software SMI

B/D/F/Type: 0/2/1/PCI
Address Offset: E0-E1h
Default Value: 0000h
Access: R/WO; R/WC
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2 Function 0 address E0h-E1h must be reserved for this register.

Bit	Access	Default Value	Description
15:8	R/WO	00h	**SW Scratch Bits:**
7:1	R/W	00h	**Software Flag:** Used to indicate caller and SMI function desired, as well as return result
0	R/WC	0b	**(G)MCH Software SMI Event:** When Set this bit will trigger an SMI. Software must write a 0 to clear this bit



8.2.26 LBB - Legacy Backlight Brightness

B/D/F/Type: 0/2/1/PCI
Address Offset: F4-F7h
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register can be accessed by byte, word, or dword PCI configuration cycles. A write to this register will cause the Backlight Event (Display B Interrupt) if enabled.

Bit	Access	Default Value	Description
31:24	R/W	N/A	**LBPC Scratch Trigger3:** When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR, etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	R/W	N/A	**LBPC Scratch Trigger2:** When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	R/W	N/A	**LBPC Scratch Trigger1:** When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	R/W	N/A	**Legacy Backlight Brightness (LBES):** The value of 0 is the lowest brightness setting and 255 is the brightest. A write to this register will cause a flag to be set (LBES) in the PIPEBSTATUS register and cause an interrupt if Backlight event in the PIPEBSTATUS register and cause an Interrupt if Backlight Event (LBEE) and Display B Event is enabled by software.

8.2.27 ASLS - ASL Storage

B/D/F/Type: 0/2/1/PCI
Address Offset: FC-FFh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access	Default Value	Description
31:0	R/W	00000000h	R/W according to a software controlled usage to support device switching

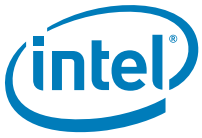
8.3 Device 2 – PCI I/O Registers

The following are not PCI configuration registers; they are I/O registers. This mechanism allows access to internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

8.4 Device 2 I/O Configuration Registers

Table 14. MMIO Configuration Registers Summary Table

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
MMIO Address Register	Index	IOBAR + 0	IOBAR + 3	00000000h	R/W
MMIO Data Register	Data	IOBAR + 4	IOBAR + 7	00000000h	R/W



8.4.1 Index - MMIO Address Register

B/D/F/Type: 0/2/0/PCI IO
Address Offset: IOBAR + 0h
Default Value: 00000000h
Access: R/W
Size: 32 bits

MMIO_INDEX: A 32-bit IO write to this port loads the offset of the MMIO register that needs to be accessed. An IO Read returns the current value of this register. An 8-/16-bit IO write to this register is completed by the (G)MCH but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

Bit	Access	Default Value	Description
31:2	R/W	00000000h	**Reserved**
1:0	R/W	00b	**Target:** 00:MMIO Registers Others:Reserved

8.4.2 Data - MMIO Data Register

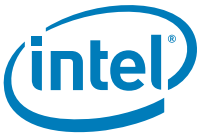
B/D/F/Type: 0/2/0/PCI IO
Address Offset: IOBAR + 4h
Default Value: 00000000h
Access: R/W
Size: 32 bits

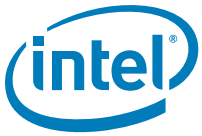
MMIO_DATA: A 32-bit IO write to this port is re-directed to the MMIO register/GTT location pointed to by the MMIO-index register. A 32-bit IO read to this port is re-directed to the MMIO register address pointed to by the MMIO-index register regardless of the target selection in MMIO_INDEX(1:0). 8- or 16-bit IO writes are completed by the (G)MCH and may have un-intended side effects, hence must not be used to access the data port. 8- or 16-bit IO reads are completed normally.

Note: If the target field in MMIO Index selects “GTT”, Reads to MMIO data return 0’s and not the value programmed in the GTT memory corresponding to the offset programmed in MMIO index.

Bit	Access	Default Value	Description
31:0	R/W	00000000h	**MMIO Data Window**

§





9 System Address Map

The Mobile Intel 945GM/GME/PM and Intel 945GT Express Chipsets support up to 4 GB of addressable memory space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1-MB region which is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. Attribute programming is described in Chapter 5. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained in Section 9.9.

Addressing of memory ranges larger than 4 GB is **not** supported. The HREQ [4:3] FSB pins are decoded to determine whether the access is above or below 4 GB.

Note: The Mobile Intel 945GM/GME/PM and Intel 945GT Express Chipsets are capable of supporting up to 4 GB of physical memory. All other variants, except Ultra Mobile 945GU Express Chipset, support only up to 2 GB of physical memory. The Ultra Mobile 945GU Express Chipset supports up to 1 GB.

The (G)MCH does not support the PCI dual address cycle (DAC) mechanism, PCI Express 64-bit prefetchable memory transactions, or any other addressing mechanism that allows addressing of greater than 4 GB on either the DMI or PCI Express interface. The (G)MCH does not limit DRAM space in hardware. There is no hardware lock to stop someone from inserting more memory than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI. The exception to this rule is VGA ranges, which may be mapped to PCI Express, DMI, or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the internal graphics device respectively. The (G)MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS.

The Address Map includes a number of programmable ranges:

1. Device 0:

A. EPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4-KB window)

B. MCHBAR – Memory mapped range for internal (G)MCH registers. For example, memory buffer register controls. (16-KB window)

C. PCIEXBAR – Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0-FFFh) and Extended configuration space (100h-FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the *PCI Express* Base Specification*. (64-MB, 128-MB, or 256-MB window).

D. DMIBAR –This window is used to access registers associated within the MCH/ICH (DMI) register memory range. (4-KB window)

E. GGC – (G)MCH graphics control register. Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes. (0-MB to 64-MB options).

Device 1, Function 0:

MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.

PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.

IOBASE1/IOLIMIT1 – PCI Express port IO access window.

Device 2, Function 0:

MMADR – IGD registers and internal graphics instruction port. (512-KB window)

IOBAR – I/O access window for internal graphics. Through this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note this allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTADR table.

GMADR – Internal graphics translation window. (256-MB window)

GTTADR – Internal graphics translation table location. (256-KB window).

Device 2, Function 1:

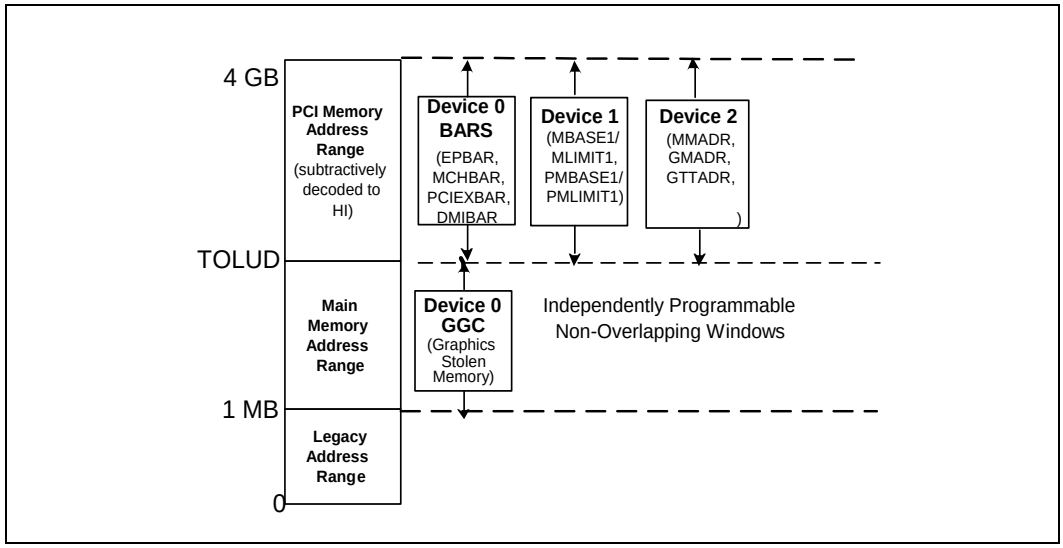
MMADR – Function 1 IGD registers and internal graphics instruction port. (512-KB window)

The rules for the above programmable ranges are:

1. ALL of these ranges MUST be unique and NON-OVERLAPPING. **It is the BIOS or system designers responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.**
2. In the case of overlapping ranges with memory, the memory decode will be given priority.
3. There are **no** Hardware Interlocks to prevent problems in the case of overlapping ranges.
4. Accesses to overlapped ranges may produce indeterminate results.
5. The only peer-to-peer cycles allowed below the top of memory (register TOLUD) are DMI to PCI Express VGA range writes. Note that peer to peer cycles to the Internal Graphics VGA range are not supported.

Figure 10 represents system memory address map in a simplified form.

Figure 10. System Address Ranges

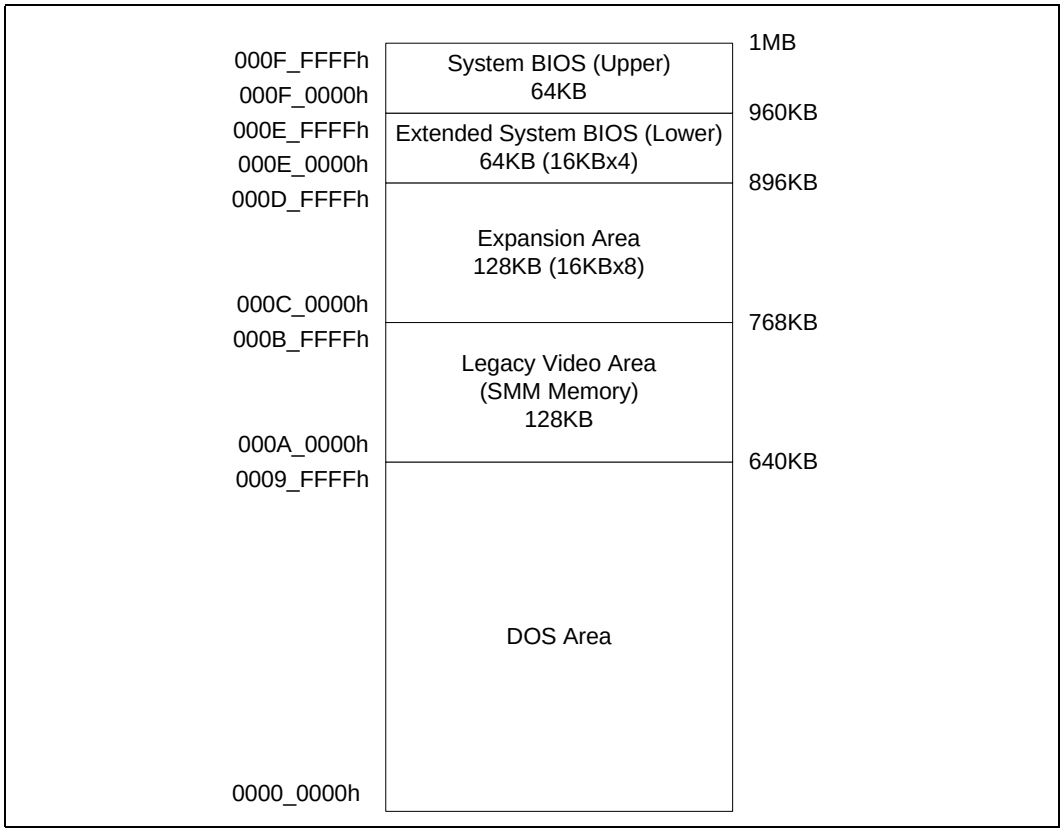


9.1 Legacy Address Range

This area is divided into the following address regions:

- 0 - 640 KB – DOS Area
- 640 - 768 KB – Legacy Video Buffer Area
- 768 - 896 KB in 16-KB sections (total of eight sections) – Expansion Area
- 896 -960 KB in 16-KB sections (total of four sections) – Extended System BIOS Area
- 960 KB - 1 MB Memory – System BIOS Area

Figure 11. DOS Legacy Address Range

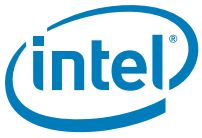


9.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the (G)MCH.

9.1.2 Legacy Video Area (A_0000h-B_FFFFh)

The legacy 128-KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The (G)MCH always decodes internally mapped devices first. Internal to the (G)MCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configuration bits (VGA Enable and MDAP). This region is also the default for SMM space.



9.1.2.1 Compatible SMRAM Address Range (A_0000h-B_FFFFh)

When compatible SMM space is enabled, SMM-mode CPU accesses to this range are routed to physical system DRAM at 000A 0000h - 000B FFFFh. Non-SMM-mode CPU accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area if IGD is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as Peer cycles, and will master abort on PCI if no external VGA device claims them.

9.1.2.2 Monochrome Adapter (MDA) Range (B_0000h-B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI (depending on configuration bits). Since the monochrome adapter may be mapped to any one of these devices, the (G)MCH must decode cycles in the MDA range (000B_0000h - 000B_7FFFh) and forward either to IGD, PCI Express, or the DMI. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the (G)MCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI Express, and/or the DMI.

9.1.3 Expansion Area (C_0000h-D_FFFFh)

This 128-KB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight, 16-KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through (G)MCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 15. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000H - 0C3FFFH	W/R	Add-on BIOS
0C4000H - 0C7FFFH	W/R	Add-on BIOS
0C8000H - 0CBFFFH	W/R	Add-on BIOS
0CC000H - 0CFFFFH	W/R	Add-on BIOS
0D0000H - 0D3FFFH	W/R	Add-on BIOS
0D4000H - 0D7FFFH	W/R	Add-on BIOS
0D8000H - 0DBFFFH	W/R	Add-on BIOS
0DC000H - 0DFFFFH	W/R	Add-on BIOS

9.1.4 Extended System BIOS Area (E_0000h-E_FFFFh)

This 64-KB area (000E_0000h – 000E_FFFFh) is divided into four, 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 16. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000H - 0E3FFFH	W/R	BIOS Extension
0E4000H - 0E7FFFH	W/R	BIOS Extension
0E8000H - 0EBFFFH	W/R	BIOS Extension
0EC000H - 0EFFFFH	W/R	BIOS Extension

9.1.5 System BIOS Area (F_0000h-F_FFFFh)

This area is a single, 64-KB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to DMI. By manipulating the Read/Write attributes, the (G)MCH can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 17. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000H - 0FFFFFH	WE RE	BIOS Area

9.1.6 Programmable Attribute Map (PAM) Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM Memory Area.

The (G)MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there normally will not be IWB cycles targeting DMI.

However, DMI becomes the default target for CPU and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RC it is possible to get IWB cycles targeting DMI. This may occur for DMI originated cycles to disabled PAM regions.

For example, say that a particular PAM region is set for “Read Disabled” and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is “Read Disabled” the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the (G)MCH to hang.

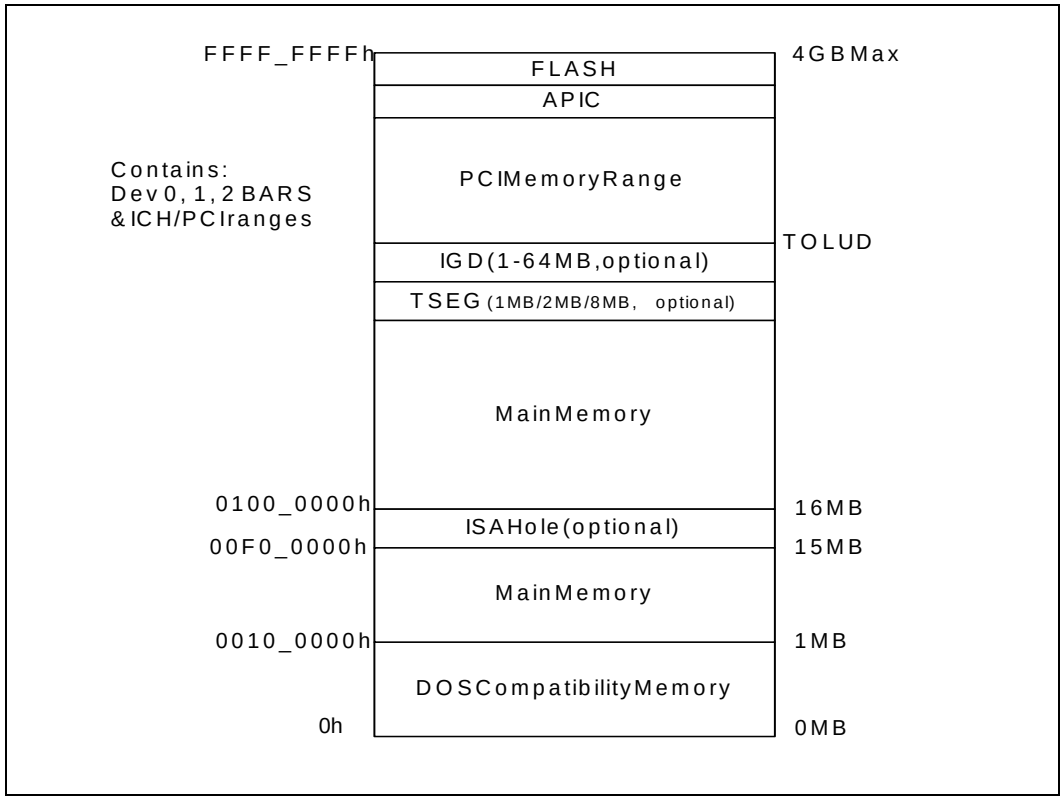
9.2 Main Memory Address Range (1 MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the (G)MCH (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the (G)MCH to the DRAM unless they fall into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

The (G)MCH provides a maximum DRAM address decode space of 4 GB. The (G)MCH does not remap APIC or PCI Express memory space. This means that as the amount of physical memory populated in the system reaches 4 GB, there will be physical memory that exists yet is non-addressable and therefore unusable by the system.

The (G)MCH does not limit DRAM address space in hardware.

Figure 12. Main Memory Address Range



9.2.1 ISA Hole (15 MB–16 MB)

A hole can be created at 15 MB–16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15 MB–16 MB hole is an optionally enabled ISA hole.

Video accelerators originally used this hole. It is also used for validation by customer teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15- to 16-MB window.

9.2.2 TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of physical memory. SMM-mode CPU accesses to enabled TSEG access the physical DRAM at the same address. Non-CPU originated accesses are not allowed to SMM space. PCI Express, DMI, and Internal Graphics originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, CPU accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses (see Table 19). Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB or 8 MB.

9.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions**. Table 18 details the location and attributes of the regions. How to enable and disable these ranges are described in the (G)MCH Control Register Device 0 (GGC).

Table 18. Pre-allocated Memory Example for 64-MB DRAM, 1-MB VGA, and 1-MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03DF_FFFFh	R/W	Available System Memory 62 MB
03E0_0000h – 03EF_FFFFh	SMM Mode Only - CPU Reads	TSEG Address Range & Pre-allocated Memory
03F0_0000h – 03FF_FFFFh	R/W	Pre-allocated Graphics VGA memory. 1 MB (or 4/8/16/32/64 MB) when IGD is enabled

9.3 PCI Memory Address Range (TOLUD – 4 GB)

This address range, from the top of physical memory to 4 GB (top of addressable memory space supported by the (G)MCH) is normally mapped to the DMI Interface.

Exceptions to this mapping include the BAR memory mapped regions, which include: EPBAR, MCHBAR, DMIBAR.

In the PCI Express port, there are two exceptions to this rule:

- Addresses decoded to the PCI Express Memory Window defined by the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers are mapped to PCI Express.
- Addresses decoded to PCI Express Configuration Space are mapped based on Bus, Device, and Function number. (PCIEXBAR range).

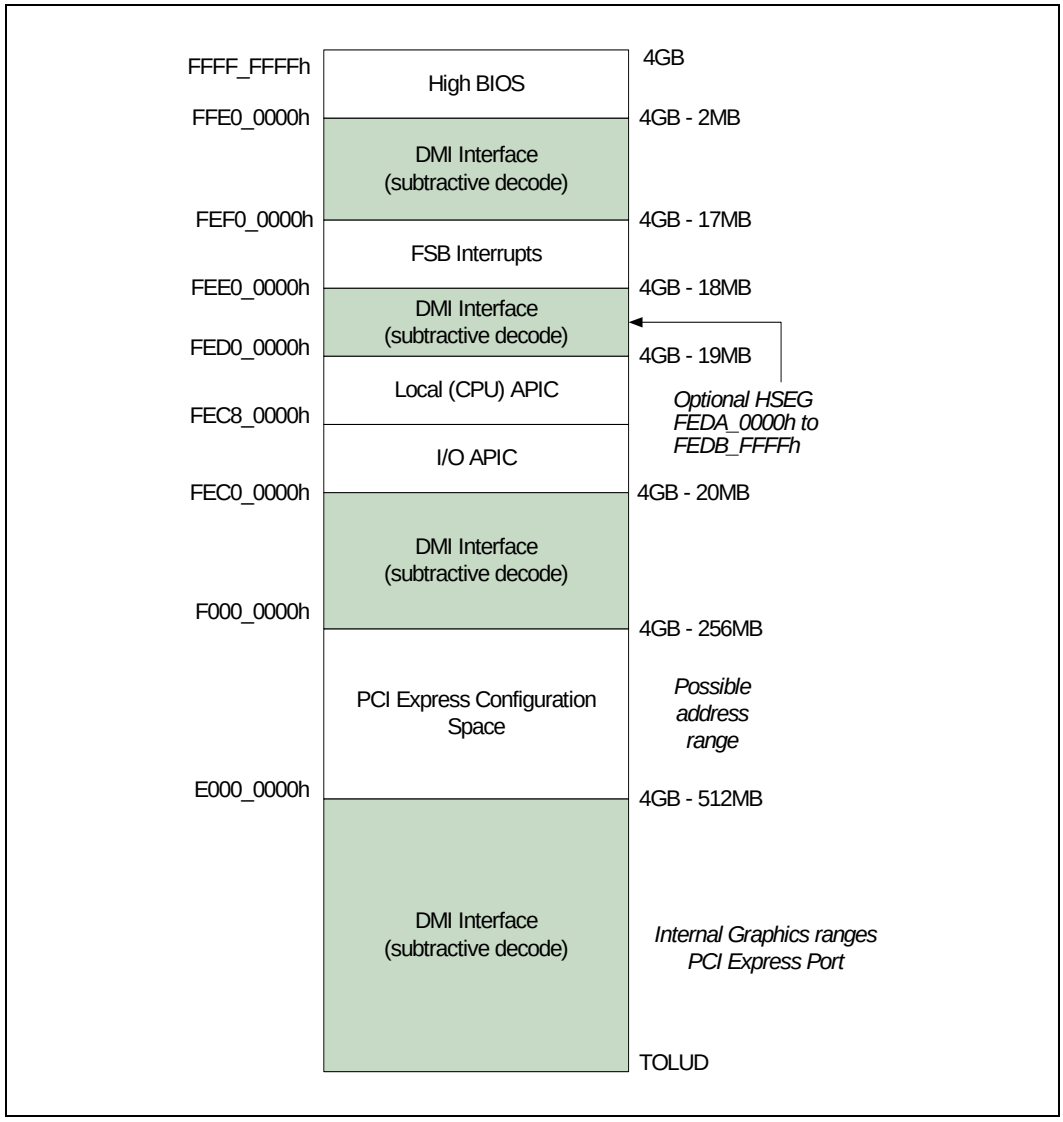
Note: AGP Aperture no longer exists with PCI Express.

In an internal graphics configuration, there are three exceptions to this rule:

1. Addresses decoded to the Graphics Memory Range. (GMADR range)
2. Addresses decoded to the Graphics Translation Table range (GTTADR range).
3. Addresses decoded to the Memory Mapped Range of the Internal Graphics Device (MMADR range). There is a MMADR range for Device 2 Function 0 and a MMADR range for Device 2 Function 1. Both ranges are forwarded to the internal graphics device.

Note: The exceptions listed above for internal graphics and the PCI Express ports **MUST NOT overlap with APCI Configuration Space, FSB Interrupt Space and High BIOS Address Range.**

Figure 13. PCI Memory Address Range



9.3.1 APIC Configuration Space (FEC0_0000h-FECF_FFFFh)

This range is reserved for APIC configuration space which includes the default I/O APIC configuration space from FEC0_0000h to FEC7_0FFFh. The default Local (CPU) APIC configuration space goes from FEC8_0000h to FECF_FFFFh.

CPU accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the CPU. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each CPU should be relocated to the FEC0_0000h (4 GB-20 MB) to FECF_FFFFh range so that one MTRR can be programmed to 64 KB for the Local and I/O APICs. The I/O APIC(s) usually reside in the ICH portion of the chip set or as a stand-alone component(s).

I/O APIC units will be located beginning at the default address FEC0_0000h. The first I/O APIC will be located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where *x* is I/O APIC unit number 0 through F(hex). This address range will normally be mapped to DMI.

Note: There is no provision to support an I/O APIC device on PCI Express.

9.3.2 HSEG (FEDA_0000h-FEDB_FFFFh)

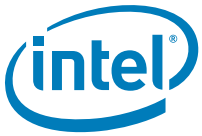
This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM memory. It is sometimes called the High SMM memory space. SMM-mode CPU accesses to the optionally enabled HSEG are remapped to 000A_0000h - 000B_FFFFh. Non-SMM mode CPU accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All Cacheline writes with WB attribute or implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

9.3.3 FSB Interrupt Memory Space (FEE0_0000-FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express, Internal Graphics, or DMI may issue a Memory Write to 0FEEx_xxxxh. The (G)MCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The (G)MCH terminates the FSB transaction by providing the response and asserting HTRDY#. This Memory Write cycle does not go to DRAM.

9.3.4 High BIOS Area

The top 2 MB (FFE0_0000h -FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset. This region is mapped to DMI so that the upper subset of this region aliases to the 16-MB–256-KB range. The actual address space required for the BIOS is less than 2 MB but the minimum CPU MTRR range for this region is 2 MB so that full 2 MB must be considered.



9.4 PCI Express Configuration Address Space

The Device 0 register (PCIEXBAR), defines the base address for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. This is a 256-MB block of addresses below top of addressable memory (currently 4 GB) and is aligned to a 256-MB boundary. BIOS must assign this address range such that it will not conflict with any other address ranges.

For more configuration information, refer to Chapter 4.

9.4.1 PCI Express Graphics Attach

The (G)MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in (G)MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base register (MBASE) and Memory Limit register (MLIMIT) registers.
- The second range is controlled via the Prefetchable Memory Base (PMBASE) and Prefetchable Memory Limit (PMLIMIT) registers.

The (G)MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

Memory_Base_Address ≤ Address ≤ Memory_Limit_Address

Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

It is essential to support a separate Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the (G)MCH Device 1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the Device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

9.4.2 AGP DRAM Graphics Aperture

Unlike AGP, PCI Express has no concept of aperture for PCI Express devices. As a result, there is no need to translate addresses from PCI Express. Therefore, the (G)MCH has no APBASE and APSIZE registers.

9.5 Graphics Memory Address Ranges

The (G)MCH can be programmed to direct memory accesses to IGD when addresses are within any of three ranges specified via registers in (G)MCH's Device 2 configuration space.

- The Memory Map Base register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base register (GTTADR) is used to access the translation table.

Normally these ranges will reside above the Top-of-Main-DRAM and below High BIOS and APIC address ranges. They normally reside above the top of memory (TOLUD) so they do not steal any physical DRAM memory space.

GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

9.5.1 Graphics Register Ranges

This section provides a high-level register map (register groupings per function) for the integrated graphics. The memory and I/O maps for the graphics registers are shown in Figure 14, except PCI Configuration registers. The VGA and Extended VGA registers can be accessed via standard VGA I/O locations as well as via memory-mapped locations. In addition, the memory map contains allocation ranges for various functions. The memory space address listed for each register is an offset from the base memory address programmed into the MMADR register (PCI configuration offset 14h). The same memory space can be accessed via dword accesses to I/OBAR. Through the IOBAR, I/O registers MMIO_index and MMIO_data are written.

VGA and Extended VGA Control Registers (00000h–00FFFh):

These registers are located in both I/O space and memory space. The VGA and Extended VGA registers contain the following register sets: General Control/Status, Sequencer (SRxx), Graphics Controller (GRxx), Attribute Controller (ARxx), VGA Color Palette, and CRT Controller (CRxx) registers.

Instruction, Memory, and Interrupt Control Registers (01000h–02FFFh):

The Instruction and Interrupt Control registers are located in main memory space and contain the types of registers listed in the following sections.

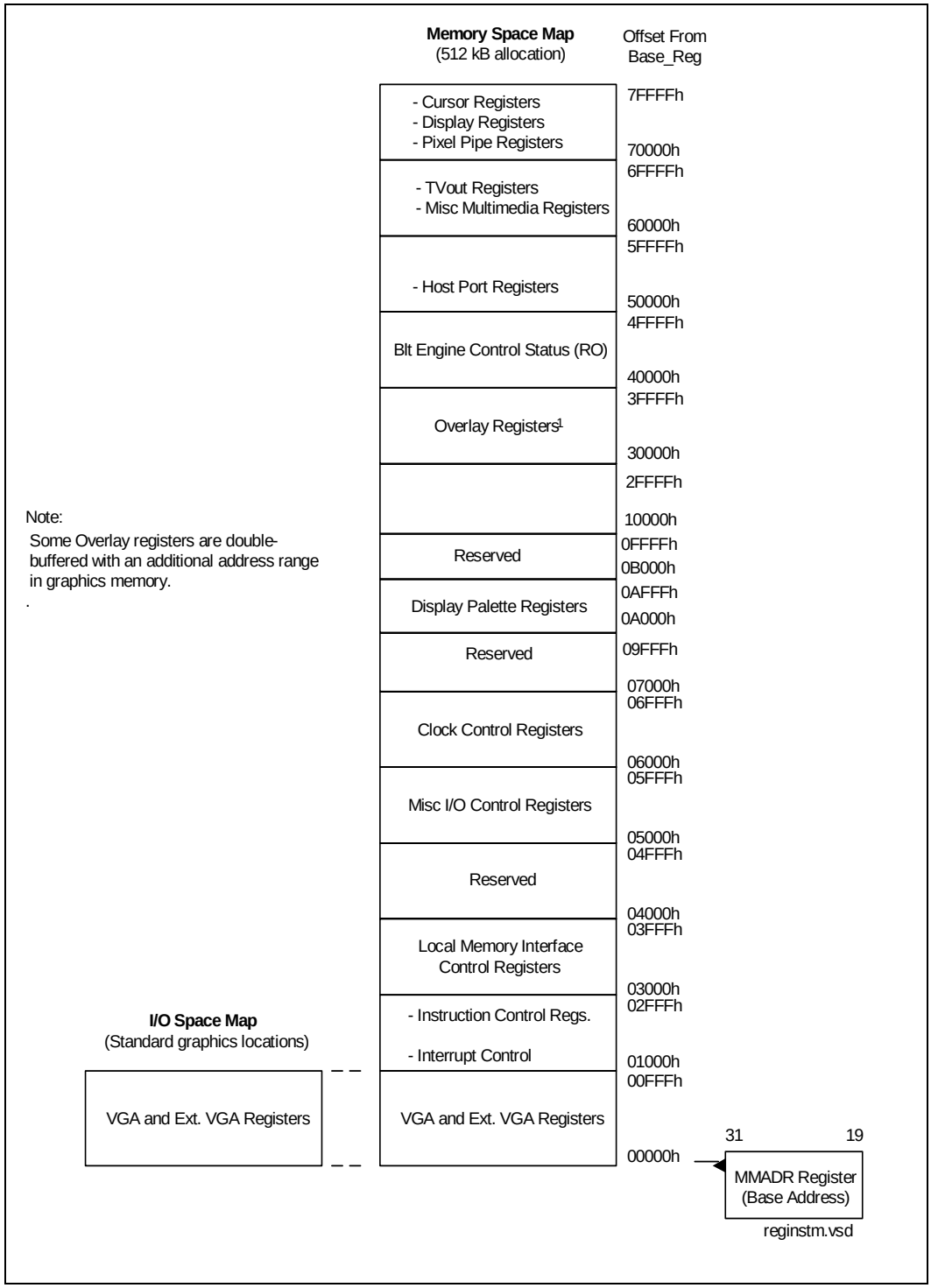
9.5.2 I/O Mapped Access to Device 2 MMIO Space

If Device 2 is enabled, and Function 0 within Device 2 is enabled, then IGD registers can be accessed using the IOBAR.

MMIO_Index: MMIO_INDEX is a 32-bit register. An I/O write to this port loads the address of the MMIO register that needs to be accessed. I/O Reads returns the current value of this register.

MMIO_Data: MMIO_DATA is a 32-bit register. An I/O write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. An I/O read to this port is re-directed to the MMIO register pointed to by the MMIO-index register.

Figure 14. Graphics Register Memory and I/O Map



9.6 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The (G)MCH supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. (G)MCH provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.
- Above 1-MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. The TSEG area lies below IGD stolen memory.

The above 1-MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

Note: DMI and PCI Express masters are not allowed to access the SMM space.

9.6.1 SMM Space Definition

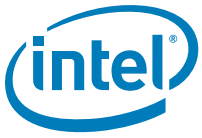
SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the CPU to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space are different address ranges. Note that the High DRAM space is the same as the Compatible Transaction Address space. Table 19 describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

These abbreviations are used later in the table describing SMM Space Transaction Handling.

Table 19. SMM Space Definition Summary

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN



9.7 SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any "PCI" devices (including DMI, PCI Express, and graphics devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
- Any address translated through the GMADR must not target DRAM from A_0000-F_FFFF.

9.7.1 SMM Space Combinations

When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1) the Compatible SMM space is effectively disabled. CPU originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP), otherwise they are forwarded to the DMI. PCI Express and DMI originated accesses are **never** allowed to access SMM space.

Table 20. SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

9.7.2 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at powerup. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 21. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	CPU in SMM Mode	SMM Code Access	SMM Data Access
0	x	X	x	x	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	x	Invalid	Invalid
1	1	X	x	0	Disable	Disable
1	1	0	x	1	Enable	Enable
1	1	1	x	1	Enable	Disable

9.7.3 SMM Space Decode and Transaction Handling

Only the CPU is allowed to access SMM space. PCI Express and DMI originated transactions are not allowed to SMM space.

9.7.4 CPU WB Transaction to an Enabled SMM Address Space

CPU Writeback transactions (REQ[1]# = 0) to enabled SMM address space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

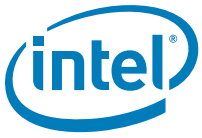
9.8 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into (G)MCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. CPU bus transactions are routed accordingly.

9.9 I/O Address Space

The (G)MCH does not support the existence of any other I/O devices beside itself on the CPU bus. The (G)MCH generates either DMI or PCI Express bus cycles for all CPU I/O accesses that it does not claim. Within the host bridge the (G)MCH contains two internal registers in the CPU I/O space, Configuration Address register (CONFIG_ADDRESS) and the Configuration Data register (CONFIG_DATA). These locations are used to implement a configuration space access mechanism.

The CPU allows 64 k+3 bytes to be addressed within the I/O space. The (G)MCH propagates the CPU I/O address without any translation on to the destination bus and therefore provides addressability for 64 k+3 byte locations. Note that the upper three locations can be accessed only during I/O address wrap-around when CPU bus HAB_16



address signal is asserted. HAB_16 is asserted on the CPU bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HAB_16 is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are **not** posted. Memory writes to ICH or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to PCI Express.

The (G)MCH responds to I/O cycles initiated on PCI Express or DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

For Intel® Pentium® M processor, Intel Core Duo processor, Intel Core Solo processor, and Mobile Intel® Pentium® 4 processor with 1-MB L2 cache processors, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the CPU as 1 transaction. The (G)MCH will break this into two separate transactions. This has not been done on previous chipsets. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into two transactions by the CPU.

9.9.1 PCI Express I/O Address Mapping

The (G)MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when CPU initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in (G)MCH Device 1 configuration space.

The (G)MCH positively decodes I/O accesses to PCI Express I/O address space as defined by the following equation:

I/O_Base_Address ≤ CPU I/O Cycle Address ≤ I/O_Limit_Address

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

The (G)MCH also forwards accesses to the Legacy VGA I/O ranges according to the settings in the Device 1 configuration registers BCTRL (VGA Enable) and PCICMD1 (IOAE1), unless a second adapter (monochrome) is present on the DMI Interface/PCI. The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set, the (G)MCH will decode legacy monochrome IO ranges and forward them to the DMI Interface. The IO ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3Bah and 3BFh.

Note that the (G)MCH Device 1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI Express.

9.10 (G)MCH Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A_0000 – 000A_FFFF
MDA = 000B_0000 – 000B_7FFF
VGAB = 000B_8000 – 000B_FFFF

MAINMEM = 0100_0000 to TOLUD

9.10.1 Legacy VGA and I/O Range Decode Rules

The legacy 128-KB VGA memory range 000A_0000h-000B_FFFFh can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the (G)MCH always decodes internally mapped devices first. Internal to the (G)MCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

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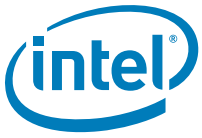


10 Functional Description

10.1 Host Interface

10.1.1 FSB Source Synchronous Transfers

The (G)MCH supports the Intel Core Duo and Intel Core Solo processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At 133-MHz and 166-MHz bus clock the address signals run at 266 and 333 MT/s for a maximum address queue rate of 66 M and 83 M addresses/sec. The data is quad pumped and an entire 64-B cache line can be transferred in two bus clocks. At 133-MHz and 166-MHz bus clock, the data signals run at 533 MHz and 667 MHz for a maximum bandwidth of 4.3 GB/s and 5.3 GB/s respectively.

10.1.2 FSB IOQ Depth

The Scalable Bus supports up to 12 simultaneous outstanding transactions.

10.1.3 FSB OOQ Depth

The (G)MCH supports only one outstanding deferred transaction on the FSB.

10.1.4 FSB GTL+ Termination

The (G)MCH integrates GTL+ termination resistors on die.

10.1.5 FSB Dynamic Bus Inversion

The (G)MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the CPU. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the (G)MCH. HDINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

HDINV[3:0]#	Data Bits
HDINV[0]#	HD[15:0]#
HDINV[1]#	HD[31:16]#
HDINV[2]#	HD[47:32]#
HDINV[3]#	HD[63:48]#

Whenever the processor or the (G)MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus the corresponding HDINV# signal will be asserted and the data will be inverted prior to being driven on the bus. Whenever the CPU or the (G)MCH receives data it monitors HDINV[3:0]# to determine if the corresponding data segment should be inverted.

10.1.6 FSB Interrupt Overview

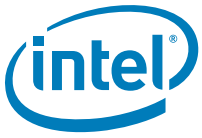
The Intel Core Duo and Intel Core Solo processor supports FSB interrupt delivery. They do **not** support the APIC serial bus interrupt delivery mechanism. Interrupt related messages are encoded on the FSB as “Interrupt Message Transactions”. FSB interrupts may originate from the CPUs on the FSB, or from a downstream device on the DMI or PCI Express Graphics Attach. In the later case, the (G)MCH drives the “Interrupt Message Transaction” on the FSB.

In the IOxAPIC environment, an interrupt is generated from the IOxAPIC to a CPU in the form of an upstream Memory Write. The ICH contains IOxAPICs, and its interrupts are generated as upstream DMI Memory Writes. Furthermore, the *PCI Local Bus Specification* and *PCI Express* Base Specification* define MSI’s (Message Signaled Interrupts) that are also in the form of Memory Writes. A PCI device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC. The IOxAPIC in turn generates an interrupt as an upstream DMI Memory Write. Alternatively, the MSI may directly route to the FSB. The target of an MSI is dependent on the address of the interrupt Memory Write. The (G)MCH forwards upstream DMI and PCI Express Graphics Attach low priority Memory Writes to address 0FEEx_xxxxh to the FSB as “Interrupt Message Transactions”.

The (G)MCH also broadcasts EOI cycles generated by a CPU downstream to the PCI Express Port and DMI interfaces.

10.1.7 APIC Cluster Mode Support

This is required for backwards compatibility with existing software, including various OS’s. As one example, beginning with Microsoft Windows* 2000 there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.



10.2 System Memory Controller

10.2.1 Functional Overview

Mobile Intel 945GM/GME/PM/GMS/GSE, 943/940GML and Intel 945GT Express Chipset system memory controller supports DDR2 SDRAMs.

Note: For Ultra Mobile 945GU Express Chipset system memory controller functional overview, see Section 10.2.2.

Three memory channel organizations are supported:

- Single-channel (Single SO-DIMM per channel)
- Dual-channel symmetric (Single SO-DIMM per channel)
- Dual-channel asymmetric (Single SO-DIMM per channel)

Each channel has a 64-bit data interface and the frequencies supported are 400 MHz, 533 MHz and 667 MHz.

Note: Mobile Intel 945GM/GME/PM/GMS/GSE, 943/940GML and Intel 945GT Express Chipsets support only one SO-DIMM connector per channel.

When configured as a dual-channel system, each channel can have one or two ranks populated. So in either case there can be a maximum of 4 ranks (2 double-sided SO-DIMMs) populated.

Table 22. System Memory Organization Support for DDR2

DDR2						
Tech	**Width**	**Page Size**	**Banks**	**Smallest Increments**	**Largest Increments**	**Maximum Capacity**
256 Mb	X8	8K	4	256 MB	512 MB	1 GB
256 Mb	X16	4K	4	128 MB	256 MB	512 MB
512 Mb	X8	8K	4	512 MB	1 GB	2 GB
512 Mb	X16	8K	4	256 MB	512 MB	1 GB
1 Gb	X8	8K	8	1 GB	2 GB	4 GB
1 Gb	X16	8K	8	512 MB	1 GB	2 GB

10.2.2 Functional Overview For Ultra Mobile Intel® 945GU Express Chipset

The Ultra Mobile Intel 945GU Express Chipset system memory controller supports DDR2 SDRAMs.

One memory channel organizations is supported:

- Single-channel (memory down)

The channel has a 64-bit data interface and the frequency supported is 400 MHz.

Note: SO-DIMMS are not supported.

Table 23. System Memory Organization Support for DDR2

DDR2						
Tech	**Width**	**Page Size**	**Banks**	**Smallest Increments**	**Largest Increments**	**Maximum Capacity**
256 Mb	X16	4K	4	128 MB	256 MB	512 MB
512 Mb	X16	8K	4	256 MB	512 MB	1 GB
1 Gb	X16	8K	8	512 MB	1 GB	2 GB

10.2.3 Memory Channel Organization Modes

The system memory controller supports three styles of memory organization (Single-channel, Dual-channel Symmetric and Dual-channel Asymmetric). Rules for populating SO-DIMM slots are included in this chapter.

10.2.3.1 Dual-channel Symmetric Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels, and the switch happens after each cache line (64-byte boundary). The channel selection address bit is controlled by DCC[10:9]. If a second request sits behind the first, and that request is to an address on the second channel, that request can be sent before data from the first request has returned. Due to this feature, some progress is made even during page conflict scenarios. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels. The drawback of Symmetric mode is that the system designer must populate both channels of memory so that they have equal capacity, but the technology and device width may vary from one channel to the other.

Table 24. Sample System Memory Organization with Symmetric Channels

	Channel A Population	**DRBs in Channel A**	**Channel B Population**	**DRBs in Channel B**
Rank 1	512 MB	1024 MB	512 MB	1024 MB
Rank 0	512 MB	512 MB	512 MB	512 MB

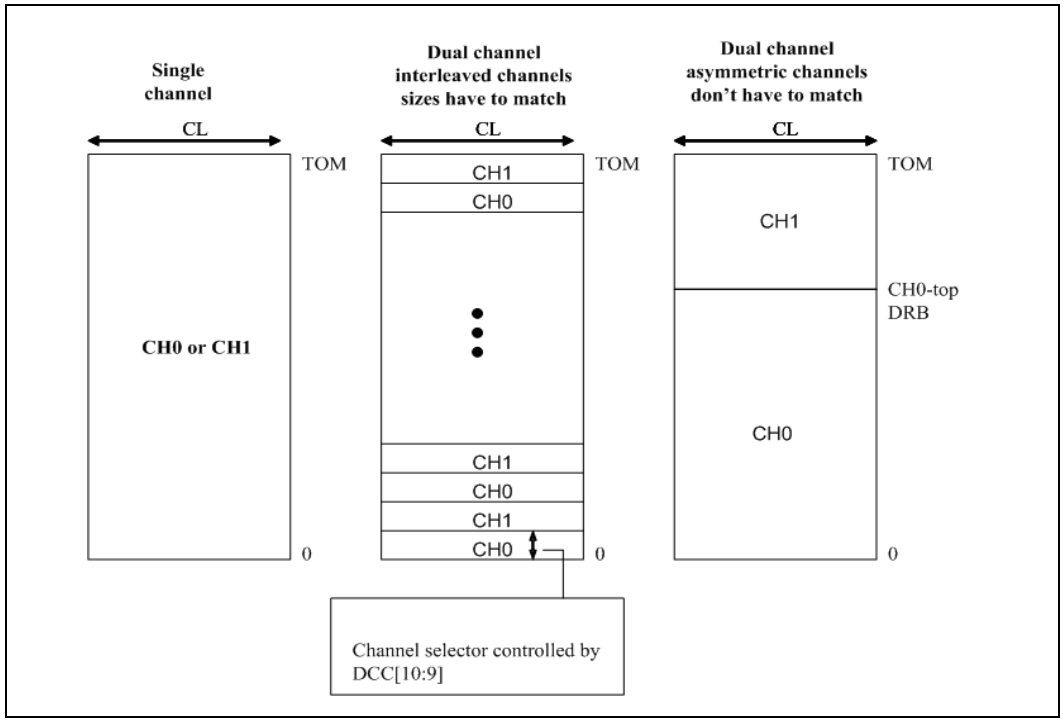
10.2.3.2 Dual-channel Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel A and stay there until the end of the highest rank in channel A, then addresses continue from the bottom of channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel. The system designer is free to populate or not to populate any rank on either channel, including either degenerate single-channel case.

Table 25. Sample System Memory Organization with Asymmetric Channels

	Channel A Population	DRBs in Channel A	Channel B Population	DRBs in Channel B
Rank 1	1024 MB	1536 MB	512 MB	768 MB
Rank 0	512 MB	512 MB	256 MB	256 MB

Figure 15. System Memory Styles



10.2.4 DRAM Technologies and Organization

All standard 256-Mb, 512-Mb, and 1-Gb technologies and addressing are supported for x16 and x8 devices.

The (G)MCH supports various page sizes. Page size is individually selected for every rank; 4 k and 8 k for Asymmetric, Symmetric, or Single-channel modes.

The DRAM sub-system supports single or dual-channels, 64-bit wide per channel.

The maximum number of ranks for dual-channel and single-channel configurations are described below:

- If configured as a dual-channel system, each channel can have one or two ranks populated
- If configured as a single-channel system, that channel can have one, two or three ranks populated.

Mixed mode double-sided SO-DIMMs (x8 and x16 on the same SO-DIMM) are not supported.

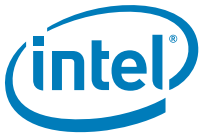
By using 1-Gb technology, the largest memory capacity is 4 GB (128M x 8b x 8 devices x 4 ranks = 4 GB). This is achieved using stacked SO-DIMMs. With non-stacked SO-DIMMs, the maximum memory capacity is 2 GB (64M x 16b x 4 devices x 4 ranks = 2 GB).

By using 256-Mb technology, the smallest memory capacity is 128 MB (16M x 16b x 4 devices x 1 ranks = 128 MB).

10.2.4.1 Rules for Populating SO-DIMM Slots

In all modes, the frequency of System Memory will be the lowest frequency of all SO-DIMMs in the system, as determined through the SPD registers on the SO-DIMMs. In both single-channel and dual-channel configurations, the Mobile Intel 945GM/GME/PM/GMS/GSE, 943/940GML and Intel 945GT Express Chipsets support only one SO-DIMM connector per channel.

- In the Single-channel mode, only channel A (channel 0) may be used.
- In Dual-channel Symmetric mode, both SO-DIMM slots must be populated, but the total amount of memory in each channel must be the same. The device technologies may differ.
- In Dual-channel Asymmetric mode, the total memory in the two channels need not be equal (one slot could even be unpopulated).



10.2.4.2 Pin Connectivity for Single- and Dual-channel Modes

Table 26. DDR2 Dual-channel Pin Connectivity

Dual Channel		
JEDEC Pin Mapping	**Channel A**	**Channel B**
CK[1:0]	SM_CK[1:0]	SM_CK[3:2]
CKB[1:0]	SM_CK#[1:0]	SM_CK#[3:2]
CSB[1:0]	SM_CS#[1:0]	SM_CS#[3:2]
CKE[1:0]	SM_CKE[1:0]	SM_CKE[3:2]
ODT[1:0]	SM_ODT[1:0]	SM_ODT[3:2]
BS[2:0]	SA_BS[2:0]	SB_BS[2:0]
MA[13:0]	SA_MA[13:0]	SB_MA[13:0]
RAS#	SA_RAS#	SB_RAS#
CAS#	SA_CAS#	SB_CAS#
WE#	SA_WE#	SB_WE#
DQ[63:0]	SA_DQ[63:0]	SB_DQ[63:0]
DQS[7:0]	SA_DQS[7:0]	SB_DQS[7:0]
DQS[7:0]#	SA_DQS#[7:0]	SB_DQS#[7:0]
DM[7:0]	SA_DM[7:0]	SB_DM[7:0]

Table 27. DDR2 Single-channel Pin Connectivity

JEDEC Pin Mapping	Channel A
CK_1:0	SM_CK[1:0]
CK#_1:0	SM_CK#[1:0]
CS#_1:0	SM_CS#[1:0]
CKE_1:0	SM_CKE[1:0]
ODT_1:0	SM_ODT[1:0]
BS_2:0	SA_BS[2:0]
MA_13:0	SA_MA[13:0]
RAS#	SA_RAS#
CAS#	SA_CAS#
WE#	SA_WE#
DQ_63:0	SA_DQ[63:0]
DQS_7:0	SA_DQS[7:0]
DQS#_7:0	SA_DQS#[7:0]
DM_7:0	SA_DM[7:0]

10.2.5 DRAM Address Mapping

The Table 28 and Table 29 below show the DRAM Address Mapping on the Mobile Intel 945GM/GME/PM/GMS/GSE, 943/940GML and Intel 945GT Express Chipsets in the Dual-channel mode without Enhanced Addressing.Table 30 and, Table 31 show the Address Mapping with Enhanced Address Swap. Table 32 and Table 33 shows the Address Mapping with Enhanced Address XOR configurations.

For DRAM address mapping on the Ultra Mobile Intel 945GU Express Chipset, refer to Figure 28, Figure 30, and Figure 32.

Enhanced Addressing swaps the MSB controlling one of the Bank Select lines with bit 18 (which normally controls row address bit 2). Without Enhanced Addressing, rank bits are the most significant two bits of the address. With Enhanced Addressing, the rank bits are always bits 19 and 20.

In the tables below,

- — ‘r’ indicates a Row Address bit,
- — ‘b' indicates a Bank Select bit,
- — ‘c’ indicates a Column Address bit,
- — ‘h’ indicates a Channel Select bit,
- — ‘s’ indicates that the bit is part of the decode for a Chip Select (rank select) bit

Different ranks may use different technologies or organizations, and it is recommended to check the DRB register programming to determine which channel and rank an address belongs to.

Both s and h are provided for the example of a homogenous population only. Column bit 10 is always used for an Auto Precharge indication.

Note: The Mobile Intel 943/940GML Express Chipset does not support Enhanced Addressing modes.

Note: The mapping detailed below applies to Single-Channel modes of operation also, except for symmetric addressing.

Table 28. DRAM Device Configurations –Single-channel/Dual-channel Asymmetric Mode (Sheet 1 of 2)

Technology (Mb)	256	256	512	512	1024	1024
Row Bits	13	13	13	14	13	14
Column Bits	9	10	10	10	10	10
Bank Bits	2	2	2	2	3	3
Width (b)	16	8	16	8	16	8
Rows	8192	8192	8192	16384	8192	16384
Columns	512	1024	1024	1024	1024	1024
Banks	4	4	4	4	8	8
Page Size (KB)	4	8	8	8	8	8
Devices per Rank	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	512	1024
Depth (M)	16	32	32	64	64	128

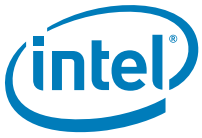


Table 28. DRAM Device Configurations –Single-channel / Dual-channel Asymmetric Mode (Sheet 2 of 2)

Addr Bits [n:0]	26	27	27	28	28	29
Host Address Bit	Memory Address Bit					
31	-	-	-	-	-	-
30	-	-	-	-	-	-
29	-	-	-	-	-	R 13
28	-	-	-	r 13	r 11	R 11
27	-	R 12	r 12	r 12	r 12	R 12
26	r 10	R 10	r 10	r 10	r 10	R 10
25	r 9	r 9	r 9	r 9	r 9	R 9
24	r 8	r 8	r 8	r 8	r 8	R 8
23	r 7	r 7	r 7	r 7	r 7	R 7
22	r 6	r 6	r 6	r 6	r 6	R 6
21	r 5	r 5	r 5	r 5	r 5	R 5
20	r 4	r 4	r 4	r 4	r 4	R 4
19	r 3	r 3	r 3	r 3	r 3	R 3
18	r 2	r 2	r 2	r 2	r 2	R 2
17	r 1	r 1	r 1	r 1	r 1	R 1
16	r 0	r 0	r 0	r 0	r 0	R 0
15	r 11	R 11	r 11	r 11	b 0	B 0
14	r 12	b 1	b 1	b 1	b 1	B 1
13	b 0	b 0	b 0	b 0	b 2	B 2
12	b 1	c 9	c 9	c 9	c 9	C 9
11	c 8	c 8	c 8	c 8	c 8	C 8
10	c 7	c 7	c 7	c 7	c 7	C 7
9	c 6	c 6	c 6	c 6	c 6	C 6
8	c 5	c 5	c 5	c 5	c 5	C 5
7	c 4	c 4	c 4	c 4	c 4	C 4
6	c 3	c 3	c 3	c 3	c 3	C 3

Table 29. DRAM Device Configurations – Dual-channel Symmetric Mode (Sheet 1 of 2)

Technology (Mb)	256	256	512	512	1024	1024
Row Bits	13	13	13	14	13	14
Column Bits	9	10	10	10	10	10
Bank Bits	2	2	2	2	3	3
Width (b)	16	8	16	8	16	8
Rows	8192	8192	8192	16384	8192	16384
Columns	512	1024	1024	1024	1024	1024
Banks	4	4	4	4	8	8
Page Size (KB)	4	8	8	8	8	8
Devices per Rank	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	512	1024
Depth (M)	16	32	32	64	64	128
Addr Bits [n:0]	26	27	27	28	28	29
Host Address Bit	Mem Addr-Bit					
31	-	-	-	-	-	-
30	-	-	-	-	-	r 13
29	-	-	-	r 13	r 11	r 11
28	-	r 12	r 12	r 12	r 12	r 12
27	R 10	r 10	r 10	r 10	r 10	r 10
26	r 9	r 9	r 9	r 9	r 9	r 9
25	r 8	r 8	r 8	r 8	r 8	r 8
24	r 7	r 7	r 7	r 7	r 7	r 7
23	r 6	r 6	r 6	r 6	r 6	r 6
22	r 5	r 5	r 5	r 5	r 5	r 5
21	r 4	r 4	r 4	r 4	r 4	r 4
20	r 3	r 3	r 3	r 3	r 3	r 3
19	r 2	r 2	r 2	r 2	r 2	r 2
18	r 1	r 1	r 1	r 1	r 1	r 1
17	r 0	r 0	r 0	r 0	r 0	r 0
16	R 11	r 11	r 11	r 11	b 0	b 0

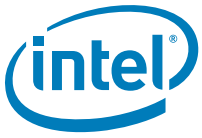


Table 29. DRAM Device Configurations – Dual-channel Symmetric Mode (Sheet 2 of 2)

15	R 12	b 1	b 1	b 1	b 1	b 1
14	b 0	b 0	b 0	b 0	b 2	b 2
13	b 1	c 9	c 9	c 9	c 9	c 9
12	c 8	c 8	c 8	c 8	c 8	c 8
11	c 7	c 7	c 7	c 7	c 7	c 7
10	c 6	c 6	c 6	c 6	c 6	c 6
9	c 5	c 5	c 5	c 5	c 5	c 5
8	c 4	c 4	c 4	c 4	c 4	c 4
7	c 3	c 3	c 3	c 3	c 3	c 3
6	h	h	h	h	H	H
5	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0

Table 30. DRAM Device Configurations – Single-channel/Dual-channel Asymmetric Mode with Enhanced Addressing Swap (0) (Sheet 1 of 2)

Technology (Mb)	256	256	512	512	1024	1024
Row Bits	13	13	13	14	13	14
Column Bits	9	10	10	10	10	10
Bank Bits	2	2	2	2	3	3
Width (b)	16	8	16	8	16	8
Rows	8192	8192	8192	16384	8192	16384
Columns	512	1024	1024	1024	1024	1024
Banks	4	4	4	4	8	8
Page Size (KB)	4	8	8	8	8	8
Devices per Rank	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	512	1024
Depth (M)	16	32	32	64	64	128
Addr Bits [n:0]	26	27	27	28	28	29
Host Address Bit	**Mem Addr-Bit**					
31	-	-	-	-	-	-

Table 30. DRAM Device Configurations – Single-channel / Dual-channel Asymmetric Mode with Enhanced Addressing Swap (0) (Sheet 2 of 2)

30	-	-	-	-	-	r 3
29	-	-	-	r 3	r 3	r 13
28	-	r 3	r 3	r 13	r 11	r 11
27	r 3	r 12	r 12	r 12	r 12	r 12
26	r 10	r 10	r 10	r 10	r 10	r 10
25	r 9	r 9	r 9	r 9	r 9	r 9
24	r 8	r 8	r 8	r 8	r 8	r 8
23	r 7	r 7	r 7	r 7	r 7	r 7
22	r 6	r 6	r 6	r 6	r 6	r 6
21	r 5	r 5	r 5	r 5	b 2	b 2
20	r 4	r 4	r 4	r 4	r 4	r 4
19	s 0	s 0	s 0	s 0	s 0	s 0
Host Address Bit	**Mem Addr-Bit**					
18	b 1	b 1	b 1	b 1	b 1	b 1
17	r 1	r 1	r 1	r 1	r 1	r 1
16	r 0	r 0	r 0	r 0	r 0	r 0
15	r 11	R 11	r 11	r 11	r 5	r 5
14	r 12	r 2	r 2	r 2	r 2	r 2
13	r 2	b 0	b 0	b 0	b 0	b 0
12	b 0	c 9	c 9	c 9	c 9	c 9
11	c 8	c 8	c 8	c 8	c 8	c 8
10	C 7	c 7	c 7	c 7	c 7	c 7
9	C 6	c 6	c 6	c 6	c 6	c 6
8	C 5	c 5	c 5	c 5	c 5	c 5
7	C 4	c 4	c 4	c 4	c 4	c 4
6	C 3	c 3	c 3	c 3	c 3	c 3
5	C 2	c 2	c 2	c 2	c 2	c 2
4	C 1	c 1	c 1	c 1	c 1	c 1
3	C 0	c 0	c 0	c 0	c 0	c 0

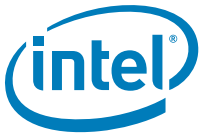


Table 31. DRAM Device Configurations –Dual-channel Symmetric Mode with Enhanced Addressing Swap (Sheet 1 of 2)

Technology (Mb)	256	256	512	512	1024	1024
Row Bits	13	13	13	14	13	14
Column Bits	9	10	10	10	10	10
Bank Bits	2	2	2	2	3	3
Width (b)	16	8	16	8	16	8
Rows	8192	8192	8192	16384	8192	16384
Columns	512	1024	1024	1024	1024	1024
Banks	4	4	4	4	8	8
Page Size (KB)	4	8	8	8	8	8
Devices per Rank	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	512	1024
Depth (M)	16	32	32	64	64	128
Addr Bits [n:0]	26	27	27	28	28	29
31	-	-	-	-	-	r 3
30	-	-	-	r 3	r 3	r 13
29	-	r 3	r 3	r 13	r 11	r 11
28	R 3	R 12	r 12	r 12	r 12	r 12
27	r 10	R 10	r 10	r 10	r 10	r 10
26	R 9	r 9	r 9	r 9	r 9	r 9
25	R 8	r 8	r 8	r 8	r 8	r 8
24	R 7	r 7	r 7	r 7	r 7	r 7
23	R 6	r 6	r 6	r 6	r 6	r 6
22	R 5	r 5	r 5	r 5	b 2	b 2
21	R 4	r 4	r 4	r 4	r 4	r 4
20	S 0	s 0	s 0	s 0	s 0	s 0
19	B 1	b 1	b 1	b 1	b 1	b 1
18	R 1	r 1	r 1	r 1	r 1	r 1
17	R 0	r 0	r 0	r 0	r 0	r 0
16	r 11	R 11	r 11	r 11	r 5	r 5

Table 31. DRAM Device Configurations –Dual-channel Symmetric Mode with Enhanced Addressing Swap (Sheet 2 of 2)

15	r 12	r 2	r 2	r 2	r 2	r 2
14	R 2	b 0	b 0	b 0	b 0	b 0
13	b 0	c 9	c 9	c 9	c 9	c 9
12	c 8	c 8	c 8	c 8	c 8	c 8
11	c 7	c 7	c 7	c 7	c 7	c 7
10	c 6	c 6	c 6	c 6	c 6	c 6
9	c 5	c 5	c 5	c 5	c 5	c 5
8	c 4	c 4	c 4	c 4	c 4	c 4
7	c 3	c 3	c 3	c 3	c 3	c 3
6	h	h	h	H	H	H
5	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0

Table 32. DRAM Device Configurations – Single-channel / Dual-channel Asymmetric Mode with Enhanced Addressing XOR (Sheet 1 of 2)

Technology (Mb)	256	256	512	512	1024	1024
Row Bits	13	13	13	14	13	14
Column Bits	9	10	10	10	10	10
Bank Bits	2	2	2	2	3	3
Width (b)	16	8	16	8	16	8
Rows	8192	8192	8192	16384	8192	16384
Columns	512	1024	1024	1024	1024	1024
Banks	4	4	4	4	8	8
Page Size (KB)	4	8	8	8	8	8
Devices per Rank	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	512	1024
Depth (M)	16	32	32	64	64	128
Addr Bits [n:0]	26	27	27	28	28	29
Host Address Bit	**Mem Addr-Bit**					
31	-	-	-	-	-	-

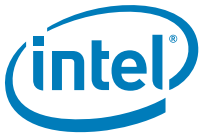


Table 32. DRAM Device Configurations – Single-channel/Dual-channel Asymmetric Mode with Enhanced Addressing XOR (Sheet 2 of 2)

30	-	-	-	-	-	r 3
29	-	-	-	r 3	r 3	r 13
28	-	r 3	r 3	r 13	r 11	r 11
27	r 3	r 12	r 12	r 12	r 12	r 12
26	r 10	r 10	r 10	r 10	r 10	r 10
25	r 9	r 9	r 9	r 9	r 9	r 9
24	r 8	r 8	r 8	r 8	r 8	r 8
23	r 7	r 7	r 7	r 7	r 7	r 7
22	r 6	r 6	r 6	r 6	r 6	r 6
21	r 5	r 5	r 5	r 5	r 5	r 5
20	r 4	r 4	r 4	r 4	r 4	r 4
19	r0 xor s0	r0 xor s 0	r0 xor s0	r0 xor s0	r0 xor s0	r0 xor s0
18	r 2	r 2	r 2	r 2	r 2	r 2
17	r 1	r 1	r 1	r 1	r 1	r 1
16	R 0	r 0	r 0	r 0	r 0	r 0
15	r 11	r 11	r 11	r 11	r 4 xor b 0	r 4 xor b 0
14	r 12	r 5 xor b 1	r 5 xor b 1	r 5 xor b 1	r 5 xor b 1	r 5 xor b 1
13	r 4 xor b 0	r 4 xor b 0	r 4 xor b 0	r 4 xor b 0	r 2 xor b 2	r 2 xor b 2
12	r 5 xor b 1	c 9	c 9	c 9	c 9	c 9
11	C 8	c 8	c 8	c 8	c 8	c 8
10	C 7	c 7	c 7	c 7	c 7	c 7
9	C 6	c 6	c 6	c 6	c 6	c 6
8	C 5	c 5	c 5	c 5	c 5	c 5
7	C 4	c 4	c 4	c 4	c 4	c 4
6	C 3	c 3	c 3	c 3	c 3	c 3
5	C 2	c 2	c 2	c 2	c 2	c 2
4	C 1	c 1	c 1	c 1	c 1	c 1
3	C 0	c 0	c 0	c 0	c 0	c 0

Table 33. DRAM Device Configurations – Dual-channel Symmetric Mode with Enhanced Addressing XOR (Sheet 1 of 2)

Technology (Mb)	256	256	512	512	1024	1024
Row Bits	13	13	13	14	13	14
Column Bits	9	10	10	10	10	10
Bank Bits	2	2	2	2	3	3
Width (b)	16	8	16	8	16	8
Rows	8192	8192	8192	16384	8192	16384
Columns	512	1024	1024	1024	1024	1024
Banks	4	4	4	4	8	8
Page Size (KB)	4	8	8	8	8	8
Devices per Rank	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	512	1024
Depth (M)	16	32	32	64	64	128
Addr Bits [n:0]	26	27	27	28	28	29
31	-	-	-	-	-	r 3
30	-	-	-	r 3	r 3	r 13
29	-	r 3	r 3	r 13	r 11	r 11
28	R 3	r 12	r 12	r 12	r 12	r 12
27	r 10	r 10	r 10	r 10	r 10	r 10
26	R 9	r 9	r 9	r 9	r 9	r 9
25	R 8	r 8	r 8	r 8	r 8	r 8
24	R 7	r 7	r 7	r 7	r 7	r 7
23	R 6	r 6	r 6	r 6	r 6	r 6
22	R 5	r 5	r 5	r 5	r 5	r 5
21	R 4	r 4	r 4	r 4	r 4	r 4
20	r0 xor s 0	r0 xor s 0	r0 xor s 0	r0 xor s 0	r0 xor s 0	R0 xor s 0
19	r 2	r 2	r 2	r 2	r 2	r 2
18	r 1	r 1	r 1	r 1	r 1	r 1
17	r 0	r 0	r 0	r 0	r 0	r 0
16	r 11	r 11	r11	r11	r4 xor b0	r4 xor b0

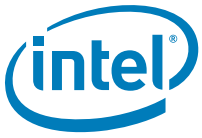


Table 33. DRAM Device Configurations – Dual-channel Symmetric Mode with Enhanced Addressing XOR (Sheet 2 of 2)

15	r 12	r 5 xor b1	r 5 xor b1	R5 xor b1	r5 xor b1	r5 xor b1
14	r 4 xor b0	r 4 xor b0	r 4 xor b0	R4 xor b0	r2 xor b2	r2 xor b2
13	r 5 xor b1	c 9	c 9	c 9	c 9	c 9
12	c 8	c 8	c 8	c 8	c 8	c 8
11	c 7	c 7	c 7	c 7	c 7	c 7
10	c 6	c 6	c 6	c 6	c 6	c 6
9	c 5	c 5	c 5	c 5	c 5	c 5
8	c 4	c 4	c 4	c 4	c 4	c 4
7	c 3	c 3	c 3	c 3	c 3	c 3
6	h	h	h	h	h	H
5	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0

10.2.6 DRAM Clock Generation

The Mobile Intel 945GM/GME/PM/GMS/GSE, 943/940GML and Intel 945GT Express Chipsets generate two differential clock pairs for every supported SO-DIMM.

10.2.7 DDR2 On Die Termination

On die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each DQ, DQS/DQS# and DM signal for x8 configurations via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the termination resistance for the DQ, DM, DQS, and DQS# signals to be located inside the DRAM devices themselves instead of on the motherboard. The (G)MCH drives out the required ODT signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted SO-DIMM rank to enable or disable their termination resistance.

ODT operation follows these general rules:

WRITE

- Chipset: ODT off
- DRAM:
  - — If one slot populated but has two ranks, turn on termination in the written rank.
  - — If one slot/one rank, turn on that rank's termination.

READ

- Chipset: ODT on
- DRAM: ODT off

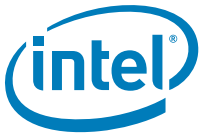
Table 34 details the ODT values supported by the Mobile Intel 945GM/GME/PM/GMS/GSE, 943/940GML and Intel 945GT Express Chipsets.

Table 34. ODT Settings Supported by the Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets

Express Chipset	Supported DDR2-Speeds per Chipset	ODT Options Required by the Intel® DDR2 JEDEC Specification Addendum	ODT Setting Supported per Each Chipset Memory Configuration
Ultra Mobile Intel® 945GU	400	50, 75, 150	150 (Dual Channel) 75 (Single Channel)
Mobile Intel® 945GM/GME	400, 533, 667		
Intel® 945GT	400, 533, 667		
Mobile Intel® 945PM	400, 533, 667		
Mobile Intel® 945GMS/GSE	400, 533		
Mobile Intel® 943/940GML	400, 533		

10.2.8 DRAM Power Management

The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets implement extensive support for power management on the SDRAM interface through Clock Enable (CKE) signals. (G)MCH drives 4 CKE pins (2 per channel) to perform the power management operations.



10.2.8.1 Self Refresh Entry and Exit Operation

When entering the Suspend-To-RAM (STR) state, (G)MCH will flush pending cycles and then enter all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices will perform self-refresh.

10.2.8.2 Dynamic Rank Power Down Operation

The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets implement aggressive CKE control to dynamically put the DRAM devices in a power down state. The (G)MCH controller can be configured to put the devices in *active power down* (CKE deassertion with open pages) or *precharge power down* (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages are needed to be closed before putting the devices in power down mode.

If dynamic power down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

10.2.8.3 DRAM I/O Power Management

(G)MCH implements several power saving features where different groups of IO buffers are disabled when safe to do so in a dynamic fashion thereby saving IO power. These features are listed below.

- SO-DIMM clock gating disable – The Mobile Intel 945GM/GME/PM/GMS/GSE, 943/940GML and Intel 945GT Express Chipsets have 2 clock pairs per SO-DIMM. If only one SO-DIMM is populated, it allows the other 2 clock pairs to be disabled.
- Address and control tri-state enable – If CKE for any given rank is deasserted, the CS# to that rank is disabled. If all CKEs are deasserted (such as in S3), All address and control buffers (excluding CKEs) are disabled.
- Data sense amp disable (self refresh, dynamic) - When all the SDRAM ranks have been put in a self refresh state, or during normal operation, if no memory accesses are pending, the sense amplifiers for all data buffers are turned off.
- Output only sense amp disable – Sense amplifiers of all IO buffers which are functionally outputs only (everything except DQ and DQS) are turned off.

10.2.9 System Memory Throttling

The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets have two independent mechanisms, (i) (G)MCH Thermal Management and (ii) DRAM Thermal Management that cause system memory bandwidth throttling. For more information on System Memory Throttling, see Section 10.7.4.

- (G)MCH Thermal management is to ensure that the chipset is operating within thermal limits. The implementation provides a mechanism that controls the amount of (G)MCH initiated DDR2 IO bandwidth to a programmable limit. The mechanism can be initiated by a thermal sensor trip or by write bandwidth measurement exceeding a programmed threshold.
- DRAM Thermal management is to ensure that the DRAM chips are operating within thermal limits. DRAM s are organized as ranks. Each rank heats up independently based on the activity it is subject to by the (G)MCH. A rank may heat up by different amounts based on the type of activity it is subject to. For example the amount of heat contributed by a read command is different when compared to a write command to a rank. Throttling can be initiated by an external thermal sensor trip or by DRAM activity measurement exceeding a programmed threshold.

10.3 PCI Express-Based External Graphics

See the current *PCI Express* Base Specification* for details on PCI Express.

This (G)MCH is part of a PCI Express root complex. This means it connects a host CPU/ memory subsystem to a PCI Express Hierarchy. The control registers for this functionality are located in Device 1 configuration space and two Root Complex Register Blocks (RCRBs).

10.3.1 PCI Express Architecture

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load - store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 2.5 GHz (250 MHz internally) results in 2.5 GB/s direction which provides a 250 MB/s communications channel in each direction (500 MB/s total) that is close to twice the data rate of classic PCI per lane.

10.3.1.1 Layering Overview

The representation of layers in the PCI Express architecture (transaction layer, data link layer, and physical layer) is to simplify the understanding of the high-level functionality.

PCI Express uses packets to communicate information between components. Packets are formed in the transaction and data link layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side the reverse process occurs and packets get transformed from their physical layer representation to the data link layer representation and finally (for transaction layer packets) to the form that can be processed by the transaction layer of the receiving device.

10.3.1.2 Transaction Layer

The upper layer of the PCI Express architecture is the transaction layer. The transaction layer's primary responsibility is the assembly and disassembly of transaction layer packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The transaction layer also manages flow control of TLPs.

10.3.1.3 Data Link Layer

The middle layer in the PCI Express stack, the data link layer, serves as an intermediate stage between the transaction layer and the physical layer. Responsibilities of data link layer include link management, error detection, and error correction.

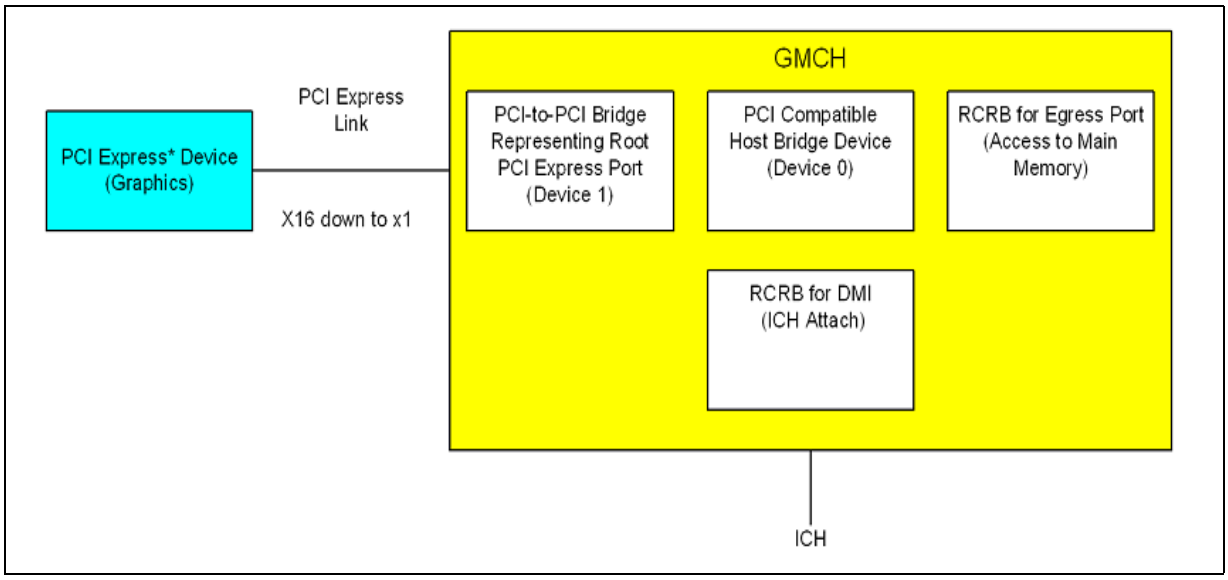
10.3.1.4 Physical Layer

The physical layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

10.3.1.5 PCI Express Configuration Mechanism

The PCI Express (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 16. PCI Express Related Register Structures in (G)MCH



PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by the current *PCI Local Bus Specification*. PCI Express configuration space is divided into a conventional PCI 2.3 compatible region, which consists of the first 256 bytes of a logical device's configuration space and an extended PCI Express region which consists of the remaining configuration space. The conventional PCI 2.3 compatible region can be accessed using either the mechanisms defined in the current *PCI Local Bus Specification*, or using the enhanced PCI Express configuration access mechanism described in the *PCI Express Enhanced Configuration Mechanism* section of the *PCI Express* Base Specification*.

The PCI Express host bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only.

See the current *PCI Local Bus Specification* for details of both the conventional PCI 2.3 compatible and PCI Express Enhanced configuration mechanisms and transaction rules.

10.3.2 Serial Digital Video Output (SDVO)

The SDVO description is located here because it is muxed onto the PCI Express x16 port pins. The AC/DC specifications are identical to the PCI Express Graphics interface.

SDVO electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependant upon the active display resolution and timing. The port can be dynamically configured in several modes to support display configurations.

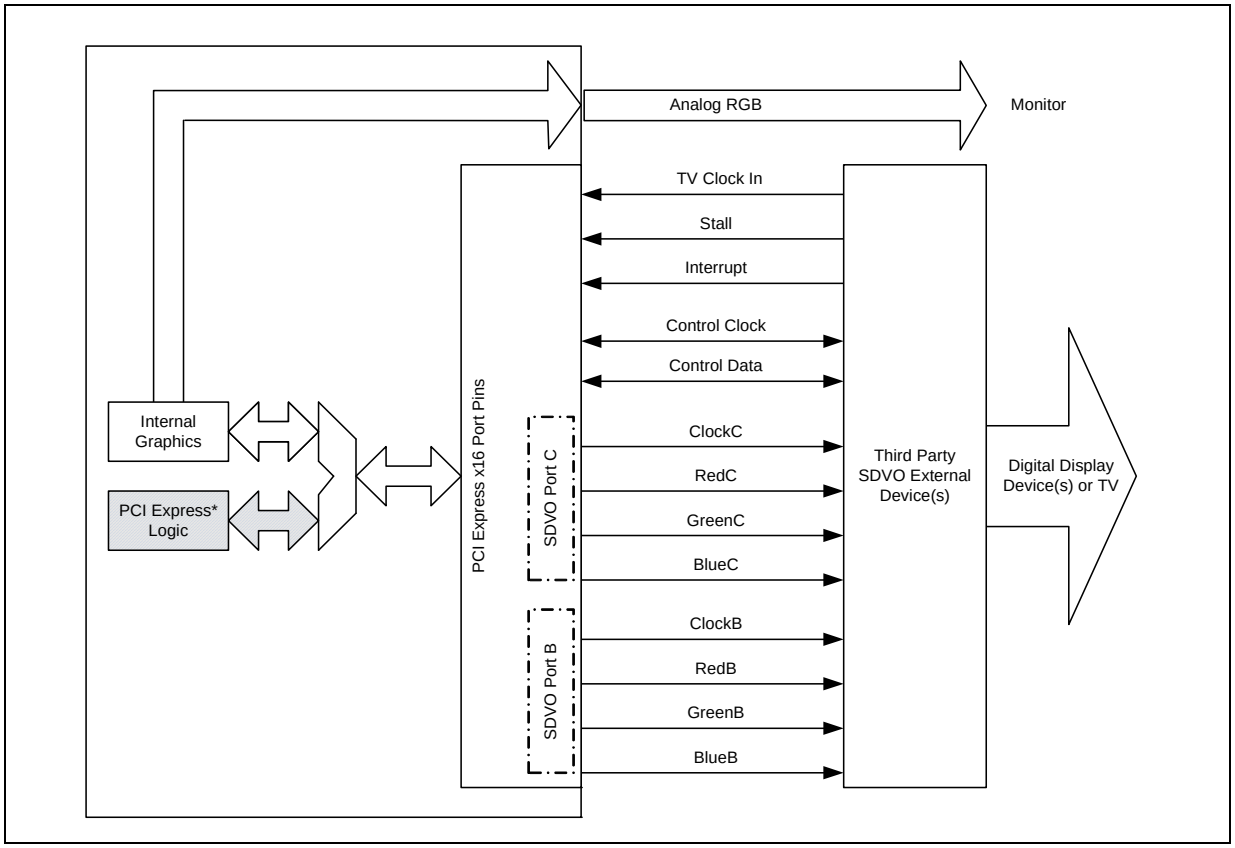
Essentially, an SDVO port will transmit display data in a high-speed, serial format across differential AC coupled signals. An SDVO port consists of a sideband differential clock pair and a number of differential data pairs.

10.3.2.1 SDVO Capabilities

SDVO ports can support a variety of display types including LVDS, DVI, TV-Out, and external CE type devices. the Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets utilize an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings. The Internal Graphics controller can have one or two SDVO ports multiplexed on the x16 PCI Express interface, in the case of the Mobile Intel 945GM/GME and Intel 945GT Express Chipsets.

The SDVO port defines a two-wire point-to-point communication path between the SDVO device and (G)MCH. The SDVO Control Clock and Data provide similar functionality to I^2C. However unlike I^2C, this interface is intended to be point-to-point (from the (G)MCH to the SDVO device) and will require the SDVO device to act as a switch and direct traffic from the SDVO Control bus to the appropriate receiver. Additionally, this Control bus will be able to run at faster speeds (up to 1 MHz) than a traditional I^2C interface would.

Figure 17. SDVO Conceptual Block Diagram



10.3.2.2 Concurrent SDVO/PCIe Operation

The Mobile Intel 945GM/GME and Intel 945GT Express Chipset variant supports concurrent operation of the SDVO port with video capture via x1 PCIe interface. Note that the only type of data supported over the x1 PCIe link is video capture.

The PCI Express lanes comprise a standard PCI Express link and must always originate with lane 0 on the PCI Express connector. The only supported PCIe width when SDVO is present is x1.

This concurrency is supported in reversed and non-reversed configurations. Mirroring / Reversing are always about the axis between lanes 7 and 8. When SDVO is reversed, SDVO lane 0 corresponds to what would be PCIe pin/connector lane 15 (mirrored to higher lane numbers).

Hardware reset straps are used to determine which of the six configurations below is desired.

Table 35. Concurrent SDVO / PCIe Configuration Strap Controls

Configuration Number	Description	Slot Reversed Strap (CFG9)	SDVO Present Strap (SDVO_CTRLDATA)	SDVO/PCIe* Concurrent Strap (CFG 20)
1	PCIe-only not reversed	High	Low	Low
2	PCIe-only reversed	Low	Low	Low
3	SDVO-only not reversed	High	High	Low
4	SDVO-only reversed	Low	High	Low
5	SDVO & PCIe not reversed	High	High	High
6	SDVO & PCIe reversed	Low	High	High

NOTE: Details of the implementations are below corresponding to the configuration number.

Figure 18. SDVO/PCIe Non-Reversed Configurations

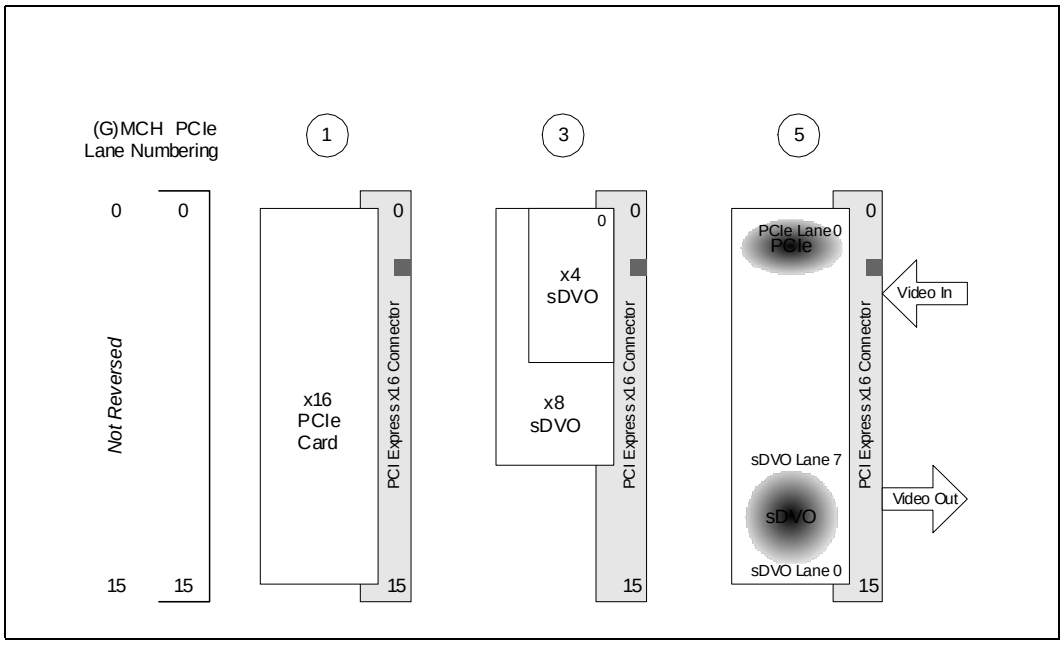
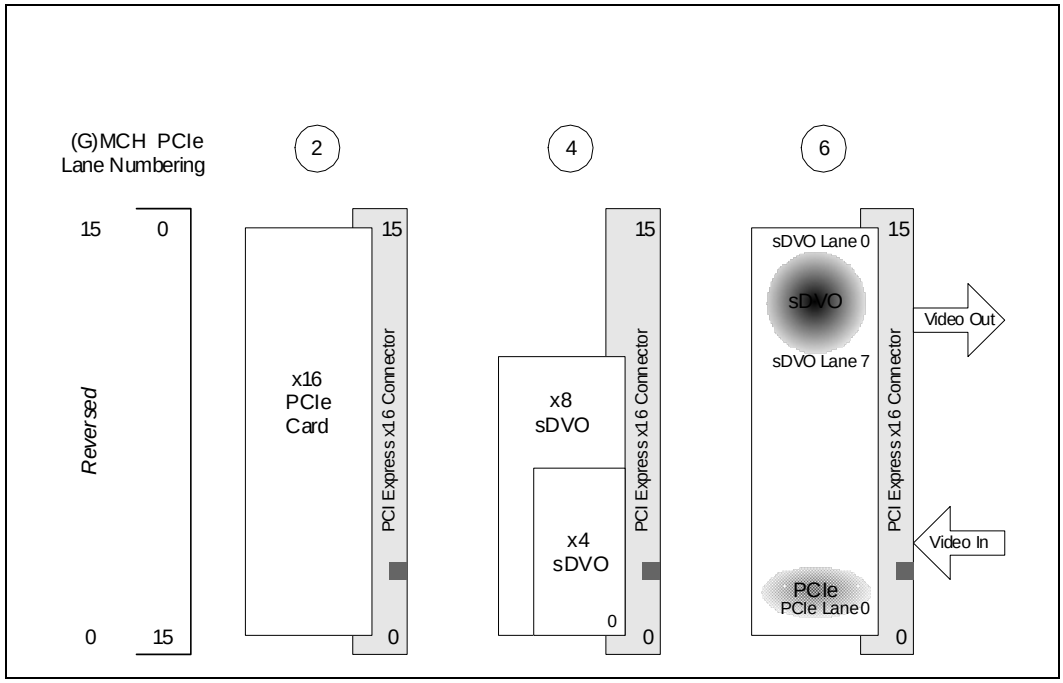


Figure 19. SDVO/PCIe Reversed Configurations



10.3.2.2.1 SDVO Signal Mapping

The table below shows the mapping of SDVO signals to the PCIe lanes in the various possible configurations as determined by the strapping configuration. Note that slot-reversed configurations do not apply to the integrated-graphics only variants.

Table 36. Configuration-wise Mapping of SDVO Signals on the PCIe Interface (Sheet 1 of 2)

SDVO Signal	Configuration-wise Mapping			
	SDVO Only – Normal (3)	SDVO Only – Reversed (4)	Concurrent SDVO and PCIe – Normal (5)	Concurrent SDVO and PCIe* – Reversed (6)
SDVOB_RED#	EXP_TXN0	EXP_TXN15	EXP_TXN15	EXP_TXN0
SDVOB_RED	EXP_TXP0	EXP_TXP15	EXP_TXP15	EXP_TXP0
SDVOB_GREEN#	EXP_TXN1	EXP_TXN14	EXP_TXN14	EXP_TXN1
SDVOB_GREEN	EXP_TXP1	EXP_TXP14	EXP_TXP14	EXP_TXP1
SDVOB_BLUE#	EXP_TXN2	EXP_TXN13	EXP_TXN13	EXP_TXN2
SDVOB_BLUE	EXP_TXP2	EXP_TXP13	EXP_TXP13	EXP_TXP2
SDVOB_CLKN	EXP_TXN3	EXP_TXN12	EXP_TXN12	EXP_TXN3
SDVOB_CLKP	EXP_TXP3	EXP_TXP12	EXP_TXP12	EXP_TXP3
SDVOC_RED#	EXP_TXN4	EXP_TXN11	EXP_TXN11	EXP_TXN4
SDVOC_RED	EXP_TXP4	EXP_TXP11	EXP_TXP11	EXP_TXP4
SDVOC_GREEN#	EXP_TXN5	EXP_TXN10	EXP_TXN10	EXP_TXN5

Table 36. Configuration-wise Mapping of SDVO Signals on the PCIe Interface (Sheet 2 of 2)

SDVO Signal	Configuration-wise Mapping			
	SDVO Only – Normal (3)	SDVO Only – Reversed (4)	Concurrent SDVO and PCIe – Normal (5)	Concurrent SDVO and PCIe* – Reversed (6)
SDVOC_GREEN	EXP_TXP5	EXP_TXP10	EXP_TXP10	EXP_TXP5
SDVOC_BLUE#	EXP_TXN6	EXP_TXN9	EXP_TXN9	EXP_TXN6
SDVOC_BLUE	EXP_TXP6	EXP_TXP9	EXP_TXP9	EXP_TXP6
SDVOC_CLKN	EXP_TXN7	EXP_TXN8	EXP_TXN8	EXP_TXN7
SDVOC_CLKP	EXP_TXP7	EXP_TXP8	EXP_TXP8	EXP_TXP7
SDVO_TVCLKIN#	EXP_RXN0	EXP_RXN15	EXP_RXN15	EXP_RXN0
SDVO_TVCLKIN	EXP_RXP0	EXP_RXP15	EXP_RXP15	EXP_RXP0
SDVOB_INT#	EXP_RXN1	EXP_RXN14	EXP_RXN14	EXP_RXN1
SDVOB_INT	EXP_RXP1	EXP_RXP14	EXP_RXP14	EXP_RXP1
SDVO_FLDSTALL#	EXP_RXN2	EXP_RXN13	EXP_RXN13	EXP_RXN2
SDVO_FLDSTALL	EXP_RXP2	EXP_RXP13	EXP_RXP13	EXP_RXP2
SDVOC_INT#	EXP_RXN5	EXP_RXN10	EXP_RXN10	EXP_RXN5
SDVOC_INT	EXP_RXP5	EXP_RXP10	EXP_RXP10	EXP_RXP5

NOTE: Slot reversal is not supported on Intel 945GMS/GU/GSE Express Chipset. Only Signals highlighted in BROWN are applicable to the Intel 945GMS/GU/GSE Express Chipset. Note that on the Intel® 945GU Express Chipset, SDVO_FLDSTALL#/SDVO/FLDSTALL are referred to as SDVO_FLDSTALLN/SDVO/FLDSTALLP.

10.3.2.3 SDVO Modes

The port can be dynamically configured in several modes:

Standard – Baseline SDVO functionality. Supports Pixel Rates between 25 and 200 MP/s. Utilizes three data pairs to transfer RGB data.

Dual Standard – Utilizes Standard data streams across both SDVO B and SDVO C. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 and 200 MP/s. There are two types of dual standard modes:

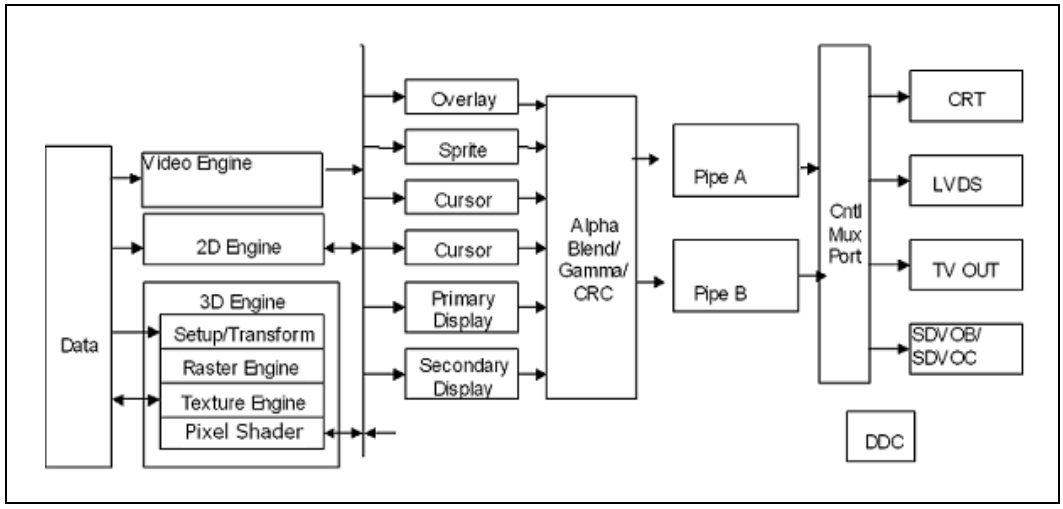
— Dual Independent Standard - In Dual Independent Standard mode, each SDVO channel will see a different pixel stream. The data stream across SDVO B will not be the same as the data stream across SDVO C.

— Dual Simultaneous Standard - In Dual Simultaneous Standard mode, both SDVO channels will see the same pixel stream. The data stream across SDVO B will be the same as the data stream across SDVO C. The display timings will be identical, but the transfer timings may not be - i.e., SDVO B Clocks and Data may not be perfectly aligned with SDVO C Clock and Data as seen at the SDVO device(s). Since this utilizes just a single data stream, it utilizes a single pixel pipeline within the (G)MCH.

10.4 Integrated Graphics Controller

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset internal graphics devices contain several types of components. The major components in the IGD are the engines, planes, pipes and ports. The (G)MCH has a 3D/2D Instruction Processing unit to control the 3D and 2D engines. The IGD's 3D and 2D engines are fed with data through the memory controller. The outputs of the engines are surfaces sent to memory, which are then retrieved and processed by (G)MCH planes.

Figure 20. (G)MCH Graphics Controller Block Diagram



The (G)MCH contains a variety of planes, such as display, overlay, cursor and VGA. A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of combined planes and a timing generator. The (G)MCH has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe.

The entire IGD is fed with data from its memory controller. The (G)MCH's graphics performance is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller (e.g., single-channel DDR2 533), the rest of the IGD will also be affected.

10.4.1 3D Graphics Processing

10.4.1.1 3D Graphics Pipeline

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset graphics are the next step in the evolution of integrated graphics.

The 3D graphics pipeline for the Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset graphics have a deep pipelined architecture in which each stage can simultaneously operate on different primitives or on different portions of the same primitive.

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset graphics are optimized by using current and future Intel processor family for advance software based transform and lighting (geometry processing) as defined by Microsoft DirectX API. Within the IGD, the rasterization engine converts vertices to pixels and the texture engine applies textures to pixels. The rasterization engine takes textured pixels and applies lighting and other environmental affects to produce the final pixel value. From the rasterization stage the final pixel value is written to the frame buffer in memory so that it can be displayed.

10.4.1.2 3D Engine

The 3D engine of the Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets have been designed with a deep pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive.

The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the Setup Engine, Rasterizer, Texture Pipeline, and Raster Pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.

The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

10.4.1.3 4X Faster Setup Engine

The setup stage of the pipeline takes the input data associated with each vertex of 3D primitive and computes the various parameters required for scan conversion. In formatting this data, the (G)MCH maintains sub-pixel accuracy.

10.4.1.3.1 3D Primitives and Data Formats Support

The 3D primitives rendered by (G)MCH are points, lines, discrete triangles, line strips, triangle strips, triangle fans and polygons. In addition to this, (G)MCH supports the Microsoft DirectX Flexible Vertex Format (FVF), which enables the application to specify a variable length of parameter list obviating the need for sending unused information to the hardware. Strips, Fans and Indexed Vertices as well as FVF, improve the vertex rate delivered to the setup engine significantly.

10.4.1.3.2 Pixel Accurate “Fast” Scissoring and Clipping Operation

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets support 2D clipping to a scissor rectangle within the drawing window. Objects are clipped to the scissor rectangle, avoiding processing pixels that fall outside the rectangle. The (G)MCH’s clipping and scissoring in hardware reduce the need for software to clip objects, and thus improve performance. During the setup stage, (G)MCH clips objects to the scissor window.

A scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region than the hardware renders to. The scissor rectangle needs to be pixel accurate, and independent of line and point width. (G)MCH will support a single scissor box rectangle, which can be enabled or disabled. The rectangle is defined as an Inclusive box. Inclusive is defined as “draw the pixel if it is inside the scissor rectangle.”

10.4.1.3.3 Depth Bias

The Mobile Intel 945GM/GME and Intel945GT Express Chipsets support source Depth Biasing in the Setup Engine. Depth Bias value is specified in the vertex command packet on a per primitive basis. The value ranges from -1 to 1. The Depth Bias value is added to the z value of the vertices. This is used for coplanar polygon priority. If two polygons are to be rendered which are coplanar, due to the inherent precision differences induced by unique x, y and z values, there is no guarantee which polygon will be closer or farther. By using Depth Bias, it is possible to offset the destination z value (compare value) before comparing with the new z value.

10.4.1.3.4 B ackface Culling

As part of the setup, the Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets discard polygons from further processing, if they are facing away from or towards the user’s viewpoint. This operation, referred to as “Back Face Culling” is accomplished based on the “clockwise” or “counter-clockwise” orientation of the vertices on a primitive. This can be enabled or disabled by the driver.

10.4.1.3.5 Color Shading Modes

The Raster Engine supports the flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

Flat shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex’s attribute values for the other two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.

OpenGL and D3D use a different vertex to select the flat shaded color. This vertex is defined as the “provoking vertex.” In the case of strips/fans, after the first triangle, attributes on every vertex that define a primitive are used to select the flat color of the primitive. A state variable is used to select the “flat color” prior to rendering the primitive.

Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue). Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has a different value.

All the attributes can be selected independently from one of the shading modes by setting the appropriate value state variables.

10.4.1.4 Rasterizer

Working on a per-polygon basis, the rasterizer uses the vertex and edge information is used to identify all pixels affected by features being rendered.

10.4.1.4.1 Pixel Rasterization Rules

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets support both SGI OpenGL* and D3D pixel rasterization rules to determine whether a pixel is filled by the triangle or line. For both D3D and OpenGL modes, a top-left filling convention for filling geometry will be used. Pixel rasterization rule on rectangle primitive is also supported using the top-left fill convention.

10.4.1.4.2 Pixel Pipeline

The pixel pipeline function combines, for each pixel, the interpolated vertex components from the scan conversion function, texel values from the texture samplers, and the pixel's current values from the color and/or depth buffers. This combination is performed via a programmable pixel shader engine, followed by a pipeline for optional pixel operations performed in a specific order. The result of these operations can be written to the color and depth buffers.

10.4.1.5 2D Functionality

10.4.1.5.1 Block Level Transfer (BLT) Function

The stretch BLT function can stretch source data in the X and Y directions to a destination larger or smaller than the source. The stretch BLT functionality expands a region of memory into a larger or smaller region using replication and interpolation. The stretch BLT function also provides format conversion and data alignment.

10.4.1.6 Texture Engine

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets allow an image, pattern, or video to be placed on the surface of a 3D polygon.

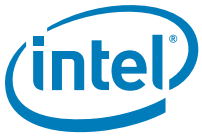
The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the rasterizer. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear and bilinear interpolation), and YUV to RGB conversions.

10.4.1.6.1 Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance.

10.4.1.6.2 Texture Formats and Storage

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets support up to 32 bits of color for textures.



10.4.1.6.3 Texture Decompression

DirectX supports Texture Compression to reduce the bandwidth required to deliver textures. As the textures' average size gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide a mechanism for compressing textures. Texture decompression formats supported include DXT1, DXT2, DXT3, DXT4, DXT5 and FXT1.

10.4.1.6.4 Texture ChromaKey

ChromaKey describes a method of removing a specific color or range of colors from a texture map before it is applied to an object. For "nearest" texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For "linear" texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

10.4.1.6.5 Texture Map Filtering

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets support many texture mapping modes. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets support up to 12 Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. Textures need not be square. Included in the texture processor is a texture cache, which provides efficient MIP-mapping.

The (G)MCH supports 9 types of texture filtering:

- Nearest (Point Filtering): Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present).
- Linear (Bilinear Filtering): A weighted average of a 2x2 area of texels surrounding the desired pixel is used. (This is used if only one LOD is present).
- Nearest MIP Nearest (Point Filtering): This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel is used.
- Linear MIP Nearest (Bilinear MIP Mapping): This is used if many LODs are present. The nearest LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel is used (four texels). This is also referred to as Bilinear MIP Mapping.
- Nearest MIP Linear (Point MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and within each LOD the texel with coordinates nearest to the desired pixel is selected. The Final texture value is generated by linear interpolation between the two texels selected from each of the MIP Maps.
- Linear MIP Linear (Trilinear MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each MIP Map is generated (four texels per MIP Map). The Final texture value is generated by linear interpolation between the two texels generated for each of the MIP Maps. Trilinear MIP Mapping is used minimize the visibility of LOD transitions across the polygon.
- Anisotropic MIP Nearest (Anisotropic Filtering): This is used if many LODs are present. The nearest LOD is determined for up to each of 4 sub-samples for the desired pixel. These four sub-samples are then bilinear filtered and averaged together.

- Anisotropic MIP Linear: Anistropic filtering is performed on the two nearest LODs. The two LOD's are then blended together in a linear fashion
- Anisotropic with only one LOD: The texture map has only one LOD (not MIP-mapped), from which the sampling is done. Anisotropic filtering is then performed on this image.

10.4.1.6.6 Multiple Texture Composition

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets also perform multiple texture composition. This allows the combination of two or greater MIP Maps to produce a new one with new LODs and texture attributes in a single or iterated pass. Flexible vertex format support allows multitexturing because it makes it possible to pass more than one texture in the vertex structure.

10.4.1.6.7 Cubic Environment Mapping

Environment maps allow applications to render scenes with complex lighting and reflections while significantly decreasing CPU load. There are several methods to generate environment maps such as spherical, circular and cubic. The (G)MCH supports cubic reflection mapping over spherical and circular since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

Cubic Mapping requires a texture map for each of the 6 cube faces. These can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction. Per-vertex vectors (normal, reflection or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces is calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.

Multiple texture map surfaces arranged into a cubic environment map is supported. Supports CLAMP and CUBE texture address mode for Cube maps.

A new format is supported for Compressed Cube maps that allow each mip/face to exist in its own compression block.

10.4.1.6.8 Pixel Shader

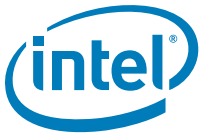
The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets have a Microsoft DirectX9 PS 2.0-compliant Pixel shader. This includes Perspective-correct diffuse and specular color interpolation via internal use of texco-ords. Has also support for non-perspective correct texture coordinates as well as support for Fog parameter separate from Specular Alpha.

10.4.1.6.9 Color Dithering

Color Dithering helps to hide color quantization errors. Color Dithering takes advantage of the human eye's propensity to "average" the colors in a small area. Input color, alpha, and fog components are converted from 5 or 6-bit component to 8-bit components by dithering. Dithering is performed on blended textured pixels with random lower bits to avoid visible boundaries between the relatively discrete 5/6-bit colors. Dithering is not performed on the components in 32-bit mode

10.4.1.6.10 Vertex and Per Pixel Fogging

Fogging is used to create atmospheric effects such as low visibility conditions in flight simulator- type games. It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (fewer polygons), thereby improving the rendering speed or frame rate. Fog is simulated by attenuating the color of an object with the fog color as a function of distance. The higher the density (lower visibility for distant



objects). There are two ways to implement the fogging technique: per-vertex (linear) fogging and per-pixel (non-linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small. With large polygons (such as a ground plane depicting an airport runway), the per-vertex technique results in unnatural fogging.

The (G)MCH supports both types of fog operations, vertex and per pixel or table fog. If fog is disabled, the incoming color intensities are passed unchanged to the destination blend unit.

10.4.1.6.11 Alpha Blending (Frame Buffer)

Alpha Blending adds the material property of transparency or opacity to an object. Alpha blending combines a source pixel color (RSGSBS) and alpha (AS) component with a destination pixel color (RDGDBD) and alpha (AD) component. For example, this is so that a glass surface on top (source) of a red surface (destination) would allow much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha are supported.

10.4.1.6.12 Microsoft DirectX* and SGI OpenGL* Logic Ops

Both APIs provide a mode to use bitwise ops in place of alpha blending. This is used for rubber- banding, i.e., draw a rubber band outline over the scene using an XOR operation. Drawing it again restores the original image without having to do a potentially expensive redraw.

10.4.1.6.13 Color Buffer Formats: 8, 16, or 32 Bits per Pixel (Destination Alpha)

The raster engine will support 8-, 16-, and 32-bit color buffer formats. The 8-bit format is used to support planar YUV420 format, which used only in Motion Compensation and Arithmetic Stretch format. The bit format of Color and Z will be allowed to mix.

The (G)MCH supports both double and triple buffering, where one buffer is the primary buffer used for display and one or two are the back buffer(s) used for rendering.

The frame buffer of the (G)MCH contains at least two hardware buffers: the Front Buffer (display buffer) and the Back Buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible (via an instruction) or copied to the front buffer (via a 2D BLT operation). Rendering to one and displaying from the other remove the possibility of image tearing. This also speeds up the display process over a single buffer. Additionally, triple back buffering is also supported. The instruction set of the (G)MCH provides a variety of controls for the buffers (e.g., initializing, flip, clear, etc.).

10.4.1.6.14 Depth Buffer

The raster engine will be able to read and write from this buffer and use the data in per fragment operations that determine whether resultant color and depth value of the pixel for the fragment are to be updated or not.

Typical applications for entertainment or visual simulations with exterior scenes require far/near ratios of 1000 to 10000. At 1000, 98% of the range is spent on the first 2% of the depth. This can cause hidden surface artifacts in distant objects, especially when using 16-bit depth buffers. A 24-bit Z-buffer provides 16 million Z-values, as opposed to only 64 K with a 16-bit Z buffer.

10.4.1.6.15 Stencil Buffer

The Raster Engine will provide 8-bit stencil buffer storage in 32-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis, conditionally eliminating a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects, such as decals, outlining, shadows and constructive solid geometry rendering.

10.4.1.6.16 2D Engine

The (G)MCH contains BLT functionality, and an extensive set of 2D instructions. To take advantage of the 3D drawing engine's functionality, some BLT functions such as Alpha BLTs, arithmetic (bilinear) stretch BLTs, rotations, transposing pixel maps, limited color space conversion, and DIBs make use of the 3D renderer.

10.4.1.6.17 Mobile Intel 945GM/GME and Intel 945GT Express Chipset VGA Registers

The 2D registers are a combination of registers for the original the Video Graphics Array (VGA) and others that Intel has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

10.4.1.6.18 Logical 128-Bit Fixed BLT and 256 Fill Engine

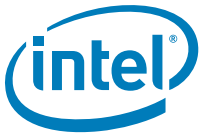
Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows* operating systems. The 128-bit (G)MCH BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8, 16, or 32 bits per pixel.

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset BLT engine has the ability to expand monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the (G)MCH can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.



The (G)MCH has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The (G)MCH can perform hardware clipping during BLTs.

10.4.1.7 Video Engine

10.4.1.7.1 Hardware Motion Compensation

The Motion Compensation (MC) process consists of reconstructing a new picture by predicting (either forward, backward or bidirectionally) the resulting pixel colors from one or more reference pictures. The (G)MCH receives the video stream and implements Motion Compensation and subsequent steps in hardware. Performing Motion Compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

The Motion Compensation functionality is overloaded onto the texture cache and texture filter. The texture cache is used to typically access the data in the reconstruction of the frames and the filter is used in the actual motion compensation process. To support this overloaded functionality the texture cache additionally supports the following input format: YUV420 planar

10.4.1.7.2 4-Channel MPEG YUV

The peformance of present generation IGD is significantly faster than that of the previous generations.

10.4.1.7.3 Sub-Picture Support

Sub-picture is used for two purposes, one is Subtitles for movie captions, etc. (which are superimposed on a main picture), and Menus used to provide some visual operation environments the user of a content player.

DVD allows movie subtitles to be recorded as Sub-pictures. On a DVD disc, it is called “Subtitle” because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for Subtitles, they can be used for various applications, for example, as Subtitles in different languages or other information to be displayed.

There are two kinds of Menus, the System Menus and other In-Title Menus. First, the System Menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title menus can be programmed as a combination of Sub-picture and Highlight commands to be displayed during playback of the disc.

The (G)MCH supports sub-picture for DVD and DBS by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The (G)MCH can utilize four methods when dealing with sub-pictures. The flexibility enables the (G)MCH to work with all sub- picture formats.

10.4.1.7.4 De-interlacing Support

For display on a progressive computer monitor, interlaced data that has been formatted for display on interlaced monitors (TV), needs to be de-interlaced. The simple approaches to de-interlacing create unwanted display artifacts. More advanced de-interlacing techniques have a large cost associated with them. The compromise solution is to provide a low cost but effective solution and enable both hardware and software based external solutions. Software based solutions are enabled through a high bandwidth transfer to system memory and back.

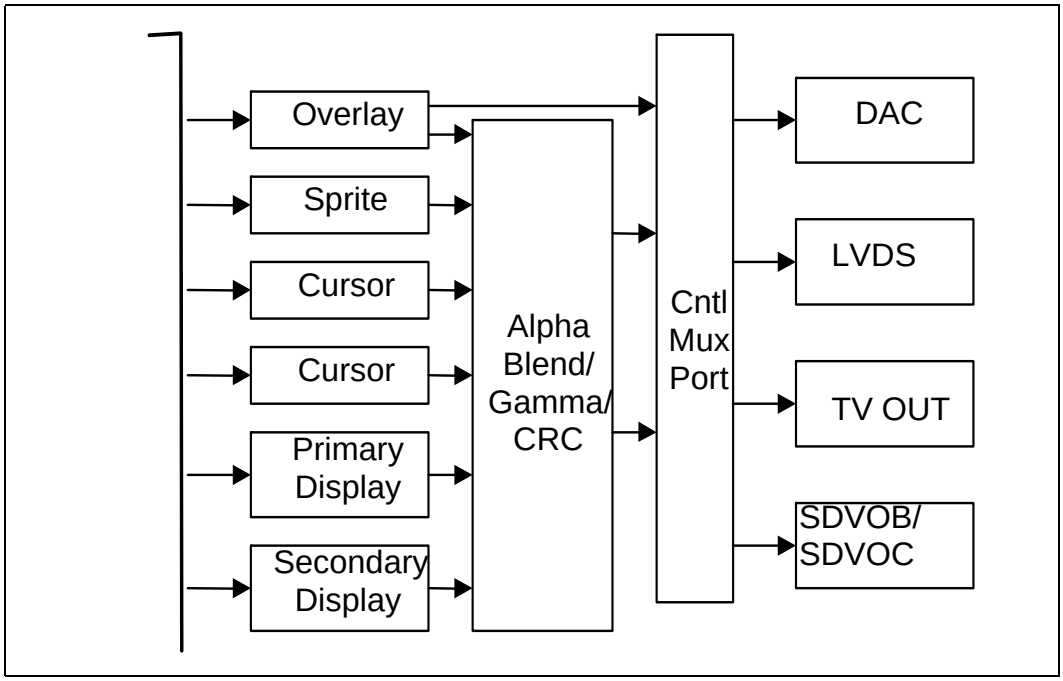
10.4.1.7.5 Advanced Deinterlacing and Dynamic Bob and Weave

Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. There are several schemes to deinterlace the video stream: line replication, vertical filtering, field merging and vertical temporal filtering. Field merging takes lines from the previous field and inserts them into the current field to construct the frame – this is known as Weaving. This is the best solution for images with little motion however, showing a frame that consists of the two fields will have serration or feathering of moving edges when there is motion in the scene. Vertical filtering or “Bob” interpolates adjacent lines rather replicating the nearest neighbor. This is the best solution for images with motion however, it will have reduced spatial resolution in areas that have no motion and introduces jaggies. In absence of any other deinterlacing, these form the baseline and are supported by the (G)MCH.

10.5 Display Interfaces

The display is the defining portion of a graphics controller. The display converts a set of source images or surfaces, combines them and sends them out at the proper timing to an output interface connected to a display device. Along the way, the data can be converted from one format to another, stretched or shrunk, and color corrected or gamma converted.

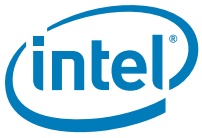
Figure 21. Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset Display Pipe Block Diagram



10.5.1 Display Overview

The IGD display can be broken down into three components:

- Display Planes
- Display Pipes
- Display Ports



10.5.2 Planes

The (G)MCH contains a variety of planes, such as VGA, Cursor, Overlay, Sprite, Primary and Secondary. A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular areas in memory with a similar set of characteristics. They are also associated with a particular destination pipe.

10.5.2.1 Display Plane

The primary and secondary display plane works in an indexed mode, hi-color mode or a true color mode. The true color mode allows for an 8-bit alpha channel. One of the primary operations of the display plane is the set mode operation. The set-mode operation occurs when it is desired to enable a display, change the display timing, or source format. The secondary display plane can be used as a primary surface on the secondary display or as a sprite planes on either the primary or secondary display.

10.5.2.2 Cursor Plane

The cursor plane is one of the simplest display planes. With a few exceptions, the cursor plane supports sizes of 64 x 64, 128 x 128 and 256 x 256 fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted.

10.5.2.3 VESA / VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. VGA Timings are generated based on the VGA register values (the Hi-res timing generator registers are not used).

10.5.2.3.1 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing Plug and Play systems to be realized. Support for DDC 1 and 2 is implemented. the Mobile Intel 945GM/GME/PM/GMS/GSE, 943/940GML and Intel 945GT Express Chipsets use the CRTDDCCLK and CRTDDCDATA signals to communicate with the analog monitor. These signals are generated at 2.5 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The (G)MCH implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 1 MHz.

10.5.2.4 Overlay Plane

The overlay engine provides a method of merging either video capture data (from an external Video Capture device) or data delivered by the CPU, with the graphics data on the screen. The source data can be mirrored horizontally or vertically or both.

10.5.2.4.1 Source / Destination Color Keying / ChromaKeying

Overlay source/destination ChromaKeying enables blending of the overlay with the underlying graphics background. Destination color keying/ChromaKeying can be used to handle occluded portions of the overlay window on a pixel by pixel basis that is actually an underlay. Destination ChromaKeying would only be used for YUV pass through to TV. Destination color keying supports a specific color (8- or 15-bit) mode as well as 32-bit alpha blending.

Source color keying/ChromaKeying is used to handle transparency based on the overlay window on a pixel by pixel basis. This is used when “blue screening” an image to overlay the image on a new background later.

10.5.2.4.2 Gamma Correction

To compensate for overlay color intensity loss due to the non-linear response between display devices, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

10.5.2.4.3 YUV to RGB Conversion

The format conversion can be bypassed in the case of RGB source data. The format conversion assumes that the YUV data is input in the 4:4:4 format and uses the full range scale.

10.5.3 Display Pipes

The display consists of two pipes:

- Display Pipe A
- Display Pipe B

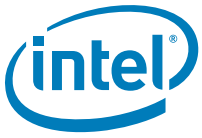
A pipe consists of a set of combined planes and a timing generator. The timing generators provide the basic timing information for each of the display pipes. The (G)MCH has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe.

Pipe A can operate in a single-wide or “double-wide” mode. In double-wide mode, the pipe transfers data at 2x graphics core clock though it is effectively limited by the perspective display port. The display planes and the cursor plane will provide a “double wide” mode to feed the pipe.

10.5.3.1 Clock Generator Units (DPLL)

The clock generator units provide a stable frequency for driving display devices. It operates by converting an input reference frequency into an output frequency. The timing generators take their input from internal DPLL devices that are programmable to generate pixel clocks in the range of 25-350 MHz. Accuracy for VESA timing modes is required to be within ± 0.5%.

The DPLL can take a reference frequency from the external reference input (DREFCLKINN/P), or the TV clock input (TVCLKIN).



10.5.4 Display Ports

Display ports are the destination for the display pipe. These are the places where the data finally appears to devices outside the graphics device. The (G)MCH has one dedicated CRT display port (Analog), one TV out port (Analog), one LVDS port (Digital), and two SDVO ports (Digital).

Table 37. Display Port Characteristics

Interface Protocol		(Analog)	LVDS	Port B (Digital) SDVO 1.0	Port C (Digital)
		RGB DAC	LVDS		SDVO 1.0
SIGNALS	HSYNC	Yes Enable/ Polarity	Encoded during blanking codes		
	VSYNC	Yes Enable/ Polarity	Encoded during blanking codes		
	BLANK	No	No	Encoded	Encoded
	STALL	No	No	Yes	Yes
	Field	No	No	No	No
	Display_Enable	No	Yes(1)	Encoded	Encoded
Image Aspect Ratio		Programmable and typically 1.33:1 or 1.78:1			
Pixel Aspect Ratio		Square(1)	Square		
Voltage		RGB 0.7V p-p	1.2 VDC 300 mV p-p	Scalable 1.x V	
Clock		NA	7x Differential (Dual-channel) 3.5x Differential (Single-channel)		
Max Rate		350 Mpixel	224 MPixel (Dual-channel) 112 mpIXEL (Single-channel)	200 Mpixel	
Format		Analog RGB	Multiple 18 bpp	RGB 8:8:8 YUV 4:4:4	
Control Bus		DDC1	Optional DDC	GMBUS	
External Device		No	No	TMDS/LVDS Transmitter /TV Encoder	
Connector		VGA/DVI-		DVI/CVBS/S-Video/Component/SCART	

NOTE:
1. Single signal software selectable between display enable and Blank#

10.5.4.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality has been added to the signals to enhance that capability.

Table 38. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	2.5 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5V
	Control	Through GPIO interface

10.5.4.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. (G)MCH's integrated 400 MHz RAMDAC supports resolutions up to 2048 x 1536. Three 8-bit DACs provide the R, G, and B signals to the monitor.

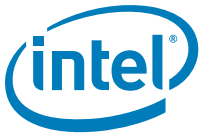
10.5.4.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.

10.5.4.2 Dedicated LFP LVDS Port

The display pipe selected by the LVDS display port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then "locked" into the registers to prevent unwanted corruption of the values. From that point on, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA. The timing signals will remain stable and active through mode changes. These mode changes include VGA to VGA, VGA to HiRes, HiRes to VGA, and HiRes to HiRes.

The transmitter can operate in a variety of modes and supports several data formats. The serializer supports 6-bit color and Single- or Dual-channel operating modes. The display stream from the display pipe is sent to the LVDS transmitter port at the dot



clock frequency, which is determined by the panel timing requirements. The output of LVDS is running at a fixed multiple of the dot clock frequency, which is determined by the mode of operation; single- or dual-channel.

Depending on configuration and mode, a single channel can take 18 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on three differential data pair outputs. A dual-channel interface converts 36 bits of color information plus the 3 bits of timing control and outputs it on six sets of differential data outputs.

This display port is normally used in conjunction with the pipe functions of panel scaling and 6-to 8-bit dither. This display port is also used in conjunction with the panel power sequencing and additional associated functions.

When enabled, the LVDS constant current drivers consume significant power. Individual pairs or sets of pairs can be selected to be powered down when not being used. When disabled, individual or sets of pairs will enter a low power state. When the port is disabled all pairs enters a low power mode. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

10.5.4.2.1 LVDS Panel Support

Table 39. LVDS Panel Support at 60 Hz

LVDS Panel (Express Chipset)	SXGA+ (1400 x 1050)	UXGA (1600 x 1200)	QXGA 2048x1536
945GT (@1.5 V core)	Y	Y	Y
945GM/GME	Y	Y	N
945GMS/GSE	Y	Y	N
940GML	Y	N	N
943GML	Y	N	N

NOTE:
1. It is recommended to use the OEM Modes Program (OMP) Tool to determine the capabilities of each variant for resolutions and refresh rates not included here.

Note: The Ultra Mobile Intel 945GU Express Chipset supports up to XGA (1024 x 768) internal and SXGA (1280 x 1024) external.

Note: The Ultra Mobile Intel 945GU Express Chipset supports 25 MHz - 112 MHz single channel; @18 bpp.

10.5.4.2.2 LVDS Interface Signals

LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics. There are two LVDS transmitter channels (channel A and channel B) in the LVDS interface. Each channel consists of 3-data pairs and a clock pair. The interface consists of a total of eight differential signal pairs of which six are data and two are clocks. The phase locked transmit clock is transmitted in parallel with the data being sent out over the data pairs and over the LVDS clock pair.

Each channel supports transmit clock frequency ranges from 25 MHz to 112 MHz, which provides a throughput of up to 784 Mbps on each data output and up to 112 MP/s on the input. When using both channels, they each operate at the same frequency each carrying a portion of the data. The maximum pixel rate is increased to 224 MP/s but may be limited to less than that due to restrictions elsewhere in the circuit.

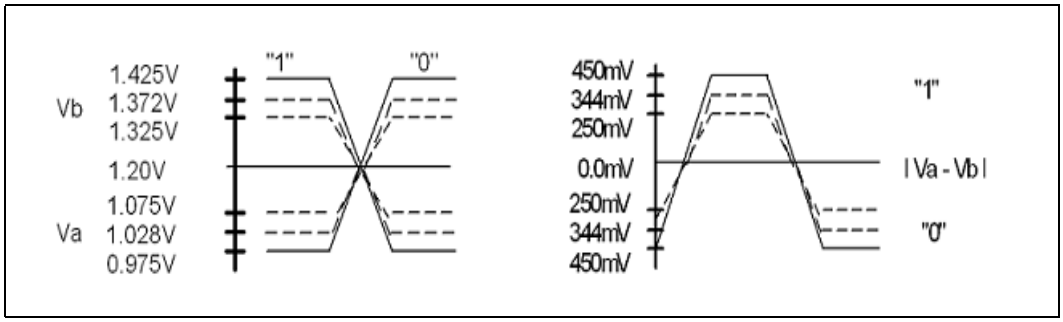
The LVDS Port enable bit enables or disables the entire LVDS interface. When the port is disabled, it will be in a low power state. Once the port is enabled, individual driver pairs will be disabled based on the operating mode. Disabled drivers can be powered down for reduced power consumption or optionally fixed to forced 0's output.

10.5.4.2.3 LVDS Data Pairs and Clock Pairs

The LVDS data and clock pairs are identical buffers and differ only in the use defined for that pair. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals. The pixel bus data to serial data mapping options are specified elsewhere. A single- or dual-clock pair is used to transfer clocking information to the LVDS receiver. A serial pattern of 1100011 represents one cycle of the clock.

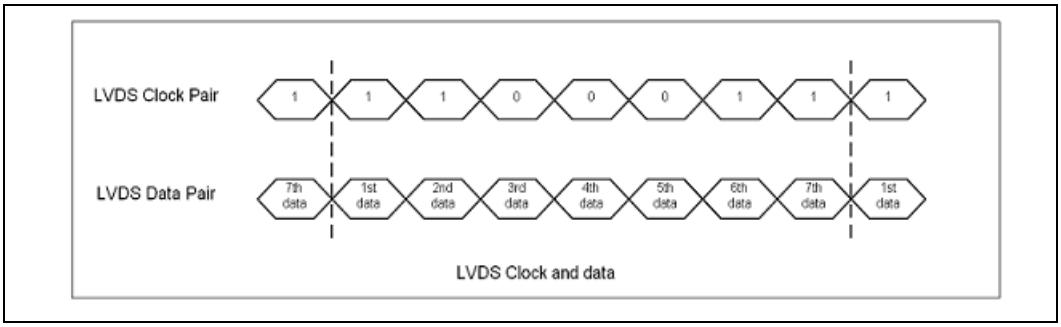
There are two LVDS transmitter channels (channel A and channel B) in the LVDS interface. Each channel contains 1 clock pair and 3-data pair of low voltage differential swing signals. Figure 22 shows a pair of LVDS signals and swing voltage.

Figure 22. LVDS Signals and Swing Voltage



1's and 0's are represented the differential voltage between the pair of signals.

Figure 23. LVDS Clock and Data Relationship



10.5.4.2.4 LVDS Pair States

The LVDS pairs can be put into one of five states, powered down tri-state, powered down 0 V, common mode, send 0's, or active. When in the active state, several data formats are supported. When in powered down state, the circuit enters a low power state and drives out 0 V or tri-states on both the output pins for the entire channel. The common mode tri-state is both pins of the pair set to the common mode voltage. These are the signals that optionally get used when driving either 18-bpp panels or dual-channel with a single clock. When in the send 0's state, the circuit is powered up but sends only 0 for the pixel color data regardless what the actual data is with the clock lines and timing signals sending the normal clock and timing data.

10.5.4.2.5 Single-channel versus Dual-channel Mode

Both Single-channel and Dual-channel modes are available to allow interfacing to either Single- or Dual-channel panel interfaces. This LVDS port can operate in Single-channel or Dual-channel mode. Dual-channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single-channel. In general, one channel will be used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel will be sent out channel A. All horizontal timings for active, sync, and blank will be limited to be on two pixel boundaries in the two channel modes.

10.5.4.2.6 LVDS Channel Skew

When in Dual-channel mode, the two channels must meet the panel requirements with respect to the inter channel skew.

10.5.4.2.7 LVDS PLL

The Display PLL is used to synthesize the clocks that control transmission of the data across the LVDS interface. The three operations that are controlled are the pixel rate, the load rate, and the IO shift rate. These are synchronized to each other and have specific ratios based on Single-channel or Dual-channel mode. If the pixel clock is considered the 1x rate, a 7x or 3.5 speeds IO_shift clock needed for the high speed serial outputs setting the data rate of the transmitters. The load clock will have either a 1x or 0.5x ratio to the pixel clock.

10.5.4.3 Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. In order to meet the panel power timing specification requirements, two signals, PANELVDDEN and PANELBKLTEN are provided to control the timing sequencing function of the panel and the backlight power supplies.

10.5.4.3.1 Panel Power Sequence States

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

A requested power-up sequence is only allowed to begin after the power cycle delay time requirement T4 is met.

Figure 24. Panel Power Sequencing

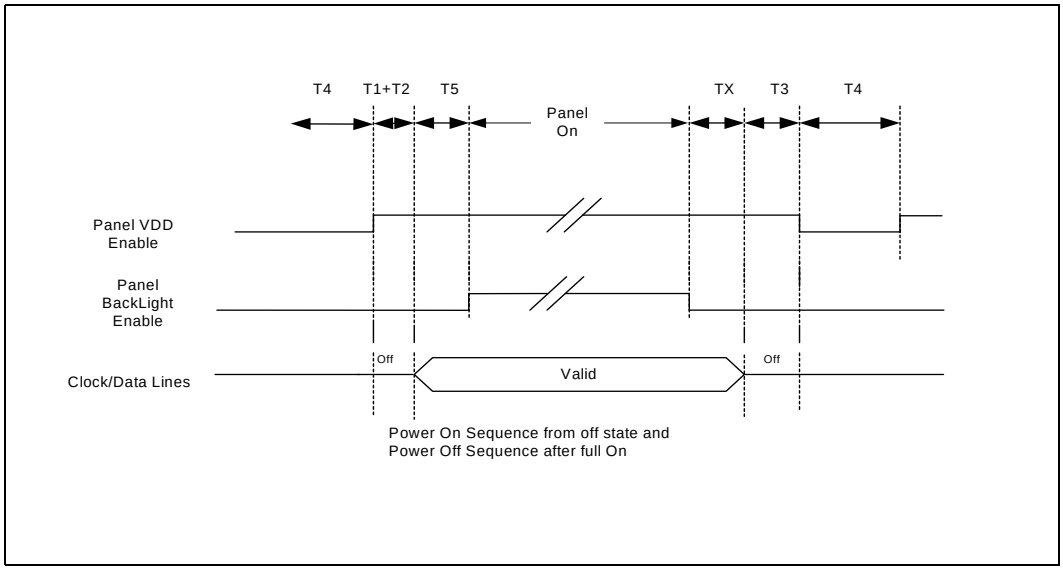


Table 40. Panel Power Sequencing Timing Parameters

Panel Power Sequence Timing Parameters			Min	Max	Name	Units
Spec Name	From	To				
Vdd On	0.1 Vdd	0.9 Vdd	0	100	T1	ms/10
LVDS Active	Vdd Stable On	LVDS Active	0	500	T2	ms/10
Backlight	LVDS Active	Backlight on	200		T5	ms
Backlight State	Backlight Off	LVDS off	X	X	TX	ms
LVDS State	LVDS Off	Start power off	0	50	T3	ms
Power cycle Delay	Power Off	Power On Sequence Start	0	400	T4	ms

10.5.4.4 SDVO Digital Display Port

10.5.4.4.1 SDVO

Intel SDVO ports can support a variety of display types – LVDS, DVI, TV-Out, etc, and external CE type devices. The (G)MCH utilizes an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings.

10.5.4.4.2 SDVO DVI

DVI, a 3.3 V flat panel interface standard, is a prime candidate for SDVO. The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets provide unscaled mode where the display is centered on the panel.

Monitor Hot Plug functionality is supported for TMDS devices.

Note: Hot Plug is not supported on the Ultra Mobile Intel 945GU Express Chipset.

10.5.4.4.3 SDVO LVDS

The Mobile Intel 945GM/GME/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets may use the SDVO port to drive an LVDS transmitter. Flat Panel is a fixed resolution display. The (G)MCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The (G)MCH will however, provide unscaled mode where the display is centered on the panel. Scaling in the LVDS transmitter through the SDVO stall input pair is also supported.

10.5.4.4.4 SDVO TV-Out

The SDVO port supports both standard and high-definition TV displays in a variety of formats. The SDVO port generates the proper blank and sync timing, but the external encoder is responsible for generation of the proper format signal and output timings.

(G)MCH will support NTSC/PAL/SECAM standard definition formats. The (G)MCH will generate the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal.

The TV-out interface on (G)MCH is addressable as a master device. This allows an external TV encoder device to drive a pixel clock signal on SDVO_TVCLKIN[+/-] that the (G)MCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.

10.5.4.4.5 Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing will be generated with pixel granularity to allow more overscan ratios to be supported.

10.5.4.4.6 Direct YUV from Overlay

When source material is in the YUV format and is destined for a device that can take YUV format data in, it is desired to send the data without converting it to RGB. This avoids the truncation errors associated with multiple color conversion steps. The common situation will be that the overlay source data is in the YUV format and will bypass the conversion to RBG as it is sent to the TV port directly.

10.5.4.4.7 Analog Content Protection

Analog content protection may be provided through the external encoder.

10.5.4.4.8 Connectors

Target TV connector support includes the CVBS, S-Video, Analog Component (Y Pb Pr), and SCART connectors. The external TV encoder will determine the method of support.

10.5.4.4.9 Control Bus

The SDVO port defines a two-wire communication path between the SDVO device(s) and (G)MCH. Traffic destined for the PROM or DDC will travel across the Control bus, and will then require the SDVO device to act as a switch and direct traffic from the Control bus to the appropriate receiver. Additionally, the Control bus is able to operate at up to 1 MHz.

10.5.5 Multiple Display Configurations

Since the (G)MCH has several display ports available for its two pipes, it can support up to two different images on different display devices. Timings and resolutions for these two images may be different. The (G)MCH is incapable of operating in parallel with an external PCI Express graphics device. The (G)MCH can, however, work in conjunction with a PCI graphics adapter.

10.6 Power Management

10.6.1 Overview

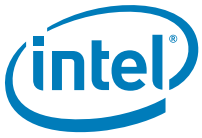
- ACPI 1.0b and 2.0 Compliant
- ACPI S0, S3, S4, S5
- CPU States C0, C1, C2, C3, C4 states
- Internal Graphics Display Device States: D0, D1, D3
- Graphics Display Adapter States: D0, D3.
- PCI Express Link States: L0, L0s, L1, L2, L3
- HSLPCPU# output
- Dual Frequency Graphics Technology
- Dynamic I/O power reductions

10.6.2 ACPI States Supported

The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset family supports the following ACPI states:

10.6.2.1 System

G0/S0	Full On
G1/S1	Not supported.
G1/S2	Not supported.
G1/S3-Cold	Suspend to RAM (STR). Context saved to memory.
G1/S3-Hot	Suspend to RAM (STR). All voltage supplies except the CPU Core and FSB VTT left enabled
G1/S4	Suspend to Disk (STD). All power lost (except wakeup on ICH)
G2/S5	Soft off. All power lost (except wakeup on ICH). Total reboot.
G3	Mechanical off. All power (AC and battery) removed from system.



10.6.2.2 CPU

C0	Full On
C1	Auto Halt
C2	Stop Clock. Clock stopped to CPU core.
C3	Deep Sleep. Clock to CPU stopped.
C4	Deeper Sleep. Same as C3 with reduced voltage on the CPU.

10.6.2.3 Internal Graphics Display Device Control

D0	Display Active
D1	Low power state, low latency recovery, Standby display
D3	Power off display

10.6.2.4 Internal Graphics Adapter

D0	Full on, Display Active
D3 Hot	Graphics clocks off and display inactive as much as possible
D3 Cold	Power off

10.6.3 Interface Power States Supported

10.6.3.1 PCI Express Link States

L0	Full on – Active Transfer State
L0s	First Active Power Management low power state – Low exit latency
L1	Lowest Active Power Management - Longer exit latency
L2/L3 Ready	Lower link state with power applied – Long exit latency
L3	Lowest power state (power off) – Longest exit latency

10.6.3.2 Main Memory States

Power up	CKE Asserted. Active Mode
Precharge Power down	CKE deasserted (not self-refresh) with all banks closed
Active Power down	CKE deasserted (not self-refresh) with min. one bank active
Self-Refresh	CKE deasserted using device self-refresh

10.6.4 Power Management Overview

10.6.4.1 Dynamic Power Management on I/O

(G)MCH provides several features to reduce I/O power dynamically.

10.6.4.1.1 System Memory

- dynamic rank power down
- Conditional memory self-refresh based on CPU state, PCI Express link states, and graphics/display activity
- Dynamic ODT disable when MCH is driving
- DPWR# signal to disable CPU sense amps when no read return data pending

10.6.4.1.2 PCI Express

- Active power management support using L0, L0s, and L1 states
- All inputs and outputs disabled in L2/L3 Ready state

10.6.4.2 System Memory Power Management

The main memory is power managed during normal operation and in low power ACPI Cx states.

Each row has a separate CKE (clock enable) pin that is used for power management.

dynamic rank power down is employed during normal operation. Based on idle conditions to a given row of memory that memory row may be powered down. If the pages for a row have all been closed at the time of power down, then the device will enter the active power down state. If pages remain open at the time of power down the devices will enter the precharge power down state.

10.6.4.2.1 Disabling Unused System Memory Outputs

Any System Memory interface signal that goes to a SO-DIMM connector in which it is not connected to any actual memory devices (such as SO-DIMM connector is unpopulated, or is single-sided) will be tri-stated.

The benefits of disabling unused SM signals are:

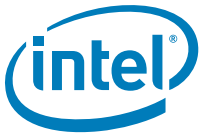
- Reduce Power Consumption
- Reduce possible overshoot/undershoot signal quality issues seen by the (G)MCH I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given row is not populated (as determined by the DRAM rank boundary register values) then the corresponding chip select and SCKE signals will not be driven.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

10.6.4.2.2 Dynamic Row Power Management

Dynamic row power-down is employed during normal operation. Based on idle conditions, a given memory row may be powered down. If the pages for a row have all been closed at the time of power down, then the device will enter the precharge power-down state. If pages remain open at the time of power-down the devices will enter the active power-down state.



10.6.4.2.3 Conditional Self-Refresh

The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets support a conditional self-refresh entry in the C3 and C4 states, based on the graphics/display (if internal graphics is being used) and (optionally) on the state of the PCI Express links.

The dependency on PCI Express link state is configurable, but the target behavior is to enter self-refresh for C3/C4 as long as there as no memory requests to service.

Though the dependencies on this behavior are configurable, the target usage is shown in the table below.

Table 41. Targeted Memory State Conditions

Mode	Memory State with Internal Graphics	Memory State with External Graphics
C0, C1	Dynamic memory row power down based on idle conditions	Dynamic memory row power down based on idle conditions
C2, C3, C4	Dynamic memory row power down based on idle conditions If all PCI Express* links are in L1 and the graphics engine is idle, the (G)MCH enters self-refresh for C3 and C4 states. Otherwise, it enters dynamic memory row power down mode based on idle conditions	Dynamic memory row power down based on idle conditions If all PCI Express links are in L1 and the graphics engine is idle the chipset enters self-refresh. Otherwise, it enters dynamic memory row power down mode based on idle conditions
S3/S3-Hot	Self Refresh Mode	Self Refresh Mode
S4	Memory power down (contents lost)	Memory power down (contents lost)

10.6.5 Chipset State Combinations

(G)MCH supports the state combinations listed in the Table 42 and Table 43.

Table 42. G, S and C State Combinations

Global (G) State	Sleep (S) State	CPU (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1	Auto-Halt	On	Auto Halt
G0	S0	C2	Stop Grant	On	Stop Grant
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C4	Deeper Sleep	On	Deep Sleep with CPU voltage lowered.
G1	S3-Cold	power off		Off, except RTC	Suspend to RAM
G1	S3-Hot	power off		Off, except RTC	Suspend to RAM – MCH power enabled
G1	S4	power off		Off, except RTC	Suspend to Disk
G2	S5	power off		Off, except RTC	Soft Off
G3	NA	power off		power off	Hard Off

Table 43. D, S, and C State Combinations

Graphics Adapter (D) State	Sleep (S) State	CPU (C) State	
D0	S0	C0	Full On, Displaying.
D0	S0	C1	Auto-Halt, Displaying
D0	S0	C2	Quick Start, Displaying
D0	S0	C3	Deep Sleep, Displaying
D0	S0	C4	Deeper Sleep, Displaying
D1	S0	C0-2	Not Displaying
D1	S0	C3	Not Displaying
D3	S0	C0-2/ C3/C4	Not Displaying
D3	S3	---	Not Displaying (G)MCH may power off
D3	S4	---	Not Displaying Suspend to disk

10.6.5.1 CPU Sleep (HCPUSLP#) Signal Definition

The CPU's sleep signal (SLP#) reduces power in the CPU by gating off unused clocks. Unlike earlier configurations, this signal can be driven only by the (G)MCH's HCPUSLP# signal. Moving this ability to the (G)MCH allows dynamic use of the SLP# signal during the CPU's C2 state to reduce CPU power further while not performing snoops during C2. Since the ICH is unaware of the snoop operations being done by the (G)MCH, the HCPUSLP# signal was only asserted during the C3 states and below.

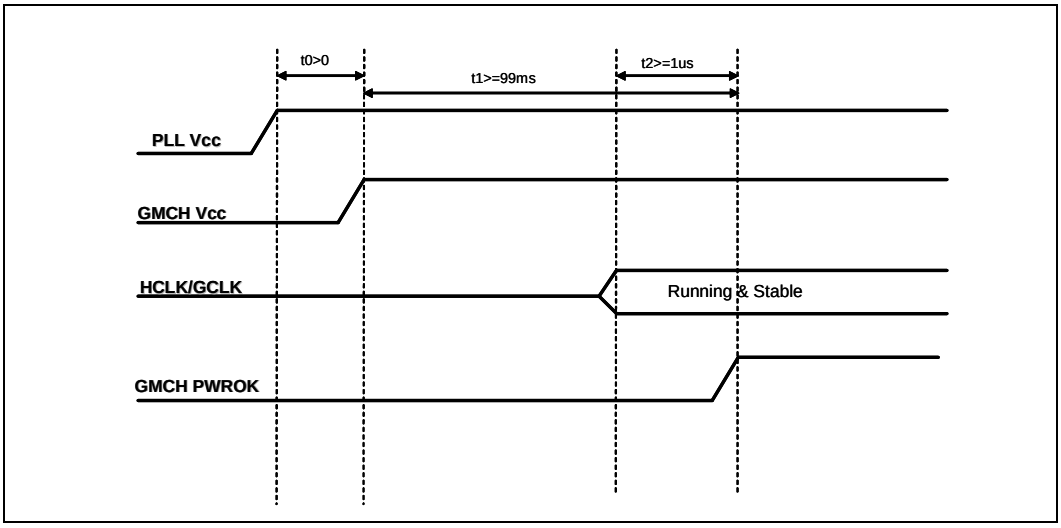
The (G)MCH host interface controller will ensure that no transactions will be initiated on the FSB without having first met the required timing from the SLP# deassertion to the assertion of BPRI#. This time is programmable from 0 to 31 clocks (8-clock default).

(G)MCH will control HCPUSLP# and enforce the configured timing rules associated with this. This allows the (G)MCH to enforce the timing of the SLP# deassertion to BPRI# assertion during C3 to C2 or C3 to C0 transitions.

10.6.6 PWROK Timing Requirements for Power-up, Resume from S3-Cold and S3-Hot

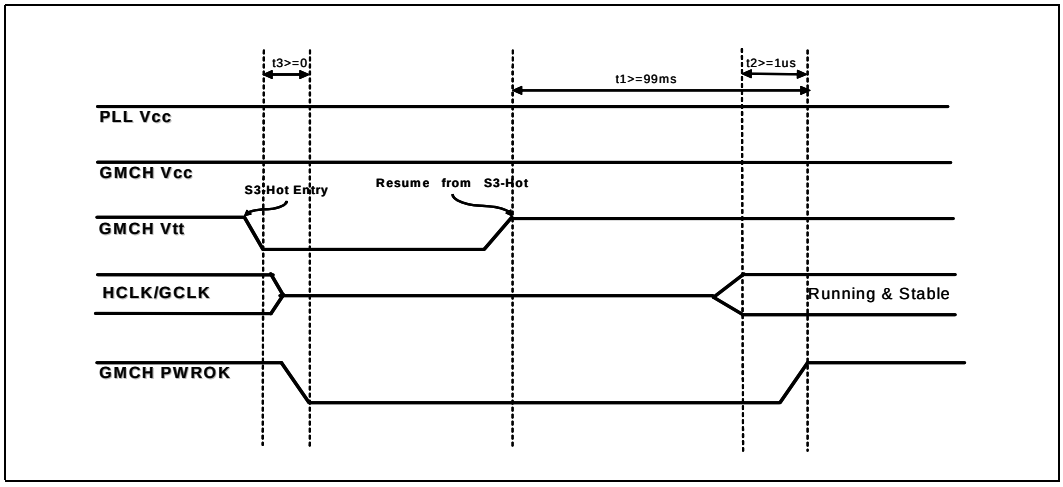
The diagrams below highlight the timing requirements for the (G)MCH PWROK signal for Power-up, resume from S3-Cold and S3-Hot:

Figure 25. Upon Power-up and Resume from S3-Cold



NOTE:
1. Timings t1, t2 apply for both Power-up and Resume from S3-Cold events.
2. t1: All (G)MCH power supplies should be valid at least 99ms before PWROK assertion.
3. t2: (G)MCH clocks should be running and stable at least 1us before PWROK assertion.

Figure 26. Upon Resume from S3-Hot



NOTE:
1. Pwrok **should** be disabled when in S3-Hot.
2. PLL Vcc and (G)MCH Vcc are ON in S3-hot, with only (G)MCH Vtt disabled.
3. t1: All (G)MCH power supplies should be valid at least 99ms before PWROK assertion.
4. t2: (G)MCH clocks should be running and stable at least 1us before PWROK assertion.

10.6.7 External Thermal Sensor PM_EXTTS1#: Implementation for Fast C4/C4E Exit

This is an alternate functionality for the EXTTS1# signal, on the Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset family. This implementation enables power savings by speeding up the C4 exit latency. To enable power savings, the PM_EXTTS1# of the (G)MCH and the DPSLPVR signal of should be connected as shown in Figure 27 below. The DPRSLPVR signal of the ICH needs to be connected to the DPRSLPVR signal of the IMVP6 via a 500-Ω series isolation resistor. The pull-up on the PM_EXTTS1# signal should be removed in this particular implementation.

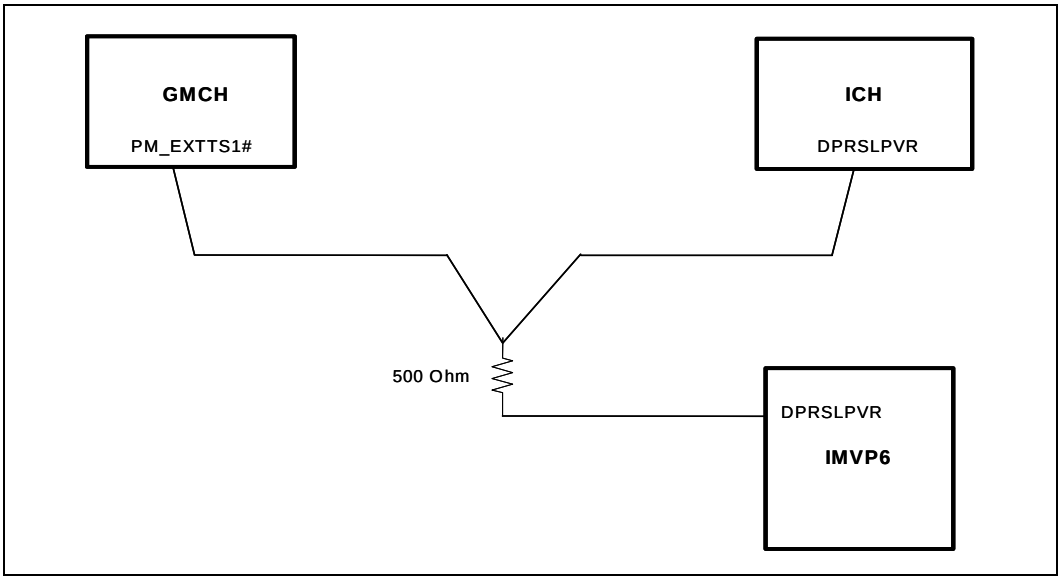
This implementation enables power-savings by increasing average C-state residency of the Intel Core Duo and Intel Core Solo processor (The probability of the CPU going into C4/C4E state increases if the exit latency is reduced).

With this implementation, PM_EXTTS1# **cannot** be used for thermal throttling of Memory. If this implementation is chosen, system designers shall need to ensure that the memory Auto-refresh rate programmed on their systems is the most appropriate for their thermal solution and choice of memory.

Intel strongly recommends the implementation described above, to enable greater power savings on Intel Centrino Duo technology. For details of the recommended routing topologies and guidelines, please contact your Intel Field Representative.

Note: EXTTS0# cannot be used in this manner. For details on the conventional use of the EXTTS1# signal see Section 10.7.2

Figure 27. EXTTS1# Implementation for Fast C4/C4E Exit



10.6.8 Aux0 Trip on EXTTS0#

With Fast C4/C4E Exit implemented, the EXTTS1# pin no longer functions as an external thermal sensor event. This functionality is now available on the EXTTS#0 pin via BIOS option. Please see register EXTTSCS; MCHBAR Offset CFFh and register ECO; MCHBAR Offset FFCh.

Note: EXTTS0# will not support Hot or Catastrophic trip points if Aux0 Trip on EXTTS0# is enabled.

10.6.9 CLKREQ# - Mode of Operation

The CLKREQ# signal is driven by the (G)MCH to control the PCIe clock to the External Graphics and the DMI clock. When both the DMI and PCIe links (if supported) are in L1, with CPU in C3/C4/C4e state, the (G)MCH deasserts CLKREQ# to the clock chip, allowing it to gate the GCLK differential clock pair to the (G)MCH, in turn disabling the PCIe and DMI clocks inside the (G)MCH.
The following requirements must be met for the (G)MCH to support CLKREQ# functionality:

- ASPM is enabled on the platform
- Bit 19 of UPMC3 set to 1

10.7 Thermal Management

System level thermal management requires comprehending thermal solutions for two domains of operation:

1. Robust Thermal Solution Design: Proper system design should include implementation of a robust thermal solution. The system's thermal solution should be capable of dissipating the platform's TDP power while keeping all components (particularly (G)MCH, for the purposes of this discussion) below the relevant Tdie_max under the intended usage conditions. Such conditions include ambient air temperature and available airflow inside the notebook.
2. Thermal Failsafe Protection Assistance: As a backup to the implemented thermal solution, the system design should provide a method to provide additional thermal protection for the components of concern (particularly (G)MCH, for purposes of this discussion). The failsafe assistance mechanism is to help manage components from being damaged by excessive thermal stress under situations in which the implemented thermal solution is inadequate or has failed.

This chapter covers the thermal failsafe assistance mechanisms that are available for the (G)MCH and recommends a usage model designed to accomplish the failsafe Protection Assistance.

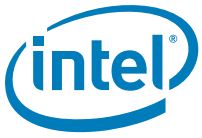
The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets provide two internal thermal sensors, plus hooks for an external thermal sensor mechanism. These can be used for detecting the component temperature and for triggering thermal control within the (G)MCH. The (G)MCH has implemented several silicon level thermal management features that can lower both (G)MCH and DDR power during periods of high activity. These features can help control temperature of the (G)MCH and DDR and thus help prevent thermally induced component failures. These features include:

- Memory throttling triggering by memory heating
- Memory throttling triggering by (G)MCH heating
- THRMTRIP# support

10.7.1 Internal Thermal Sensor

The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets incorporate two on-die thermal sensors for thermal management.

When "tripped" at various values, the thermal sensors may be programmed to cause hardware throttling and/or software interrupts. Hardware throttling includes main memory programmable throttling thresholds. Sensor trip points may also be programmed to be generated various interrupts, including SCI, SMI, SERR, or an internal graphics INTR.



10.7.1.1 Internal Thermal Sensor Operation

The internal thermal sensor reports four trip points, Aux0, Aux1, Hot, and Catastrophic trip points in the increasing order of temperature.

10.7.1.1.1 Trip Points

Aux0 Temperature Trip Point

This trip point may be set dynamically if desired and provides an interrupt to software when it is crossed in either direction. When the Aux0 trip point is reached, the chipset triggers an interrupt to the ACPI BIOS to allow fan control. The Auxiliary0 temperature trip point does not automatically causes any hardware throttling, but may be used by SW to trigger interrupt.

Aux1 Temperature Trip Point

This trip point may be set dynamically if desired and provides an interrupt to software when it is crossed in either direction. The Auxiliary1 temperature trip point does not automatically cause any hardware throttling, but may be used by SW to trigger interrupt.

Hot Temperature Trip Point

This trip point is set at the temperature at which the MCH must start throttling. It may optionally enable hardware render and write throttling when the temperature is exceeded. The chipset starts throttling once it detects that it is getting into higher temperatures than expected. This trip point may provide an interrupt to software when it is crossed in either direction.

Catastrophic Trip Point

This trip point is set at the temperature at which the (G)MCH must be shut down immediately without any software support. The catastrophic trip point may be programmed to generate an interrupt, enable throttling, or immediately shut down the system (via Halt, or via THRMTRIP# assertion).

Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register to select what type of interrupt is generated. Crossing a trip point is implemented as edge detection on each trip point in order to generate the interrupts. Either edge (i.e., crossing the trip point in either direction) generates the interrupt.

Table 44. Recommended Programming for Available Trip Points

Zone	Nominal Trip Points	Recommended Action
Catastrophic	$T_{Catastrophic}$ = 132°C ± 5°C ($T_{die,max}$ + 27°C ± $T_{accuracy}$)	Halt Operation
Hot	T_{hot} = 110 °C ± 5°C($T_{die,max}$ + 5°C ± $T_{accuracy}$)	Initiate Throttling
Aux1 & Aux0	OEM Decision, based on OEM criteria (for example: Taux = Temp at which an auxiliary fan should be turned on)	OEM Decision, based on OEM criteria

NOTE: $T_{die,max}$ = 105°C

Note: Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register which can be programmed to select the type of interrupt to be generated.Crossing a trip point may also initiate hardware-based throttling without software intervention

10.7.1.1.2 Thermal Sensor Accuracy

Thermal sensor accuracy ($T_{accuracy}$), for (G)MCH is ±5°C for temperature range 85°C to 132°C. This value is based on product characterization and is not guaranteed by manufacturing test.

Software has the ability to program the Tcat, Thot, and Taux trip points, but these trip points should be selected with consideration for the thermal sensor accuracy and the quality of the platform thermal solution. Overly conservative (unnecessarily low) temperature settings may unnecessarily degrade performance due to frequent throttling, while overly aggressive (dangerously high) temperature settings may fail to protect the part against permanent thermal damage.

10.7.1.2 Sample Programming Model

Intel reference and driver code do not use the thermal sensor interrupts.

10.7.1.2.1 Setting Trip Point for Hot Temperature and Generating an SERR Interrupt

- Program the Thermal Hot Temperature Setting register (THTS).
- In Thermal Sensor Control register (TSC), set thermal sensor enable bit (TSE), sequencer enable bits (SE), thermal sensor output select bit (TSOS), and the hysteresis value (if applicable).
- In the Thermal Interrupt Steering (TIS) register, set the Hot/Aux SMI/SERR steering bit.
- In Thermal Error Command register (TERRCMD), set the SERR on High bit
- Program the global thermal interrupt enabling registers

10.7.1.2.2 Temperature Rising above the Hot Trip Point

- The TERRSTS [High Thermal Sensor Event] is set when SERR interrupt is generated.
- Clear this bit of the TERRSTS register to allow subsequent interrupts of this type to get registered.
- Clear the global thermal sensor event bit in the Error Status register
- In thermal sensor status register (TSS), the Hot Trip indicator (HTI) bit is set if this condition is still valid by the time the software gets to read the register.

10.7.1.2.3 Determining the Current Temperature As Indicated by the Thermometer

- In Thermal Sensor Control register (TSC), set thermal sensor enable bit (TSE), sequencer enable bit (SE), thermal sensor output select bit (TSOS), and the hysteresis value (if applicable).
- Read the value in the Thermometer Reading register (TRR). Allow enough time for the entire thermometer sequence to complete (less than 5 msec in 512 clock mode, i.e., 5 msec = 512*4*256/100 MHz). Reading is not valid unless TSS[Sequencer Output Valid] = 1

10.7.1.2.4 Hysteresis Operation

- Hysteresis provides a small amount of positive feedback to the thermal sensor circuit to prevent a trip point from flipping back and forth rapidly when the temperature is right at the trip point.
- The digital hysteresis offset is programmable to be 0,1, 2…15, which corresponds to an offset in the range of approximately 0 to 7°C.

10.7.1.2.5 Thermal Throttling Options

The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets have two independent mechanisms that cause system memory throttling.

- (G)MCH Thermal Management: This is to ensure that the chipset is operating within thermal limits. The mechanism can be initiated by a thermal sensor (internal or external) trip or by write bandwidth measurement exceeding a programmed threshold via a weighted input averaging filter.
- DRAM Thermal Management: This is to ensure that the DRAM chips are operating within thermal limits. The Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipsets can control the amount of (G)MCH - initiated bandwidth per rank to a programmable limit via a weighted input averaging filter. Throttling can be initiated by an external thermal sensor trip or by DRAM activity measurement exceeding a programmed threshold.

10.7.2 External Thermal Sensor Interface Overview

While it is possible for Intel to set throttling values which will minimally impact typical application performance in a typical environment, due to the possibility that a bad thermal platform solution can cause overheating of box skin temperature, and that such a bad platform is unlikely to include external thermal sensors for its SO-DIMMS, it become necessary for the customers to have a means to determine the settings for their platforms throttling. This is further complicated by the fact that different memory vendors will have varying thermal performance.

An external thermal sensor with a serial interface such as the National Semi LM77, LM87 - or other - may be placed next to a SO- DIMM (or any other appropriate platform location), or a remote Thermal Diode (see Maxim 6685) may be placed next to the SO-DIMM (or any other appropriate platform location) and connected to the external Thermal Sensor.

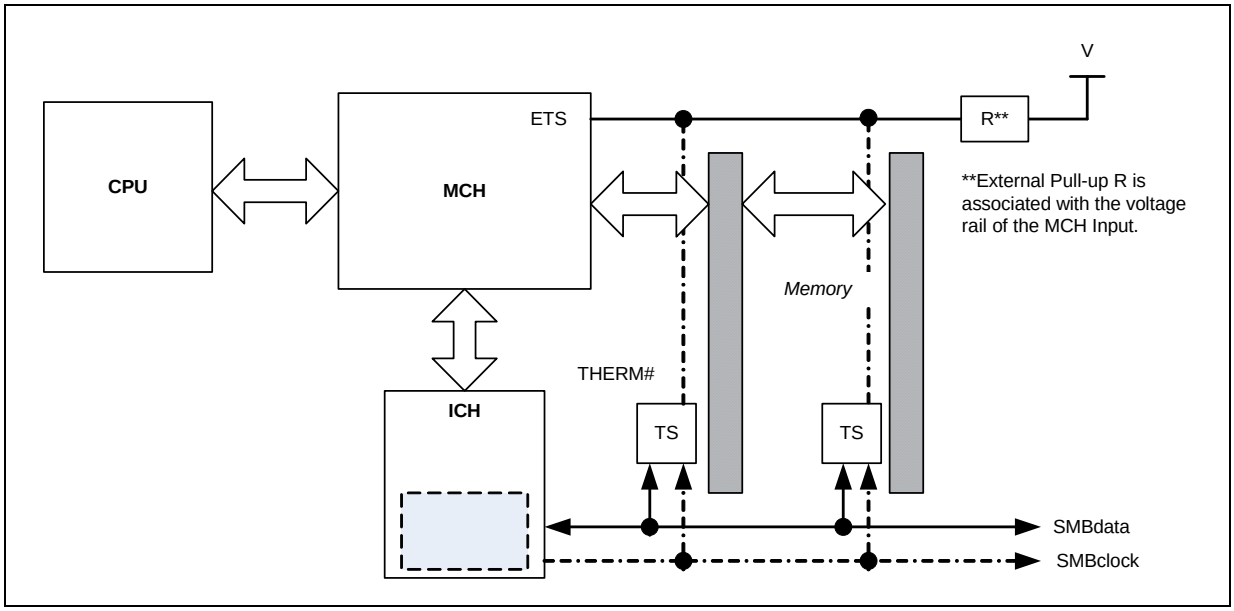
The External Sensor can be connected to the ICH via the SMBus Interface to allow programming and setup by BIOS software over the serial interface. The External Sensor's output should include at least one Active-Low Open-Drain signal indicating an Over-Temp condition (e.g., LM77 T_CRIT# or INT# in comparator mode), which remains asserted for as long as the Over-Temp Condition exists, and deasserts when Temperature has returned to within normal operating range. This External Sensor output will be connected to the (G)MCH input (EXTTS0#) and will trigger a preset Interrupt and/or Throttle on a level-sensitive basis. If the External Sensor has two trip point outputs, the other can be connected to the (G)MCH EXTTS1# input to trigger a preset interrupt or throttle action.

Additional external Thermal Sensor's outputs, for multiple sensors, can be wire-OR'd together allow signaling from multiple sensors located physically separately. Software can, if necessary, distinguish which SO-DIMM(s) is the source of the over-temp through the serial interface. However, since the SO-DIMM's will be located on the same Memory Bus Data lines, any (G)MCH-based Read Throttle will apply equally.

Note: The use of external sensors that include an internal pull-up resistor on the open-drain thermal trip output is discouraged; however it may be possible depending on the size of the pull-up and the voltage of the sensor.

The PM_ EXTTS1# signal may be optionally used to improve exit latency from the C4E state. See Section 10.6.7 for more details.

Figure 28. Platform External Sensor



10.7.3 THRMTRIP# Operation

Assertion of the (G)MCH's THRMTRIP# (Thermal Trip) indicates that its junction temperature has reached a level beyond which damage may occur. Upon assertion of THRMTRIP#, the (G)MCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the core junction temperature. Once activated, THRMTRIP# remains latched until RSTIN# is asserted. The (G)MCH THRMTRIP# and CPU THRMTRIP# signals connect to Intel 82801GBM.

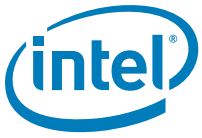
10.7.4 DT (Delta Temperature) in SPD and VTS (Virtual Thermal Sensor)

DT in SPD (Delta Temperature in SPD) is a system/platform level power/thermal management feature for memory. As frequency increases, DRAM current/power increases making it challenging to maintain a safe margin to thermal limits.

DT in SPD stores key temperature rise data and a DRAM maximum T-case data in SPD. Information on the power consumption and temperature rise for various types of transactions is stored in the SPD. The (G)MCH configures itself with this information at boot time. This allows the (G)MCH to perform memory throttling optimized to that particular DRAM.

DT in SPD makes possible a '**Virtual Thermal Sensor**' in the (G)MCH, improving upon the earlier technique of pure bandwidth-based throttling, irrespective of the characteristics of the DRAM module.

- DDR2 module vendors report in SPD the delta temperature rise parameter and T-case max
- System adjusts performance based on SPD contents (e.g., via BIOS)



When process shrinks or other power optimizations occur and current/power dissipation decreases, the system can use this knowledge to optimize power/thermal management and regain system performance. DT in SPD is a JEDEC Standard for DDR2 memory

Note: For accurate VTS operation, DRAM modules need to implement DT in SPD. In the event of DRAM modules not having DT information in SPD, the (G)MCH shall rely on the settings programmed by BIOS to the event weight registers during memory initialization.

10.8 Clocking

10.8.1 Overview

The (G)MCH has a total of 4 PLLs which is used for many internal clocks. The PLLs are:

- Host PLL – Generates the main core clocks in the host clock domain. Can also be used to generate memory and internal graphics core clocks. Uses the host clock (HCLKN/HCLKP) as a reference.
- PCI Express PLL – Generates all PCI Express related clocks, including the DMI that connects to the ICH. This PLL uses the 100 MHz (GCLKN/GCLKP) as a reference.
- Display PLL A – Generates the internal clocks for Display A. Uses the low voltage 96 MHz differential clock, DREF_CLKIN, as a reference.
- Display PLL B – Generates the internal clocks for Display A or Display B. Uses the low voltage 96 MHz differential clock, DREF_CLKIN, as a reference. Also may optionally use DREF_SSCCLKIN as a reference for SSC support for LVDS display on pipe B.

10.8.2 (G)MCH Reference Clocks

Reference Input Clocks	Input Frequency	Associated PLL
HCLKP / HCLKN	133 MHz / 166 MHz	Host / Memory / Graphics Core
DREF_CLKN / DREF_CLKP	96 MHz	Display PLL A
DREF_SSCCLKN / DREF_SSCCLKP	96 MHz (non-SSC)/ 100 MHz (SSC)	Display PLL B
GCLKP / GCLKN	100 MHz	PCI Express* / DMI PLL

10.8.3 Host/Memory/Graphics Core Clock Frequency Support

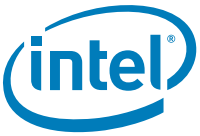
Table 45. Host/Graphics Clock Frequency Support for 1.05 V Core Voltage for the Mobile Intel 945GM/GME/GMS/GU/GSE and 940 GML Express Chipsets

Host	Memory	Display Clock (MHz)	Render Clock (MHz)
533 MHz	DDR2 400	200 (945GM/GME/GMS/GSE) 200 (943/940GML) 133 (940GML and 945GU)	250 (Intel 945GM/GME) 200 (Intel 943GML) 166 (Intel 945GMS/GSE and 943/940GML) 133 (Intel 945GU)
533 MHz	DDR2 533	200 (945GM/GME/GMS/GSE) 200 (943/940GML) 133 (940GML)	250 (Intel 945GM/GME) 200 (Intel 943GML) 166 (Intel 945GMS/GSE and 943/940GML)
667 MHz	DDR2 400	200 (945GM/GME/GMS)	250 (Intel 945GM/GME), 166 (Intel 945GMS and 940GML)
667 MHz	DDR2 533	200 (945GM/GME/GMS)	250 (Intel 945GM/GME), 166 (Intel 945GMS and 940GML)
667 MHz	DDR2 667	200 (945GM/GME)	250 (Intel 945GM/GME)

Table 46. Host/Graphics Clock Frequency Support at 1.5 V Core Voltage for the Intel 945GT Express Chipset Only

Host	Memory	Display Clock (MHz)	Render Clock (MHz)
533 MHz	DDR2 400	320 (945GT)	400 (Intel 945GT)
533 MHz	DDR2 533	320 (945GT)	400 (Intel 945GT)
667 MHz	DDR2 400	320 (945GT)	400 (Intel 945GT)
667 MHz	DDR2 533	320 (945GT)	400 (Intel 945GT)
667 MHz	DDR2 667	320 (945GT)	400 (Intel 945GT)

§



11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 47 lists the Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the AC and DC tables.

Table 47. Absolute Maximum Ratings (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
T_{die}	Die Temperature under Bias	0	105	°C	1
$T_{storage}$	Storage Temperature	-55	150	°C	2,3
(G)MCH Core					
VCC	1.05-V Core Supply Voltage with Respect to VSS	-0.3	1.65	V	
VCC	1.5-V Core Supply Voltage with Respect to VSS	-0.3	1.65	V	
Host Interface					
VTT (FSB Vccp)	1.05-V AGTL+ buffer DC Input Voltage with Respect to VSS	-0.3	1.65	V	
DDR2 Interface (400 MTs /533 MTs/ /667 MTs)					
VCCSM	1.8-V DDR2 Supply Voltage with Respect to Vss.	-0.3	1.90	V	
DMI /PCI Express* Graphics/SDVO Interface					
VCC3G	1.5-V PCI-Express Supply Voltage with Respect to VSS	-0.3	1.65	V	
VCCA_3GBG	2.5-V Analog Supply Voltage with Respect to VSSA3GBG	-0.3	2.65	V	
CRT DAC Interface (8-bit DAC)					
VCCA_CRTDAC	2.5-V DAC Supply Voltage with Respect to VSSA_CRTDAC	-0.3	2.65	V	
VCC_SYNC	2.5-V CRT Sync Supply Voltage	-0.3	2.65	V	
HV CMOS Interface					
VCCHV	3.3-V Supply Voltage with Respect to VSS	-0.3	3.65	V	
TV OUT Interface (10-bit DAC)					
VCCD_TVDAC	1.5-V TV Supply	-0.3	1.65	V	
VCCA_TVDACA VCCA_TVDACB VCCA_TVDACC	3.3-V TV Analog Supply	-0.3	3.65	V	

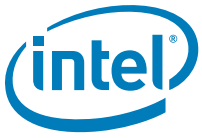
Table 47. Absolute Maximum Ratings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
VCCA_TVBG	3.3-V TV Analog Supply	-0.3	3.65	V	
VCCDQ_TVDAC	1.5-V Quiet Supply	-0.3	1.65	V	
LVDS Interface					
VCCD_LVDS	1.5-V LVDS Digital Power Supply	-0.3	1.65	V	
VCCTX_LVDS	2.5-V LVDS Data/Clock Transmitter Supply Voltage with Respect to VSS	-0.3	2.65	V	
VCCA_LVDS	2.5-V LVDS Analog Supply voltage with Respect to VSS	-0.3	2.65	V	
PLL Analog Power Supplies					
VCCA_HPLL, VCCA_MPLL, VCCD_HMPLL, VCCA_3GPLL, VCCA_DPLLA, VCCA_DPLLB	1.5-V Power Supply for various PLL	-0.3	1.65	V	
VCC_AUX	Power Supply for DDR2 DLL, DDR2 HSIO and FSB HSIO	-0.3	1.65	V	

Caution: At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits. At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded. Although the device contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Note:

1. Functionality is not guaranteed for parts that exceed Tdie temperature above 105ºC. Tdie is measured at top center of the package. Full performance may be affected if the on-die thermal sensor is enabled.
2. Possible damage to the (G)MCH may occur if the (G)MCH storage temperature exceeds 150ºC. Intel does not guarantee functionality for parts that have exceeded temperatures above 150ºC due to spec violation.
3. Storage temperature is applicable to storage conditions only. In this scenario, the device must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. This rating applies to the silicon and does not include any tray or packaging.



11.2 Power Characteristics

Table 48. Non Memory Power Characteristics (Sheet 1 of 2)

Symbol	Parameter	Core Voltage and Frequency	TDP	Unit	Notes
TDP	Mobile Intel® 945GM/GME Express Chipset	1.05V/250 MHz	7.0	W	1
	Mobile Intel® 945PM Express Chipset	1.05 V/N/A	6.0		1
	Mobile Intel® 945GMS/GSE Express Chipset	1.05V/166 MHz	5.5[1]-6.0[2]		1,10
	Mobile Intel® 943GML Express Chipset	1.05V/200 MHz	7.0		1
	Mobile Intel® 940GML Express Chipset	1.05V/166 MHz	7.0		1
	Intel® 945GT Express Chipset	1.5 V/400 MHz	15.0		1
	Ultra Mobile Intel® 945GU Express Chipset	1.05 V/250 MHz	5		1

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
I_{VTT}	VTT Supply Current (1.05 V)	VTT			800	mA	3,9
I_{VTT}	VTT Supply Current (1.05 V) for Mobile Intel 945GMS/ GU/GSE Express Chipset	VTT			780	mA	3,9
I_{VCC1_05}	1.05-V Core Supply Current (External GFX)	VCC			1500	mA	3,5
I_{VCC1_05}	1.05-V Core Supply Current (Integrated GFX)	VCC			3500	mA	3,5
I_{VCC1_50}	1.50-V Core Supply Current (Integrated GFX)	VCC			5500	mA	3,5
I_{VCC1_05}	1.05-V Core Supply Current for Mobile Intel 945GMS/GU/GSE Express Chipset (Integrated GFX)	VCC			2940	mA	3,5
I_{VCC3G}	1.5-V PCI Express* Supply Current	VCC3G, VCCA_3GPLL			1500	mA	3, 4, 8
I_{VCC3G}	1.5-V PCI Express Supply Current for Mobile Intel 945GMS/GU/GSE Express Chipset (Integrated GFX)	VCC3G, VCCA_3GPLL			400	mA	3, 4, 8
I_{VCCA_3GBG}	2.5-V PCI Express Analog Supply Current	VCCA_3GBG			2	mA	3
I_{VCCD_LVDS}	1.5-V LVDS (Digital) Supply Current	VCCD_LVDS			20	mA	3
I_{VCCA_LVDS}	2.5-V LVDS (Analog) Supply Current	VCCA_LVDS			10	mA	3
I_{VCCTX_LVDS}	2.5-V LVDS (I/O) Supply Current	VCCTX_LVDS			60	mA	3
I_{VCCCRT}	2.5-V CRT DAC Supply Current (IvccADAC) 2.5-V CRT Sync Supply Current (Ivccsync)	VCCA_CRTDAC VCC_SYNC			70	mA	3,8
I_{VCCHV}	3.3-V HV CMOS Supply Current	VCCHV			40	mA	3

Table 48. Non Memory Power Characteristics (Sheet 2 of 2)

Symbol	Parameter	Core Voltage and Frequency	TDP			Unit	Notes
I_{VCCD_TVDAC}	1.5-V TV Supply Current (Ivcc_TVDAC 1.5-V TV Quiet Supply Current (IVccQ_TVDAC)	VCCD_TVDAC VCCQ_TVDAC			24	mA	3,8
$I_{VCCTVDAC}$	3.3-V TV Analog Supply Current (IvccATVDAC) 3.3 V TV Bandgap Supply Current (IvccATVBG)	VCCA_TVBG VCCA_TVDACA VCCA_TVDACB VCCA_TVDACC			120	mA	3,8
$I_{VCCAHPLL}$	Host PLL Supply Current	VCCA_HPLL			45	mA	3
$I_{VCCADPLLA,B}$	Display PLLA Supply Display PLLB Supply Current	VCCA_DPLLA VCCA_DPLLB			50 50	mA mA	3
$I_{VCCAMPLL}$	Memory PLL Supply Current	VCCA_MPLL			45	mA	3
$I_{VCCDHMPLL}$	HMPLL Supply Current for Digital Interface	VCCD_HMPLL			150	mA	3

NOTES:

1. This spec is the Thermal Design Power and is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component. It does not represent the expected power generated by a power virus. Studies by Intel indicate that no application will cause thermally significant power dissipation exceeding this specification, although it is possible to concoct higher power synthetic workloads that write but never read. Under realistic read/write conditions, this higher power workload can only be transient and is accounted in the Icc (max) spec. Tdie is measured at the top center of the package.
2. These current levels can happen simultaneously, and can be summed into one supply.
3. Estimate is only for max current coming through the chipset's supply balls.
4. Rail includes PLL current.
5. Includes maximum leakage.
6. Calculated for highest future projected frequencies.
7. Iccmax is determined on a per-interface basis, and all cannot happen simultaneously.
8. Iccmax number includes max current for all signal names listed in the table.
9. May vary from CPU as this estimate does not include sense Amps, as they are on a separate rail, or signals that are CPU specific.
10. [1]TDP specified for 533 MTs FSB and 400 MTs DDR2; [2]TDP specified for 667 MTs FSB and 533 MTs DDR2.

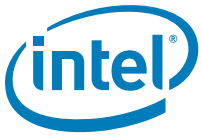


Table 49. DDR2 (400 MTs/533 MTs/667 MTs) Power Characteristics

Symbol	Parameter	Min	Type	Max	Unit	Notes
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V, 400 MTs) Supply Current		1 Channel 2 Channel	1300 2400	mA mA	
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V, 400 MTs) Supply Current for Mobile Intel® 945GMS/GU/ GSE Express Chipset		1 Channel	1500	mA mA	
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V, 533 MTs) Supply Current		1 Channel 2 Channel	1500 2800	mA mA	
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V, 533 MTs) Supply Current for Mobile Intel 945GMS/GU/GSE Express Chipset		1 Channel	1720	mA mA	
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V, 667 MTs) Supply Current		1 Channel 2 Channel	1700 3200	mA mA	
I_{SUS_VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V) Standby Supply Current			~5	mA	1
I_{SMVREF} (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current			10	µA	
I_{SUS_SMVREF} (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) Standby Supply Current			10	µA	1
I_{TTRC} (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current			32	mA	
I_{SUS_TTRC} (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Standby Supply Current			~0	µA	1

NOTE:
1. Standby refers to system memory in Self Refresh during S3 (STR)

Table 50. VCC_AUX Power Characteristics VCC_AUX = 1.5 V ±75 mV (Bandlimited to 20 MHz)

Symbol	Parameter	Min	Type	Max	Unit	Notes
I_{VCCAUX}	Supply current for DDR2 DLL, DDR2 and FSB HSIO			1900	mA	1
I_{VCCAUX}	Supply current for DDR2 DLL, DDR2 and FSB HSIO for Mobile Intel® 945GMS/GU/GSE Express Chipset.			1250	mA	1

NOTE:
1. Calculated for highest frequency of operation.

11.3 Signal Groups

The signal description includes the type of buffer used for the particular signal:

AGTL+	Advanced GTL+ interface signal
Analog	Analog signal interface
DDR2	DDR2 system memory (1.8 V CMOS buffers)
DMI	Direct Media Interface
HVCMOS	3.3-V tolerant high voltage CMOS buffers
LVDS	Low voltage differential signal interface
PCI Express* GFX/ Serial DVO	PCI Express Graphics/Serial DVO interface signals. These signals are compatible with current *PCI Express* Base Specification* signaling environment AC specifications. The buffers are **not** 3.3 V tolerant.
Ref	Voltage reference signal
SSTL-1.8	1.8-V tolerant stub series termination logic

Table 51. Signal Groups for Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset (Sheet 1 of 4)

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	AGTL+ Input/Outputs	HADS#, HBNR#, HBREQ0#,HDBSY#, HDRDY#, HDINV[3:0]#, HA[31:3]#, HADSTB[1:0]#, HD[63:0]#,HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#, THERMTRIP#,	
(b)	AGTL+ Common Clock Outputs	HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#, HDPWR#	
(c)	CMOS Output	HCPUSLP#	CMOS Type Buffer with Vtt
(d)	AGTL+ Asynchronous Input	HLOCK#	
(e)	Analog Host I/F Ref & Comp. Signals	HVREF, HXSWING, HYSWING, HXRCOMP, HXSCOMP, HYRCOMP, HYSCOMP	

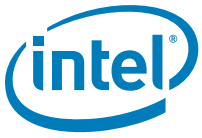


Table 51. Signal Groups for Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset (Sheet 2 of 4)

Signal Group	Signal Type	Signals	Notes
Serial DVO or PCI Express* Graphics Interface Signal Groups			
(f)	PCI-E GFX/SDVO Input	**PCI-E GFX Interface:** EXP_A_RXN(15:0), EXP_A_RXP(15:0) **SDVO Interface:** SDVO_TVCLKIN#, SDVO_TVCLKIN, SDVO_INT, SDVO_INT#, SDVO_FLDSTALL#, SDVO_FLDSTALL	Please see Section 10.3.2.2 for SDVO & PCI Express GFX Pin Mapping
(g)	PCI-E GFX/SDVO Output	**PCI-E GFX Interface:**EXP_A_TXN(15:0), EXP_A_TXP(15:0) **SDVO Interface:** SDVOB_RED#, SDVOB_RED, SDVOB_GREEN#, SDVOB_GREEN, SDVOB_BLUE#, SDVOB_BLUE, SDVOB_CLKN, SDVOB_CLKP, SDVOC_RED#/ SDVOB_ALPHA#, SDVOC_RED/ SDVOB_ALPHA, SDVOC_GREEN#, SDVOC_GREEN, SDVOC_BLUE#, SDVOC_BLUE, SDVOC_CLKN, SDVOC_CLKP	Please see Section 10.3.2.2 for SDVO & PCI Express GFX Pins Mapping
(h)	Analog PCI-E GFX/SDVO I/F Compensation Signals	EXP_A_COMPO EXP_A_COMPI	
DDR2 Interface Signal Groups			
(l)	SSTL – 1.8 DDR2 CMOS I/O	DQ (SA_DQ[63:0], SB_DQ[63:0]) DQS (SA_DQS[7:0], SB_DQS[7:0]) DQS# (SA_DQS[7:0]#, SB_DQS[7:0]#)	
(j)	SSTL – 1.8 DDR2 CMOS Output	DM (SA_DM[7:0], SB_DM[7:0]) MA (SA_MA[13:0], SB_MA[13:0] BS (SA_BS[2:0], SB_BS[2:0]) RAS# (SA_RAS#, SB_RAS#) CAS# (SA_CAS#, SB_CAS#) WE# (SA_WE#, SB_WE#) SM_ODT[3:0] SM_CKE[3:0], SM_CS[3:0]# SM_CK[3:0], SM_CK[3:0]#	
(k)	DDR2 Reference Voltage	SMVREF(1:0)	
(ka)	DDR2 Compensation Signals	SM_RCOMPN, SM_RCOMPP, SM_OCDCOMP[1:0]	
LVDS Signal Groups			
(l)	LVDS Outputs	LADATAP[2:0], LADATAN[2:0], LACLKP, LACLKN, LBDATAP[2:0], LBDATAN[2:0], LBCLKP, LBCLKN	
(m)	Analog LVDS Miscellaneous	LIBG	Current Mode Reference pin. DC Spec. not required

Table 51. Signal Groups for Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset (Sheet 3 of 4)

Signal Group	Signal Type	Signals	Notes
CRT DAC Signal Groups			
(n)	Analog Current Outputs	CRT_RED, CRT_RED#, CRT_GREEN, CRT_GREEN#, CRT_BLUE, CRT_BLUE#	Please refer to CRT/Analog VESA spec & Section 11.4.2
(o)	Analog/Ref DAC Miscellaneous	CRT_IREF	Current Mode Reference pin. DC Spec. not required
(p)	Analog Output	CRT_HSYNC, CRT_VSYNC	Please refer to CRT/Analog VESA spec & Section 11.4.2
TV DAC Signal Groups			
(q)	Analog Current Outputs	TVDAC_A, TVDAC_B, TVDAC_C, TV_IRTNA, TV_IRTNB, TV_IRTNC	
(r)	Analog/Ref DAC Miscellaneous	TV_IREF	Current Mode Reference pin. DC Spec. not required
Clocks, Reset, and Miscellaneous Signal Groups			
s	HVCMOS Input	PM_EXT_TS[1:0]#	
t	Low Voltage Diff. Clock Input	HCLKP(BCLK0/BCLK), HCLKN(BCLK1/BCLK#), DREF_CLKP, D_CLKN, DREF_SSCLKP, DREF_SSCLK, GCLKP, GCLKN	
u	HVCMOS Output	LVDD_EN, LBKLT_EN, LBKLT_CTL, LCTLA_CLK, ICH_SYNC#, TVDCONSEL[1:0]	
ua	Open Drain Output	CLKREQ#	
v	HVCMOS I/O	PM_BM_BUSY#	
va	Open Drain I/O	DDCCLK, DDCDATA, LDDC_CLK, LDDC_DATA, SDVOCTRL_CLK, SDVOCTRL_DATA, LCTLB_DATA, LCTLA_CLK	
w	AGTL+ Input/Output	CFG[17:3], H_BSEL[2:0] / CFG[2:0]	
x	HVCMOS Input	RSTIN#, PWROK, CFG[20:18]	

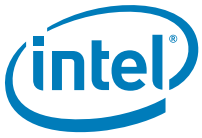


Table 51. Signal Groups for Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset (Sheet 4 of 4)

Signal Group	Signal Type	Signals	Notes
I/O Buffer Supply Voltages			
y	AGTL+ Termination Voltage	VTT (V_{CCP})	
z	SVDO,DMI, PCI Express GFX Voltages	VCC3G, VCCA_3GBG	
aa	1.8-V DDR2 Supply Voltage	VCCSM	
ab	(G)MCH Core	VCC	
ac	HV Supply Voltage	VCCHV	
ad	TV DAC Supply Voltage	VCCD_TVDAC, VCCDQ_TVDAC	
ae	TV DAC Band Gap and Channel Supply	VCCA_TVBG, VCCA_TVDACA,VCCA_TVDACB, VCCA_TVDACC	
af	CRT DAC Supply Voltage	VCCA_CRTDAC, VCC_SYNC	
ag	PLL Supply Voltages	VCCA_HPLL, VCCA_MPLL, VCCD_HMPLL VCCA_3GPLL, VCCA_DPLLA, VCCA_DPLLB	
ah	1.5-V LVDS Digital Supply	VCCD_LVDS	
ai	2.5-V LVDS Data/CLK Transmitter Supply	VCCTX_LVDS	
aj	2.5-V LVDS analog Supply	VCCA_LVDS	
ak	1.5-V Power Supply for DDR2 DDL, DDR2 HSIO and FSB HSIO	VCC_AUX	

Table 52. Signal Groups for Intel 945GMS/GU/GSE Express Chipset (Sheet 1 of 4)

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	AGTL+ Input/Outputs	HADS#, HBNR#, HBREQ0#,HDBSY#, HDRDY#, HDINV[3:0]#, HA[31:3]#, HADSTB[1:0]#, HD[63:0]#,HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#, THERMTRIP#,	
(b)	AGTL+ Common Clock Outputs	HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#, HDPWR#	
(c)	CMOS Output	HCPUSLP#	CMOS Type Buffer with Vtt
(d)	AGTL+ Asynchronous Input	HLOCK#	
(e)	Analog Host I/F Ref & Comp. Signals	HVREF, HXSWING, HYSWING, HXRCOMP, HXSCOMP, HYRCOMP, HYSCOMP	

Table 52. Signal Groups for Intel 945GMS/GU/GSE Express Chipset (Sheet 2 of 4)

Signal Group	Signal Type	Signals	Notes
Serial DVO or PCI-Express* Graphics Interface Signal Groups			
(f)	SDVO Input	**SDVO Interface:** SDVO_TVCLKIN#, SDVO_TVCLKIN, SDVOB_INT#, SDVOB_INT, SDVO_FLDSTALL#, SDVO_FLDSTALL	Please see Section 10.3.2.2 for SDVO & PCI Express GFX Pin Mapping
(g)	SDVO Output	**SDVO Interface:** SDVOB_RED#, SDVOB_RED, SDVOB_GREEN#, SDVOB_GREEN, SDVOB_BLUE#, SDVOB_BLUE, SDVOB_CLKN, SDVOB_CLKP	Please see Section 10.3.2.2 for SDVO Pin Mapping
(h)	SDVO I/F Compensation Signals	EXP_A_COMPO EXP_A_COMPI	
DDR2 Interface Signal Groups			
(l)	SSTL – 1.8 DDR2 CMOS I/O	DQ (SA_DQ[63:0]) DQS (SA_DQS[7:0]) DQS# (SA_DQS[7:0]#)	
(j)	SSTL – 1.8 DDR2 CMOS Output	DM (SA_DM[7:0]) MA (SA_MA[13:0], SB_MA[13:0]) BS (SA_BS[2:0], SB_BS[2:0]) RAS# (SA_RAS#, SB_RAS#) CAS# (SA_CAS#, SB_CAS#) WE# (SA_WE#, SB_WE#) SM_ODT[3:0] SM_CKE[3:0], SM_CS[3:0]# SM_CK[3:0], SM_CK[3:0]#	
(k)	DDR2 Reference Voltage	SMVREF(1:0)	
(ka)	DDR2 compensation signals	SM_RCOMPN, SM_RCOMPP, SM_OCDCOMP[1:0]	
LVDS Signal Groups			
(l)	LVDS Outputs	LADATAP[2:0], LADATAN[2:0], LACLKP, LACLKN, LBDATAP[2:0], LBDATAN[2:0], LBCLKP, LBCLKN	
(m)	Analog LVDS Miscellaneous	LIBG	Current Mode Reference pin. DC Spec. not required

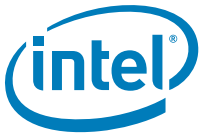


Table 52. Signal Groups for Intel 945GMS/GU/GSE Express Chipset (Sheet 3 of 4)

Signal Group	Signal Type	Signals	Notes
CRT DAC Signal Groups (Not on Intel 945GU)			
(n)	Analog Current Outputs	CRT_RED, CRT_RED#, CRT_GREEN, CRT_GREEN#, CRT_BLUE, CRT_BLUE#	Please refer to CRT/Analog VESA spec & Section 11.4.2
(o)	Analog/Ref DAC Miscellaneous	CRT_IREF	Current Mode Reference pin. DC Spec. not required
(p)	Analog Output	CRT_HSYNC, CRT_VSYNC	Please refer to CRT/Analog VESA spec & Section 11.4.2
TV DAC Signal Groups			
(q)	Analog Current Outputs	TVDAC_A, TVDAC_B, TVDAC_C, TV_IRTNA, TV_IRTNB, TV_IRTNC	Please refer to CRT/Analog VESA spec & Section 11.4.3
(r)	Analog/Ref DAC Miscellaneous	TV_IREF	Current Mode Reference pin. DC Spec. not required
Clocks, Reset, and Miscellaneous Signal Groups			
(s)	HVCMOS Input	PM_EXT_TS[1:0]#	
(t)	Low Voltage Diff. Clock Input	HCLKP(BCLK0/BCLK), HCLKN(BCLK1/BCLK#), DREF_CLKP, DREF_CLKN, DREF_SSCLKP, DREF_SSCLKN, GCLKP, GCLKN	
(u)	HVCMOS Output	LVDD_EN, LBKLT_EN, LBKLT_CTL, LCTLA_CLK, ICH_SYNC#, TVDCONSEL[1:0]	
(ua)	Open Drain output	CLKREQ#	
(v)	HVCMOS I/O	PM_BM_BUSY#	
(va)	Open Drain I/O	DDCCLK, DDCDATA, LDDC_CLK, LDDC_DATA, SDVOCTRL_CLK, SDVOCTRL_DATA, LCTLB_DATA, LCTLA_CLK	
(w)	AGTL+ input/output	CFG[3], CFG[5], CFG[6], H_BSEL[2:0] / CFG[2:0]	
(x)	HVCMOS Input	RSTIN#, PWROK, CFG[19]	

Table 52. Signal Groups for Intel 945GMS/GU/GSE Express Chipset (Sheet 4 of 4)

Signal Group	Signal Type	Signals	Notes
I/O Buffer Supply Voltages			
(y)	AGTL+ Termination Voltage	VTT (Vccp)	
(z)	SDVO, DMI, PCI Express GFX Voltages	VCC3G, VCCA_3GBG	
(aa)	1.8 V DDR2 Supply Voltage	VCCSM	
(ab)	(G)MCH Core	VCC	
(ac)	HV Supply Voltage	VCCHV	
(ad)	TV DAC Supply Voltage	VCCD_TVDAC, VCCDQ_TVDAC	
(ae)	TV DAC Band Gap and Channel Supply	VCCA_TVBG, VCCA_TVDACA,VCCA_TVDACB, VCCA_TVDACC	
(af)	CRT DAC Supply Voltage	VCCA_CRTDAC, VCC_SYNC	
(ag)	PLL Supply Voltages	VCCA_HPLL, VCCA_MPLL, VCCD_HMPLL VCCA_3GPLL, VCCA_DPLLA, VCCA_DPLLB	
(ah)	1.5 V LVDS Digital Supply	VCCD_LVDS	
(ai)	2.5 V LVDS Data/CLK Transmitter Supply	VCCTX_LVDS	
(aj)	2.5 V LVDS Analog Supply	VCCA_LVDS	
(ak)	1.5V Power Supply for DDR2 DLL, DDR2 HSIO and FSB HSIO	VCC_AUX	

11.4 DC Characteristics

11.4.1 General DC Characteristics

Table 53. DC Characteristics (Sheet 1 of 4)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I/O Buffer Supply Voltage							
VCC	(ab)	1.05 V (G)MCH Core Supply Voltage	1.0	1.05	1.1	V	
VCC	(ab)	1.5 V (G)MCH Core Supply Voltage	1.425	1.50	1.575	V	
VTT	(y)	1.05 V Host AGTL+ Termination Voltage	0.9975	1.05	1.1025	V	
VCCSM (DDR2)	(aa)	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	
VCC3G	(z)	DMI, SDVO, PCI Express GFX Supply Voltage	1.425	1.5	1.575	V	
VCCA_3GBG	(z)	DMI, SDVO, PCI Express GFX Analog Voltage	2.32	2.5	2.625	V	

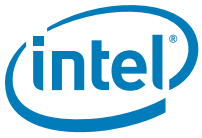


Table 53. DC Characteristics (Sheet 2 of 4)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
VCCHV	(ac)	HV CMOS Supply Voltage	3.135	3.3	3.465	V	
VCCD_TVDAC	(ad)	TV DAC Supply Voltage	1.425	1.5	1.575	V	
VCCDQ_TVDAC	(ad)	TV DAC Quiet Supply Voltage	1.425	1.5	1.575	V	
VCCA_TVDACA VCCA_TVDACB VCCA_TVDACC VCCA_TVBG	(ae)	TV DAC Analog & Band Gap Supply Voltage	3.135	3.3	3.465	V	
VCCA_CRTDAC	(af)	CRT DAC Supply Voltage	2.32	2.5	2.625	V	
VCC_SYNC	(af)	CRT DAC SYNC Supply Voltage	2.32	2.5	2.625	V	
VCCA_HPLL, VCCA_MPLL, VCCD_HMPLL VCCA_3GPLL, VCCA_DPLLA, VCCA_DPLLB	(ag)	Various PLLS Analog Supply Voltages	1.425	1.5	1.575	V	1 - Ripple Noise spec.
VCCD_LVDS	(ah)	Digital LVDS Supply Voltage	1.425	1.5	1.575	V	
VCCTX_LVDS	(ai)	Data/Clock Transmitter LVDS Supply Voltage	2.375	2.5	2.625	V	
VCCA_LVDS	(aj)	Analog LVDS Supply Voltage	2.375	2.5	2.625	V	
VCC_AUX	(ak)	Supply for DDR2 DLLs, DDR2 and FSB HSIO	1.425	1.5	1.575	V	
Reference Voltages							
HVREF	(e)	Host Address and Data Reference Voltage	2/3 x VTT – 2%	2/3 x VTT	2/3 x VTT + 2%	V	
HXSWING HYSWING	(e)	Host Compensation Reference Voltage	0.3125 x VTT – 2%	0.3125x VTT	0.3125x VTT + 2%	V	
SMVREF (DDR2)	(k)	DDR2 Reference Voltage	0.49 x VCCSM	0.50 x VCCSM	0.51 x VCCSM	V	
Host Interface							
V_{IL_H}	(a,d,w)	Host AGTL+ Input Low Voltage	-0.10	0	(2/3 x VTT) – 0.1	V	
V_{IH_H}	(a,d,w)	Host AGTL+ Input High Voltage	(2/3 x VTT) +0.1	VTT (1.05)	VTT +0.1	V	
V_{OL_H}	(a,b,w)	Host AGTL+ Output Low Voltage			(0.3125 x VTT) +0.1	V	
V_{OH_H}	(a,b,w)	Host AGTL+ Output High Voltage	VTT-0.1		VTT	V	
I_{OL_H}	(a,b,w)	Host AGTL+ Output Low Current			VTT_{max} / (1-0.3125)Rtt_{min}	mA	Rtt_{min}= 50 ohm

Table 53. DC Characteristics (Sheet 3 of 4)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I_{LEAK_H}	(a,d,w)	Host AGTL+ Input Leakage Current			20	uA	V_{OL}<Vpad< Vtt
C_{PAD}	(a,d,w)	Host AGTL+ Input Capacitance	2		3.5	pF	
V_{OL_H}	(c)	CMOS Output Low Voltage			0.1 VTT	V	I_{OL} = 1 mA
V_{OH_H}	(c)	CMOS Output High Voltage	0.9VTT		VTT	V	I_{OH} = 1 mA
DDR2 Interface							
$V_{IL(DC)}$ (DDR2)	(l)	DDR2 Input Low Voltage			SMVREF_ 0.125	V	
$V_{IH(DC)}$ (DDR2)	(l)	DDR2 Input High Voltage	SMVREF + 0.125			V	
$V_{IL(AC)}$ (DDR2)	(i)	DDR2 Input Low Voltage			SMVREF_ 0.250	V	
$V_{IH(AC)}$ (DDR2)	(i)	DDR2 Input High Voltage	SMVREF + 0.250			V	
V_{OL} (DDR2)	(i, j)	DDR2 Output Low Voltage			0.3	V	2
V_{OH} (DDR2)	(i, j)	DDR2 Output High Voltage	1.5			V	2
I_{Leak} (DDR2)	(i)	Input Leakage Current			±10	µA	
$C_{I/O}$ (DDR2)	(i, j)	DDR2 Input/Output Pin Capacitance	3.0		6.0	pF	
1.5-V PCI Express Interface 1.0a (includes PCI Express GFX and SDVO)							
$V_{TX\text{-}DIFF\ P\text{-}P}$	(f, g)	Differential Peak to Peak Output Voltage	0.400		0.6	V	3, 4
$V_{TX\_CM\text{-}ACp}$	(f, g)	AC Peak Common Mode Output Voltage			20	mV	3
$Z_{TX\text{-}DIFF\text{-}DC}$	(f, g)	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX\text{-}DIFF\ p\text{-}p}$	(f, g)	Differential Input Peak to Peak Voltage	0.175		1.2	V	3, 4
$V_{RX\_CM\text{-}ACp}$	(f, g)	AC peak Common Mode Input Voltage			150	mV	
Clocks, Reset, and Miscellaneous Signals							
V_{IL}	(s)	Input Low Voltage			0.8	V	
V_{IH}	(s)	Input High Voltage	2.0			V	
I_{LEAK}	(s)	Input Leakage Current			±10	µA	
C_{IN}	(s)	Input Capacitance	3.0		6.0	pF	
V_{IL}	(t)	Input Low Voltage		0		V	
V_{IH}	(t)	Input High Voltage	0.660	0.710	0.850	V	

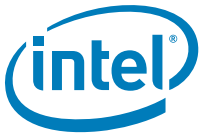


Table 53. DC Characteristics (Sheet 4 of 4)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{CROSS}	(t)	Crossing Voltage	0.45x (V_{IH} - V_{IL})	0.5x (V_{IH} - V_{IL})	0.55x (V_{IH} - V_{IL})	V	
C_{IN}	(t)	Input Capacitance	1.0		3.0	pF	
V_{OL}	(u, v, ua, va)	Output Low Voltage (CMOS Outputs)			0.4	V	
V_{OH}	(u, v)	Output High Voltage (CMOS Outputs)	2.8			V	
I_{OL}	(u, v)	Output Low Current (CMOS Outputs)			1	mA	@V_{OL_HI} max
I_{OH}	(u, v)	Output High Current (CMOS Outputs)	-1			mA	@V_{OH_HI} min
V_{IL}	(v, va, x)	Input Low Voltage (DC)			1	V	
V_{IH}	(v, va, x)	Input High Voltage (DC)	1.5			V	
I_{LEAK}	(v)	Crossing Voltage			±10	µA	
C_{IN}	(v, va, x)	Input Capacitance	3.0		6.0	pF	
LVDS Interface: Functional Operating Range (VCC=2.5 V ±5%)							
V_{OD}	(l)	Differential Output Voltage	250	350	450	mV	
ΔV_{OD}	(l)	Change in V_{OD} between Complementary Output States			50	mV	
V_{OS}	(l)	Offset Voltage	1.125	1.25	1.375	V	
ΔV_{OS}	(l)	Change in V_{OS} between Complementary Output States			50	mV	
I_{Os}	(l)	Output Short Circuit Current		-3.5	-10	mA	
I_{OZ}	(l)	Output TRI-STATE Current		±1	±10	µA	

NOTES:

1. Following are the noise rejection specifications for PLL supplies.

VCCA_HPLL	34 dB(A) attenuation of power supply noise in 1 MHz(f1) to 66 MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 120 mV
VCCA_MPLL	34 dB(A) attenuation of power supply noise in 1 MHz(f1) to 66 MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 120 mV
VCCD_HMPLL	peak to peak noise should be limited to < 120 mV
VCCA_3GPLL	< 0 dB(A) in 0 to 1MHz, 20 dB(A) attenuation of power supply noise in 1 MHz(f1) to 1.25 GHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 40 mV

VCCA_DPLLA	20 dB(A) attenuation of power supply noise in 10 kHz(f1) to 2.5 MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 100 mV
VCCA_DPLLB	20 dB(A) attenuation of power supply noise in 10 kHz(f1) to 2.5 MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 100 mV
VccAux	30 dB(A) attenuation of power supply noise in 10 MHz (f1) to 266 MHz (f2), < 0.2 dB gain in pass band and peak to peak noise should be limited to < 120 mv
Vcc3G	< 0 dB(A) in 0 to 1.5 MHz, 20 dB(A) attenuation of power supply noise in 1.5 MHz(f1) to 1.25 GHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 40 mV

2. Determined with 2x (G)MCH DDR/DDR2 buffer strength settings into a 50 to 0.5xVCCSM (DDR/DDR2) test load.
3. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of the *PCI Express* Base Specification* and measured over any 250 consecutive TX UI's. Specified at the measurement point and measured over any 250 consecutive ULS. The test load shown in receiver compliance eye diagram of the *PCI Express* Base Specification*. Should be used as the RX device when taking measurements.
4. Low voltage PCI Express (PCI Express Graphics/SDVO) interface.

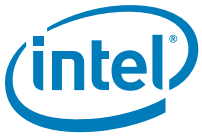
11.4.2 CRT DAC DC Characteristics

Note: This section is Not for the 945GU Express Chipset.

Table 54. CRT DAC DC Characteristics: Functional Operating Range (VCCADAC = 2.5 V 5%)

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution		8		Bits	(1)
Max Luminance (full-scale)	0.665	0.700	0.770	V	(1, 2, 4) white video level voltage
Min Luminance		0.000		V	(1, 3, 4) black video level voltage
LSB Current		73.2		µA	(4, 5)
Integral Linearity (INL)	-1.0		+1.0	LSB	(1, 6)
Differential Linearity (DNL)	-1.0		+1.0	LSB	(1, 6)
Video channel-channel voltage amplitude mismatch			6	%	(7)
Monotonicity	Guaranteed				

NOTES:
1. Measured at each R, G, B termination according to the *VESA Test Procedure - Evaluation of Analog Display Graphics Subsystems Proposal* (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude
4. Defined for a double 75-Ω termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA video signal standards.
7. Max full-scale voltage difference among R,G,B outputs (percentage of steady-state full-scale voltage).



11.4.3 TV DAC DC Characteristics

Table 55. TV DAC DC Characteristics: Functional Operating Range (VCCATVDAC [A,B,C] = 3.3 V 5%)

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution	10			Bits	Measured at low-frequency
ENOB (Effective Number of Bits)	7.5			Bits	@ NTSC/PAL Video BW
Max Luminance (full-scale)	1.235	1.3	1.365	V	For composite video signal Notes 1, 3, and 4
Max Luminance (full-scale)	1.045	1.1	1.155	V	For S-Video signal Notes 1, 3, and 4
Max Luminance (full-scale)	0.665	0.7	0.735	V	For component video signal Notes 1, 3, and 4
Min Luminance	-0.1	0	+0.1	mV	Measured at DC Note 2
Integral Linearity (INL)	-0.5		+0.5	LSB	Note 5
Differential Linearity (DNL)	-0.5		+0.5	LSB	Note 5
SNR	48			dB	RMS @ NTSC/PAL Video BW
Video channel-channel voltage amplitude mismatch	-3		+3	%	Note 6
Monotonicity	Guaranteed				

NOTES:
1. Max steady-state amplitude
2. Min steady-state amplitude
3. Defined for a double 75-Ω termination.
4. Set by external reference resistor value.
5. INL and DNL measured and calculated based on the method given in VESA video signal standards.
6. Max full-scale voltage difference among the outputs (percentage of steady-state full-scale voltage).

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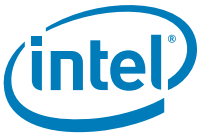
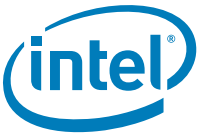




12 Strapping Configuration

Table 56. Mobile Intel 945GM/GME/PM/GMS/GU/GSE, 943/940GML and Intel 945GT Express Chipset Strapping Signals and Configuration

Pin Name	Strap Description	Configuration	Notes
CFG[2:0]	FSB Frequency Select	000 = FSB400 (Ultra Mobile only) 001 = FSB533 011 = FSB667 Others = Reserved	1,2
CFG[4:3]	Reserved		1,2
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)	1,2,3
CFG6	Reserved		1,2
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)	1
CFG8	Reserved		
CFG9	PCI Express* Graphics Lane Reversal	0 = Reverse Lanes, 15->0, 14->1 etc... 1 = Normal operation (Default): Lane Numbered in Order	1,3
CFG[11:10]	Reserved		
CFG[13:12]	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation (Default)	1
CFG[15:14]	Reserved		
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)	1
CFG17	Reserved		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present	1,2
CFG[18]	VCC Select	0 = 1.05 V (Default) 1 = 1.5 V	1
CFG[19]	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes, 3->0, 2->1 etc ***Note:*** Mobile Intel® 945GMS/GSE Express Chipset does not support DMI lane reversal	1,2
CFG[20]	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port	1,3

NOTES:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal

2. The straps marked in Brown only are available on Mobile Intel 945GMS/GSE Express Chipset. Definitions for CFG straps 3 and 6 are reserved on the Mobile Intel 945GMS/GSE Express Chipset.
3. CFG5 cannot be configured to x4 width for the Mobile Intel 945GMS/GSE Express Chipset. A pull-down is required to configure it to x2 DMI width.

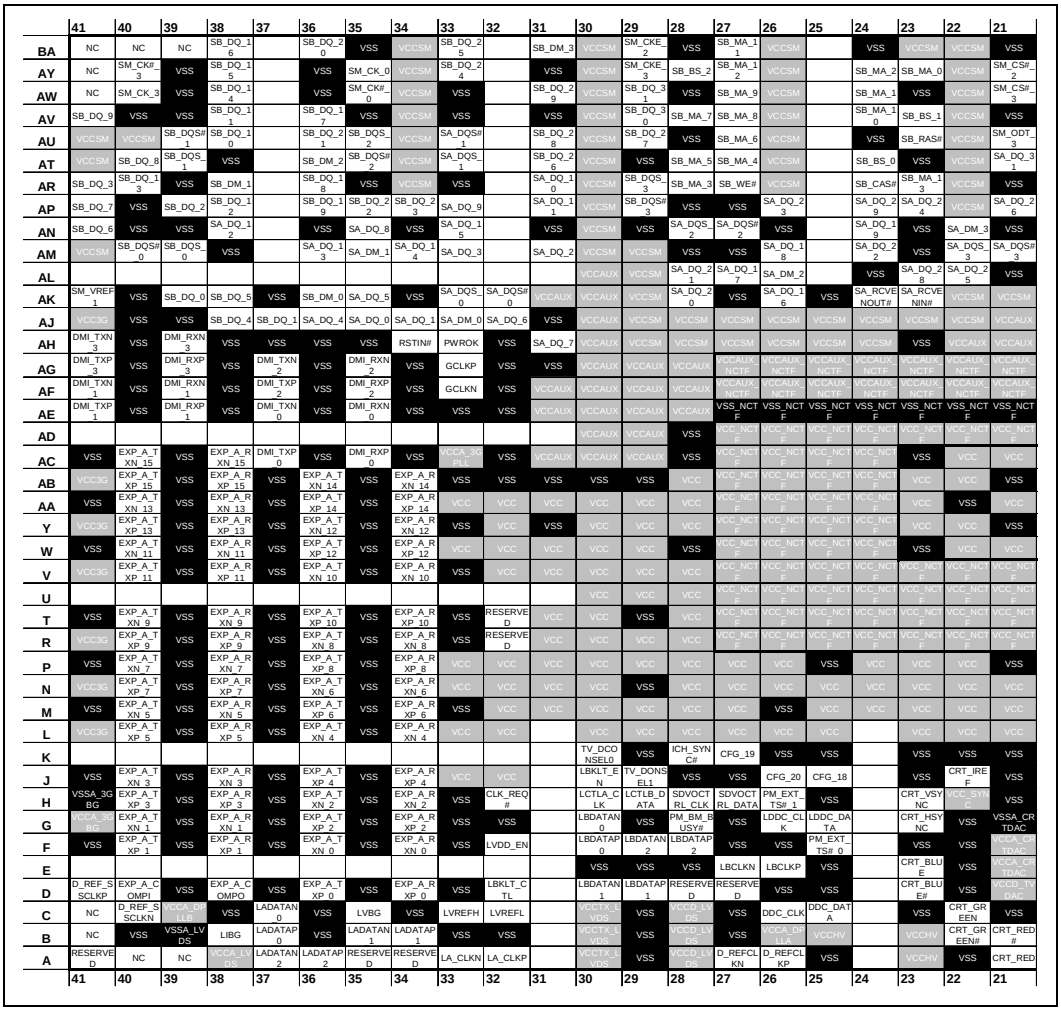
§

13 Ballout and Package Information

This section describes the ballout and pin list for the Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipsets

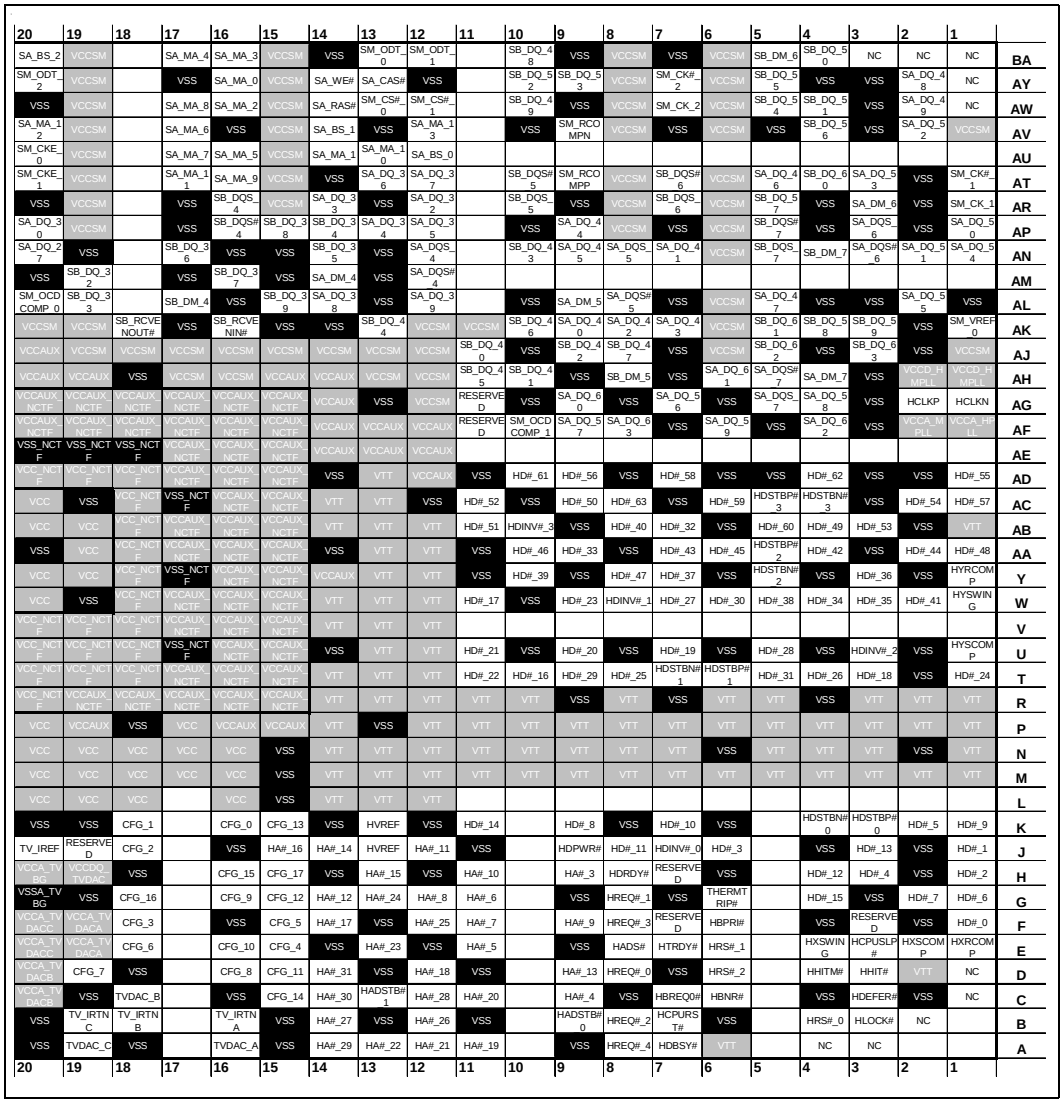
13.1 Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Ballout Diagram

Figure 29. Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Ballout Diagram (Top) Left Half

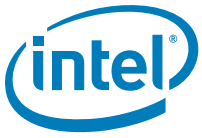


	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
BA	NC	NC	NC	SB_DQ_16		SB_DQ_20	VSS	VCCSM	SB_DQ_25		SB_DM_3	VCCSM	SM_CKE_2	VSS	SB_MA_11	VCCSM		VSS	VCCSM	VCCSM	VSS
AY	NC	SM_CK#_3	VSS	SB_DQ_15		VSS	SM_CK_0	VCCSM	SB_DQ_24		VSS	VCCSM	SM_CKE_3	SB_BS_2	SB_MA_12	VCCSM		SB_MA_2	SB_MA_0	VCCSM	SM_CS#_2
AW	NC	SM_CK_3	VSS	SB_DQ_14		VSS	SM_CK#_0	VCCSM	VSS		SB_DQ_29	VCCSM	SB_DQ_31	VSS	SB_MA_9	VCCSM		SB_MA_1	VSS	VCCSM	SM_CS#_3
AV	SB_DQ_9	VSS	VSS	SB_DQ_11		SB_DQ_17	VSS	VCCSM	VSS		VSS	VCCSM	SB_DQ_30	SB_MA_7	SB_MA_8	VCCSM		SB_MA_10	SB_BS_1	VCCSM	VSS
AU	VCCSM	VCCSM	SB_DQS#_1	SB_DQ_10		SB_DQ_21	SB_DQS_2	VCCSM	SA_DQS#_1		SB_DQ_28	VCCSM	SB_DQ_27	VSS	SB_MA_6	VCCSM		VSS	SB_RAS#	VCCSM	SM_ODT_3
AT	VCCSM	SB_DQ_8	SB_DQS_1	VSS		SB_DM_2	SB_DQS#_2	VCCSM	SA_DQS_1		SB_DQ_26	VCCSM	VSS	SB_MA_5	SB_MA_4	VCCSM		SB_BS_0	VSS	VCCSM	SA_DQ_31
AR	SB_DQ_3	SB_DQ_13	VSS	SB_DM_1		SB_DQ_18	VSS	VCCSM	VSS		SA_DQ_10	VCCSM	SB_DQS_3	SB_MA_3	SB_WE#	VCCSM		SB_CAS#	SB_MA_13	VCCSM	VSS
AP	SB_DQ_7	VSS	SB_DQ_2	SB_DQ_12		SB_DQ_19	SB_DQ_22	SB_DQ_23	SA_DQ_9		SA_DQ_11	VCCSM	SB_DQS#_3	VSS	VSS	SA_DQ_23		SA_DQ_29	SA_DQ_24	VCCSM	SA_DQ_26
AN	SB_DQ_6	VSS	VSS	SA_DQ_12		VSS	SA_DQ_8	VSS	SA_DQ_15		VSS	VCCSM	VSS	SA_DQS_2	SA_DQS#_2	VSS		SA_DQ_19	VSS	SA_DM_3	VSS
AM	VCCSM	SB_DQS#_0	SB_DQS_0	VSS		SA_DQ_13	SA_DM_1	SA_DQ_14	SA_DQ_3		SA_DQ_2	VCCSM	VCCSM	VSS	VSS	SA_DQ_18		SA_DQ_22	VSS	SA_DQS_3	SA_DQS#_3
AL												VCCAUX	VCCSM	SA_DQ_21	SA_DQ_17	SA_DM_2		VSS	SA_DQ_28	SA_DQ_25	VSS
AK	SM_VREF_1	VSS	SB_DQ_0	SB_DQ_5	VSS	SB_DM_0	SA_DQ_5	VSS	SA_DQS_0	SA_DQS#_0	VCCAUX	VCCAUX	VCCSM	SA_DQ_20	VSS	SA_DQ_16	VSS	SA_RCVENOUT#	SA_RCVENIN#	VCCSM	VCCSM
AJ	VCC3G	VSS	VSS	SB_DQ_4	SB_DQ_1	SA_DQ_4	SA_DQ_0	SA_DQ_1	SA_DM_0	SA_DQ_6	VSS	VCCAUX	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCAUX
AH	DMI_TXN_3	VSS	DMI_RXN_3	VSS	VSS	VSS	VSS	RSTIN#	PWROK	VSS	SA_DQ_7	VCCAUX	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VSS	VCCAUX	VCCAUX
AG	DMI_TXP_3	VSS	DMI_RXP_3	VSS	DMI_TXN_2	VSS	DMI_RXN_2	VSS	GCLKP	VSS	VSS	VCCAUX	VCCAUX	VCCAUX	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF
AF	DMI_TXN_1	VSS	DMI_RXN_1	VSS	DMI_TXP_2	VSS	DMI_RXP_2	VSS	GCLKN	VSS	VCCAUX	VCCAUX	VCCAUX	VCCAUX	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF
AE	DMI_TXP_1	VSS	DMI_RXP_1	VSS	DMI_TXN_0	VSS	DMI_RXN_0	VSS	VSS	VSS	VCCAUX	VCCAUX	VCCAUX	VCCAUX	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF
AD												VCCAUX	VCCAUX	VSS	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
AC	VSS	EXP_A_TXN_15	VSS	EXP_A_RXN_15	DMI_TXP_0	VSS	DMI_RXP_0	VSS	VCCA_3GPLL	VSS	VCCAUX	VCCAUX	VCCAUX	VSS	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS	VCC	VCC
AB	VCC3G	EXP_A_TXP_15	VSS	EXP_A_RXP_15	VSS	EXP_A_TXN_14	VSS	EXP_A_RXN_14	VSS	VSS	VSS	VSS	VSS	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC	VCC	VSS
AA	VSS	EXP_A_TXN_13	VSS	EXP_A_RXN_13	VSS	EXP_A_TXP_14	VSS	EXP_A_RXP_14	VCC	VCC	VCC	VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC	VSS	VCC
Y	VCC3G	EXP_A_TXP_13	VSS	EXP_A_RXP_13	VSS	EXP_A_TXN_12	VSS	EXP_A_RXN_12	VSS	VCC	VSS	VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC	VCC	VSS
W	VSS	EXP_A_TXN_11	VSS	EXP_A_RXN_11	VSS	EXP_A_TXP_12	VSS	EXP_A_RXP_12	VCC	VCC	VCC	VCC	VCC	VSS	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS	VCC	VCC
V	VCC3G	EXP_A_TXP_11	VSS	EXP_A_RXP_11	VSS	EXP_A_TXN_10	VSS	EXP_A_RXN_10	VSS	VCC	VCC	VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
U												VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
T	VSS	EXP_A_TXN_9	VSS	EXP_A_RXN_9	VSS	EXP_A_TXP_10	VSS	EXP_A_RXP_10	VSS	RESERVED	VCC	VCC	VSS	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
R	VCC3G	EXP_A_TXP_9	VSS	EXP_A_RXP_9	VSS	EXP_A_TXN_8	VSS	EXP_A_RXN_8	VSS	RESERVED	VCC	VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
P	VSS	EXP_A_TXN_7	VSS	EXP_A_RXN_7	VSS	EXP_A_TXP_8	VSS	EXP_A_RXP_8	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VCC	VSS
N	VCC3G	EXP_A_TXP_7	VSS	EXP_A_RXP_7	VSS	EXP_A_TXN_6	VSS	EXP_A_RXN_6	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC
M	VSS	EXP_A_TXN_5	VSS	EXP_A_RXN_5	VSS	EXP_A_TXP_6	VSS	EXP_A_RXP_6	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VCC	VCC	VCC
L	VCC3G	EXP_A_TXP_5	VSS	EXP_A_RXP_5	VSS	EXP_A_TXN_4	VSS	EXP_A_RXN_4	VCC	VCC		VCC	VCC	VCC	VCC	VCC	VCC		VCC	VCC	VCC
K												TV_DCONSEL0	VSS	ICH_SYNC#	CFG_19	VSS	VSS	VSS	VSS	VSS	VSS
J	VSS	EXP_A_TXN_3	VSS	EXP_A_RXN_3	VSS	EXP_A_TXP_4	VSS	EXP_A_RXP_4	VCC	VCC		LBKLT_EN	TV_DONSEL1	VSS	VSS	CFG_20	CFG_18		VSS	CRT_IREF	VSS
H	VSSA_3GBG	EXP_A_TXP_3	VSS	EXP_A_RXP_3	VSS	EXP_A_TXN_2	VSS	EXP_A_RXN_2	VSS	CLK_REQ#		LCTLA_CLK	LCTLB_DATA	SDVOCTRL_CLK	SDVOCTRL_DATA	PM_EXT_TS#_1	VSS		CRT_VSYNC	VCC_SYNC	VSS
G	VCCA_3GBG	EXP_A_TXN_1	VSS	EXP_A_RXN_1	VSS	EXP_A_TXP_2	VSS	EXP_A_RXP_2	VSS	VSS		LBDATAN0	VSS	PM_BM_BUSY#	VSS	LDDC_CLK	LDDC_DATA		CRT_HSYNC	VSS	VSSA_CRTDAC
F	VSS	EXP_A_TXP_1	VSS	EXP_A_RXP_1	VSS	EXP_A_TXN_0	VSS	EXP_A_RXN_0	VSS	LVDD_EN		LBDATAP0	LBDATAN2	LBDATAP2	VSS	VSS	PM_EXT_TS#_0		VSS	VSS	VCCA_CRTDAC
E												VSS	VSS	VSS	LBCLKN	LBCLKP	VSS		CRT_BLUE	VSS	VCCA_CRTDAC
D	D_REF_SSCLKP	EXP_A_COMPI	VSS	EXP_A_COMPO	VSS	EXP_A_TXP_0	VSS	EXP_A_RXP_0	VSS	LBKLT_CTL		LBDATAN1	LBDATAP1	RESERVED	RESERVED	VSS	VSS		CRT_BLUE#	VSS	VCCD_DAC
C	NC	D_REF_SSCLKN	VCCA_DPLL_LVDS	VSS	LADATAN0	VSS	LVBG	VSS	LVREFH	LVREFL		VCCTX_LVDS	VSS	VCCD_LVDS	VSS	DDC_CLK	DDC_DATA		VSS	CRT_GREEN	VSS
B	NC	VSS	VSSA_LVDS	LIBG	LADATAP0	VSS	LADATAN1	LADATAP1	VSS	VSS		VCCTX_LVDS	VSS	VCCD_LVDS	VSS	VCCA_DPLLA	VCCHV		VCCHV	CRT_GREEN#	CRT_RED#
A	RESERVED	NC	NC	VCCA_LVDS	LADATAN2	LADATAP2	RESERVED	RESERVED	LA_CLKN	LA_CLKP		VCCTX_LVDS	VSS	VCCD_LVDS	D_REFCLKN	D_REFCLKP	VSS		VCCHV	VSS	CRT_RED
	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21

Figure 30. Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Ballout Diagram (Top) Right Half



20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
SA_BS_2	VCCSM		SA_MA_4	SA_MA_3	VCCSM	VSS	SM_ODT_0	SM_ODT_1		SB_DQ_48	VSS	VCCSM	VSS	VCCSM	SB_DM_6	SB_DQ_50	NC	NC	NC	BA
SM_ODT_2	VCCSM		VSS	SA_MA_0	VCCSM	SA_WE#	SA_CAS#	VSS		SB_DQ_52	SB_DQ_53	VCCSM	SM_CK#_2	VCCSM	SB_DQ_55	VSS	VSS	SA_DQ_48	NC	AY
VSS	VCCSM		SA_MA_8	SA_MA_2	VCCSM	SA_RAS#	SM_CS#_0	SM_CS#_1		SB_DQ_49	VSS	VCCSM	SM_CK_2	VCCSM	SB_DQ_54	SB_DQ_51	VSS	SA_DQ_49	NC	AW
SA_MA_12	VCCSM		SA_MA_6	VSS	VCCSM	SA_BS_1	VSS	SA_MA_13		VSS	SM_RCOMPN	VCCSM	VSS	VCCSM	VSS	SB_DQ_56	VSS	SA_DQ_52	VCCSM	AV
SM_CKE_0	VCCSM		SA_MA_7	SA_MA_5	VCCSM	SA_MA_1	SA_MA_10	SA_BS_0												AU
SM_CKE_1	VCCSM		SA_MA_11	SA_MA_9	VCCSM	VSS	SA_DQ_36	SA_DQ_37		SB_DQS#5	SM_RCOMPP	VCCSM	SB_DQS#6	VCCSM	SA_DQ_46	SB_DQ_60	SA_DQ_53	VSS	SM_CK#_1	AT
VSS	VCCSM		VSS	SB_DQS_4	VCCSM	SA_DQ_33	VSS	SA_DQ_32		SB_DQS_5	VSS	VCCSM	SB_DQS_6	VCCSM	SB_DQ_57	VSS	SA_DM_6	VSS	SM_CK_1	AR
SA_DQ_30	VCCSM		VSS	SB_DQS#4	SB_DQ_38	SB_DQ_34	SA_DQ_34	SA_DQ_35		VSS	SA_DQ_44	VCCSM	VSS	VCCSM	SB_DQS#7	VSS	SA_DQS_6	VSS	SA_DQ_50	AP
SA_DQ_27	VSS		SB_DQ_36	VSS	VSS	SB_DQ_35	VSS	SA_DQS_4		SB_DQ_43	SA_DQ_45	SA_DQS_5	SA_DQ_41	VCCSM	SB_DQS_7	SB_DM_7	SA_DQS#6	SA_DQ_51	SA_DQ_54	AN
VSS	SB_DQ_32		VSS	SB_DQ_37	VSS	SA_DM_4	VSS	SA_DQS#4												AM
SM_OCDCOMP_0	SB_DQ_33		SB_DM_4	VSS	SB_DQ_39	SA_DQ_38	VSS	SA_DQ_39		VSS	SA_DM_5	SA_DQS#5	VSS	VCCSM	SA_DQ_47	VSS	VSS	SA_DQ_55	VSS	AL
VCCSM	VCCSM	SB_RCVENOUT#	VSS	SB_RCVENIN#	VSS	VSS	SB_DQ_44	VCCSM	VCCSM	SB_DQ_46	SA_DQ_40	SA_DQ_42	SA_DQ_43	VCCSM	SB_DQ_61	SB_DQ_58	SB_DQ_59	VSS	SM_VREF_0	AK
VCCAUX	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	SB_DQ_40	VSS	SB_DQ_42	SB_DQ_47	VSS	VCCSM	SB_DQ_62	VSS	SB_DQ_63	VSS	VCCSM	AJ
VCCAUX	VCCAUX	VSS	VCCSM	VCCSM	VCCAUX	VCCAUX	VCCSM	VCCSM	SB_DQ_45	SB_DQ_41	VSS	SB_DM_5	VSS	SA_DQ_61	SA_DQS#7	SA_DM_7	VSS	VCCD_HMPLL	VCCD_HMPLL	AH
VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUX	VSS	VCCSM	RESERVED	VSS	SA_DQ_60	VSS	SA_DQ_56	VSS	SA_DQS_7	SA_DQ_58	VSS	HCLKP	HCLKN	AG
VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUX	VCCAUX	VCCAUX	RESERVED	SM_OCDCOMP_1	SA_DQ_57	SA_DQ_63	VSS	SA_DQ_59	VSS	SA_DQ_62	VSS	VCCA_MPLL	VCCA_HPLL	AF
VSS_NCTF	VSS_NCTF	VSS_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUX	VCCAUX	VCCAUX												AE
VCC_NCTF	VCC_NCTF	VCC_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VSS	VTT	VCCAUX	VSS	HD#_61	HD#_56	VSS	HD#_58	VSS	VSS	HD#_62	VSS	VSS	HD#_55	AD
VCC	VSS	VCC_NCTF	VSS_NCTF	VCCAUXNCTF	VCCAUXNCTF	VTT	VTT	VSS	HD#_52	VSS	HD#_50	HD#_63	VSS	HD#_59	HDSTBP#3	HDSTBN#3	VSS	HD#_54	HD#_57	AC
VCC	VCC	VCC_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VTT	VTT	VTT	HD#_51	HDINV#_3	VSS	HD#_40	HD#_32	VSS	HD#_60	HD#_49	HD#_53	VSS	VTT	AB
VSS	VCC	VCC_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VSS	VTT	VTT	VSS	HD#_46	HD#_33	VSS	HD#_43	HD#_45	HDSTBP#2	HD#_42	VSS	HD#_44	HD#_48	AA
VCC	VCC	VCC_NCTF	VSS_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUX	VTT	VTT	VSS	HD#_39	VSS	HD#_47	HD#_37	VSS	HDSTBN#2	VSS	HD#_36	VSS	HYRCOMP	Y
VCC	VSS	VCC_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VTT	VTT	VTT	HD#_17	VSS	HD#_23	HDINV#_1	HD#_27	HD#_30	HD#_38	HD#_34	HD#_35	HD#_41	HYSWING	W
VCC_NCTF	VCC_NCTF	VCC_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VTT	VTT	VTT												V
VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS_NCTF	VCCAUXNCTF	VCCAUXNCTF	VSS	VTT	VTT	HD#_21	VSS	HD#_20	VSS	HD#_19	VSS	HD#_28	VSS	HDINV#_2	VSS	HYSCOMP	U
VCC_NCTF	VCC_NCTF	VCC_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VTT	VTT	VTT	HD#_22	HD#_16	HD#_29	HD#_25	HDSTBN#1	HDSTBP#1	HD#_31	HD#_26	HD#_18	VSS	HD#_24	T
VCC_NCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VCCAUXNCTF	VTT	VTT	VTT	VTT	VTT	VSS	VTT	VSS	VTT	VTT	VSS	VTT	VTT	VTT	R
VCC	VCCAUX	VSS	VCC	VCCAUX	VCCAUX	VTT	VSS	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	P
VCC	VCC	VCC	VCC	VCC	VSS	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VSS	VTT	VTT	VTT	VSS	VTT	N
VCC	VCC	VCC	VCC	VCC	VSS	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	M
VCC	VCC	VCC		VCC	VSS	VTT	VTT	VTT												L
VSS	VSS	CFG_1		CFG_0	CFG_13	VSS	HVREF	VSS	HD#_14		HD#_8	VSS	HD#_10	VSS		HDSTBN#0	HDSTBP#0	HD#_5	HD#_9	K
TV_IREF	RESERVED	CFG_2		VSS	HA#_16	HA#_14	HVREF	HA#_11	VSS		HDPWR#	HD#_11	HDINV#_0	HD#_3		VSS	HD#_13	VSS	HD#_1	J
VCCA_TVBG	VCCDQ_TVDAC	VSS		CFG_15	CFG_17	VSS	HA#_15	VSS	HA#_10		HA#_3	HDRDY#	RESERVED	VSS		HD#_12	HD#_4	VSS	HD#_2	H
VSSA_TVBG	VSS	CFG_16		CFG_9	CFG_12	HA#_12	HA#_24	HA#_8	HA#_6		VSS	HREQ#_1	VSS	THERMTRIP#		HD#_15	VSS	HD#_7	HD#_6	G
VCCA_TDACC	VCCA_TVDACA	CFG_3		VSS	CFG_5	HA#_17	VSS	HA#_25	HA#_7		HA#_9	HREQ#_3	RESERVED	HBPRI#		VSS	RESERVED	VSS	HD#_0	F
VCCA_TVDCC	VCCA_TVDCA	CFG_6		CFG_10	CFG_4	VSS	HA#_23	VSS	HA#_5		VSS	HADS#	HTRDY#	HRS#_1		HXSWING	HCPUSLP#	HXSCOMP	HXRCOMP	E
VCCA_TDACB	CFG_7	VSS		CFG_8	CFG_11	HA#_31	VSS	HA#_18	VSS		HA#_13	HREQ#_0	VSS	HRS#_2		HHITM#	HHIT#	VTT	NC	D
VCCA_TDACB	VSS	TVDAC_B		VSS	CFG_14	HA#_30	HADSTB#1	HA#_28	HA#_20		HA#_4	VSS	HBREQ0#	HBNR#		VSS	HDEFER#	VSS	NC	C
VSS	TV_IRTNC	TV_IRTNB		TV_IRTNA	VSS	HA#_27	VSS	HA#_26	VSS		HADSTB#0	HREQ#_2	HCPURST#	VSS		HRS#_0	HLOCK#	NC		B
VSS	TVDAC_C	VSS		TVDAC_A	VSS	HA#_29	HA#_22	HA#_21	HA#_19		VSS	HREQ#_4	HDBSY#	VTT		NC	NC			A
20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	



13.2 Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Pin List

Please refer to Chapter 2 for specific details on pin functionality.

Table 57. Host Interface Signals (Sheet 1 of 2)

Ball	Signal
E8	HADS#
C6	HBNR#
F6	HBPRI#
C7	HBREQ0#
B7	HCPURST#
A7	HDBSY#
C3	HDEFER#
J7	HDINV#_0
W8	HDINV#_1
U3	HDINV#_2
AB10	HDINV#_3
H8	HDRDY#
H11	HA#_10
J12	HA#_11
G14	HA#_12
D9	HA#_13
J14	HA#_14
H13	HA#_15
J15	HA#_16
F14	HA#_17
D12	HA#_18
A11	HA#_19
C11	HA#_20
A12	HA#_21
A13	HA#_22
E13	HA#_23
G13	HA#_24
F12	HA#_25
B12	HA#_26
B14	HA#_27
C12	HA#_28
A14	HA#_29
H9	HA#_3
C14	HA#_30

Ball	Signal
D14	HA#_31
C9	HA#_4
E11	HA#_5
G11	HA#_6
F11	HA#_7
G12	HA#_8
F9	HA#_9
B9	HADSTB#_0
C13	HADSTB#_1
F1	HD#_0
J1	HD#_1
K7	HD#_10
J8	HD#_11
H4	HD#_12
J3	HD#_13
K11	HD#_14
G4	HD#_15
T10	HD#_16
W11	HD#_17
T3	HD#_18
U7	HD#_19
H1	HD#_2
U9	HD#_20
U11	HD#_21
T11	HD#_22
W9	HD#_23
T1	HD#_24
T8	HD#_25
T4	HD#_26
W7	HD#_27
U5	HD#_28
T9	HD#_29
J6	HD#_3
W6	HD#_30

Ball	Signal
T5	HD#_31
AB7	HD#_32
AA9	HD#_33
W4	HD#_34
W3	HD#_35
Y3	HD#_36
Y7	HD#_37
W5	HD#_38
Y10	HD#_39
H3	HD#_4
AB8	HD#_40
W2	HD#_41
AA4	HD#_42
AA7	HD#_43
AA2	HD#_44
AA6	HD#_45
AA10	HD#_46
Y8	HD#_47
AA1	HD#_48
AB4	HD#_49
K2	HD#_5
AC9	HD#_50
AB11	HD#_51
AC11	HD#_52
AB3	HD#_53
AC2	HD#_54
AD1	HD#_55
AD9	HD#_56
AC1	HD#_57
AD7	HD#_58
AC6	HD#_59
G1	HD#_6
AB5	HD#_60
AD10	HD#_61

Table 57. Host Interface Signals (Sheet 2 of 2)

Ball	Signal
AD4	HD#_62
AC8	HD#_63
G2	HD#_7
K9	HD#_8
K1	HD#_9
K4	HDSTBN#_0
T7	HDSTBN#_1
Y5	HDSTBN#_2
AC4	HDSTBN#_3
K3	HDSTBP#_0

Ball	Signal
T6	HDSTBP#_1
AA5	HDSTBP#_2
AC5	HDSTBP#_3
D3	HHIT#
D4	HHITM#
B3	HLOCK#
D8	HREQ#_0
G8	HREQ#_1
B8	HREQ#_2
F8	HREQ#_3

Ball	Signal
A8	HREQ#_4
E7	HTRDY#
B4	HRS#_0
E6	HRS#_1
D6	HRS#_2
J9	HDPWR#
E3	HCPUSLP#
G6	THRMTRIP#

Table 58. Host Reference and Compensation Signals

Ball	Signal
J13	HVREF
K13	HVREF
E1	HXRCOMP
E2	HXSCOMP
E4	HXSWING
Y1	HYRCOMP
U1	HYSCOMP
W1	HYSWING

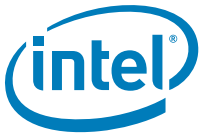


Table 59. DDR2 Channel A Signals

Ball	Signal
AJ35	SA_DQ_0
AJ34	SA_DQ_1
AR31	SA_DQ_10
AP31	SA_DQ_11
AN38	SA_DQ_12
AM36	SA_DQ_13
AM34	SA_DQ_14
AN33	SA_DQ_15
AK26	SA_DQ_16
AL27	SA_DQ_17
AM26	SA_DQ_18
AN24	SA_DQ_19
AM31	SA_DQ_2
AK28	SA_DQ_20
AL28	SA_DQ_21
AM24	SA_DQ_22
AP26	SA_DQ_23
AP23	SA_DQ_24
AL22	SA_DQ_25
AP21	SA_DQ_26
AN20	SA_DQ_27
AL23	SA_DQ_28
AP24	SA_DQ_29
AM33	SA_DQ_3
AP20	SA_DQ_30
AT21	SA_DQ_31
AR12	SA_DQ_32
AR14	SA_DQ_33
AP13	SA_DQ_34
AP12	SA_DQ_35
AT13	SA_DQ_36
AT12	SA_DQ_37
AL14	SA_DQ_38
AL12	SA_DQ_39
AJ36	SA_DQ_4

Ball	Signal
AK7	SA_DQ_43
AP9	SA_DQ_44
AN9	SA_DQ_45
AT5	SA_DQ_46
AL5	SA_DQ_47
AY2	SA_DQ_48
AW2	SA_DQ_49
AK35	SA_DQ_5
AP1	SA_DQ_50
AN2	SA_DQ_51
AV2	SA_DQ_52
AT3	SA_DQ_53
AN1	SA_DQ_54
AL2	SA_DQ_55
AG7	SA_DQ_56
AF9	SA_DQ_57
AG4	SA_DQ_58
AF6	SA_DQ_59
AJ32	SA_DQ_6
AG9	SA_DQ_60
AH6	SA_DQ_61
AF4	SA_DQ_62
AF8	SA_DQ_63
AH31	SA_DQ_7
AN35	SA_DQ_8
AP33	SA_DQ_9
AJ33	SA_DM_0
AM35	SA_DM_1
AL26	SA_DM_2
AN22	SA_DM_3
AM14	SA_DM_4
AL9	SA_DM_5
AR3	SA_DM_6
AH4	SA_DM_7
AK32	SA_DQS#_0

Ball	Signal
AM12	SA_DQS#_4
AL8	SA_DQS#_5
AN3	SA_DQS#_6
AH5	SA_DQS#_7
AK33	SA_DQS_0
AT33	SA_DQS_1
AN28	SA_DQS_2
AM22	SA_DQS_3
AN12	SA_DQS_4
AN8	SA_DQS_5
AP3	SA_DQS_6
AG5	SA_DQS_7
AY16	SA_MA_0
AU14	SA_MA_1
AU13	SA_MA_10
AT17	SA_MA_11
AV20	SA_MA_12
AV12	SA_MA_13
AW16	SA_MA_2
BA16	SA_MA_3
BA17	SA_MA_4
AU16	SA_MA_5
AV17	SA_MA_6
AU17	SA_MA_7
AW17	SA_MA_8
AT16	SA_MA_9
AU12	SA_BS_0
AV14	SA_BS_1
BA20	SA_BS_2
AW14	SA_RAS#
AY13	SA_CAS#
AY14	SA_WE#
AK23	SA_RCVENIN#
AK24	SA_RCVENOUT#

Table 59. DDR2 Channel A Signals

Ball	Signal	Ball	Signal	Ball	Signal
AK9	SA_DQ_40	AU33	SA_DQS#_1		
AN7	SA_DQ_41	AN27	SA_DQS#_2		
AK8	SA_DQ_42	AM21	SA_DQS#_3		

Table 60. DDR2 Channel B Signals (Sheet 1 of 2)

Ball	Signal	Ball	Signal	Ball	Signal
AK39	SB_DQ_0	AN10	SB_DQ_43	AP16	SB_DQS#_4
AJ37	SB_DQ_1	AK13	SB_DQ_44	AT10	SB_DQS#_5
AU38	SB_DQ_10	AH11	SB_DQ_45	AT7	SB_DQS#_6
AV38	SB_DQ_11	AK10	SB_DQ_46	AP5	SB_DQS#_7
AP38	SB_DQ_12	AJ8	SB_DQ_47	AM39	SB_DQS_0
AR40	SB_DQ_13	BA10	SB_DQ_48	AT39	SB_DQS_1
AW38	SB_DQ_14	AW10	SB_DQ_49	AU35	SB_DQS_2
AY38	SB_DQ_15	AK38	SB_DQ_5	AR29	SB_DQS_3
BA38	SB_DQ_16	BA4	SB_DQ_50	AR16	SB_DQS_4
AV36	SB_DQ_17	AW4	SB_DQ_51	AR10	SB_DQS_5
AR36	SB_DQ_18	AY10	SB_DQ_52	AR7	SB_DQS_6
AP36	SB_DQ_19	AY9	SB_DQ_53	AN5	SB_DQS_7
AP39	SB_DQ_2	AW5	SB_DQ_54	AY23	SB_MA_0
BA36	SB_DQ_20	AY5	SB_DQ_55	AW24	SB_MA_1
AU36	SB_DQ_21	AV4	SB_DQ_56	AV24	SB_MA_10
AP35	SB_DQ_22	AR5	SB_DQ_57	BA27	SB_MA_11
AP34	SB_DQ_23	AK4	SB_DQ_58	AY27	SB_MA_12
AY33	SB_DQ_24	AK3	SB_DQ_59	AR23	SB_MA_13
BA33	SB_DQ_25	AN41	SB_DQ_6	AY24	SB_MA_2
AT31	SB_DQ_26	AT4	SB_DQ_60	AR28	SB_MA_3
AU29	SB_DQ_27	AK5	SB_DQ_61	AT27	SB_MA_4
AU31	SB_DQ_28	AJ5	SB_DQ_62	AT28	SB_MA_5
AW31	SB_DQ_29	AJ3	SB_DQ_63	AU27	SB_MA_6
AR41	SB_DQ_3	AP41	SB_DQ_7	AV28	SB_MA_7
AV29	SB_DQ_30	AT40	SB_DQ_8	AV27	SB_MA_8
AW29	SB_DQ_31	AV41	SB_DQ_9	AW27	SB_MA_9
AM19	SB_DQ_32	AK36	SB_DM_0	AT24	SB_BS_0
AL19	SB_DQ_33	AR38	SB_DM_1	AV23	SB_BS_1
AP14	SB_DQ_34	AT36	SB_DM_2	AY28	SB_BS_2
AN14	SB_DQ_35	BA31	SB_DM_3	AU23	SB_RAS#
AN17	SB_DQ_36	AL17	SB_DM_4	AR24	SB_CAS#

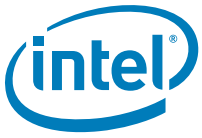


Table 60. DDR2 Channel B Signals (Sheet 2 of 2)

Ball	Signal
AM16	SB_DQ_37
AP15	SB_DQ_38
AL15	SB_DQ_39
AJ38	SB_DQ_4
AJ11	SB_DQ_40
AH10	SB_DQ_41
AJ9	SB_DQ_42

Ball	Signal
AH8	SB_DM_5
BA5	SB_DM_6
AN4	SB_DM_7
AM40	SB_DQS#_0
AU39	SB_DQS#_1
AT35	SB_DQS#_2
AP29	SB_DQS#_3

Ball	Signal
AR27	SB_WE#
AK16	SB_RCVENIN#
AK18	SB_RCVENOUT#

Table 61. DDR2 Common Signals

Ball	Signal
AW35	SM_CK#_0
AT1	SM_CK#_1
AY7	SM_CK#_2
AY40	SM_CK#_3
AY35	SM_CK_0
AR1	SM_CK_1
AW7	SM_CK_2
AW40	SM_CK_3
AW13	SM_CS#_0
AW12	SM_CS#_1
AY21	SM_CS#_2
AW21	SM_CS#_3
AU20	SM_CKE_0
AT20	SM_CKE_1
BA29	SM_CKE_2
AY29	SM_CKE_3
BA13	SM_ODT_0
BA12	SM_ODT_1
AY20	SM_ODT_2
AU21	SM_ODT_3

Table 62. DDR2 Reference and Compensation Signals

Ball	Signal
AV9	SM_RCOMPN
AT9	SM_RCOMPP
AK1	SM_VREF_0

Ball	Signal
AK41	SM_VREF_1
AL20	SM_OCDCOMP0
AF10	SM_OCDCOMP1

Table 63. PEG Interface Signals

Ball	Signal
F34	EXP_A_RXN_0
G38	EXP_A_RXN_1
V34	EXP_A_RXN_10
W38	EXP_A_RXN_11
Y34	EXP_A_RXN_12
AA38	EXP_A_RXN_13
AB34	EXP_A_RXN_14
AC38	EXP_A_RXN_15
H34	EXP_A_RXN_2
J38	EXP_A_RXN_3
L34	EXP_A_RXN_4
M38	EXP_A_RXN_5
N34	EXP_A_RXN_6
P38	EXP_A_RXN_7
R34	EXP_A_RXN_8
T38	EXP_A_RXN_9
D34	EXP_A_RXP_0
F38	EXP_A_RXP_1
T34	EXP_A_RXP_10
V38	EXP_A_RXP_11
W34	EXP_A_RXP_12
Y38	EXP_A_RXP_13
AA34	EXP_A_RXP_14
AB38	EXP_A_RXP_15
G34	EXP_A_RXP_2
H38	EXP_A_RXP_3
J34	EXP_A_RXP_4
L38	EXP_A_RXP_5
M34	EXP_A_RXP_6
N38	EXP_A_RXP_7
P34	EXP_A_RXP_8
R38	EXP_A_RXP_9
F36	EXP_A_TXN_0

Ball	Signal
G40	EXP_A_TXN_1
V36	EXP_A_TXN_10
W40	EXP_A_TXN_11
Y36	EXP_A_TXN_12
AA40	EXP_A_TXN_13
AB36	EXP_A_TXN_14
AC40	EXP_A_TXN_15
H36	EXP_A_TXN_2
J40	EXP_A_TXN_3
L36	EXP_A_TXN_4
M40	EXP_A_TXN_5
N36	EXP_A_TXN_6
P40	EXP_A_TXN_7
R36	EXP_A_TXN_8
T40	EXP_A_TXN_9
D36	EXP_A_TXP_0
F40	EXP_A_TXP_1
T36	EXP_A_TXP_10
V40	EXP_A_TXP_11
W36	EXP_A_TXP_12
Y40	EXP_A_TXP_13
AA36	EXP_A_TXP_14
AB40	EXP_A_TXP_15
G36	EXP_A_TXP_2
H40	EXP_A_TXP_3
J36	EXP_A_TXP_4
L40	EXP_A_TXP_5
M36	EXP_A_TXP_6
N40	EXP_A_TXP_7
P36	EXP_A_TXP_8
R40	EXP_A_TXP_9
D40	EXP_A_COMPI
D38	EXP_A_COMPO

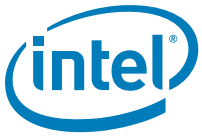


Table 64. DMI Signals

Ball	Signal	Ball	Signal
AE35	DMI_RXN_0	AE37	DMI_TXN_0
AF39	DMI_RXN_1	AF41	DMI_TXN_1
AG35	DMI_RXN_2	AG37	DMI_TXN_2
AH39	DMI_RXN_3	AH41	DMI_TXN_3
AC35	DMI_RXP_0	AC37	DMI_TXP_0
AE39	DMI_RXP_1	AE41	DMI_TXP_1
AF35	DMI_RXP_2	AF37	DMI_TXP_2
AG39	DMI_RXP_3	AG41	DMI_TXP_3

Table 65. CRT DAC Signals

Ball	Signal
A21	CRT_RED
B21	CRT_RED#
C22	CRT_GREEN
B22	CRT_GREEN#
E23	CRT_BLUE
D23	CRT_BLUE#
J22	CRT_IREF
G23	CRT_HSYNC
H23	CRT_VSYNC

Table 66. Analog TV-out Signals

Ball	Signal
A16	TVDAC_A
C18	TVDAC_B
A19	TVDAC_C
B16	TV_IRTNA
B18	TV_IRTNB
B19	TV_IRTNC
J20	TV_IREF
J29	TV_DCONSEL1
K30	TV_DCONSEL0

Table 67. LVDS Signals

Ball	Signal
C37	LADATAN_0
B35	LADATAN_1
A37	LADATAN_2
B37	LADATAP_0
B34	LADATAP_1
A36	LADATAP_2
A33	LA_CLKN
A32	LA_CLKP
F30	LBDATAP_0
D29	LBDATAP_1
F28	LBDATAP_2
G30	LBDATAN_0
D30	LBDATAN_1
F29	LBDATAN_2
E27	LBCLKN
E26	LBCLKP
F32	LVDD_EN
J30	LBKLT_EN
D32	LBKLT_CTL
B38	LIBG
C33	LVREFH
C32	LVREFL
C35	LVBG

Table 68. Display Data Channel Signals

Ball	Signal
H30	LCTLA_CLK
H29	LCTLB_DATA
C26	CRT_DDC_CLK
C25	CRT_DDC_DATA
G26	LDDC_CLK
G25	LDDC_DATA
H28	SDVOCTRL_CLK
H27	SDVOCTRL_DATA

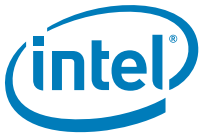


Table 69. PLL Signals

Ball	Signal
H32	CLK_REQ#
AG1	HCLKINN
AG2	HCLKINP
AF33	GCLKINN
AG33	GCLKINP
A27	D_REFCLKN
A26	D_REFCLKP
C40	D_REF_SSCLKN
D41	D_REF_SSCLKP

Table 70. Reset and Miscellaneous Signals

Ball	Signal
AH34	RSTIN#
AH33	PWROK
K16	CFG_0
K18	CFG_1
E16	CFG_10
D15	CFG_11
G15	CFG_12
K15	CFG_13
C15	CFG_14
H16	CFG_15
G18	CFG_16
H15	CFG_17
J25	CFG_18
K27	CFG_19

Ball	Signal
J18	CFG_2
J26	CFG_20
F18	CFG_3
E15	CFG_4
F15	CFG_5
E18	CFG_6
D19	CFG_7
D16	CFG_8
G16	CFG_9
G28	PM_BM_BUSY#
F25	PM_EXTTS0#
H26	PM_EXTTS1#
K28	PM_ICHSYNC#

Table 71. Reserved Signals

Ball	Signal
A35	RESERVED
A34	RESERVED
D28	RESERVED
D27	RESERVED
A41	RESERVED
AF11	RESERVED
AG11	RESERVED

Ball	Signal
F3	RESERVED
F7	RESERVED
H7	RESERVED
J19	RESERVED
R32	RESERVED
T32	RESERVED

Table 72. No Connect Signals

Ball	Signal
A3	NC
A39	NC
A4	NC
A40	NC
AW1	NC
AW41	NC
AY1	NC
AY41	NC
B2	NC
B41	NC
BA1	NC
BA2	NC
BA3	NC
BA39	NC
BA40	NC
BA41	NC
C1	NC
C41	NC
D1	NC

Table 73. Power and Ground Signals (Sheet 1 of 9)

Ball	Signal
AA19	VCC
AA21	VCC
AA23	VCC
AA28	VCC
AA29	VCC
AA30	VCC
AA31	VCC
AA32	VCC
AA33	VCC
AB19	VCC
AB20	VCC
AB22	VCC
AB23	VCC
AB28	VCC

Ball	Signal
M20	VCC
M21	VCC
M22	VCC
M23	VCC
M24	VCC
M25	VCC
M27	VCC
M28	VCC
M29	VCC
M30	VCC
M31	VCC
M32	VCC
N16	VCC
N17	VCC

Ball	Signal
P30	VCC
P31	VCC
P32	VCC
P33	VCC
R28	VCC
R29	VCC
R30	VCC
R31	VCC
T28	VCC
T30	VCC
T31	VCC
U28	VCC
U29	VCC
U30	VCC

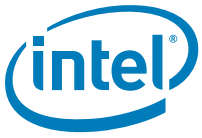


Table 73. Power and Ground Signals (Sheet 2 of 9)

Ball	Signal
AC20	VCC
AC21	VCC
AC22	VCC
J32	VCC
J33	VCC
L16	VCC
L18	VCC
L19	VCC
L20	VCC
L21	VCC
L22	VCC
L23	VCC
L25	VCC
L26	VCC
L27	VCC
L28	VCC
L29	VCC
L30	VCC
L32	VCC
L33	VCC
M16	VCC
M17	VCC
M18	VCC
M19	VCC
N19	VCC
N20	VCC
N21	VCC
N22	VCC
N23	VCC
N24	VCC
N25	VCC
N26	VCC
N27	VCC
N28	VCC
N30	VCC
N31	VCC
N32	VCC
N33	VCC

Ball	Signal
N18	VCC
P22	VCC
P23	VCC
P24	VCC
P26	VCC
P27	VCC
P28	VCC
P29	VCC
V29	VCC
V30	VCC
V31	VCC
V32	VCC
W20	VCC
W21	VCC
W22	VCC
W29	VCC
W30	VCC
W31	VCC
W32	VCC
W33	VCC
Y19	VCC
Y20	VCC
Y22	VCC
Y23	VCC
Y28	VCC
Y29	VCC
Y30	VCC
Y32	VCC
N10	VTT
A6	VTT
AA12	VTT
AA13	VTT
AB1	VTT
AB12	VTT
AB13	VTT
AB14	VTT
AC13	VTT
AC14	VTT

Ball	Signal
V28	VCC
L12	VTT
L13	VTT
L14	VTT
M1	VTT
M10	VTT
M11	VTT
M12	VTT
M13	VTT
M14	VTT
M2	VTT
M3	VTT
M4	VTT
M5	VTT
M6	VTT
M7	VTT
M8	VTT
M9	VTT
N1	VTT
N11	VTT
N12	VTT
N13	VTT
N14	VTT
N3	VTT
N4	VTT
N5	VTT
N7	VTT
N8	VTT
N9	VTT
P1	VTT
P10	VTT
P11	VTT
P12	VTT
P14	VTT
P2	VTT
P3	VTT
P4	VTT
P5	VTT

Table 73. Power and Ground Signals (Sheet 3 of 9)

Ball	Signal
P17	VCC
P20	VCC
P8	VTT
P9	VTT
R1	VTT
R10	VTT
R11	VTT
R12	VTT
R13	VTT
R14	VTT
R2	VTT
R3	VTT
R5	VTT
R6	VTT
R8	VTT
T12	VTT
T13	VTT
T14	VTT
U12	VTT
U13	VTT
V12	VTT
V13	VTT
V14	VTT
W12	VTT
W13	VTT
W14	VTT
Y12	VTT
Y13	VTT
AV19	VCCSM
AV22	VCCSM
AV26	VCCSM
AV30	VCCSM
AV34	VCCSM
AV6	VCCSM
AV8	VCCSM
AW15	VCCSM
AW19	VCCSM
AW22	VCCSM

Ball	Signal
AD13	VTT
D2	VTT
AL29	VCCSM
AV15	VCCSM
AG12	VCCSM
AH12	VCCSM
AH13	VCCSM
AH16	VCCSM
AH17	VCCSM
AH24	VCCSM
AH25	VCCSM
AH26	VCCSM
AH27	VCCSM
AH28	VCCSM
AH29	VCCSM
AJ1	VCCSM
AJ12	VCCSM
AJ13	VCCSM
AJ14	VCCSM
AJ15	VCCSM
AJ16	VCCSM
AJ17	VCCSM
AJ18	VCCSM
AJ19	VCCSM
AJ22	VCCSM
AJ23	VCCSM
AJ24	VCCSM
AJ25	VCCSM
AJ26	VCCSM
AJ27	VCCSM
AJ28	VCCSM
AJ29	VCCSM
AJ6	VCCSM
AK11	VCCSM
AK12	VCCSM
AK19	VCCSM
AK20	VCCSM
AK21	VCCSM

Ball	Signal
P6	VTT
P7	VTT
AL6	VCCSM
AM29	VCCSM
AM30	VCCSM
AM41	VCCSM
AN30	VCCSM
AN6	VCCSM
AP19	VCCSM
AP22	VCCSM
AP30	VCCSM
AP6	VCCSM
AP8	VCCSM
AR15	VCCSM
AR19	VCCSM
AR22	VCCSM
AR26	VCCSM
AR30	VCCSM
AR34	VCCSM
AR6	VCCSM
AR8	VCCSM
AT15	VCCSM
AT19	VCCSM
AT22	VCCSM
AT26	VCCSM
AT30	VCCSM
AT34	VCCSM
AT41	VCCSM
AT6	VCCSM
AT8	VCCSM
AU15	VCCSM
AU19	VCCSM
AU22	VCCSM
AU26	VCCSM
AU30	VCCSM
AU34	VCCSM
AU40	VCCSM
AU41	VCCSM

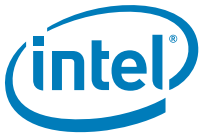


Table 73. Power and Ground Signals (Sheet 4 of 9)

Ball	Signal
AW26	VCCSM
AW30	VCCSM
AW34	VCCSM
AW6	VCCSM
AW8	VCCSM
AY15	VCCSM
AY19	VCCSM
AY22	VCCSM
AY26	VCCSM
AY30	VCCSM
AY34	VCCSM
AY6	VCCSM
AY8	VCCSM
BA15	VCCSM
BA19	VCCSM
BA22	VCCSM
BA23	VCCSM
BA26	VCCSM
BA30	VCCSM
BA34	VCCSM
BA6	VCCSM
BA8	VCCSM
AB41	VCC3G
AJ41	VCC3G
L41	VCC3G
V41	VCC3G
Y41	VCC3G
G41	VCCA_3GBG
H41	VSSA_3GBG
AF1	VCCA_HPLL
AF2	VCCA_MPLL
AH1	VCCD_HMPLL
AH2	VCCD_HMPLL
AC33	VCCA_3GPLL
B26	VCCA_DPLLA
C39	VCCA_DPLLB
A23	VCCHV
B23	VCCHV

Ball	Signal
AK22	VCCSM
AK29	VCCSM
AK6	VCCSM
H22	VCC_SYNC
A28	VCCD_LVDS
B28	VCCD_LVDS
C28	VCCD_LVDS
A30	VCCTX_LVDS
B30	VCCTX_LVDS
C30	VCCTX_LVDS
A38	VCCA_LVDS
B39	VSSA_LVDS
H20	VCCA_TVBG
G20	VSSA_TVBG
D21	VCCD_TVDAC
H19	VCCDQ_TVDAC
E19	VCCA_TVDACA
F19	VCCA_TVDACA
C20	VCCA_TVDACB
D20	VCCA_TVDACB
E20	VCCA_TVDACC
F20	VCCA_TVDACC
AC29	VCCAUX
AC30	VCCAUX
AC31	VCCAUX
AD12	VCCAUX
AD29	VCCAUX
AD30	VCCAUX
AE12	VCCAUX
AE13	VCCAUX
AE14	VCCAUX
AE28	VCCAUX
AE29	VCCAUX
AE30	VCCAUX
AE31	VCCAUX
AF12	VCCAUX
AF13	VCCAUX
AF14	VCCAUX

Ball	Signal
AV1	VCCSM
N41	VCC3G
R41	VCC3G
AG28	VCCAUX
AG29	VCCAUX
AG30	VCCAUX
AH14	VCCAUX
AH15	VCCAUX
AH19	VCCAUX
AH20	VCCAUX
AH21	VCCAUX
AH22	VCCAUX
AH30	VCCAUX
AJ20	VCCAUX
AJ21	VCCAUX
AJ30	VCCAUX
AK30	VCCAUX
AK31	VCCAUX
AL30	VCCAUX
P15	VCCAUX
P16	VCCAUX
P19	VCCAUX
Y14	VCCAUX
AG14	VCCAUX
R20	VCC_NCTF
R21	VCC_NCTF
R22	VCC_NCTF
R23	VCC_NCTF
R24	VCC_NCTF
R25	VCC_NCTF
R26	VCC_NCTF
R27	VCC_NCTF
T18	VCC_NCTF
T19	VCC_NCTF
T20	VCC_NCTF
T21	VCC_NCTF
T22	VCC_NCTF
T23	VCC_NCTF

Table 73. Power and Ground Signals (Sheet 5 of 9)

Ball	Signal
B25	VCCHV
E21	VCCA_CRTDAC
F21	VCCA_CRTDAC
G21	VSSA_CRTDAC
AD27	VCC_NCTF
V26	VCC_NCTF
V27	VCC_NCTF
W18	VCC_NCTF
W24	VCC_NCTF
W25	VCC_NCTF
W26	VCC_NCTF
Y18	VCC_NCTF
Y24	VCC_NCTF
Y25	VCC_NCTF
Y26	VCC_NCTF
Y27	VCC_NCTF
AD24	VCC_NCTF
V24	VCC_NCTF
W27	VCC_NCTF
AA18	VCC_NCTF
AA24	VCC_NCTF
AA25	VCC_NCTF
AA26	VCC_NCTF
AA27	VCC_NCTF
AB18	VCC_NCTF
AB24	VCC_NCTF
AB25	VCC_NCTF
AB26	VCC_NCTF
AB27	VCC_NCTF
AC18	VCC_NCTF
AC24	VCC_NCTF
AC25	VCC_NCTF
AC26	VCC_NCTF
AC27	VCC_NCTF
AD18	VCC_NCTF
AD19	VCC_NCTF
AD20	VCC_NCTF
AD21	VCC_NCTF

Ball	Signal
AF28	VCCAUX
AF29	VCCAUX
AF30	VCCAUX
AF31	VCCAUX
T26	VCC_NCTF
T27	VCC_NCTF
U18	VCC_NCTF
U19	VCC_NCTF
U20	VCC_NCTF
U21	VCC_NCTF
U22	VCC_NCTF
U23	VCC_NCTF
U24	VCC_NCTF
U25	VCC_NCTF
U26	VCC_NCTF
U27	VCC_NCTF
V18	VCC_NCTF
V19	VCC_NCTF
V20	VCC_NCTF
V21	VCC_NCTF
AG26	VCCAUX_NCTF
AG27	VCCAUX_NCTF
R15	VCCAUX_NCTF
AB17	VCCAUX_NCTF
AD17	VCCAUX_NCTF
T17	VCCAUX_NCTF
AF25	VCCAUX_NCTF
AF26	VCCAUX_NCTF
AF27	VCCAUX_NCTF
AG15	VCCAUX_NCTF
AG16	VCCAUX_NCTF
AG17	VCCAUX_NCTF
AG18	VCCAUX_NCTF
AG19	VCCAUX_NCTF
AG20	VCCAUX_NCTF
AG21	VCCAUX_NCTF
AG22	VCCAUX_NCTF
AG23	VCCAUX_NCTF

Ball	Signal
T24	VCC_NCTF
T25	VCC_NCTF
AD25	VCC_NCTF
AD26	VCC_NCTF
V17	VCCAUX_NCTF
AA15	VCCAUX_NCTF
AA16	VCCAUX_NCTF
AB15	VCCAUX_NCTF
AB16	VCCAUX_NCTF
AC15	VCCAUX_NCTF
AC16	VCCAUX_NCTF
AD15	VCCAUX_NCTF
AD16	VCCAUX_NCTF
AE15	VCCAUX_NCTF
AE16	VCCAUX_NCTF
AF15	VCCAUX_NCTF
AF16	VCCAUX_NCTF
AF17	VCCAUX_NCTF
AF18	VCCAUX_NCTF
AF19	VCCAUX_NCTF
AF20	VCCAUX_NCTF
AF21	VCCAUX_NCTF
AF22	VCCAUX_NCTF
AF23	VCCAUX_NCTF
AF24	VCCAUX_NCTF
R19	VCCAUX_NCTF
T15	VCCAUX_NCTF
T16	VCCAUX_NCTF
U15	VCCAUX_NCTF
U16	VCCAUX_NCTF
V15	VCCAUX_NCTF
V16	VCCAUX_NCTF
W15	VCCAUX_NCTF
W16	VCCAUX_NCTF
Y15	VCCAUX_NCTF
Y16	VCCAUX_NCTF
AA17	VCCAUX_NCTF
AE17	VCCAUX_NCTF

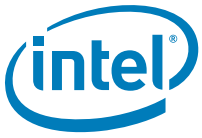


Table 73. Power and Ground Signals (Sheet 6 of 9)

Ball	Signal	Ball	Signal	Ball	Signal
AD22	VCC_NCTF	AG24	VCCAUX_NCTF	W17	VCCAUX_NCTF
AD23	VCC_NCTF	AG25	VCCAUX_NCTF	Y17	VSS_NCTF
V22	VCC_NCTF	R16	VCCAUX_NCTF	AC17	VSS_NCTF
V23	VCC_NCTF	R17	VCCAUX_NCTF	AE18	VSS_NCTF
V25	VCC_NCTF	R18	VCCAUX_NCTF	AE19	VSS_NCTF
AE23	VSS_NCTF	Y39	VSS	W39	VSS
AE24	VSS_NCTF	Y4	VSS	W41	VSS
AE25	VSS_NCTF	Y6	VSS	Y11	VSS
AE26	VSS_NCTF	Y9	VSS	Y2	VSS
AE27	VSS_NCTF	P21	VSS	Y21	VSS
U17	VSS_NCTF	P25	VSS	Y31	VSS
AE20	VSS_NCTF	P35	VSS	Y33	VSS
AE21	VSS_NCTF	P37	VSS	Y35	VSS
AE22	VSS_NCTF	P39	VSS	Y37	VSS
A15	VSS	AC41	VSS	AH35	VSS
A18	VSS	AC7	VSS	AH36	VSS
A20	VSS	AD11	VSS	AH37	VSS
A22	VSS	AD14	VSS	AH38	VSS
A25	VSS	AD2	VSS	AH40	VSS
A29	VSS	AD28	VSS	AH7	VSS
A9	VSS	AD3	VSS	AH9	VSS
AA11	VSS	AD5	VSS	AJ10	VSS
AA14	VSS	AD6	VSS	AJ2	VSS
AA20	VSS	AD8	VSS	AJ31	VSS
AA22	VSS	AE32	VSS	AJ39	VSS
AA3	VSS	AE33	VSS	AJ4	VSS
AA35	VSS	AE34	VSS	AJ40	VSS
AA37	VSS	AE36	VSS	AJ7	VSS
AA39	VSS	AE38	VSS	AK14	VSS
AA41	VSS	AE40	VSS	AK15	VSS
AA8	VSS	AF3	VSS	AK17	VSS
AB2	VSS	AF32	VSS	AK2	VSS
AB21	VSS	AF34	VSS	AK25	VSS
AB29	VSS	AF36	VSS	AK27	VSS
AB30	VSS	AF38	VSS	AK34	VSS
AB31	VSS	AF40	VSS	AK37	VSS
AB32	VSS	AF5	VSS	AK40	VSS
AB33	VSS	AF7	VSS	AL1	VSS

Table 73. Power and Ground Signals (Sheet 7 of 9)

Ball	Signal
AB35	VSS
AB37	VSS
AB39	VSS
AB6	VSS
AB9	VSS
AC10	VSS
AC12	VSS
AC19	VSS
AC23	VSS
AC28	VSS
AC3	VSS
AC32	VSS
AC34	VSS
AC36	VSS
AC39	VSS
AM38	VSS
AN13	VSS
AN15	VSS
AN16	VSS
AN19	VSS
AN21	VSS
AN23	VSS
AN26	VSS
AN29	VSS
AN31	VSS
AN34	VSS
AN36	VSS
AN39	VSS
AN40	VSS
AP10	VSS
AP17	VSS
AP2	VSS
AP27	VSS
AP28	VSS
AP4	VSS
AP40	VSS
AP7	VSS
AR13	VSS

Ball	Signal
AG10	VSS
AG13	VSS
AG3	VSS
AG31	VSS
AG32	VSS
AG34	VSS
AG36	VSS
AG38	VSS
AG40	VSS
AG6	VSS
AG8	VSS
AH18	VSS
AH23	VSS
AH3	VSS
AH32	VSS
AV13	VSS
AV16	VSS
AV21	VSS
AV3	VSS
AV31	VSS
AV33	VSS
AV35	VSS
AV39	VSS
AV40	VSS
AV5	VSS
AV7	VSS
AW20	VSS
AW23	VSS
AW28	VSS
AW3	VSS
AW33	VSS
AW36	VSS
AW39	VSS
AW9	VSS
AY12	VSS
AY17	VSS
AY3	VSS
AY31	VSS

Ball	Signal
AL10	VSS
AL13	VSS
AL16	VSS
AL21	VSS
AL24	VSS
AL3	VSS
AL4	VSS
AL7	VSS
AM13	VSS
AM15	VSS
AM17	VSS
AM20	VSS
AM23	VSS
AM27	VSS
AM28	VSS
BA28	VSS
BA35	VSS
BA7	VSS
BA9	VSS
C16	VSS
C19	VSS
C2	VSS
C21	VSS
C23	VSS
C27	VSS
C29	VSS
C34	VSS
C36	VSS
C38	VSS
C4	VSS
C8	VSS
D11	VSS
D13	VSS
D18	VSS
D22	VSS
D25	VSS
D26	VSS
D33	VSS

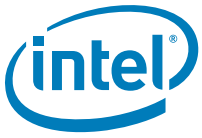


Table 73. Power and Ground Signals (Sheet 8 of 9)

Ball	Signal	Ball	Signal	Ball	Signal
AR17	VSS	AY36	VSS	D35	VSS
AR2	VSS	AY39	VSS	D37	VSS
AR20	VSS	AY4	VSS	D39	VSS
AR21	VSS	B11	VSS	D7	VSS
AR33	VSS	B13	VSS	E12	VSS
AR35	VSS	B15	VSS	E14	VSS
AR39	VSS	B20	VSS	E22	VSS
AR4	VSS	B27	VSS	E25	VSS
AR9	VSS	B29	VSS	E28	VSS
AT14	VSS	B32	VSS	E29	VSS
AT2	VSS	B33	VSS	E30	VSS
AT23	VSS	B36	VSS	E9	VSS
AT29	VSS	B40	VSS	F13	VSS
AT38	VSS	B6	VSS	F16	VSS
AU24	VSS	BA14	VSS	F2	VSS
AU28	VSS	BA21	VSS	F22	VSS
AV10	VSS	BA24	VSS	F23	VSS
F26	VSS	J39	VSS	P41	VSS
F27	VSS	J4	VSS	R33	VSS
F33	VSS	J41	VSS	R35	VSS
F35	VSS	K12	VSS	R37	VSS
F37	VSS	K14	VSS	R39	VSS
F39	VSS	K19	VSS	R4	VSS
F4	VSS	K20	VSS	R7	VSS
F41	VSS	K21	VSS	R9	VSS
G19	VSS	K22	VSS	T2	VSS
G22	VSS	K23	VSS	T29	VSS
G27	VSS	K25	VSS	T33	VSS
G29	VSS	K26	VSS	T35	VSS
G3	VSS	K29	VSS	T37	VSS
G32	VSS	K6	VSS	T39	VSS
G33	VSS	K8	VSS	T41	VSS
G35	VSS	L15	VSS	U10	VSS
G37	VSS	L35	VSS	U14	VSS
G39	VSS	L37	VSS	U2	VSS
G7	VSS	L39	VSS	U4	VSS
G9	VSS	M15	VSS	U6	VSS
H12	VSS	M26	VSS	U8	VSS

Table 73. Power and Ground Signals (Sheet 9 of 9)

Ball	Signal
H14	VSS
H18	VSS
H2	VSS
H21	VSS
H25	VSS
H33	VSS
H35	VSS
H37	VSS
H39	VSS
H6	VSS
J11	VSS
J16	VSS
J2	VSS
J21	VSS
J23	VSS
J27	VSS
J28	VSS
J35	VSS
J37	VSS

Ball	Signal
M33	VSS
M35	VSS
M37	VSS
M39	VSS
M41	VSS
N15	VSS
N2	VSS
N29	VSS
N35	VSS
N37	VSS
N39	VSS
N6	VSS
P13	VSS
P18	VSS
W35	VSS
W37	VSS

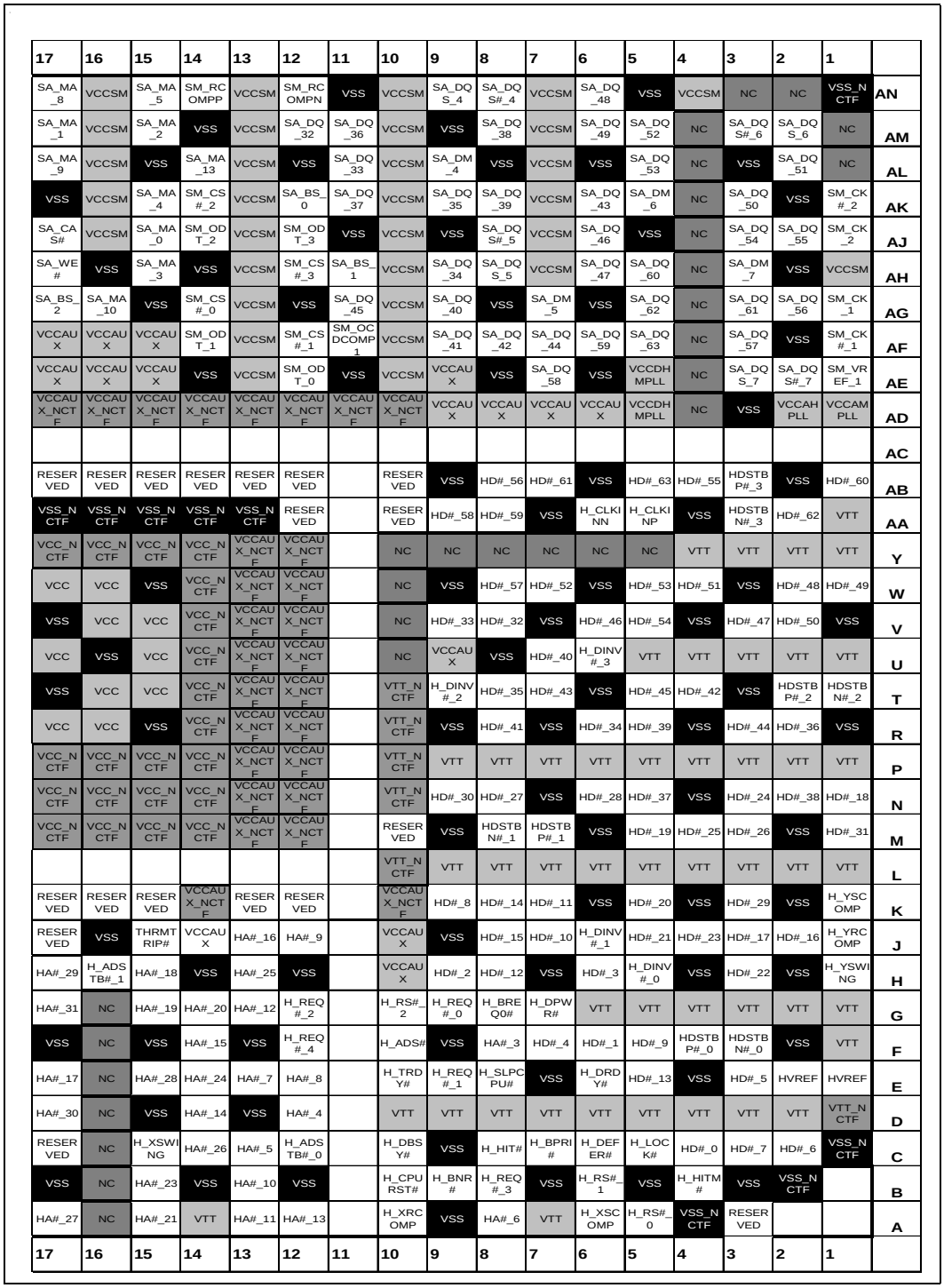
Ball	Signal
V33	VSS
V35	VSS
V37	VSS
V39	VSS
W10	VSS
W19	VSS
W23	VSS
W28	VSS

13.3 Mobile Intel 945GMS/GSE Express Chipset Ballout Diagram

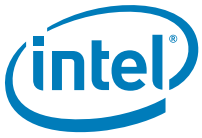
Figure 31. Mobile Intel 945GMS/GSE Express Chipset Ballout Diagram (Top) Left Half

	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
AN	VSS_NCTF	NC	NC	SM_CK#_3	VCCSM	SA_RCVENIN#	SA_DQ_24	SA_DQ_29	VSS	VCCSM		SM_CKE_1	SM_CKE_0	SB_MA_0	NC	VCCSM
AM	NC	VCCSM	VSS	SM_CK_3	VCCSM	SA_RCVENOUT#	VSS	SA_DQ_25	SA_DQS#_3	VCCSM		VSS	SB_MA_8	VSS	NC	VSS
AL	NC	SA_DQ_13	SA_DM_1	VSS	VCCSM	SA_DQ_10	SA_DQ_28	VSS	SA_DQS_3	VCCSM		SB_MA_4	SB_MA_1	SB_MA_10	NC	SA_MA_11
AK	SA_DQS_2	VSS	SA_DQ_9	SA_DQS#_1	VCCSM	VSS	SA_DQ_11	SA_DM_3	VSS	VCCSM		SB_MA_3	SB_MA_2	VSS	NC	SA_RAS#
AJ	SA_DQS#_2	SA_DQ_20	VSS	SA_DQS_1	VCCSM	SA_DQ_14	SA_DQ_15	SA_DQ_26	SA_DQ_27	VCCSM		VSS	SM_OCDCOMP0	SB_BS_1	NC	SA_MA_6
AH	VSS	SA_DQ_16	SA_DQ_8	SA_DQ_12	VCCSM	VSS	SA_DQ_18	VSS	SA_DQ_30	VCCSM		SB_MA_5	SB_BS_0	VSS	NC	VSS
AG	SM_CK#_0	VSS	SA_DQ_21		VCCSM	SA_DQ_22	SA_DQ_23	SA_DQ_31	VSS	VCCSM		SB_MA_6	SB_RAS#	SB_WE#	SB_CAS#	SA_MA_12
AF	SM_CK_0	SA_DQ_3	SA_DQ_17	SA_DM_2	VCCSM	SA_DQ_19	VSS	SM_CKE_2	SM_CKE_3	VCCSM		VSS	SB_MA_7	VSS	SA_MA_7	VSS
AE	SA_DQ_2	VSS	SA_DQ_7	VSS	VCCSM	VSS	SB_BS_2	SB_MA_12	VSS	VCCSM		SB_MA_11	SB_MA_9	SB_MA_13	VCCAUX	VCCAUX
AD	VCCAUX	VCCAUX	VCCAUX	VCCAUX	VCCAUX	VCCAUX	VCCAUX	VCCAUX	VCCAUX_NCTF	VCCAUX_NCTF		VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF
AC	SA_DQ_4	VSS	SA_DQ_0	VSS	SA_DQS#_0	SA_DQS_0	VCCAUX	VCCAUX	VCCAUX_NCTF	VCCAUX_NCTF						
AB	VCCSM	SA_DQ_5	SA_DQ_6	SA_DM_0	PWROK	SA_DQ_1	VSS	VCCAUX	VCCAUX_NCTF	RESERVED		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
AA	SM_VREF_0	VSS	VSS	VSS	VSS	VSS	VSS	G_CLKINP	VSS_NCTF	RESERVED		VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF
Y	VSS	DMI_RXN_1	DMI_RXP_1	VSS	DMI_RXN_0	DMI_RXP_0	VSS	G_CLKINN	RESERVED	RESERVED		VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
W	NC	NC	NC	NC	NC	NC	RSTIN#	VSS	NC	RESERVED		VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS	VCC
V	VSS	DMI_TXP_1	DMI_TXN_1	VSS	DMI_TXP_0	DMI_TXN_0	NC	VCCA3GPLL	VSS_NCTF	NC		VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC	VCC
U	VCC3G	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS_NCTF	NC		VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC	VSS
T	VCC3G	SDVO_CLKN	VSS	SDVO_FLDSTALL	SDVO_FLDSTALL#	VSS	VSS	VCC	VCC_NCTF	RESERVED		VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC	VCC
R	VSS	SDVO_CLKP	VSS	SDVOB_INT#	VSS	EXP_A_COMPI	VSS	VCC	VCC_NCTF	RESERVED		VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS	VCC
P	SDVO_BLUE	SDVO_BLUE#	VSS	SDVOB_INT	VSS	SDVO_RED#	VSS	VCC	VCC_NCTF	VCC_NCTF		VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
N	VCCA3GBG	SDVO_GREEN#	VSS	SDVO_TVCLKIN#	VSS	SDVO_RED	VSS	VCC	VCC_NCTF	VCC_NCTF		VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
M	VSSA3GBG	SDVO_GREEN	VSS	SDVO_TVCLKIN	VSS	EXP_A_ICOMPO	VSS	VCC	VCC_NCTF	VCC_NCTF		VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
L																
K	NC	RESERVED	RESERVED	L_VDDEN	L_VREFL	CFG_19	L_IBG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	NC
J	D_REFSSCLKINN	VCCADPLLB	VSS	L_VREFH	L_VBG	VSS	SDVO_CTRLCLK	TV_DCONSEL_1	VSS	NC	VCCSYNC	CLKREQ#	VSS	CFG_5	NC	CFG_6
H	D_REFSSCLKINP	VSS	LA_DATAP_0	L_BKLTCTL	VSS	L_DDC_DATA	SDVO_CTRLDATA	PM_EXTTS#_1	CRT_IREF	NC	VSS	CRT_DDC_DATA	VSS	CRT_DDC_CLK	NC	VSS
G	VSS	LA_DATAP_1	LA_DATAN_0	VSS	L_BKLTEN	L_DDC_CLK	VSS	TV_DCONSEL_0	VSS	NC	TV_IREF	VSS	PM_BMBUSY#	CFG_2	NC	CFG_3
F	LB_DATAN_0	LA_DATAN_1	VSS	LB_DATAN_2	LB_DATAP_2	L_CLKCTLA	CRT_VSYNC	PM_EXTTS#_0	CRT_GREEN#	NC	VSS	VCCDQTVDAC	VSS	VCCDTVDAC	NC	RESERVED
E	LB_DATAP_0	VSS	ICH_SYNC#	VSS	VSS	L_CTLBDATA	VSS	VCCHV	CRT_GREEN	NC	VSSATVBG	VSS	NC	TV_DACC_OUT	NC	CFG_1
D	LB_DATAN_1	LB_DATAP_1	LA_DATAN_2	LA_CLKN	VCCTX_LVDS	VSS	CRT_HSYNC	VCCHV	CRT_RED#	NC	VCCATVBG	VCCATVDACC	TV_IRTNC	VSS	NC	VSS
C	NC	VSS	LA_DATAP_2	LA_CLKP	VCCTX_LVDS	VCCD_LVDS	VSS	VCCHV	CRT_RED	VCCACRTDAC	NC	VCCATVDACC	TV_IRTNB	TV_DACB_OUT	NC	CFG_0
B	NC	VSSALVDS	VCCALVDS	VSS	VSS	VCCD_LVDS	VSS	VCCADPLLA	VSSACRTDAC	VCCACRTDAC	VSS	VCCATVDACB	TV_IRTNA	VCCATVDACA	NC	HA#_22
A	VSS_NCTF	NC	NC	LB_CLKN	LB_CLKP	VCCD_LVDS	D_REFCLKINN	D_REFCLKINP	VSS	CRT_BLUE	CRT_BLUE#	VCCATVDACB	TV_DACA_OUT	VCCATVDACA	NC	RESERVED
	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18

Figure 32. Mobile Intel 945GMS/GSE Express Chipset Ballout Diagram (Top) Right Half



17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
SA_MA_8	VCCSM	SA_MA_5	SM_RCOMPP	VCCSM	SM_RCOMPN	VSS	VCCSM	SA_DQS_4	SA_DQS#_4	VCCSM	SA_DQ_48	VSS	VCCSM	NC	NC	VSS_NCTF	AN
SA_MA_1	VCCSM	SA_MA_2	VSS	VCCSM	SA_DQ_32	SA_DQ_36	VCCSM	VSS	SA_DQ_38	VCCSM	SA_DQ_49	SA_DQ_52	NC	SA_DQS#_6	SA_DQS_6	NC	AM
SA_MA_9	VCCSM	VSS	SA_MA_13	VCCSM	VSS	SA_DQ_33	VCCSM	SA_DM_4	VSS	VCCSM	VSS	SA_DQ_53	NC	VSS	SA_DQ_51	NC	AL
VSS	VCCSM	SA_MA_4	SM_CS#_2	VCCSM	SA_BS_0	SA_DQ_37	VCCSM	SA_DQ_35	SA_DQ_39	VCCSM	SA_DQ_43	SA_DM_6	NC	SA_DQ_50	VSS	SM_CK#_2	AK
SA_CAS#	VCCSM	SA_MA_0	SM_ODT_2	VCCSM	SM_ODT_3	VSS	VCCSM	VSS	SA_DQS#_5	VCCSM	SA_DQ_46	VSS	NC	SA_DQ_54	SA_DQ_55	SM_CK_2	AJ
SA_WE#	VSS	SA_MA_3	VSS	VCCSM	SM_CS#_3	SA_BS_1	VCCSM	SA_DQ_34	SA_DQS_5	VCCSM	SA_DQ_47	SA_DQ_60	NC	SA_DM_7	VSS	VCCSM	AH
SA_BS_2	SA_MA_10	VSS	SM_CS#_0	VCCSM	VSS	SA_DQ_45	VCCSM	SA_DQ_40	VSS	SA_DM_5	VSS	SA_DQ_62	NC	SA_DQ_61	SA_DQ_56	SM_CK_1	AG
VCCAUX	VCCAUX	VCCAUX	SM_ODT_1	VCCSM	SM_CS#_1	SM_OCDCOMP1	VCCSM	SA_DQ_41	SA_DQ_42	SA_DQ_44	SA_DQ_59	SA_DQ_63	NC	SA_DQ_57	VSS	SM_CK#_1	AF
VCCAUX	VCCAUX	VCCAUX	VSS	VCCSM	SM_ODT_0	VSS	VCCSM	VCCAUX	VSS	SA_DQ_58	VSS	VCCDHMPLL	NC	SA_DQS_7	SA_DQS#_7	SM_VREF_1	AE
VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX_NCTF	VCCAUX	VCCAUX	VCCAUX	VCCAUX	VCCDHMPLL	NC	VSS	VCCAHPLL	VCCAMPLL	AD
																	AC
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		RESERVED	VSS	HD#_56	HD#_61	VSS	HD#_63	HD#_55	HDSTBP#_3	VSS	HD#_60	AB
VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	RESERVED		RESERVED	HD#_58	HD#_59	VSS	H_CLKINN	H_CLKINP	VSS	HDSTBN#_3	HD#_62	VTT	AA
VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		NC	NC	NC	NC	NC	NC	VTT	VTT	VTT	VTT	Y
VCC	VCC	VSS	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		NC	VSS	HD#_57	HD#_52	VSS	HD#_53	HD#_51	VSS	HD#_48	HD#_49	W
VSS	VCC	VCC	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		NC	HD#_33	HD#_32	VSS	HD#_46	HD#_54	VSS	HD#_47	HD#_50	VSS	V
VCC	VSS	VCC	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		NC	VCCAUX	VSS	HD#_40	H_DINV#_3	VTT	VTT	VTT	VTT	VTT	U
VSS	VCC	VCC	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		VTT_NCTF	H_DINV#_2	HD#_35	HD#_43	VSS	HD#_45	HD#_42	VSS	HDSTBP#_2	HDSTBN#_2	T
VCC	VCC	VSS	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		VTT_NCTF	VSS	HD#_41	VSS	HD#_34	HD#_39	VSS	HD#_44	HD#_36	VSS	R
VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		VTT_NCTF	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	P
VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		VTT_NCTF	HD#_30	HD#_27	VSS	HD#_28	HD#_37	VSS	HD#_24	HD#_38	HD#_18	N
VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCCAUX_NCTF	VCCAUX_NCTF		RESERVED	VSS	HDSTBN#_1	HDSTBP#_1	VSS	HD#_19	HD#_25	HD#_26	VSS	HD#_31	M
							VTT_NCTF	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	L
RESERVED	RESERVED	RESERVED	VCCAUX_NCTF	RESERVED	RESERVED		VCCAUX_NCTF	HD#_8	HD#_14	HD#_11	VSS	HD#_20	VSS	HD#_29	VSS	H_YSCOMP	K
RESERVED	VSS	THRMTRIP#	VCCAUX	HA#_16	HA#_9		VCCAUX	VSS	HD#_15	HD#_10	H_DINV#_1	HD#_21	HD#_23	HD#_17	HD#_16	H_YRCOMP	J
HA#_29	H_ADSTB#_1	HA#_18	VSS	HA#_25	VSS		VCCAUX	HD#_2	HD#_12	VSS	HD#_3	H_DINV#_0	VSS	HD#_22	VSS	H_YSWING	H
HA#_31	NC	HA#_19	HA#_20	HA#_12	H_REQ#_2		H_RS#_2	H_REQ#_0	H_BREQ0#	H_DPWR#	VTT	VTT	VTT	VTT	VTT	VTT	G
VSS	NC	VSS	HA#_15	VSS	H_REQ#_4		H_ADS#	VSS	HA#_3	HD#_4	HD#_1	HD#_9	HDSTBP#_0	HDSTBN#_0	VSS	VTT	F
HA#_17	NC	HA#_28	HA#_24	HA#_7	HA#_8		H_TRDY#	H_REQ#_1	H_SLPCPU#	VSS	H_DRDY#	HD#_13	VSS	HD#_5	HVREF	HVREF	E
HA#_30	NC	VSS	HA#_14	VSS	HA#_4		VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT_NCTF	D
RESERVED	NC	H_XSWING	HA#_26	HA#_5	H_ADSTB#_0		H_DBSY#	VSS	H_HIT#	H_BPRI#	H_DEFER#	H_LOCK#	HD#_0	HD#_7	HD#_6	VSS_NCTF	C
VSS	NC	HA#_23	VSS	HA#_10	VSS		H_CPURST#	H_BNR#	H_REQ#_3	VSS	H_RS#_1	VSS	H_HITM#	VSS	VSS_NCTF		B
HA#_27	NC	HA#_21	VTT	HA#_11	HA#_13		H_XRCOMP	VSS	HA#_6	VTT	H_XSCOMP	H_RS#_0	VSS_NCTF	RESERVED			A
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	



13.4 Mobile Intel 945GMS/GSE Express Chipset Pin List

Please refer to Chapter 2 for specific details on pin functionality.

Table 74. Host Interface Signals

Ball	Signal
B13	H_A#_10
A13	H_A#_11
G13	H_A#_12
A12	H_A#_13
D14	H_A#_14
F14	H_A#_15
J13	H_A#_16
E17	H_A#_17
H15	H_A#_18
G15	H_A#_19
G14	H_A#_20
A15	H_A#_21
B18	H_A#_22
B15	H_A#_23
E14	H_A#_24
H13	H_A#_25
C14	H_A#_26
A17	H_A#_27
E15	H_A#_28
H17	H_A#_29
F8	H_A#_3
D17	H_A#_30
G17	H_A#_31
D12	H_A#_4
C13	H_A#_5
A8	H_A#_6
E13	H_A#_7
E12	H_A#_8
J12	H_A#_9
F10	H_ADS#
C12	H_ADSTB#_0
H16	H_ADSTB#_1
B9	H_BNR#
C7	H_BPRI#
G8	H_BREQ0#

Ball	Signal
B10	H_CPURST#
C4	H_D#_0
F6	H_D#_1
J7	H_D#_10
K7	H_D#_11
H8	H_D#_12
E5	H_D#_13
K8	H_D#_14
J8	H_D#_15
J2	H_D#_16
J3	H_D#_17
N1	H_D#_18
M5	H_D#_19
H9	H_D#_2
K5	H_D#_20
J5	H_D#_21
H3	H_D#_22
J4	H_D#_23
N3	H_D#_24
M4	H_D#_25
M3	H_D#_26
N8	H_D#_27
N6	H_D#_28
K3	H_D#_29
H6	H_D#_3
N9	H_D#_30
M1	H_D#_31
V8	H_D#_32
V9	H_D#_33
R6	H_D#_34
T8	H_D#_35
R2	H_D#_36
N5	H_D#_37
N2	H_D#_38
R5	H_D#_39

Ball	Signal
F7	H_D#_4
U7	H_D#_40
R8	H_D#_41
T4	H_D#_42
T7	H_D#_43
R3	H_D#_44
T5	H_D#_45
V6	H_D#_46
V3	H_D#_47
W2	H_D#_48
W1	H_D#_49
E3	H_D#_5
V2	H_D#_50
W4	H_D#_51
W7	H_D#_52
W5	H_D#_53
V5	H_D#_54
AB4	H_D#_55
AB8	H_D#_56
W8	H_D#_57
AA9	H_D#_58
AA8	H_D#_59
C2	H_D#_6
AB1	H_D#_60
AB7	H_D#_61
AA2	H_D#_62
AB5	H_D#_63
C3	H_D#_7
K9	H_D#_8
F5	H_D#_9
C10	H_DBSY#
C6	H_DEFER#
E8	H_SLPCPU#
E10	H_TRDY#
H5	H_DINV#_0

Ball	Signal
J6	H_DINV#_1
T9	H_DINV#_2
U6	H_DINV#_3
G7	H_DPWR#
E6	H_DRDY#
F3	H_DSTBN#_0
M8	H_DSTBN#_1
T1	H_DSTBN#_2
AA3	H_DSTBN#_3
F4	H_DSTBP#_0
M7	H_DSTBP#_1
T2	H_DSTBP#_2
AB3	H_DSTBP#_3
C8	H_HIT#
B4	H_HITM#
C5	H_LOCK#
G9	H_REQ#_0
E9	H_REQ#_1
G12	H_REQ#_2
B8	H_REQ#_3
F12	H_REQ#_4
A5	H_RS#_0
B6	H_RS#_1
G10	H_RS#_2
J15	THRMTRIP#

Table 75. Host Reference and Compensation Signals

Ball	Signal
E2	H_VREF
E1	H_VREF
A10	H_XRCOMP
A6	H_XSCOMP
C15	H_XSWING
J1	H_YRCOMP
K1	H_YSCOMP
H1	H_YSWING

Table 76. DDR2 Channel A Signals (Sheet 1 of 2)

Ball	Signal	Ball	Signal
AK12	SA_BS_0	AG31	SA_DQ_21
AH11	SA_BS_1	AG28	SA_DQ_22
AG17	SA_BS_2	AG27	SA_DQ_23
AJ17	SA_CAS#	AN27	SA_DQ_24
AB30	SA_DM_0	AM26	SA_DQ_25
AL31	SA_DM_1	AJ26	SA_DQ_26
AF30	SA_DM_2	AJ25	SA_DQ_27
AK26	SA_DM_3	AL27	SA_DQ_28
AL9	SA_DM_4	AN26	SA_DQ_29
AG7	SA_DM_5	AF32	SA_DQ_3
AK5	SA_DM_6	AH25	SA_DQ_30
AH3	SA_DM_7	AG26	SA_DQ_31
AC31	SA_DQ_0	AM12	SA_DQ_32
AB28	SA_DQ_1	AL11	SA_DQ_33
AL28	SA_DQ_10	AH9	SA_DQ_34
AK27	SA_DQ_11	AK9	SA_DQ_35
AH30	SA_DQ_12	AM11	SA_DQ_36
AL32	SA_DQ_13	AK11	SA_DQ_37
AJ28	SA_DQ_14	AM8	SA_DQ_38
AJ27	SA_DQ_15	AK8	SA_DQ_39
AH32	SA_DQ_16	AC33	SA_DQ_4
AF31	SA_DQ_17	AG9	SA_DQ_40
AH27	SA_DQ_18	AF9	SA_DQ_41
AF28	SA_DQ_19	AF8	SA_DQ_42
AE33	SA_DQ_2	AK6	SA_DQ_43

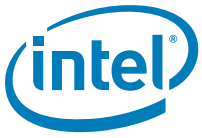


Table 76. DDR2 Channel A Signals (Sheet 2 of 2)

Ball	Signal
AJ32	SA_DQ_20
AG11	SA_DQ_45
AJ6	SA_DQ_46
AH6	SA_DQ_47
AN6	SA_DQ_48
AM6	SA_DQ_49
AB32	SA_DQ_5
AK3	SA_DQ_50
AL2	SA_DQ_51
AM5	SA_DQ_52
AL5	SA_DQ_53
AJ3	SA_DQ_54
AJ2	SA_DQ_55
AG2	SA_DQ_56
AF3	SA_DQ_57
AE7	SA_DQ_58
AF6	SA_DQ_59
AB31	SA_DQ_6
AH5	SA_DQ_60
AG3	SA_DQ_61
AG5	SA_DQ_62
AF5	SA_DQ_63
AE31	SA_DQ_7
AH31	SA_DQ_8
AK31	SA_DQ_9
AC28	SA_DQS_0
AJ30	SA_DQS_1
AK33	SA_DQS_2
AL25	SA_DQS_3
AN9	SA_DQS_4
AH8	SA_DQS_5
AM2	SA_DQS_6
AE3	SA_DQS_7

Ball	Signal
AF7	SA_DQ_44
AC29	SA_DQS#_0
AK30	SA_DQS#_1
AJ33	SA_DQS#_2
AM25	SA_DQS#_3
AN8	SA_DQS#_4
AJ8	SA_DQS#_5
AM3	SA_DQS#_6
AE2	SA_DQS#_7
AJ15	SA_MA_0
AM17	SA_MA_1
AG16	SA_MA_10
AL18	SA_MA_11
AG18	SA_MA_12
AL14	SA_MA_13
AM15	SA_MA_2
AH15	SA_MA_3
AK15	SA_MA_4
AN15	SA_MA_5
AJ18	SA_MA_6
AF19	SA_MA_7
AN17	SA_MA_8
AL17	SA_MA_9
AK18	SA_RAS#
AH17	SA_WE#
AL17	SA_MA_9
AM28	SA_RCVENOUT#
AN28	SA_RCVENIN#

Table 77. DDR2 Common Signals

Ball	Signal
AF33	SM_CK_0
AG1	SM_CK_1
AJ1	SM_CK_2
AM30	SM_CK_3
AG33	SM_CK#_0
AF1	SM_CK#_1
AK1	SM_CK#_2
AN30	SM_CK#_3
AN21	SM_CKE_0
AN22	SM_CKE_1
AF26	SM_CKE_2
AF25	SM_CKE_3
AG14	SM_CS#_0
AF12	SM_CS#_1
AK14	SM_CS#_2
AH12	SM_CS#_3
AE12	SM_ODT_0
AF14	SM_ODT_1
AJ14	SM_ODT_2
AJ12	SM_ODT_3

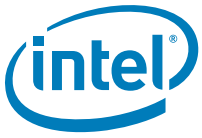


Table 78. DDR2 Additional Control Signals

Ball	Signal
AH21	SB_BS_0
AJ20	SB_BS_1
AE27	SB_BS_2
AN20	SB_MA_0
AL21	SB_MA_1
AL20	SB_MA_10
AE22	SB_MA_11
AE26	SB_MA_12
AE20	SB_MA_13
AK21	SB_MA_2
AK22	SB_MA_3
AL22	SB_MA_4
AH22	SB_MA_5
AG22	SB_MA_6
AF21	SB_MA_7
AM21	SB_MA_8
AE21	SB_MA_9
AG21	SB_RAS#
AG20	SB_WE#
AG19	SB_CAS#

Table 79. DDR2 Reference and Compensation Signals

Ball	Signals
AN12	SM_RCOMPN
AN14	SM_RCOMPP
AA33	SM_VREF_0
AE1	SM_VREF_1
AJ21	SM_OCDCOMP_0
AF11	SM_OCDCOMP_1

Table 80. DMI Signals

Ball	Signal
Y29	DMI_RXN_0
Y32	DMI_RXN_1
Y28	DMI_RXP_0
Y31	DMI_RXP_1
V28	DMI_TXN_0
V31	DMI_TXN_1
V29	DMI_TXP_0
V32	DMI_TXP_1

Table 81. CRT DAC Signals

Ball	Signal
C25	CRT_RED
D25	CRT_RED#
E25	CRT_GREEN
F25	CRT_GREEN#
A24	CRT_BLUE
A23	CRT_BLUE#
H25	CRT_IREF
D27	CRT_HSYNC
F27	CRT_VSYNC

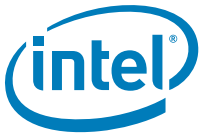


Table 82. Analog TV-out Signals

Ball	Signal
A21	TV_DACA
C20	TV_DACB
E20	TV_DACC
G26	TV_DCONSEL0
J26	TV_DCONSEL1
G23	TV_IREF
B21	TV_IRTNA
C21	TV_IRTNB
B21	TV_IRTNA
C21	TV_IRTNB
D21	TV_IRTNC

Table 83. SDVO Interface Signals

Ball	Signal
R28	EXP_A_COMPI
M28	EXP_A_ICOMPO
N30	SDVO_TVCLKIN#
R30	SDVOB_INT#
T29	SDVO_FLDSTALL#
M30	SDVO_TVCLKIN
P30	SDVOB_INT
T30	SDVO_FLDSTALL
P28	SDVOB_RED#
N32	SDVOB_GREEN#
P32	SDVOB_BLUE#
T32	SDVOB_CLKN
N28	SDVOB_RED
M32	SDVOB_GREEN
P33	SDVOB_BLUE
R32	SDVOB_CLKP

Table 84. LVDS Signals

Ball	Signal
H30	L_BKLTCTL
G29	L_BKLTEN
K27	L_IBG
J29	L_VBG
K30	L_VDDEN
J30	L_VREFH
K29	L_VREFL
D30	LA_CLKN
C30	LA_CLKP
G31	LA_DATAN_0
F32	LA_DATAN_1
D31	LA_DATAN_2
H31	LA_DATAP_0
G32	LA_DATAP_1
C31	LA_DATAP_2
A30	LB_CLKN
A29	LB_CLKP
F33	LB_DATAN_0
D33	LB_DATAN_1
F30	LB_DATAN_2
E33	LB_DATAP_0
D32	LB_DATAP_1
F29	LB_DATAP_2

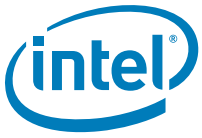


Table 85. Display Data Channel Signals

Ball	Signal
H20	CRT_DDC_CLK
H22	CRT_DDC_DATA
G28	L_DDC_CLK
H28	L_DDC_DATA
F28	L_CLKCTLA
E28	L_CTLBDATA
J27	SDVO_CTRLCLK
H27	SDVO_CTRLDATA

Table 86. PLL Signals

Ball	Signal
J22	CLKREQ#
AA6	HCLKN
AA5	HCLKP
Y26	G_CLKN
AA26	G_CLKP
A27	D_REFCLKN
A26	D_REFCLKP
J33	D_REFSSCLKN
H33	D_REFSSCLKP

Table 87. Reset and Misc. Signals

Ball	Signal
C18	CFG0
E18	CFG1
G20	CFG2
G18	CFG3
J20	CFG5
J18	CFG6
K28	CFG19
G21	PM_BMBUSY#
F26	PM_EXTTS0#
H26	PM_EXTTS1#
E31	PM_ICHSYNC#
AB29	PWROK
W27	RSTIN#

Table 88. Reserved Signal (Sheet 1 of 2)

Ball	Signal
K25	RESERVED
K26	RESERVED
K32	RESERVED
K31	RESERVED
AB13	RESERVED
AB12	RESERVED
R24	RESERVED
T24	RESERVED
M10	RESERVED
A18	RESERVED
AB10	RESERVED
AA10	RESERVED
C17	RESERVED
A3	RESERVED
K22	RESERVED
J17	RESERVED
K23	RESERVED
K17	RESERVED

Ball	Signal
AB17	RESERVED
F18	RESERVED
K15	RESERVED
K21	RESERVED
K19	RESERVED
K20	RESERVED
K24	RESERVED
Y25	RESERVED
Y24	RESERVED
AB22	RESERVED
AB21	RESERVED
AB19	RESERVED
AB16	RESERVED
AB14	RESERVED
AA12	RESERVED
W24	RESERVED
AA24	RESERVED
AB24	RESERVED

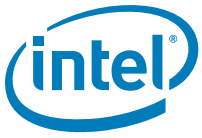


Table 88. Reserved Signal (Sheet 2 of 2)

Ball	Signal
K12	RESERVED
K13	RESERVED
K16	RESERVED

Ball	Signal
AB20	RESERVED
AB18	RESERVED
AB15	RESERVED

Table 89. No Connect Signals (Sheet 1 of 2)

Ball	Signal
Y10	NC
W33	NC
AM33	NC
AL33	NC
C33	NC
B33	NC
AN32	NC
A32	NC
W10	NC
AN31	NC
W28	NC
V27	NC
W25	NC
V24	NC
U24	NC
W29	NC
V10	NC
J24	NC
H24	NC
W32	NC
G24	NC
F24	NC
E24	NC
D24	NC
K33	NC
U10	NC
A31	NC
E21	NC
C23	NC
AN19	NC
AM19	NC

Ball	Signal
H19	NC
G19	NC
F19	NC
E19	NC
D19	NC
C19	NC
B19	NC
A19	NC
Y8	NC
K18	NC
G16	NC
F16	NC
E16	NC
D16	NC
C16	NC
B16	NC
AN2	NC
A16	NC
Y7	NC
AM4	NC
AF4	NC
AD4	NC
AL4	NC
AK4	NC
W31	NC
AJ4	NC
AH4	NC
AG4	NC
AE4	NC
AM1	NC
W30	NC

Table 89. No Connect Signals (Sheet 2 of 2)

AL19	NC
AK19	NC
AJ19	NC
AH19	NC
AN3	NC
Y9	NC
J19	NC

Y6	NC
AL1	NC
Y5	NC

Table 90. Power and Ground Signals (Sheet 1 of 5)

Ball	Signal
T26	VCC
R26	VCC
P26	VCC
N26	VCC
M26	VCC
V19	VCC
U19	VCC
T19	VCC
W18	VCC
V18	VCC
T18	VCC
R18	VCC
W17	VCC
U17	VCC
R17	VCC
W16	VCC
V16	VCC
T16	VCC
R16	VCC
V15	VCC
U15	VCC
T15	VCC
T25	VCC_NCTF
R25	VCC_NCTF
P25	VCC_NCTF
N25	VCC_NCTF
M25	VCC_NCTF
P24	VCC_NCTF

Ball	Signal
M22	VCC_NCTF
Y21	VCC_NCTF
W21	VCC_NCTF
V21	VCC_NCTF
U21	VCC_NCTF
T21	VCC_NCTF
R21	VCC_NCTF
P21	VCC_NCTF
N21	VCC_NCTF
M21	VCC_NCTF
Y20	VCC_NCTF
W20	VCC_NCTF
V20	VCC_NCTF
U20	VCC_NCTF
T20	VCC_NCTF
R20	VCC_NCTF
P20	VCC_NCTF
N20	VCC_NCTF
M20	VCC_NCTF
Y19	VCC_NCTF
P19	VCC_NCTF
N19	VCC_NCTF
M19	VCC_NCTF
Y18	VCC_NCTF
P18	VCC_NCTF
N18	VCC_NCTF
M18	VCC_NCTF
Y17	VCC_NCTF

Ball	Signal
M15	VCC_NCTF
Y14	VCC_NCTF
W14	VCC_NCTF
V14	VCC_NCTF
U14	VCC_NCTF
T14	VCC_NCTF
R14	VCC_NCTF
P14	VCC_NCTF
N14	VCC_NCTF
M14	VCC_NCTF
U33	VCC3G
T33	VCC3G
N33	VCCA3GBG
V26	VCCA3GPLL
C24	VCCACRTDAC
B24	VCCACRTDAC
B26	VCCADPLLA
J32	VCCADPLLB
AD2	VCCAHPLL
B31	VCCALVDS
AD1	VCCAMPLL
D23	VCCATVBG
B20	VCCATVDACA
A20	VCCATVDACA
B22	VCCATVDACB
A22	VCCATVDACB
D22	VCCATVDACC
C22	VCCATVDACC

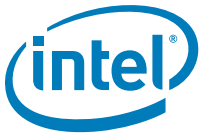


Table 90. Power and Ground Signals (Sheet 2 of 5)

Ball	Signal
N24	VCC_NCTF
M24	VCC_NCTF
Y22	VCC_NCTF
W22	VCC_NCTF
V22	VCC_NCTF
U22	VCC_NCTF
T22	VCC_NCTF
R22	VCC_NCTF
P22	VCC_NCTF
N22	VCC_NCTF
AB26	VCCAUX
AE19	VCCAUX
AE18	VCCAUX
AF17	VCCAUX
AE17	VCCAUX
AF16	VCCAUX
AE16	VCCAUX
AF15	VCCAUX
AE15	VCCAUX
J14	VCCAUX
J10	VCCAUX
H10	VCCAUX
AE9	VCCAUX
AD9	VCCAUX
U9	VCCAUX
AD8	VCCAUX
AD7	VCCAUX
AD6	VCCAUX
AD25	VCCAUX_NCTF
AC25	VCCAUX_NCTF
AB25	VCCAUX_NCTF
AD24	VCCAUX_NCTF
AC24	VCCAUX_NCTF
AD22	VCCAUX_NCTF
AD21	VCCAUX_NCTF
AD20	VCCAUX_NCTF
AD19	VCCAUX_NCTF
AD18	VCCAUX_NCTF

Ball	Signal
P17	VCC_NCTF
N17	VCC_NCTF
M17	VCC_NCTF
Y16	VCC_NCTF
P16	VCC_NCTF
N16	VCC_NCTF
M16	VCC_NCTF
Y15	VCC_NCTF
P15	VCC_NCTF
N15	VCC_NCTF
R13`	VCCAUX_NCTF
P13	VCCAUX_NCTF
N13	VCCAUX_NCTF
M13	VCCAUX_NCTF
AD12	VCCAUX_NCTF
Y12	VCCAUX_NCTF
W12	VCCAUX_NCTF
V12	VCCAUX_NCTF
U12	VCCAUX_NCTF
T12	VCCAUX_NCTF
R12	VCCAUX_NCTF
P12	VCCAUX_NCTF
N12	VCCAUX_NCTF
M12	VCCAUX_NCTF
AD11	VCCAUX_NCTF
AD10	VCCAUX_NCTF
K10	VCCAUX_NCTF
AE5	VCCDHMPLL
AD5	VCCDHMPLL
C28	VCCDLVDS
B28	VCCDLVDS
A28	VCCDLVDS
F22	VCCDQTVDAC
F20	VCCDTVDAC
E26	VCCHV
D26	VCCHV
C26	VCCHV
AB33	VCCSM

Ball	Signal
AD33	VCCAUX
AD32	VCCAUX
AD31	VCCAUX
AD30	VCCAUX
AD29	VCCAUX
AD28	VCCAUX
AD27	VCCAUX
AC27	VCCAUX
AD26	VCCAUX
AC26	VCCAUX
AM24	VCCSM
AL24	VCCSM
AK24	VCCSM
AJ24	VCCSM
AH24	VCCSM
AG24	VCCSM
AF24	VCCSM
AE24	VCCSM
AN18	VCCSM
AN16	VCCSM
AM16	VCCSM
AL16	VCCSM
AK16	VCCSM
AJ16	VCCSM
AN13	VCCSM
AM13	VCCSM
AL13	VCCSM
AK13	VCCSM
AJ13	VCCSM
AH13	VCCSM
AG13	VCCSM
AF13	VCCSM
AE13	VCCSM
AN10	VCCSM
AM10	VCCSM
AL10	VCCSM
AK10	VCCSM
AJ10	VCCSM

Table 90. Power and Ground Signals (Sheet 3 of 5)

Ball	Signal	Ball	Signal	Ball	Signal
AD17	VCCAUX_NCTF	AM32	VCCSM	AH10	VCCSM
AD16	VCCAUX_NCTF	AN29	VCCSM	AG10	VCCSM
AD15	VCCAUX_NCTF	AM29	VCCSM	AF10	VCCSM
AD14	VCCAUX_NCTF	AL29	VCCSM	AE10	VCCSM
K14	VCCAUX_NCTF	AK29	VCCSM	AN7	VCCSM
AD13	VCCAUX_NCTF	AJ29	VCCSM	AM7	VCCSM
Y13	VCCAUX_NCTF	AH29	VCCSM	AL7	VCCSM
W13	VCCAUX_NCTF	AG29	VCCSM	AK7	VCCSM
V13	VCCAUX_NCTF	AF29	VCCSM	AJ7	VCCSM
U13	VCCAUX_NCTF	AE29	VCCSM	AH7	VCCSM
T13	VCCAUX_NCTF	AN24	VCCSM	AN4	VCCSM
AH1	VCCSM	B30	VSS	AG25	VSS
J23	VCCSYNC	AA29	VSS	AE25	VSS
D29	VCCTXLVDS	U29	VSS	J25	VSS
C29	VCCTXLVDS	R29	VSS	G25	VSS
AH33	VSS	P29	VSS	A25	VSS
Y33	VSS	N29	VSS	H23	VSS
V33	VSS	M29	VSS	F23	VSS
R33	VSS	H29	VSS	B23	VSS
G33	VSS	E29	VSS	AM22	VSS
AK32	VSS	B29	VSS	AJ22	VSS
AG32	VSS	AK28	VSS	AF22	VSS
AE32	VSS	AH28	VSS	G22	VSS
AC32	VSS	AE28	VSS	E22	VSS
AA32	VSS	AA28	VSS	J21	VSS
U32	VSS	U28	VSS	H21	VSS
H32	VSS	T28	VSS	F21	VSS
E32	VSS	J28	VSS	AM20	VSS
C32	VSS	D28	VSS	AK20	VSS
AM31	VSS	AM27	VSS	AH20	VSS
AJ31	VSS	AF27	VSS	AF20	VSS
AA31	VSS	AB27	VSS	D20	VSS
U31	VSS	AA27	VSS	W19	VSS
T31	VSS	Y27	VSS	R19	VSS
R31	VSS	U27	VSS	AM18	VSS
P31	VSS	T27	VSS	AH18	VSS
N31	VSS	R27	VSS	AF18	VSS
M31	VSS	P27	VSS	U18	VSS

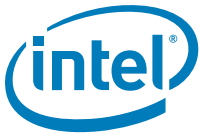


Table 90. Power and Ground Signals (Sheet 4 of 5)

Ball	Signal	Ball	Signal	Ball	Signal
J31	VSS	N27	VSS	H18	VSS
F31	VSS	M27	VSS	D18	VSS
AL30	VSS	G27	VSS	AK17	VSS
AG30	VSS	E27	VSS	V17	VSS
AE30	VSS	C27	VSS	T17	VSS
AC30	VSS	B27	VSS	F17	VSS
AA30	VSS	AL26	VSS	B17	VSS
Y30	VSS	AH26	VSS	AH16	VSS
V30	VSS	W26	VSS	U16	VSS
U30	VSS	U26	VSS	J16	VSS
G30	VSS	AN25	VSS	AL15	VSS
E30	VSS	AK25	VSS	AG15	VSS
W15	VSS	AL6	VSS	AA20	VSS_NCTF
R15	VSS	AG6	VSS	AA19	VSS_NCTF
F15	VSS	AE6	VSS	AA18	VSS_NCTF
D15	VSS	AB6	VSS	AA17	VSS_NCTF
AM14	VSS	W6	VSS	AA16	VSS_NCTF
AH14	VSS	T6	VSS	AA15	VSS_NCTF
AE14	VSS	M6	VSS	AA14	VSS_NCTF
H14	VSS	K6	VSS	AA13	VSS_NCTF
B14	VSS	AN5	VSS	A4	VSS_NCTF
F13	VSS	AJ5	VSS	A33	VSS_NCTF
D13	VSS	B5	VSS	B2	VSS_NCTF
AL12	VSS	AA4	VSS	AN1	VSS_NCTF
AG12	VSS	V4	VSS	C1	VSS_NCTF
H12	VSS	R4	VSS	M33	VSSA3GBG
B12	VSS	N4	VSS	B25	VSSACRTDAC
AN11	VSS	K4	VSS	B32	VSSALVDS
AJ11	VSS	H4	VSS	E23	VSSATVBG
AE11	VSS	E4	VSS	A14	VTT
AM9	VSS	AL3	VSS	D10	VTT
AJ9	VSS	AD3	VSS	P9	VTT
AB9	VSS	W3	VSS	L9	VTT
W9	VSS	T3	VSS	D9	VTT
R9	VSS	B3	VSS	P8	VTT
M9	VSS	AK2	VSS	L8	VTT
J9	VSS	AH2	VSS	D8	VTT
F9	VSS	AF2	VSS	P7	VTT

Table 90. Power and Ground Signals (Sheet 5 of 5)

Ball	Signal
C9	VSS
A9	VSS
AL8	VSS
AG8	VSS
AE8	VSS
U8	VSS
AA7	VSS
V7	VSS
R7	VSS
N7	VSS
H7	VSS
E7	VSS
B7	VSS
U4	VTT
P4	VTT
L4	VTT
G4	VTT
D4	VTT
Y3	VTT
U3	VTT
P3	VTT
L3	VTT
G3	VTT
D3	VTT
Y2	VTT

Ball	Signal
AB2	VSS
M2	VSS
K2	VSS
H2	VSS
F2	VSS
V1	VSS
R1	VSS
AN33	VSS_NCTF
AA25	VSS_NCTF
V25	VSS_NCTF
U25	VSS_NCTF
AA22	VSS_NCTF
AA21	VSS_NCTF
U2	VTT
P2	VTT
L2	VTT
G2	VTT
D2	VTT
AA1	VTT
Y1	VTT
U1	VTT
P1	VTT
L1	VTT
G1	VTT
F1	VTT

Ball	Signal
L7	VTT
D7	VTT
A7	VTT
P6	VTT
L6	VTT
G6	VTT
D6	VTT
U5	VTT
P5	VTT
L5	VTT
G5	VTT
D5	VTT
Y4	VTT
T10	VTT_NCTF
R10	VTT_NCTF
P10	VTT_NCTF
N10	VTT_NCTF
L10	VTT_NCTF
D1	VTT_NCTF

13.5 Intel 945GU Express Chipset (G)MCH Ballout

Figure 33 through Figure 38 show the 945GU Express chipset ballout from the top of the package view. Table 91 lists the ballout arranged by signal name.

Figure 33. Intel 82945GU (G)MCH Ballout – Top View (Upper Left Quadrant; Columns 1–16)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A			NC2		NC1		HDRDY#		HTRDY#		HA5#		HREQ0#		HA14#		A
B		NC3		HRS1#		HBNR#		HDEFER#		HADS#		HA9#		HREQ4#		HREQ2#	B
C	NC4		VSS		VSS		VSS		VSS		VSS		VSS		VSS		C
D		RSVD		HBPRI#		HRS2#		HHITM#		HBREQ0#		HA3#		HADSTB0#		HA11#	D
E	NC5		HRS0#		VSS		VSS		VSS		VSS		VSS		VSS		E
F		VSS		THRMTRIP#		HHIT#		HYSWING		HYRCOMP		HA6#		HREQ3#		HA12#	F
G	HDPWR#		VSS		VSS		VSS		VSS		VSS		VSS		VSS		G
H		HCPUSLP#		RSVD		HCPURST#		HDBSY#		HVREF		HYSCOMP		HREQ1#		HA4#	H
J	HLOCK#		VSS		VSS		VSS		VSS		VSS		VCC_AUX		VSS		J
K		HD8#		VSS		HD0#		HD6#		HVREF		VCC_AUX		VSS		VTT	K
L	HD2#		VSS		VSS		VSS		VSS		VTT		VTT		VTT		L
M		HDSTBN0#		HDSTBP0#		HD3#		HD15#		HD9#		VTT		VCCA _NCTF		VTT _NCTF	M
N	HD10#		VSS		VSS		VSS		VSS		VTT		VSS _NCTF		VTT _NCTF		N
P		HD5#		HD12#		HD7#		HD4#		HDINV0#		VSS		VTT_NCTF		VCCA _NCTF	P
R	HD11#		VSS		VSS		VSS		VSS		VSS		VTT _NCTF		NC34		R
T		HD22#		HD13#		HD1#		HD16#		HD14#		VTT		VTT_NCTF		VCCA _NCTF	T
U	HD29#		VSS		VSS		VSS		VSS		VTT		VSS _NCTF		VCCA _NCTF		U
V		HD23#		HD17#		HD25#		HD21#		VSS		VSS		VCCA _NCTF		VCCA _NCTF	V
W	HD20#		VSS		VSS		VSS		VSS		VSS		VTT _NCTF		VCCA _NCTF		W
Y		HDSTBP1#		HDSTBN1#		HDINV1#		HD19#		HD24#		VTT		VCCA _NCTF		VCCA _NCTF	Y
AA	HD18#		VSS		VSS		VSS		VSS		VTT		VSS _NCTF		VCCA _NCTF		AA
AB		HD30#		HD31#		HD26#		HD27#		VTT		VSS		VCCA _NCTF		VCCA _NCTF	AB
AC	HD28#		VSS		VSS		VSS		VSS		VCC_AUX		VCCA _NCTF		VCCA _NCTF		AC
AD		HD41#		HD34#		HD38#		HD43#		HCLKP		VCCA_MPLL		VCCA _NCTF		VCCA _NCTF	AD
AE	HD37#		VSS		VSS		VSS		VSS		VSS		VTT _NCTF		VCCA _NCTF		AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 34. Intel 82945GU (G)MCH Ballout – Top View (Lower Left Quadrant; Columns 1–16)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
AF		HD42#		HD44#		HD39#		HDINV2#		HCLKN		VCCA_HPLL		VCCA_NCTF		VCCA_NCTF	AF
AG	VSS		VSS		VSS		VSS		VSS		VSS		VCCA_NCTF		VCCA_NCTF		AG
AH		HDSTBP2#		HDSTBN2#		HD47#		HD45#		HD32#		VCCD_HMPLL		VCCA_NCTF		VCCA_NCTF	AH
AJ	HD36#		VSS		VSS		VSS		VSS		VCCD_HMPLL		VCCA_NCTF		VCCA_NCTF		AJ
AK		HD56#		HD46#		HD35#		HD40#		HD33#		VCC_AUX		VCCA_NCTF		VCCA_NCTF	AK
AL	HD55#		VSS		VSS		VSS		VSS		VCC_AUX		VCCA_NCTF		VCCA_NCTF		AL
AM		HD54#		HD53#		HD50#		HD48#		HD52#		VCC_AUX		VCCA_NCTF		VCCA_NCTF	AM
AN	HD49#		VSS		VSS		VSS		VSS		VCC_AUX		NC		VCCA_NCTF		AN
AP		HDSTBP3#		HDSTBN3#		HD57#		HD61#		HD59#		VCC_AUX		VCCA_NCTF		VCCA_NCTF	AP
AR	VSS		VSS		VSS		VSS		VSS		VCC_AUX		NC		VCCA_NCTF		AR
AT		HD62#		HDINV3#		HD58#		HD63#		HD60#		VCC_AUX		VCCA_NCTF		VCCA_NCTF	AT
AU	HD51#		VSS		VSS		VSS		VSS		VCC_AUX		NC		VCCA_NCTF		AU
AV		VSS		SA_DQ_57		VSS		SA_DQ_61		VCC_AUX		VCC_AUX		VCCA_NCTF		VCCA_NCTF	AV
AW	VSS		VSS		VSS		VSS		VSS		VCC_AUX		NC		NC		AW
AY		SA_DQ_58		SA_DQ_62		SA_DQ_56		SA_DQS#_7		VCCSM		VSS		VCCSM		VSS	AY
BA	SA_DQ_63		VSS		VSS		VSS		VSS		VCCSM		VSS		VCCSM		BA
BB		SA_DQ_59		SA_DQ_60		SA_DM_7		SA_DQS_7		VSS		VCCSM		VSS		VCCSM	BB
BC	SM_VREF0		VSS		VSS		VSS		SM_CS#_1		SA_DQ_41		SA_BS_0		SA_RAS#		BC
BD		SA_DQ_55		SA_DQ_52		SA_DQ_53		SM_ODT_1		VSS		VSS		VSS		VSS	BD
BE	SA_DQ_51		VSS		VSS		SA_DQ_48		SA_DQ_46		SA_DQ_40		SM_ODT_0		SM_CK#_1		BE
BF		SA_DQ_50		VSS		VSS		VSS		VSS		VSS		VSS		VSS	BF
BG	NC6		SA_DQ_54		SA_DQ_49		SA_DQS#_6		SA_DQ_43		SA_DQ_45		SA_DQS#_5		SM_CK_1		BG
BH		NC7		VSS		VSS		VSS		VSS		VSS		VSS		VSS	BH
BJ	NC8		NC9		SA_DM_6		SA_DQS_6		SA_DQ_47		SA_DQ_42		SA_DQS_5		SM_CS#_0		BJ
BK		NC10		NC11		VSS		VSS		SA_DQ_44		SA_DM_5		SA_MA_13		SA_MA_3	BK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

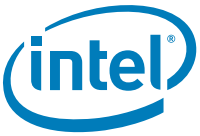


Figure 35. Intel 82945GU (G)MCH Ballout – Top View (Upper Middle Quadrant; Columns 17–33)

	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	
A	HA13#		HA15#		HA30#		RSVD		HA21#		HA28#		CFG_15		CFG_9		CFG_3	A
B		HA8#		RSVD		HA18#		HADSTB1#		HA26#		HA17#		CFG_17		CFG_13		B
C	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	C
D		HA10#		HXRCOMP		HA27#		HA31#		HA19#		HA29#		CFG_10		CFG_11		D
E	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	E
F		HA16#		HXSWING		HA24#		HA25#		HA22#		CFG_14		VCCA _TVDACA1		VCCA _TVDACB1		F
G	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	G
H		HA7#		HXSCOMP		HA23#		HA20#		H_BSEL1		CFG_8		VCCA_TV DACA0		VCCA _TVDACB0		H
J	VTT		VSS		VTT		VSS		VTT		VSS		VSS		VSS		VSS	J
K		VSS		VTT		VSS		VTT		CFG_5		CFG_6		VCCD _TVDAC		VCCA _TVBG		K
L	CFG_12		H_BSEL0		VCC_AUX		CFG_7		CFG _16		H_BSEL2		VCC _AUX		VCC _AUX		VCC	L
M		VSS _NCTF		VCCA _NCTF		VSS _NCTF		VCCA _NCTF		VSS _NCTF		VCCA _NCTF		VCCA _NCTF		VSS_NCTF		M
N	NC33		VCCA_NC TF		NC31		VCCA_ NCTF		NC29		VCCA_ NCTF		VCCA _NCTF		NC27		VCC _NCTF	N
P		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VSS _NCTF		VCC_NCTF		P
R	VCCA_ NCTF		NC32		VCC A_NCTF		NC30		VCCA_ NCTF		VCC _NCTF		NC28		VCC _NCTF		NC26	R
T		VCCA _NCTF		VCCA _NCTF		VCCA_ NCTF		VCCA _NCTF		VCC _NCTF		VS S_NCTF		VCC _NCTF		VSS_NCTF		T
U	VCCA_ NCTF		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC	U
V		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		V
W	VCCA_ NCTF		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS	W
Y		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		Y
AA	VCCA_ NCTF		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC	AA
AB		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		AB
AC	VCCA_ NCTF		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS	AC
AD		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		AD
AE	VCCA_ NCTF		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC	AE
	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	

Figure 36. Intel 82945GU (G)MCH Ballout – Top View (lOwer Middle Quadrant; Columns 17–33)

	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	
AF		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		AF
AG	VCCA _NCTF		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS	AG
AH		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		AH
AJ	VCCA _NCTF		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC	AJ
AK		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		AK
AL	VCCA _NCTF		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS	AL
AM		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		AM
AN	VCCA _NCTF		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC	AN
AP		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		AP
AR	VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA_N CTF		VCCA _NCTF	AR
AT		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		AT
AU	VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA_N CTF		VCCA _NCTF	AU
AV		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		VCCA _NCTF		AV
AW	NC		NC		NC		VSS _NCTF		VCCA _NCTF		VSS _NCTF		VCCA _NCTF		VSS_NC TF		VCCA _NCTF	AW
AY		VCCSM		VSS		VCCSM		VSS		VCC _AUX		VSS		VCCSM		VSS		AY
BA	VSS		VCCSM		VSS		VCCSM		VCC _AUX		VCC _AUX		VSS		VCCSM		VSS	BA
BB		VSS		VCCSM		VSS		VCCSM		VCCSM		VCCSM		VSS		VCCSM		BB
BC	SA_MA_8		NC		SA_MA _7		SA_RCV ENIN#		SA_DQ _27		SA_DQ _30		SA _DQ_28		SM_CKE _0		SM _CK#_0	BC
BD		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		BD
BE	SA_MA_0		SA_MA_ 2		SA_MA _9		SA_BS_1		SA_DQ _39		SA_DM_4		SA _DQS_4		SM_CKE _1		SM_CK_0	BE
BF		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		BF
BG	SA_CAS#		SA_MA_ 10		SA_MA _1		SA_MA_6		SA_DQ _37		SA_DQ _38		SA _DQS#_4		SA_DQ_2 9		SA _DQS_3	BG
BH		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		BH
BJ	SA_MA_4		SA_WE#		SA_MA _11		SA_MA _12		SA_DQ _34		SA_DQ _32		SA _DQ_36		SA_DQ_2 6		SA _DQS#_3	BJ
BK		SA_BS _2		SA_MA _5		SM _RCOMPN		SM _RCOMPP		SA_DQ _35		SA_DQ _33		SA _DQ_31		SA _DQ_25		BK
	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	

Figure 37. Intel 82945GU (G)MCH Ballout – Top View (Upper Right Quadrant; Columns 34–50)

	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	
A		VSS		TVDAC_B		VSS		CFG_19		LCTLA_CLK		LBKLT_CTL		NC22		NC20		A
B	CFG_4		TV_IRTNB		TV_IRTNC		VSS		LCTLB_DATA		PM_EXTTS1#		LVDD_EN		NC21		NC19	B
C		VSS		VSS		VSS		ICH_SYNC#		VSS		VSS		VSS		NC18		C
D	VSS		TVDAC_A		TVDAC_C		VCCA_DPLLA		VCCHV		PM_BM_BUSY#		LDDC_CLK		VCCD_LVDS2		NC17	D
E		VSS		VSS		VSS		VSS		VSS		LBKLT_EN		CFG_20		VCCD_LVDS1		E
F	VCCA_TVDACC1		TV_IRTNA		TV_IREF		VCCHV		VCCHV		VSS		VSS		VSS		VCCD_LVDS0	F
G		VSS		VSS		VSS		VSS		VSS		LDDC_DATA		RSVD		VSS		G
H	VCCA_TVDACC0		VCCDQ_TVDAC		VSS		PM_EXTTS0#		VCCTX_LVDS2		VSS		VSS		CFG_18		SDVOCTRL_CLK	H
J		VSS		VSS		VSS		VSS		VCCTX_LVDS1		VSS		VSS		VSS		J
K	VSSA_TVBG		VCC		VCC		VSS		VCCTX_LVDS0		CLK_REQ#		SDVOCTRL_DATA		DREF_CLKN		DREF_CLKP	K
L		VCC		VCC		VCC		VCC		VSSA_LVDS		VSS		VSS		VSS		L
M	VCC_NCTF		VCC_NCTF		VCC_NCTF		VCC_NCTF		VSS		LVBG		LIBG		VCCA_DPLLB1		VCCA_DPLLB0	M
N		NC25		VCC_NCTF		NC23		VCC		VCCA_LVDS		VSS		VSS		VSS		N
P	VSS_NCTF		VCC_NCTF		VSS_NCTF		VCC_NCTF		VSS		LVREFL		LVREFH		VSS		VSS	P
R		VCC_NCTF		NC24		VCC_NCTF		VCC		VSS		VSS		VSS		VSS		R
T	VCC_NCTF		VSS_NCTF		VCC_NCTF		VCC_NCTF		VSS		LA_CLKP		LA_CLKN		LA_DATAN2		LA_DATAP2	T
U		VSS		VCC_NCTF		VSS_NCTF		VCC		VSS		VSS		VSS		VSS		U
V	VSS		VCC_NCTF		VSS_NCTF		VCC_NCTF		VCC		LA_DATAN1		LA_DATAP1		LA_DATAN0		LA_DATAP0	V
W		VCC		VSS_NCTF		VCC_NCTF		VCC		VSS		VSS		VSS		VSS		W
Y	VCC		VSS_NCTF		VCC_NCTF		VCC_NCTF		VCCA_3GBG		EXP_A_RXN_0		EXP_A_RXP_0		DREF_SSCLKP		DREF_SSCLKN	Y
AA		VSS		VCC_NCTF		VSS_NCTF		VCC		VSS		VSS		VSS		VSS		AA
AB	VSS		VCC_NCTF		VSS_NCTF		VCC_NCTF		VSSA_3GBG		EXP_A_TXP_0		EXP_A_TXN_0		EXP_A_ICOMPO		EXP_A_COMPI	AB
AC		VCC		VSS_NCTF		VCC_NCTF		VSS		VSS		VSS		VSS		VSS		AC
AD	VCC		VSS_NCTF		VCC_NCTF		VSS_NCTF		VCC3G		GCLKP		GCLKN		SDVO_FLDSTALLP		SDVO_FLDSTALLN	AD
AE		VSS		VCC_NCTF		VSS_NCTF		VSS		VSS		VSS		VSS		VSS		AE
	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	

Figure 38. Intel 82945GU (G)MCH Ballout – Top View (Lower Right Quadrant; Columns 34–50)

	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	
AF	VSS		VCC_NCTF		VSS_NCTF		VSS_NCTF		VCC3G		SDVO_CLKN		SDVO_CLKP		SDVO_BLUE#		SDVO_BLUE	AF
AG		VCC		VSS_NCTF		VCC_NCTF		VCCA_3GPLL		VSS		VSS		VSS		VSS		AG
AH	VCC		VSS_NCTF		VCC_NCTF		VSS_NCTF		VCC3G		SDVO_INT		SDVO_INT#		SDVO_TVCLKIN		SDVO_TVCLKIN#	AH
AJ		VSS		VCC_NCTF		VSS_NCTF		VSS		VSS		VSS		VSS		VSS		AJ
AK	VSS		VCC_NCTF		VSS_NCTF		VCCA_NCTF		VCC3G		SDVO_GREEN		SDVO_GREEN#		SDVO_RED#		SDVO_RED	AK
AL		VCC		VSS_NCTF		VCCA_NCTF		VSS		VSS		VSS		VSS		VSS		AL
AM	VCC		VCCA_NCTF		VCCA_NCTF		VCCA_NCTF		VCC_AUX		DMI_RXP_1		DMI_RXN_1		DMI_RXP_0		DMI_RXN_0	AM
AN		VSS		VCCA_NCTF		VCCA_NCTF		VCC_AUX		VSS		VSS		VSS		VSS		AN
AP	VSS		VCCA_NCTF		VCCA_NCTF		VCCA_NCTF		VCC_AUX		DMI_TXP_1		DMI_TXN_1		DMI_TXP_0		DMI_TXN_0	AP
AR		VCCA_NCTF		VCCA_NCTF		VCCA_NCTF		VCC_AUX		VSS		VSS		VSS		VSS		AR
AT	VCCA_NCTF		VCCA_NCTF		VCCA_NCTF		VCCA_NCTF		VCC_AUX		VSS		VSS		VSS		VSS	AT
AU		VCCA_NCTF		VCCA_NCTF		VCCA_NCTF		VCC_AUX		SA_DQ_3		SA_DQ_0		PWROK		RSTIN#		AU
AV	VCCA_NCTF		VCCA_NCTF		VCCA_NCTF		VCCA_NCTF		VSS		VSS		VSS		VSS		SM_VREF1	AV
AW		VSS_NCTF		VCCA_NCTF		VCCA_NCTF		VCC_AUX		SA_DQ_11		SA_DQ_2		SA_DQS#_0		SA_DM_0		AW
AY	VCCSM		VSS		VCCSM		VCC_AUX		VSS		VSS		VSS		VSS		SA_DQ_4	AY
BA		VCCSM		VSS		VCCSM		VCC_AUX		SA_DQ_10		SA_DQ_14		SA_DQS_0		SA_DQ_5		BA
BB	VSS		VCCSM		VSS		VSS		VSS		VSS		VSS		VSS		SA_DQ_7	BB
BC		VCCSM		VCCSM		VCCSM		SA_DQ_21		SA_DQ_20		SA_DQ_13		SA_DQS#_1		SA_DQ_6		BC
BD	VSS		VSS		VCCSM		VSS		VSS		VSS		VSS		VSS		SA_DQ_1	BD
BE		VCCSM		VSS		VCCSM		SA_DQ_18		SA_DQ_16		SA_DQ_15		SA_DQS_1		SA_DM_1		BE
BF	VSS		VCCSM		VSS		VSS		VSS		VSS		VSS		VSS		NC16	BF
BG		VCCSM		VCCSM		VCCSM		SA_DQ_19		SA_DQ_17		SA_DQS#_2		SA_DQ_9		SA_DQ_12		BG
BH	VSS		VSS		VCCSM		VSS		VSS		VSS		VSS		VSS		NC15	BH
BJ		SA_DM_3		VSS		VCCSM		VSS		SA_DQ_22		SA_DQS_2		SA_DQ_8		NC14		BJ
BK	SA_DQ_24		VSS		VCCSM		VCCSM		SA_DQ_23		SA_DM_2		NC12		NC13		VSS	BK
	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	

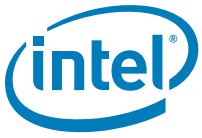


Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 1 of 11)

Signal Name	Ball #
CFG_3	A33
CFG_4	B34
CFG_5	K26
CFG_6	K28
CFG_7	L23
CFG_8	H28
CFG_9	A31
CFG_10	D30
CFG_11	D32
CFG_12	L17
CFG_13	B32
CFG_14	F28
CFG_15	A29
CFG_16	L25
CFG_17	B30
CFG_18	H48
CFG_19	A41
CFG_20	E47
CLK_REQ#	K44
DMI_RXN_0	AM50
DMI_RXN_1	AM46
DMI_RXP_0	AM48
DMI_RXP_1	AM44
DMI_TXN_0	AP50
DMI_TXN_1	AP46
DMI_TXP_0	AP48
DMI_TXP_1	AP44
DREF_CLKN	K48
DREF_CLKP	K50
DREF_SSCLKN	Y50
DREF_SSCLKP	Y48
EXP_A_COMPI	AB50
EXP_A_ICOMPO	AB48
EXP_A_RXN_0	Y44
EXP_A_RXP_0	Y46
EXP_A_TXN_0	AB46
EXP_A_TXP_0	AB44

Signal Name	Ball #
GCLKN	AD46
GCLKP	AD44
H_BSEL0	L19
H_BSEL1	H26
H_BSEL2	L27
HA3#	D12
HA4#	H16
HA5#	A11
HA6#	F12
HA7#	H18
HA8#	B18
HA9#	B12
HA10#	D18
HA11#	D16
HA12#	F16
HA13#	A17
HA14#	A15
HA15#	A19
HA16#	F18
HA17#	B28
HA18#	B22
HA19#	D26
HA20#	H24
HA21#	A25
HA22#	F26
HA23#	H22
HA24#	F22
HA25#	F24
HA26#	B26
HA27#	D22
HA28#	A27
HA29#	D28
HA30#	A21
HA31#	D24
HADS#	B10
HADSTB0#	D14
HADSTB1#	B24

Signal Name	Ball #
HBNR#	B6
HBPRI#	D4
HBREQ0#	D10
HCLKN	AF10
HCLKP	AD10
HCPURST#	H6
HCPUSLP#	H2
HD0#	K6
HD1#	T6
HD2#	L1
HD3#	M6
HD4#	P8
HD5#	P2
HD6#	K8
HD7#	P6
HD8#	K2
HD9#	M10
HD10#	N1
HD11#	R1
HD12#	P4
HD13#	T4
HD14#	T10
HD15#	M8
HD16#	T8
HD17#	V4
HD18#	AA1
HD19#	Y8
HD20#	W1
HD21#	V8
HD22#	T2
HD23#	V2
HD24#	Y10
HD25#	V6
HD26#	AB6
HD27#	AB8
HD28#	AC1
HD29#	U1

Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 2 of 11)

Signal Name	Ball #
HD30#	AB2
HD31#	AB4
HD32#	AH10
HD33#	AK10
HD34#	AD4
HD35#	AK6
HD36#	AJ1
HD37#	AE1
HD38#	AD6
HD39#	AF6
HD40#	AK8
HD41#	AD2
HD42#	AF2
HD43#	AD8
HD44#	AF4
HD45#	AH8
HD46#	AK4
HD47#	AH6
HD48#	AM8
HD49#	AN1
HD50#	AM6
HD51#	AU1
HD52#	AM10
HD53#	AM4
HD54#	AM2
HD55#	AL1
HD56#	AK2
HD57#	AP6
HD58#	AT6
HD59#	AP10
HD60#	AT10
HD61#	AP8
HD62#	AT2
HD63#	AT8
HDBSY#	H8
HDEFER#	B8
HDINV0#	P10
HDINV1#	Y6

Signal Name	Ball #
HDINV2#	AF8
HDINV3#	AT4
HDPWR#	G1
HDRDY#	A7
HDSTBN0#	M2
HDSTBN1#	Y4
HDSTBN2#	AH4
HDSTBN3#	AP4
HDSTBP0#	M4
HDSTBP1#	Y2
HDSTBP2#	AH2
HDSTBP3#	AP2
HHIT#	F6
HHITM#	D8
HLOCK#	J1
HREQ0#	A13
HREQ1#	H14
HREQ2#	B16
HREQ3#	F14
HREQ4#	B14
HRS0#	E3
HRS1#	B4
HRS2#	D6
HTRDY#	A9
HVREF	H10
HVREF	K10
HXRCOMP	D20
HXSCOMP	H20
HXSWING	F20
HYRCOMP	F10
HYSCOMP	H12
HYSWING	F8
ICH_SYNC#	C41
LA_CLKN	T46
LA_CLKP	T44
LA_DATAN0	V48
LA_DATAN1	V44
LA_DATAN2	T48

Signal Name	Ball #
LA_DATAP0	V50
LA_DATAP1	V46
LA_DATAP2	T50
LBKLT_CTL	A45
LBKLT_EN	E45
LCTLA_CLK	A43
LCTLB_DATA	B42
LDDC_CLK	D46
LDDC_DATA	G45
LIBG	M46
LVBG	M44
LVDD_EN	B46
LVREFH	P46
LVREFL	P44
NC	AN13
NC	AR13
NC	AU13
NC	AW13
NC	AW15
NC	AW17
NC	AW19
NC	AW21
NC	BC19
NC1	A5
NC2	A3
NC3	B2
NC4	C1
NC5	E1
NC6	BG1
NC7	BH2
NC8	BJ1
NC9	BJ3
NC10	BK2
NC11	BK4
NC12	BK46
NC13	BK48
NC14	BJ49
NC15	BH50

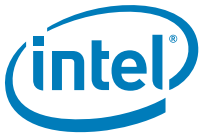


Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 3 of 11)

Signal Name	Ball #
NC16	BF50
NC17	D50
NC18	C49
NC19	B50
NC20	A49
NC21	B48
NC22	A47
NC23	N39
NC24	R37
NC25	N35
NC26	R33
NC27	N31
NC28	R29
NC29	N25
NC30	R23
NC31	N21
NC32	R19
NC33	N17
NC34	R15
PM_BM_BUSY#	D44
PM_EXTTS0#	H40
PM_EXTTS1#	B44
PWROK	AU47
RSTIN#	AU49
RSVD	A23
RSVD	B20
RSVD	D2
RSVD	G47
RSVD	H4
SA_BS_0	BC13
SA_BS_1	BE23
SA_BS_2	BK18
SA_CAS#	BG17
SA_DM_0	AW49
SA_DM_1	BE49
SA_DM_2	BK44
SA_DM_3	BJ35
SA_DM_4	BE27

Signal Name	Ball #
SA_DM_5	BK12
SA_DM_6	BJ5
SA_DM_7	BB6
SA_DQ_0	AU45
SA_DQ_1	BD50
SA_DQ_2	AW45
SA_DQ_3	AU43
SA_DQ_4	AY50
SA_DQ_5	BA49
SA_DQ_6	BC49
SA_DQ_7	BB50
SA_DQ_8	BJ47
SA_DQ_9	BG47
SA_DQ_10	BA43
SA_DQ_11	AW43
SA_DQ_12	BG49
SA_DQ_13	BC45
SA_DQ_14	BA45
SA_DQ_15	BE45
SA_DQ_16	BE43
SA_DQ_17	BG43
SA_DQ_18	BE41
SA_DQ_19	BG41
SA_DQ_20	BC43
SA_DQ_21	BC41
SA_DQ_22	BJ43
SA_DQ_23	BK42
SA_DQ_24	BK34
SA_DQ_25	BK32
SA_DQ_26	BJ31
SA_DQ_27	BC25
SA_DQ_28	BC29
SA_DQ_29	BG31
SA_DQ_30	BC27
SA_DQ_31	BK30
SA_DQ_32	BJ27
SA_DQ_33	BK28
SA_DQ_34	BJ25

Signal Name	Ball #
SA_DQ_35	BK26
SA_DQ_36	BJ29
SA_DQ_37	BG25
SA_DQ_38	BG27
SA_DQ_39	BE25
SA_DQ_40	BE11
SA_DQ_41	BC11
SA_DQ_42	BJ11
SA_DQ_43	BG9
SA_DQ_44	BK10
SA_DQ_45	BG11
SA_DQ_46	BE9
SA_DQ_47	BJ9
SA_DQ_48	BE7
SA_DQ_49	BG5
SA_DQ_50	BF2
SA_DQ_51	BE1
SA_DQ_52	BD4
SA_DQ_53	BD6
SA_DQ_54	BG3
SA_DQ_55	BD2
SA_DQ_56	AY6
SA_DQ_57	AV4
SA_DQ_58	AY2
SA_DQ_59	BB2
SA_DQ_60	BB4
SA_DQ_61	AV8
SA_DQ_62	AY4
SA_DQ_63	BA1
SA_DQS#_0	AW47
SA_DQS#_1	BC47
SA_DQS#_2	BG45
SA_DQS#_3	BJ33
SA_DQS#_4	BG29
SA_DQS#_5	BG13
SA_DQS#_6	BG7
SA_DQS#_7	AY8
SA_DQS_0	BA47

Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 4 of 11)

Signal Name	Ball #
SA_DQS_1	BE47
SA_DQS_2	BJ45
SA_DQS_3	BG33
SA_DQS_4	BE29
SA_DQS_5	BJ13
SA_DQS_6	BJ7
SA_DQS_7	BB8
SA_MA_0	BE17
SA_MA_1	BG21
SA_MA_2	BE19
SA_MA_3	BK16
SA_MA_4	BJ17
SA_MA_5	BK20
SA_MA_6	BG23
SA_MA_7	BC21
SA_MA_8	BC17
SA_MA_9	BE21
SA_MA_10	BG19
SA_MA_11	BJ21
SA_MA_12	BJ23
SA_MA_13	BK14
SA_RAS#	BC15
SA_RCVENIN#	BC23
SA_WE#	BJ19
SDVO_BLUE	AF50
SDVO_BLUE#	AF48
SDVO_CLKN	AF44
SDVO_CLKP	AF46
SDVO_FLDSTALLN	AD50
SDVO_FLDSTALLP	AD48
SDVO_GREEN	AK44
SDVO_GREEN#	AK46
SDVO_INT	AH44
SDVO_INT#	AH46
SDVO_RED	AK50
SDVO_RED#	AK48
SDVO_TVCLKIN	AH48
SDVO_TVCLKIN#	AH50

Signal Name	Ball #
SDVOCTRL_CLK	H50
SDVOCTRL_DATA	K46
SM_CK#_0	BC33
SM_CK#_1	BE15
SM_CK_0	BE33
SM_CK_1	BG15
SM_CKE_0	BC31
SM_CKE_1	BE31
SM_CS#_0	BJ15
SM_CS#_1	BC9
SM_ODT_0	BE13
SM_ODT_1	BD8
SM_RCOMPN	BK22
SM_RCOMPP	BK24
SM_VREF0	BC1
SM_VREF1	AV50
THRMTRIP#	F4
TV_IREF	F38
TV_IRTNA	F36
TV_IRTNB	B36
TV_IRTNC	B38
TVDAC_A	D36
TVDAC_B	A37
TVDAC_C	D38
VCC	AA21
VCC	AA25
VCC	AA29
VCC	AA33
VCC	AA41
VCC	AB20
VCC	AB24
VCC	AB28
VCC	AB32
VCC	AC19
VCC	AC23
VCC	AC27
VCC	AC31
VCC	AC35

Signal Name	Ball #
VCC	AD18
VCC	AD22
VCC	AD26
VCC	AD30
VCC	AD34
VCC	AE21
VCC	AE25
VCC	AE29
VCC	AE33
VCC	AF20
VCC	AF24
VCC	AF28
VCC	AF32
VCC	AG19
VCC	AG23
VCC	AG27
VCC	AG31
VCC	AG35
VCC	AH18
VCC	AH22
VCC	AH26
VCC	AH30
VCC	AH34
VCC	AJ21
VCC	AJ25
VCC	AJ29
VCC	AJ33
VCC	AK20
VCC	AK24
VCC	AK28
VCC	AK32
VCC	AL19
VCC	AL23
VCC	AL27
VCC	AL31
VCC	AL35
VCC	AM18
VCC	AM22

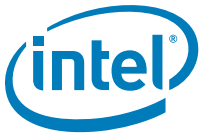


Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 5 of 11)

Signal Name	Ball #
VCC	AM26
VCC	AM30
VCC	AM34
VCC	AN21
VCC	AN25
VCC	AN29
VCC	AN33
VCC	AP20
VCC	AP24
VCC	AP28
VCC	AP32
VCC	K36
VCC	K38
VCC	L33
VCC	L35
VCC	L37
VCC	L39
VCC	L41
VCC	N41
VCC	R41
VCC	U21
VCC	U25
VCC	U29
VCC	U33
VCC	U41
VCC	V20
VCC	V24
VCC	V28
VCC	V32
VCC	V42
VCC	W19
VCC	W23
VCC	W27
VCC	W31
VCC	W35
VCC	W41
VCC	Y18
VCC	Y22

Signal Name	Ball #
VCC	Y26
VCC	Y30
VCC	Y34
VCC_AUX	AC11
VCC_AUX	AK12
VCC_AUX	AL11
VCC_AUX	AM12
VCC_AUX	AM42
VCC_AUX	AN11
VCC_AUX	AN41
VCC_AUX	AP12
VCC_AUX	AP42
VCC_AUX	AR11
VCC_AUX	AR41
VCC_AUX	AT12
VCC_AUX	AT42
VCC_AUX	AU11
VCC_AUX	AU41
VCC_AUX	AV10
VCC_AUX	AV12
VCC_AUX	AW11
VCC_AUX	AW41
VCC_AUX	AY26
VCC_AUX	AY40
VCC_AUX	BA25
VCC_AUX	BA27
VCC_AUX	BA41
VCC_AUX	J13
VCC_AUX	K12
VCC_AUX	L21
VCC_AUX	L29
VCC_AUX	L31
VCC_NCTF	AA37
VCC_NCTF	AB36
VCC_NCTF	AB40
VCC_NCTF	AC39
VCC_NCTF	AD38
VCC_NCTF	AE37

Signal Name	Ball #
VCC_NCTF	AF36
VCC_NCTF	AG39
VCC_NCTF	AH38
VCC_NCTF	AJ37
VCC_NCTF	AK36
VCC_NCTF	M34
VCC_NCTF	M36
VCC_NCTF	M38
VCC_NCTF	M40
VCC_NCTF	N33
VCC_NCTF	N37
VCC_NCTF	P32
VCC_NCTF	P36
VCC_NCTF	P40
VCC_NCTF	R27
VCC_NCTF	R31
VCC_NCTF	R35
VCC_NCTF	R39
VCC_NCTF	T26
VCC_NCTF	T30
VCC_NCTF	T34
VCC_NCTF	T38
VCC_NCTF	T40
VCC_NCTF	U37
VCC_NCTF	V36
VCC_NCTF	V40
VCC_NCTF	W39
VCC_NCTF	Y38
VCC_NCTF	Y40
VCC3G	AD42
VCC3G	AF42
VCC3G	AH42
VCC3G	AK42
VCCA_3GBG	Y42
VCCA_3GPLL	AG41
VCCA_DPLLA	D40
VCCA_DPLLB0	M50
VCCA_DPLLB1	M48

Table 91. Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 6 of 11)

Signal Name	Ball #
VCCA_HPLL	AF12
VCCA_LVDS	N43
VCCA_MPLL	AD12
VCCA_NCTF	AA15
VCCA_NCTF	AA17
VCCA_NCTF	AB14
VCCA_NCTF	AB16
VCCA_NCTF	AC13
VCCA_NCTF	AC15
VCCA_NCTF	AC17
VCCA_NCTF	AD14
VCCA_NCTF	AD16
VCCA_NCTF	AE15
VCCA_NCTF	AE17
VCCA_NCTF	AF14
VCCA_NCTF	AF16
VCCA_NCTF	AG13
VCCA_NCTF	AG15
VCCA_NCTF	AG17
VCCA_NCTF	AH14
VCCA_NCTF	AH16
VCCA_NCTF	AJ13
VCCA_NCTF	AJ15
VCCA_NCTF	AJ17
VCCA_NCTF	AK14
VCCA_NCTF	AK16
VCCA_NCTF	AK40
VCCA_NCTF	AL13
VCCA_NCTF	AL15
VCCA_NCTF	AL17
VCCA_NCTF	AL39
VCCA_NCTF	AM14
VCCA_NCTF	AM16
VCCA_NCTF	AM36
VCCA_NCTF	AM38
VCCA_NCTF	AM40
VCCA_NCTF	AN15
VCCA_NCTF	AN17
VCCA_NCTF	AN37
VCCA_NCTF	AN39
VCCA_NCTF	AP14
VCCA_NCTF	AP16
VCCA_NCTF	AP36
VCCA_NCTF	AP38
VCCA_NCTF	AP40
VCCA_NCTF	AR15
VCCA_NCTF	AR17
VCCA_NCTF	AR19
VCCA_NCTF	AR21
VCCA_NCTF	AR23
VCCA_NCTF	AR25
VCCA_NCTF	AR27
VCCA_NCTF	AR29
VCCA_NCTF	AR31
VCCA_NCTF	AR33
VCCA_NCTF	AR35
VCCA_NCTF	AR37
VCCA_NCTF	AR39
VCCA_NCTF	AT14
VCCA_NCTF	AT16
VCCA_NCTF	AT18
VCCA_NCTF	AT20
VCCA_NCTF	AT22
VCCA_NCTF	AT24
VCCA_NCTF	AT26
VCCA_NCTF	AT28
VCCA_NCTF	AT30
VCCA_NCTF	AT32
VCCA_NCTF	AT34
VCCA_NCTF	AT36
VCCA_NCTF	AT38
VCCA_NCTF	AT40
VCCA_NCTF	AU15
VCCA_NCTF	AU17
VCCA_NCTF	AU19
VCCA_NCTF	AU21
VCCA_NCTF	AU23
VCCA_NCTF	AU25
VCCA_NCTF	AU27
VCCA_NCTF	AU29
VCCA_NCTF	AU31
VCCA_NCTF	AU33
VCCA_NCTF	AU35
VCCA_NCTF	AU37
VCCA_NCTF	AU39
VCCA_NCTF	AV14
VCCA_NCTF	AV16
VCCA_NCTF	AV18
VCCA_NCTF	AV20
VCCA_NCTF	AV22
VCCA_NCTF	AV24
VCCA_NCTF	AV26
VCCA_NCTF	AV28
VCCA_NCTF	AV30
VCCA_NCTF	AV32
VCCA_NCTF	AV34
VCCA_NCTF	AV36
VCCA_NCTF	AV38
VCCA_NCTF	AV40
VCCA_NCTF	AW25
VCCA_NCTF	AW29
VCCA_NCTF	AW33
VCCA_NCTF	AW37
VCCA_NCTF	AW39
VCCA_NCTF	M14
VCCA_NCTF	M20
VCCA_NCTF	M24
VCCA_NCTF	M28
VCCA_NCTF	M30
VCCA_NCTF	N19
VCCA_NCTF	N23
VCCA_NCTF	N27
VCCA_NCTF	N29
VCCA_NCTF	P16

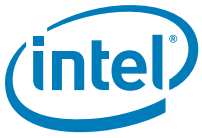


Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 7 of 11)

Signal Name	Ball #
VCCA_NCTF	P18
VCCA_NCTF	P20
VCCA_NCTF	P22
VCCA_NCTF	P24
VCCA_NCTF	P26
VCCA_NCTF	P28
VCCA_NCTF	R17
VCCA_NCTF	R21
VCCA_NCTF	R25
VCCA_NCTF	T16
VCCA_NCTF	T18
VCCA_NCTF	T20
VCCA_NCTF	T22
VCCA_NCTF	T24
VCCA_NCTF	U15
VCCA_NCTF	U17
VCCA_NCTF	V14
VCCA_NCTF	V16
VCCA_NCTF	W15
VCCA_NCTF	W17
VCCA_NCTF	Y14
VCCA_NCTF	Y16
VCCA_TVBG	K32
VCCA_TVDACA0	H30
VCCA_TVDACA1	F30
VCCA_TVDACB0	H32
VCCA_TVDACB1	F32
VCCA_TVDACC0	H34
VCCA_TVDACC1	F34
VCCD_HMPLL	AH12
VCCD_HMPLL	AJ11
VCCD_LVDS0	F50
VCCD_LVDS1	E49
VCCD_LVDS2	D48
VCCD_TVDAC	K30
VCCDQ_TVDAC	H36
VCCHV	D42
VCCHV	F40

Signal Name	Ball #
VCCHV	F42
VCCSM	AY10
VCCSM	AY14
VCCSM	AY18
VCCSM	AY22
VCCSM	AY30
VCCSM	AY34
VCCSM	AY38
VCCSM	BA11
VCCSM	BA15
VCCSM	BA19
VCCSM	BA23
VCCSM	BA31
VCCSM	BA35
VCCSM	BA39
VCCSM	BB12
VCCSM	BB16
VCCSM	BB20
VCCSM	BB24
VCCSM	BB26
VCCSM	BB28
VCCSM	BB32
VCCSM	BB36
VCCSM	BC35
VCCSM	BC37
VCCSM	BC39
VCCSM	BD38
VCCSM	BE35
VCCSM	BE39
VCCSM	BF36
VCCSM	BG35
VCCSM	BG37
VCCSM	BG39
VCCSM	BH38
VCCSM	BJ39
VCCSM	BK38
VCCSM	BK40
VCCTX_LVDS0	K42

Signal Name	Ball #
VCCTX_LVDS1	J43
VCCTX_LVDS2	H42
VSS	A35
VSS	A39
VSS	AA19
VSS	AA23
VSS	AA27
VSS	AA3
VSS	AA31
VSS	AA35
VSS	AA43
VSS	AA45
VSS	AA47
VSS	AA49
VSS	AA5
VSS	AA7
VSS	AA9
VSS	AB12
VSS	AB18
VSS	AB22
VSS	AB26
VSS	AB30
VSS	AB34
VSS	AC21
VSS	AC25
VSS	AC29
VSS	AC3
VSS	AC33
VSS	AC41
VSS	AC43
VSS	AC45
VSS	AC47
VSS	AC49
VSS	AC5
VSS	AC7
VSS	AC9
VSS	AD20
VSS	AD24

Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 8 of 11)

Signal Name	Ball #
VSS	AD28
VSS	AD32
VSS	AE11
VSS	AE19
VSS	AE23
VSS	AE27
VSS	AE3
VSS	AE31
VSS	AE35
VSS	AE41
VSS	AE43
VSS	AE45
VSS	AE47
VSS	AE49
VSS	AE5
VSS	AE7
VSS	AE9
VSS	AF18
VSS	AF22
VSS	AF26
VSS	AF30
VSS	AF34
VSS	AG1
VSS	AG11
VSS	AG21
VSS	AG25
VSS	AG29
VSS	AG3
VSS	AG33
VSS	AG43
VSS	AG45
VSS	AG47
VSS	AG49
VSS	AG5
VSS	AG7
VSS	AG9
VSS	AH20
VSS	AH24

Signal Name	Ball #
VSS	AH28
VSS	AH32
VSS	AJ19
VSS	AJ23
VSS	AJ27
VSS	AJ3
VSS	AJ31
VSS	AJ35
VSS	AJ41
VSS	AJ43
VSS	AJ45
VSS	AJ47
VSS	AJ49
VSS	AJ5
VSS	AJ7
VSS	AJ9
VSS	AK18
VSS	AK22
VSS	AK26
VSS	AK30
VSS	AK34
VSS	AL21
VSS	AL25
VSS	AL29
VSS	AL3
VSS	AL33
VSS	AL41
VSS	AL43
VSS	AL45
VSS	AL47
VSS	AL49
VSS	AL5
VSS	AL7
VSS	AL9
VSS	AM20
VSS	AM24
VSS	AM28
VSS	AM32

Signal Name	Ball #
VSS	AN19
VSS	AN23
VSS	AN27
VSS	AN3
VSS	AN31
VSS	AN35
VSS	AN43
VSS	AN45
VSS	AN47
VSS	AN49
VSS	AN5
VSS	AN7
VSS	AN9
VSS	AP18
VSS	AP22
VSS	AP26
VSS	AP30
VSS	AP34
VSS	AR1
VSS	AR3
VSS	AR43
VSS	AR45
VSS	AR47
VSS	AR49
VSS	AR5
VSS	AR7
VSS	AR9
VSS	AT44
VSS	AT46
VSS	AT48
VSS	AT50
VSS	AU3
VSS	AU5
VSS	AU7
VSS	AU9
VSS	AV2
VSS	AV42
VSS	AV44

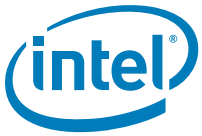


Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 9 of 11)

Signal Name	Ball #
VSS	AV46
VSS	AV48
VSS	AV6
VSS	AW1
VSS	AW3
VSS	AW5
VSS	AW7
VSS	AW9
VSS	AY12
VSS	AY16
VSS	AY20
VSS	AY24
VSS	AY28
VSS	AY32
VSS	AY36
VSS	AY42
VSS	AY44
VSS	AY46
VSS	AY48
VSS	B40
VSS	BA13
VSS	BA17
VSS	BA21
VSS	BA29
VSS	BA3
VSS	BA33
VSS	BA37
VSS	BA5
VSS	BA7
VSS	BA9
VSS	BB10
VSS	BB14
VSS	BB18
VSS	BB22
VSS	BB30
VSS	BB34
VSS	BB38
VSS	BB40
VSS	BB42
VSS	BB44
VSS	BB46
VSS	BB48
VSS	BC3
VSS	BC5
VSS	BC7
VSS	BD10
VSS	BD12
VSS	BD14
VSS	BD16
VSS	BD18
VSS	BD20
VSS	BD22
VSS	BD24
VSS	BD26
VSS	BD28
VSS	BD30
VSS	BD32
VSS	BD34
VSS	BD36
VSS	BD40
VSS	BD42
VSS	BD44
VSS	BD46
VSS	BD48
VSS	BE3
VSS	BE37
VSS	BE5
VSS	BF10
VSS	BF12
VSS	BF14
VSS	BF16
VSS	BF18
VSS	BF20
VSS	BF22
VSS	BF24
VSS	BF26
VSS	BF28
VSS	BF30
VSS	BF32
VSS	BF34
VSS	BF38
VSS	BF4
VSS	BF40
VSS	BF42
VSS	BF44
VSS	BF46
VSS	BF48
VSS	BF6
VSS	BF8
VSS	BH10
VSS	BH12
VSS	BH14
VSS	BH16
VSS	BH18
VSS	BH20
VSS	BH22
VSS	BH24
VSS	BH26
VSS	BH28
VSS	BH30
VSS	BH32
VSS	BH34
VSS	BH36
VSS	BH4
VSS	BH40
VSS	BH42
VSS	BH44
VSS	BH46
VSS	BH48
VSS	BH6
VSS	BH8
VSS	BJ37
VSS	BJ41
VSS	BK36

Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 10 of 11)

Signal Name	Ball #
VSS	BK50
VSS	BK6
VSS	BK8
VSS	C11
VSS	C13
VSS	C15
VSS	C17
VSS	C19
VSS	C21
VSS	C23
VSS	C25
VSS	C27
VSS	C29
VSS	C3
VSS	C31
VSS	C33
VSS	C35
VSS	C37
VSS	C39
VSS	C43
VSS	C45
VSS	C47
VSS	C5
VSS	C7
VSS	C9
VSS	D34
VSS	E11
VSS	E13
VSS	E15
VSS	E17
VSS	E19
VSS	E21
VSS	E23
VSS	E25
VSS	E27
VSS	E29
VSS	E31
VSS	E33

Signal Name	Ball #
VSS	E35
VSS	E37
VSS	E39
VSS	E41
VSS	E43
VSS	E5
VSS	E7
VSS	E9
VSS	F2
VSS	F44
VSS	F46
VSS	F48
VSS	G11
VSS	G13
VSS	G15
VSS	G17
VSS	G19
VSS	G21
VSS	G23
VSS	G25
VSS	G27
VSS	G29
VSS	G3
VSS	G31
VSS	G33
VSS	G35
VSS	G37
VSS	G39
VSS	G41
VSS	G43
VSS	G49
VSS	G5
VSS	G7
VSS	G9
VSS	H38
VSS	H44
VSS	H46
VSS	J11

Signal Name	Ball #
VSS	J15
VSS	J19
VSS	J23
VSS	J27
VSS	J29
VSS	J3
VSS	J31
VSS	J33
VSS	J35
VSS	J37
VSS	J39
VSS	J41
VSS	J45
VSS	J47
VSS	J49
VSS	J5
VSS	J7
VSS	J9
VSS	K14
VSS	K18
VSS	K22
VSS	K4
VSS	K40
VSS	L3
VSS	L45
VSS	L47
VSS	L49
VSS	L5
VSS	L7
VSS	L9
VSS	M42
VSS	N3
VSS	N45
VSS	N47
VSS	N49
VSS	N5
VSS	N7
VSS	N9

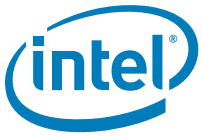


Table 91.Intel 82945GU (G)MCH Ballout By Signal Name (Sheet 11 of 11)

Signal Name	Ball #
VSS	P12
VSS	P42
VSS	P48
VSS	P50
VSS	R11
VSS	R3
VSS	R43
VSS	R45
VSS	R47
VSS	R49
VSS	R5
VSS	R7
VSS	R9
VSS	T42
VSS	U19
VSS	U23
VSS	U27
VSS	U3
VSS	U31
VSS	U35
VSS	U43
VSS	U45
VSS	U47
VSS	U49
VSS	U5
VSS	U7
VSS	U9
VSS	V10
VSS	V12
VSS	V18
VSS	V22
VSS	V26
VSS	V30
VSS	V34
VSS	W11
VSS	W21
VSS	W25
VSS	W29

Signal Name	Ball #
VSS	W3
VSS	W33
VSS	W43
VSS	W45
VSS	W47
VSS	W49
VSS	W5
VSS	W7
VSS	W9
VSS	Y20
VSS	Y24
VSS	Y28
VSS	Y32
VSS_NCTF	AA13
VSS_NCTF	AA39
VSS_NCTF	AB38
VSS_NCTF	AC37
VSS_NCTF	AD36
VSS_NCTF	AD40
VSS_NCTF	AE39
VSS_NCTF	AF38
VSS_NCTF	AF40
VSS_NCTF	AG37
VSS_NCTF	AH36
VSS_NCTF	AH40
VSS_NCTF	AJ39
VSS_NCTF	AK38
VSS_NCTF	AL37
VSS_NCTF	AW23
VSS_NCTF	AW27
VSS_NCTF	AW31
VSS_NCTF	AW35
VSS_NCTF	M18
VSS_NCTF	M22
VSS_NCTF	M26
VSS_NCTF	M32
VSS_NCTF	N13
VSS_NCTF	P30

Signal Name	Ball #
VSS_NCTF	P34
VSS_NCTF	P38
VSS_NCTF	T28
VSS_NCTF	T32
VSS_NCTF	T36
VSS_NCTF	U13
VSS_NCTF	U39
VSS_NCTF	V38
VSS_NCTF	W37
VSS_NCTF	Y36
VSSA_3GBG	AB42
VSSA_LVDS	L43
VSSA_TVBG	K34
VTT	AA11
VTT	AB10
VTT	J17
VTT	J21
VTT	J25
VTT	K16
VTT	K20
VTT	K24
VTT	L11
VTT	L13
VTT	L15
VTT	M12
VTT	N11
VTT	T12
VTT	U11
VTT	Y12
VTT_NCTF	AE13
VTT_NCTF	M16
VTT_NCTF	N15
VTT_NCTF	P14
VTT_NCTF	R13
VTT_NCTF	T14
VTT_NCTF	W13

13.6 Package Mechanical Information

13.6.1 Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Package Information

The Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipsets come in an FCBGA package, which is similar to the Mobile Processor package. The package consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

The Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset package is a 1466 ball FCBGA. Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994. The dimensions are in millimeters.

- Package parameters: 37.5 mm x 37.5 mm
- Land metal diameter: 524 microns
- Solder resist opening: 470 microns

Tolerances:

- .X - ± 0.1
- .XX - ± 0.05
- Angles - ± 1.0 degrees

Figure 39. Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Package FCBGA

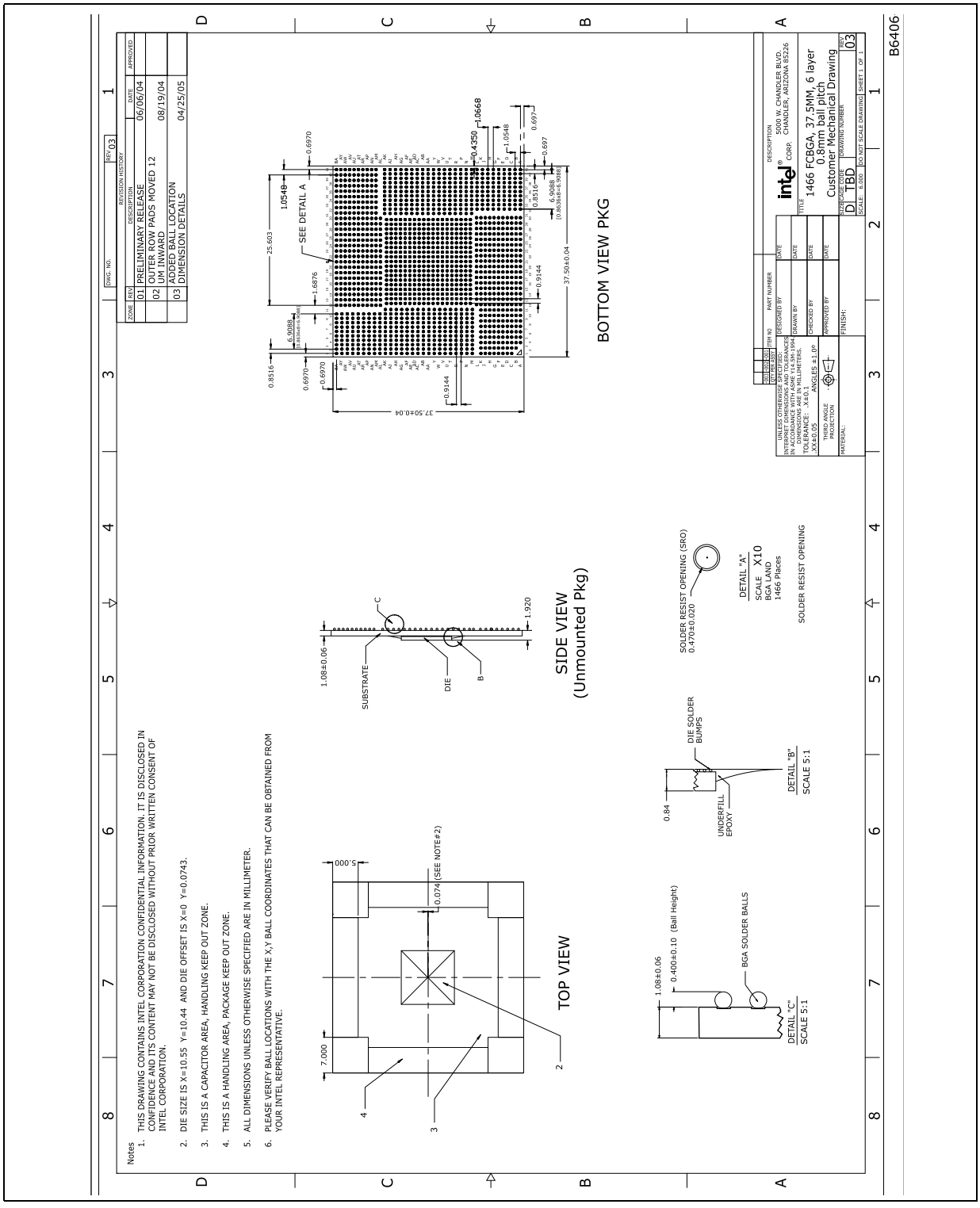


Figure 40. Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Package FCBGA (Top View)

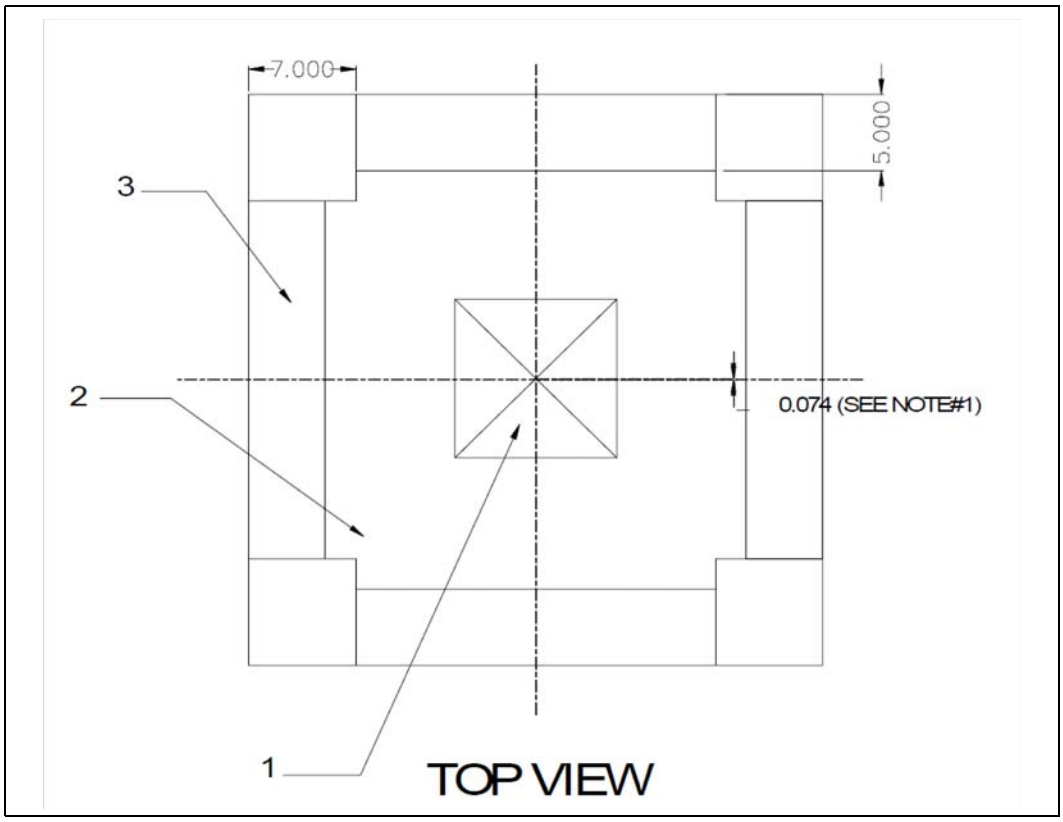


Figure 41. Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Package FCBGA (Side View)

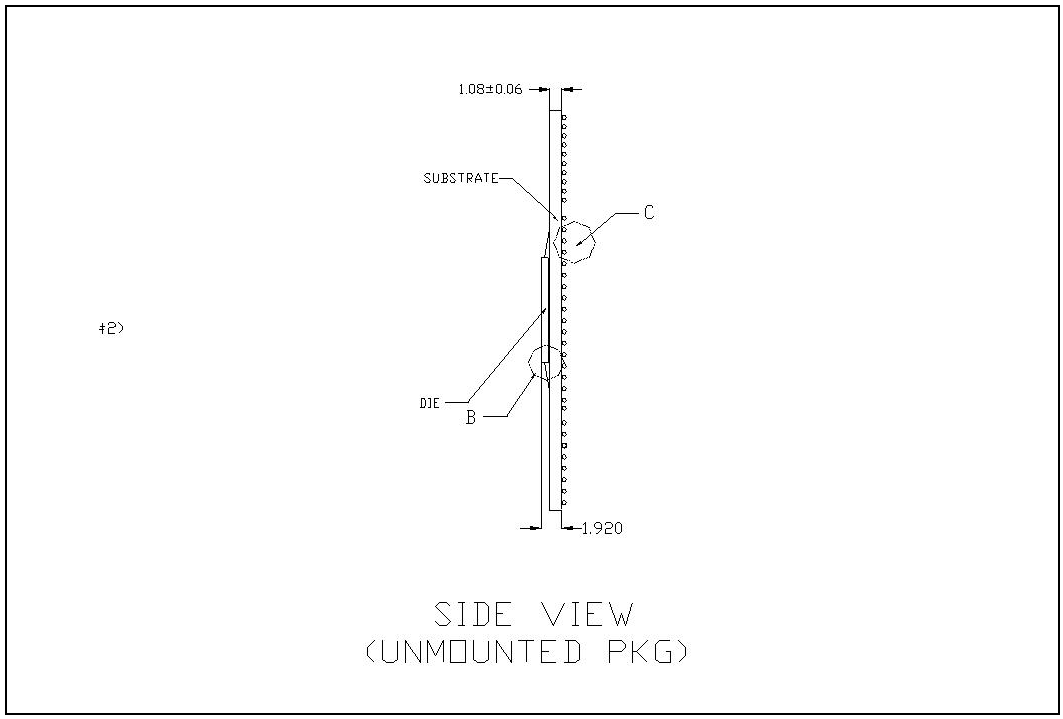


Figure 42. Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Package FCBGA (Bottom View)

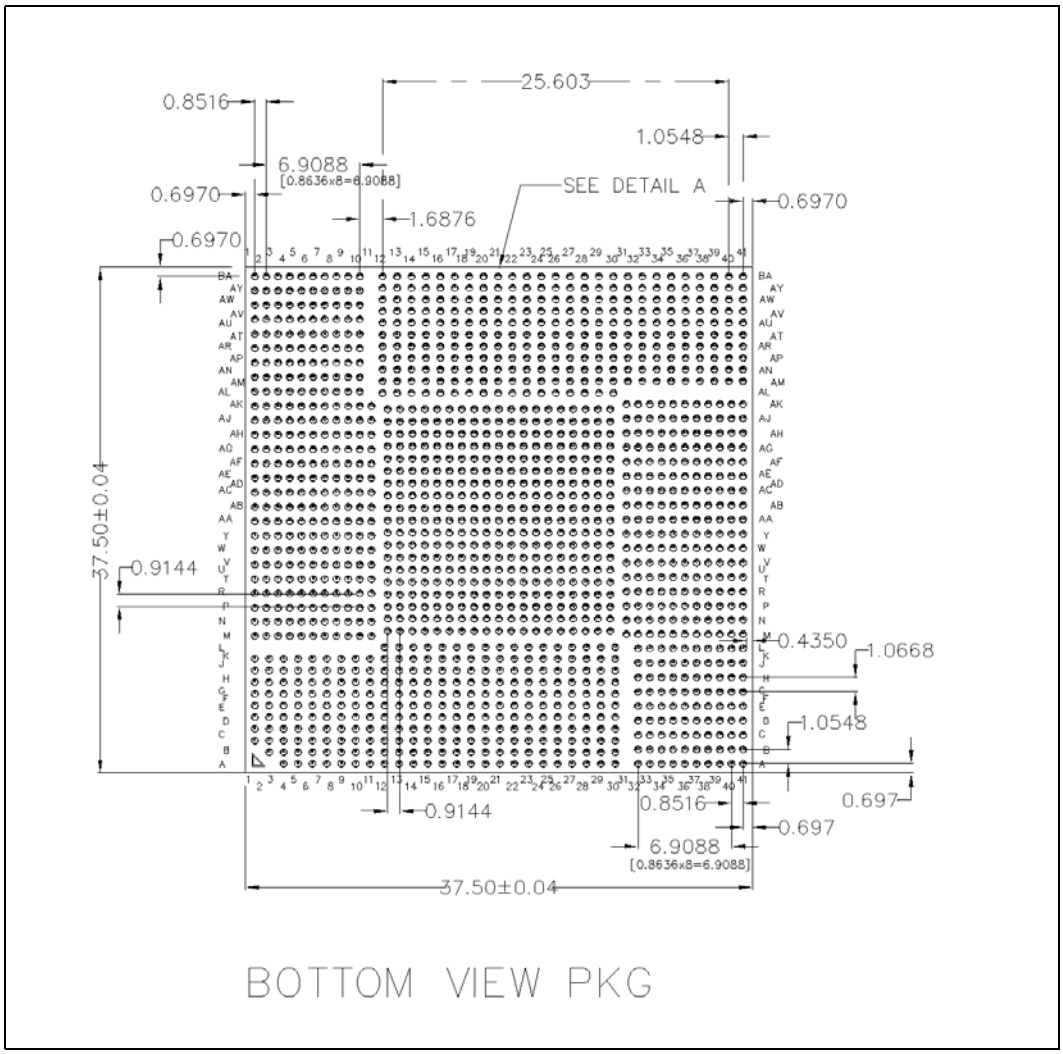
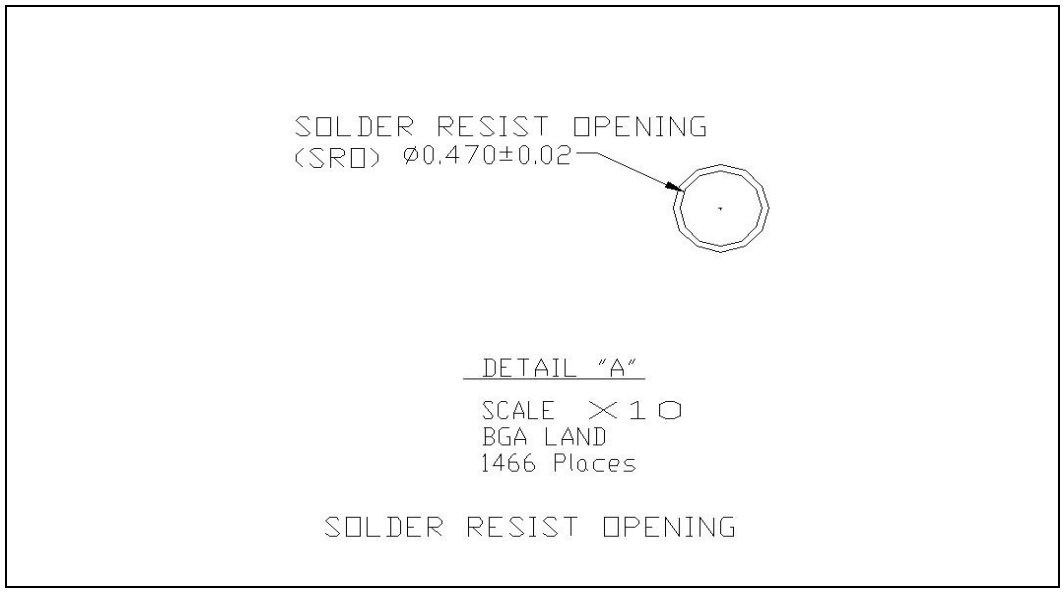


Figure 43. Mobile Intel 945GM/GME/PM, 943/940GML and Intel 945GT Express Chipset Package FCBGA SRO Details



13.6.2 Mobile Intel 945GMS/GSE Express Chipset Package Dimensions

The Intel 945GMS/GSE Express Chipset comes in an FCBGA package, which is similar to the Mobile Processor package. The package consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

The Intel 945GMS/GSE Express Chipset package is a 998 ball FCBGA. Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994. The dimensions are in millimeters.

- Package parameters: 27 mm x 27 mm
- Land metal diameter: 500 microns
- Solder resist opening: 430 microns

Tolerances:

- .X - ± 0.1
- .XX - ± 0.05
- Angles - ± 1.0 degrees

Figure 44. Mobile Intel 945GMS/GSE Express Chipset Package FCBGA

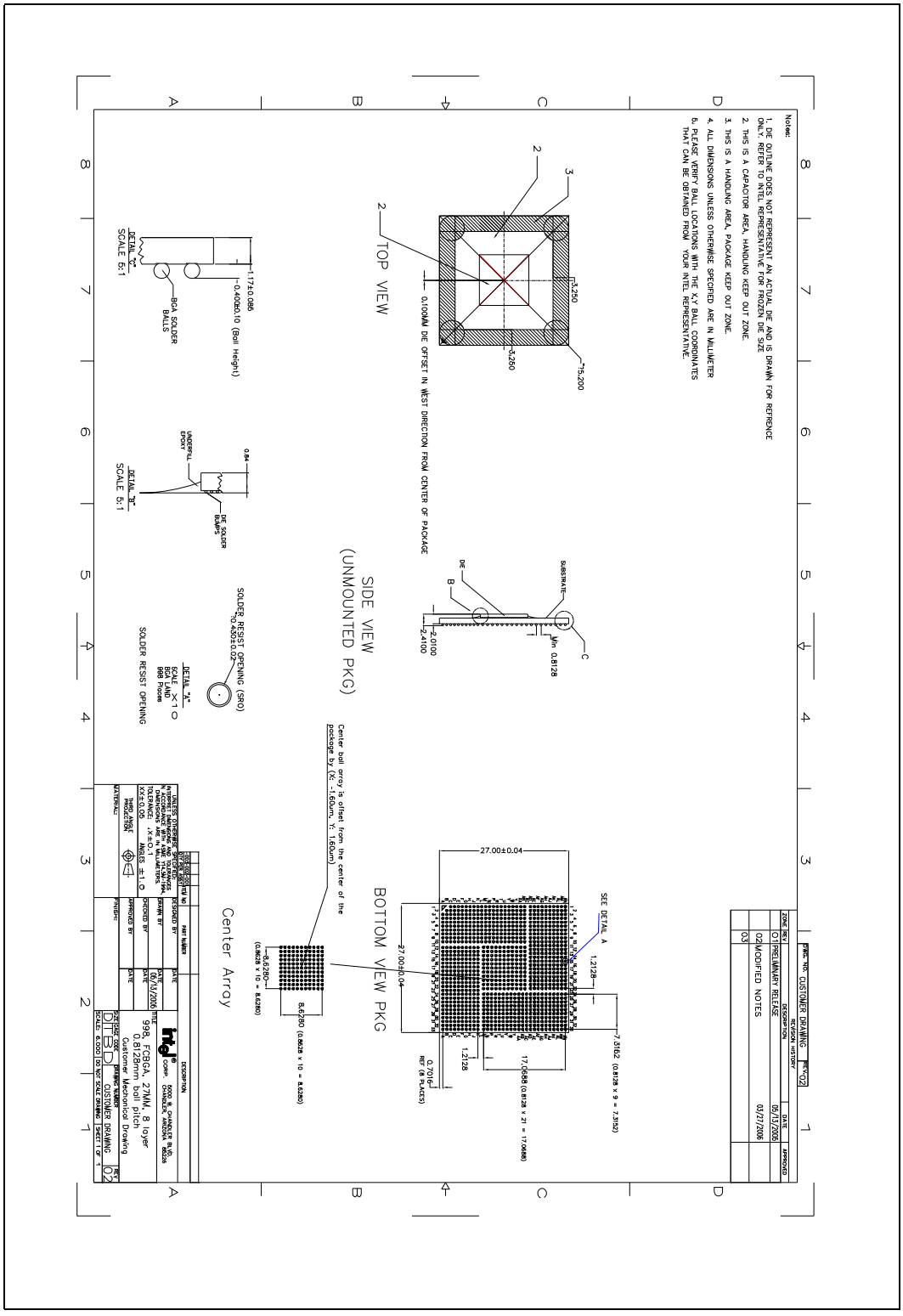


Figure 45. Mobile Intel 945GMS/GSE Express Chipset Package FCBGA (Top View)

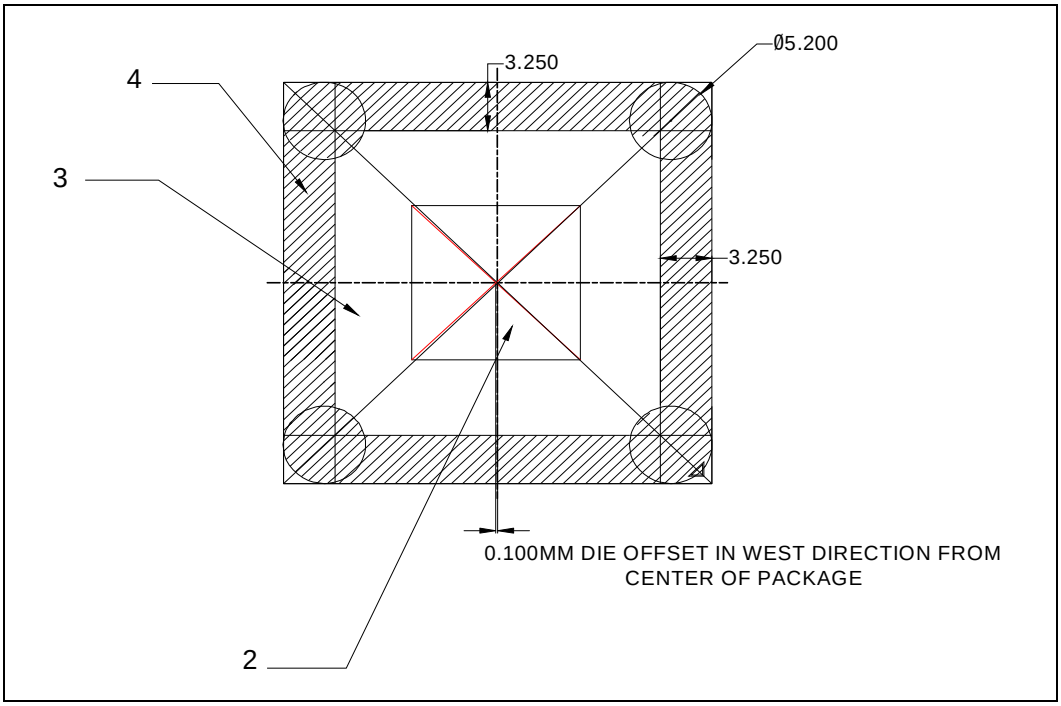


Figure 46. Mobile Intel 945GMS/GSE Express Chipset Package FCBGA (Side View)

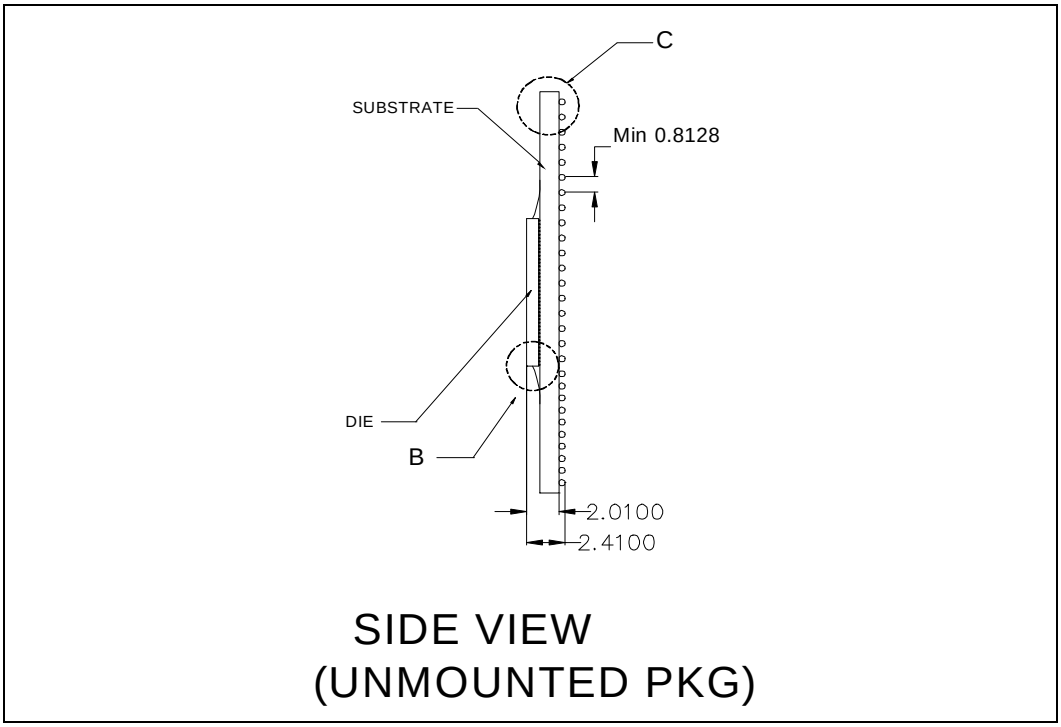


Figure 47. Mobile Intel 945GMS/GSE Express Chipset Package FCBGA (Bottom View)

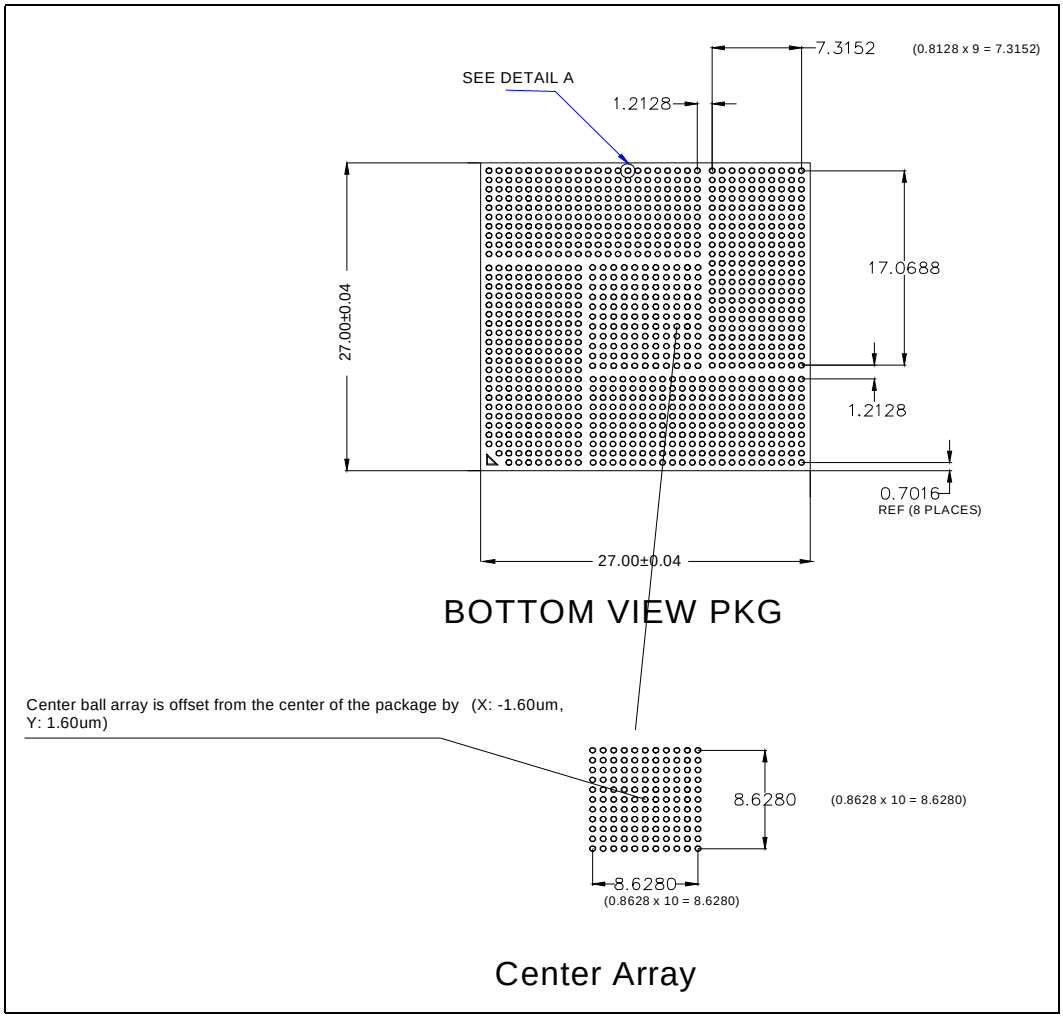
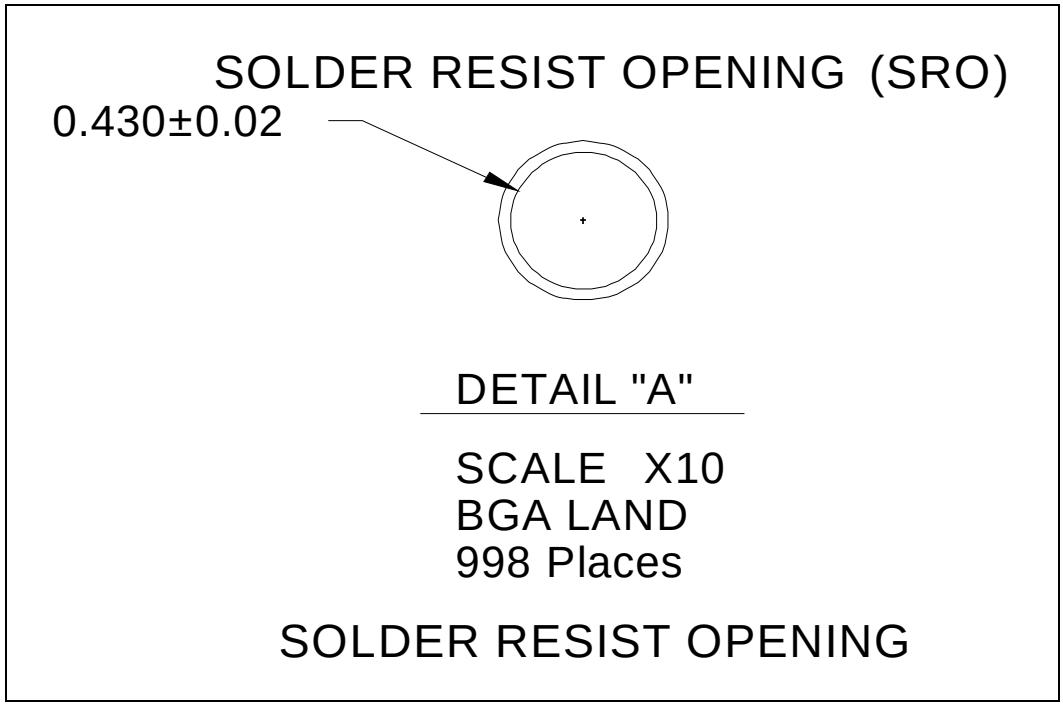


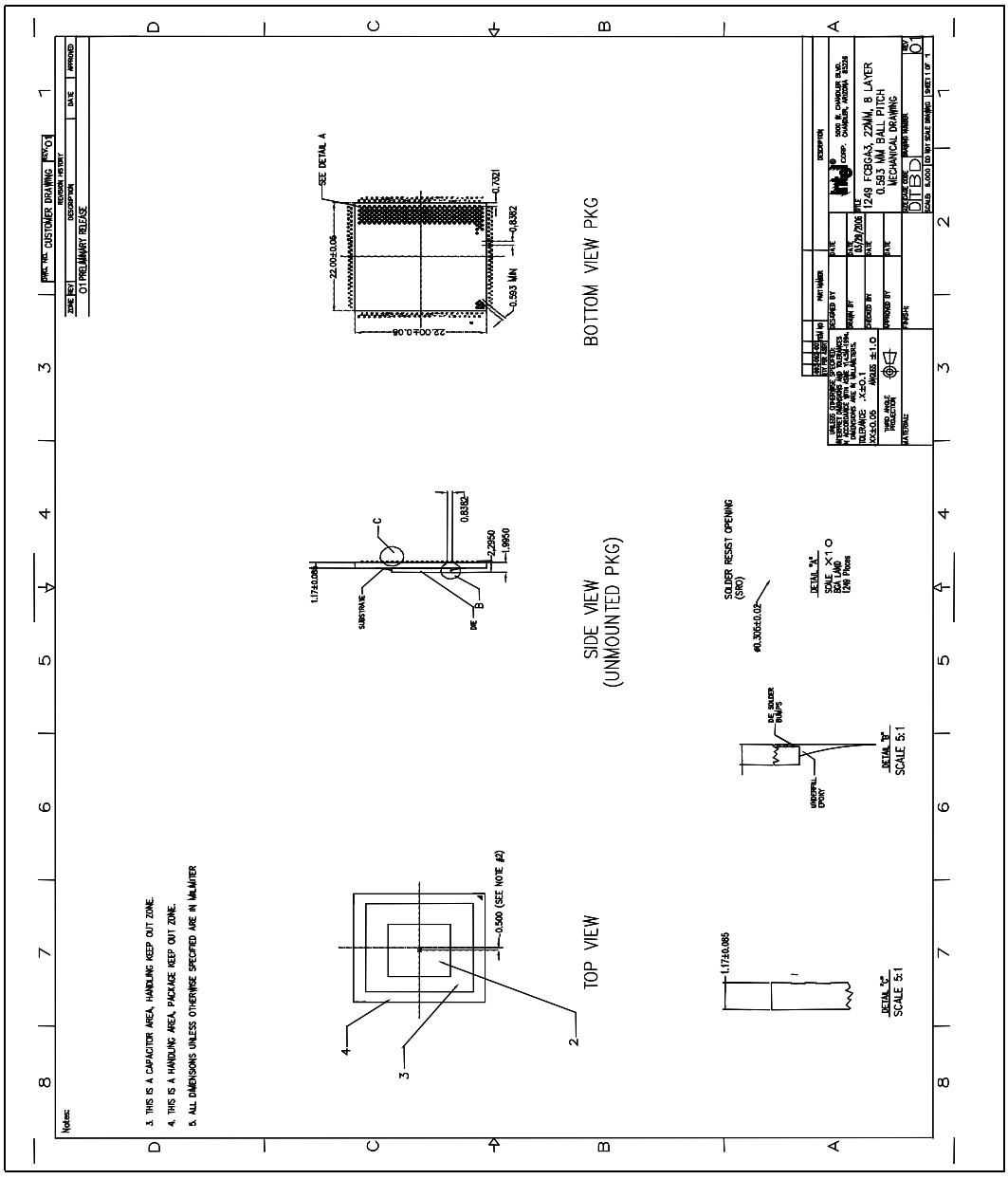
Figure 48. Mobile Intel 945GMS/GSE Express Chipset Package FCBGA SRO Details



13.6.3 Ultra Mobile Intel 945GU Express Chipset Package Information

Figure 49 is the (G)MCH package drawing. The (G)MCH is in a FCBGA package with 1429 balls. The package size is 22 mm x 22 mm. The ball pitch is 0.593-mm x 0.893-mm.

Figure 49. Intel 82945GU Package



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