



Am2976

Eleven-Bit Dynamic Memory Driver

DISTINCTIVE CHARACTERISTICS

- Internal resistors eliminate need for external series resistors and reduce package count
- Guaranteed maximum undershoot of -0.5 V on HIGH-to-LOW transition
- Glitch-free outputs during power-up and power-down
- Simple "flow-through" pinout
- Large capacitive drive capability (up to 88 DRAMS) designed to drive 16K, 64K, 256K, 1M and 4M dynamic-memory arrays
- 24-pin, 0.3-inch space-saving plastic dual in-line package and 28-pin plastic leaded chip carrier

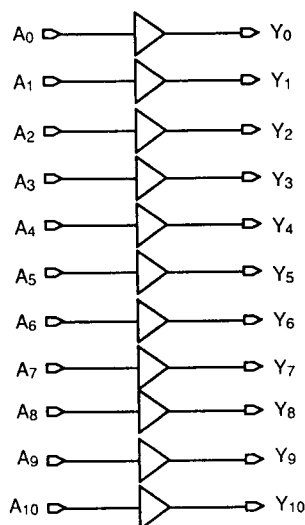
GENERAL DESCRIPTION

The Am2976 is an 11-bit bipolar Dynamic RAM Driver designed to drive the capacitive input characteristics of the address and control lines of 64K, 256K, 1M and 4M MOS dynamic RAMs. This device has non-inverting drivers and is functionally similar to the Am2966, but contains eleven drivers to accommodate wider address paths. A significant performance advantage of the increase in drivers per device is the ability to combine more signals onto a single device, thus minimizing skew time between drivers (i.e., $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$).

The architecture of the lower output driver includes an internal collector-resistor to control undershoot (not to

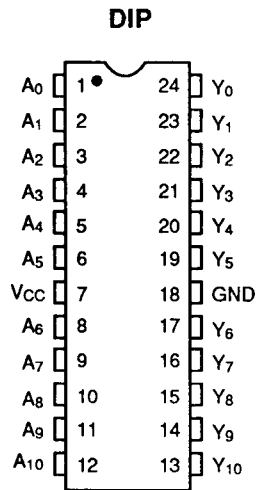
exceed -0.5 V) on the HIGH-to-LOW transition. This design also allows for control of the output fall time without slowing the output rise. The upper output driver pulls up to 2.7 V minimum to be compatible with MOS memory and is designed to have a rise time symmetrical with the low output's controlled fall times. The output impedance, 25 ohms nominal, is identical in both the logic HIGH and LOW states — this value was selected to match the intrinsic impedance of a PC board trace. The inclusion of internal resistors eliminates the need for additional external series resistors, therefore reducing package count and saving board area.

LOGIC DIAGRAM



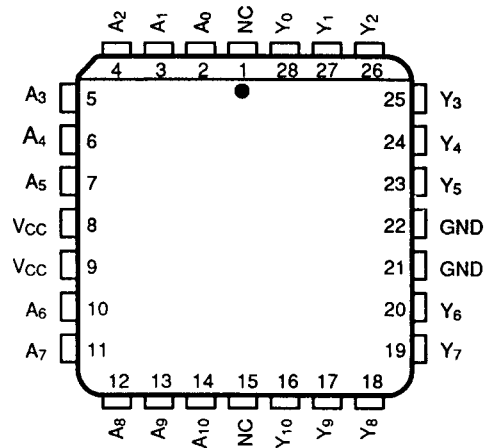
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CONNECTION DIAGRAMS



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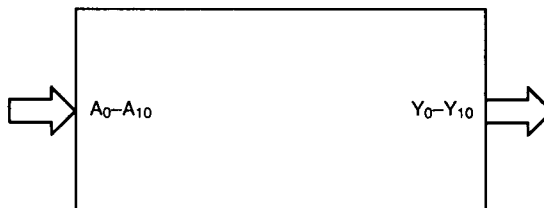
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Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Power Supply
GND = Ground

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RELATED AMD PRODUCTS

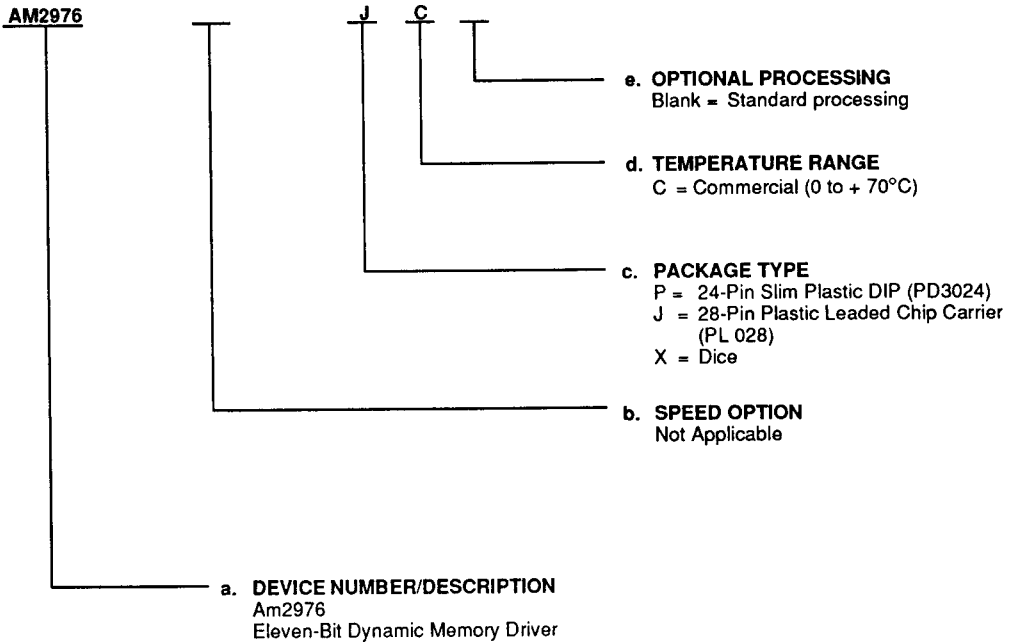
Part No.	Description
Am29368	1M Dynamic Memory Controller/Driver
Am29C60A	High Speed CMOS Cascadable 16-Bit EDC
Am29C660D	12 ns CMOS Cascadable 32-Bit EDC
Am29C668	4M Configurable Dynamic Memory Controller/Driver
Am2968A	256K Dynamic Memory Controller/Driver
Am29C983A	9-Bit x 4-Port Multiple Bus Exchange, High Speed
Am29C985	9-Bit x 4-Port Multiple Bus Exchange with Parity
Am2965/6	8-Bit Dynamic RAM Driver Inverting/Non-Inverting

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM2976	PC, JC, XC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

PIN DESCRIPTION

A₀–A₁₀

Driver (Address) Input (Inputs — 11)

These eleven pins are the inputs to the driver.

Y₀–Y₁₀

Driver (General Control) Output (Outputs — 11)

These eleven pins are the outputs from the driver.

V_{CC}, GND

Power, Ground Power Pair

TTL power and ground pins. The chip carrier package has two of each and the DIP has one of each.

FUNCTIONAL DESCRIPTION

Functional Description of the Am2976 is summarized on page one under General Description. For a Typical Out-

put Driver diagram and a Function Table, refer to Figure 1 and Table 1, which follow.

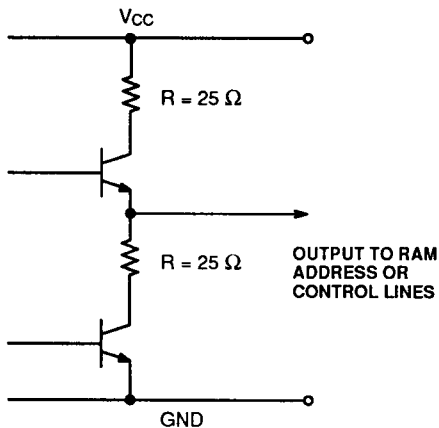


Table 1. Function Table

Inputs	Outputs
A ₀ –A ₁₀	Y ₀ –Y ₁₀
H	H
L	L

Key: H = HIGH
L = LOW

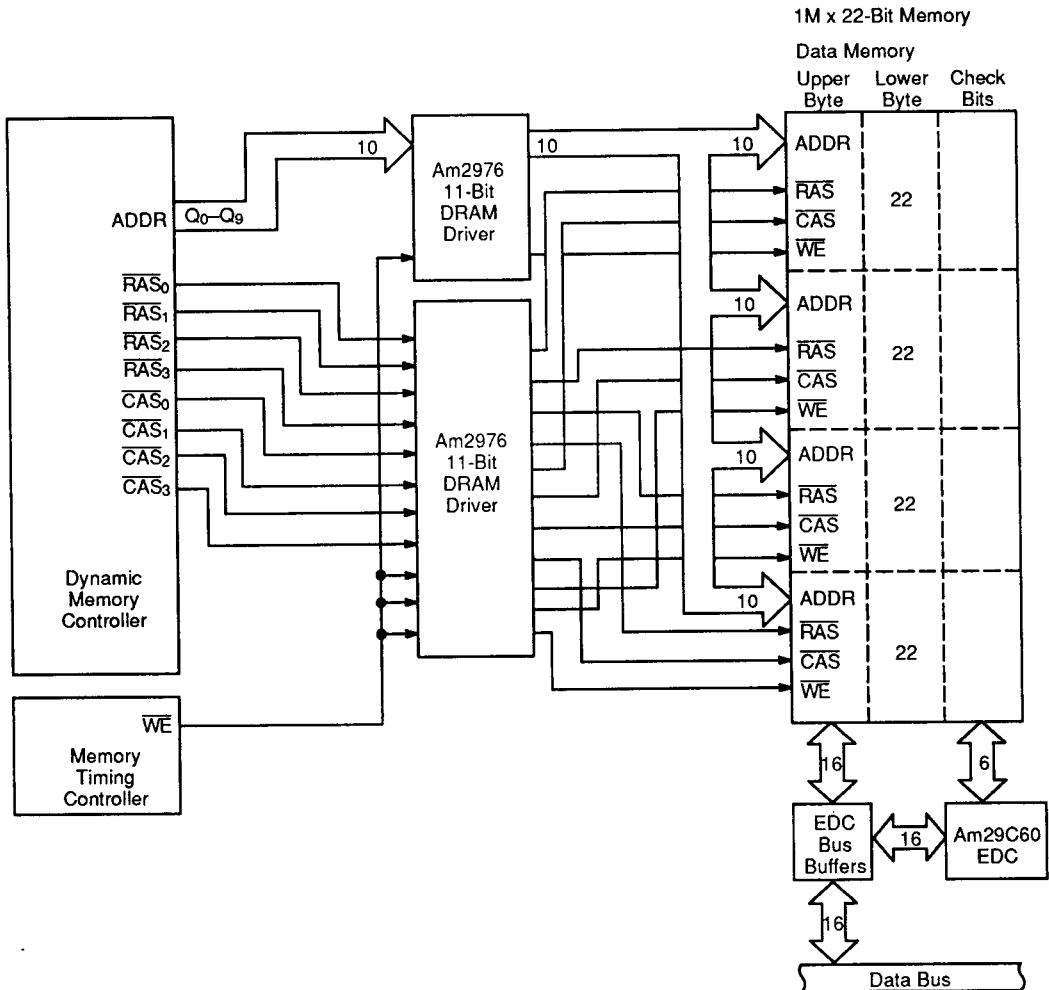
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Figure 1. Typical Output Driver

APPLICATIONS

The Am2976 is designed for use with a Dynamic Memory Controller — the Am29C668, for example — where large dynamic memories with highly capacitive input lines require additional buffering. A fully utilized memory system consists of four banks of dynamic RAMs (see Figure 2). Each bank uses identical address inputs but has individual $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ inputs. Only two de-

VICES are required to drive ten address lines, four $\overline{\text{RAS}}$ lines, four $\overline{\text{CAS}}$ lines, and four $\overline{\text{WE}}$ lines. Referencing Figure 2, note that the $\overline{\text{RAS}}$ and the $\overline{\text{CAS}}$ inputs to the memory array come from one device — thus minimizing the skew between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lines — optimizing the system's performance.



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Figure 2. Am2976 Application Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient/Case Temperature with Power Applied	-55 to +125°C
Supply Voltage with Respect to Ground	-0.5 to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	-1.5 to $V_{CC\ Max.}$
DC Input Voltage	-0.5 to +7.0 V
DC Output Short-Circuit Current	200 mA
DC Input Current	-30 to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage	5.0 V \pm 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.





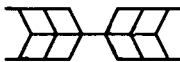
DC CHARACTERISTICS over operating ranges unless otherwise specified (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH};$ $I_{OH} = -1 \text{ mA}$	2.8		V	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.},$ $V_{IN} = V_{IH}$	$I_{OL} = 1 \text{ mA}$		0.5	V
			$I_{OL} = 12 \text{ mA}$		0.8	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs	2.0		V	
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		0.8	V	
V_I	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-1.5	V	
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = 0.4 \text{ V}$		-0.4	mA	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = 2.4 \text{ V}$		20	μA	
I_I	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = 5.5 \text{ V}$		100	μA	
I_{sc}	Output Short-Circuit Current	$V_{CC} = \text{Max. (Note 2)}$	-75	-275	mA	
I_{CC}	Power Supply Current	$T_A = 0 \text{ to } +70^\circ\text{C}$		90	mA	

Notes:

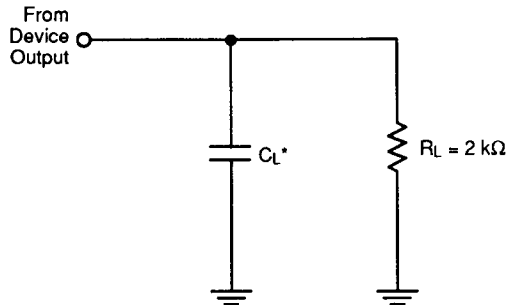
- For conditions shown as Min. or Max., use appropriate value as specified under Operation Ranges for applicable device type.
- Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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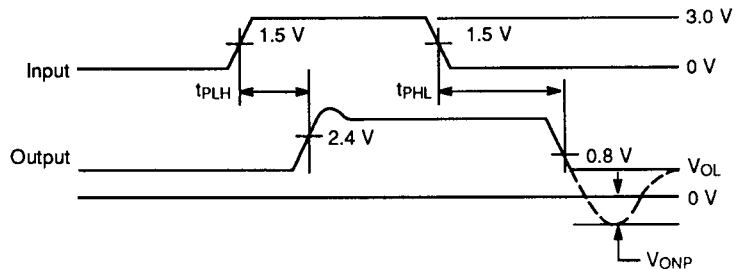
SWITCHING TEST CIRCUIT



* t_{PD} specified at $C_L = 50$ and 500 pF.

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SWITCHING TEST WAVEFORM

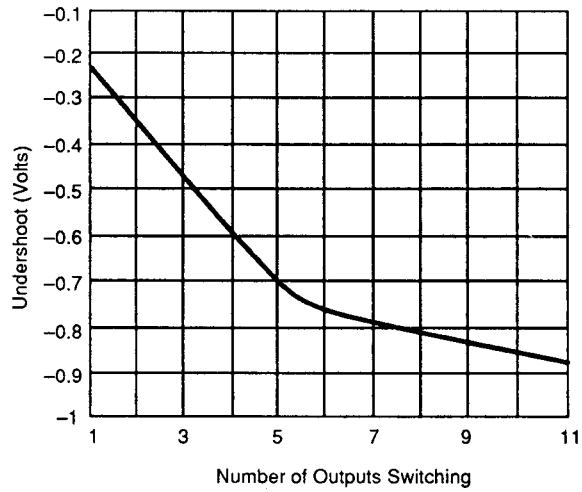


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SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	1 Output Switching		11 Outputs Switching		Unit	
			Min.	Max.	Min.	Max.		
C_L = 50 pF								
1	t _{PLH}	Propagation Delay from A _i to Y _i , LOW-to-HIGH Transition	C Devices		16		22	ns
2	t _{PHL}	Propagation Delay from A _i to Y _i , HIGH-LOW Transition	C Devices		12		14	ns
3	t _{SKEW}	Same Transition, Output to Output (Note 1)	C Devices		5		12	ns
4	t _{SKEW}	Opposite Transition, Output to Output (Note 1)	C Devices		9		16	ns
5	V _{ONP}	Output Voltage Undershoot (Note 2)	C Devices		-0.5		-1.0	V
C_L = 500 pF								
6	t _{PLH}	Propagation Delay from A _i to Y _i , LOW-HIGH Transition	C Devices		29		43	ns
7	t _{PHL}	Propagation Delay from A _i to Y _i , HIGH-LOW Transition	C Devices		33		36	ns
8	t _{SKEW}	Same Transition, Output to Output (Note 1)	C Devices		5		12	ns
9	t _{SKEW}	Opposite Transition, Output to Output (Note 1)	C Devices		9		16	ns
10	V _{ONP}	Output Voltage Undershoot (Note 2)	C Devices		-0.5		-0.5	V

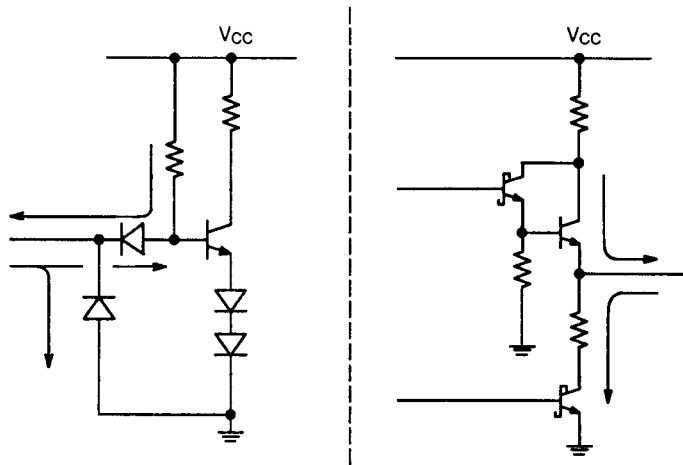
TYPICAL PERFORMANCE CURVE



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Undershoot vs. Outputs Switching

INPUT/OUTPUT CURRENT DIAGRAM



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