19-2064; Rev 1; 1/07

MAXIM

40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

General Description

The MAX9140/MAX9141 are single and the MAX9142/MAX9144 are dual/quad high-speed comparators optimized for systems powered from a 3V or 5V supply. The MAX9141 features latch enable and device shutdown. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 40ns, while supply current is only 150µA per comparator.

The input common-mode range of the MAX9140/MAX9141/MAX9142/MAX9144 extends beyond both power-supply rails. The outputs pull to within 0.3V of either supply rail without external pullup circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The MAX9140/MAX9141/MAX9142/MAX9144 are higher-speed, lower-power, and lower-cost upgrades to industry-standard comparators MAX941/MAX942/MAX944.

The MAX9140 are offered in tiny 5-pin SC70 and SOT23 packages. The MAX9141 and MAX9142 are available in 8-pin SOT23 and SO packages, while the MAX9144 is available in both 14-pin SO and TSSOP packages.

Applications

Line Receivers

Battery-Powered Systems

Threshold Detectors/Discriminators

3V/5V Systems

Zero-Crossing Detectors

Sampling Circuits

Features

- **Fast, 40ns Propagation Delay (10mV Overdrive)**
- **Low Power**
  0.45mW Power Dissipation Per Comparator (3V)
  150µA Supply Current
- **Optimized for 3V and 5V Applications (Operation Down to 2.7V)**
- **Rail-to-Rail Input Voltage Range**
- **Low, 500µV Offset Voltage**
- **Internal Hysteresis for Clean Switching**
- **Outputs Swing 300mV of Power Rails**
- **CMOS/TTL-Compatible Outputs**
- **Output Latch (MAX9141 Only)**
- **Shutdown Function (MAX9141 Only)**
- **Available in SC70 and SOT23 Packages**

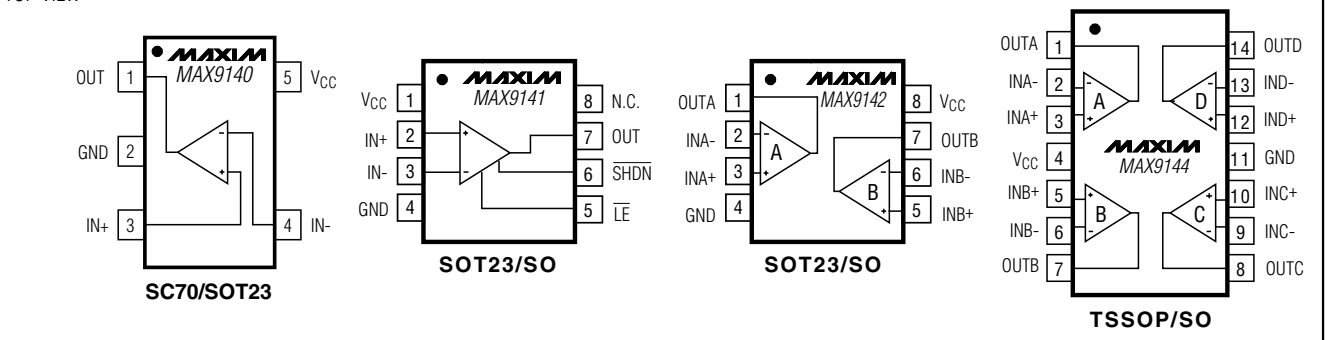
Ordering Information

PART*	PIN-PACKAGE	TOP MARK	PKG CODE
MAX9140EXK-T	5 SC70-5	ACC	X5-1
MAX9140EUK-T	5 SOT23-5	ADQP	U5-1
MAX9141EKA-T	8 SOT23-8	AAFD	K8-5
MAX9141ESA	8 SO	—	S8-2
MAX9142EKA-T	8 SOT23-8	AAFE	K8-5
MAX9142ESA	8 SO	—	S8-2
MAX9144EUD	14 TSSOP	—	U14-1
MAX9144ESD	14 SO	—	S14-1

**All devices specified over the -40°C to +85°C temperature range.*

Pin Configurations

TOP VIEW



40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Power-Supply Ranges
- Supply Voltage (V_{CC} to GND).....+6V
- Differential Input Voltage.....-0.3V to (V_{CC} + 0.3V)
- Common-Mode Input Voltage to GND ..-0.3V to (V_{CC} + 0.3V)
- $\overline{LE}$ Input Voltage (MAX9141 only) .....-0.3V to (V_{CC} + 0.3V)
- $\overline{SHDN}$ Input Voltage (MAX9141 only)....-0.3V to (V_{CC} + 0.3V)

Current into Input Pins.....±20mA

Input/Output Short-Circuit Duration to V_{CC} or GND .....Continuous

Continuous Power Dissipation (T_A = +70°C)
- 5-Pin SC70 (derate 3.1mW/°C above +70°C).....247mW
- 5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW
- 8-Pin SOT23 (derate 9.1mW/°C above +70°C).....727mW
- 8-Pin SO (derate 5.9mW/°C above +70°C).....470.6mW
- 14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
- 14-Pin SO (derate 8.33mW/°C above +70°C).....666.7mW

Operating Temperature Range .....-40°C to +85°C

Storage Temperature Range.....-65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{CM} = 0, $\overline{SHDN}$ = $\overline{LE}$ = V_{CC} (MAX9141 only), C_L = 15pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}	(Note 2)		2.7		5.5	V
Input Voltage Range	V_{CMR}	(Note 3)		-0.2		V_{CC} + 0.2	V
Input Offset Voltage	V_{OS}	(Note 4)	T_A = +25°C		0.5	2	mV
			T_A = T_{MIN} to T_{MAX}			4.5	
Input Hysteresis	V_{HYST}	(Note 5)			1.5		mV
Input Bias Current	I_B	(Note 6)			90	320	nA
Input Offset Current	I_{OS}				8	120	nA
Common-Mode Rejection Ratio	CMRR	V_{CC} = 5.5V (Note 7)			80	800	µV/V
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{CC} ≤ 5.5V			80	750	µV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA		V_{CC} - 0.425	V_{CC} - 0.3		V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.3	0.425	V
Output Leakage Current	I_{LEAK}	$\overline{SHDN}$ = GND, MAX9141 only (Note 8)			0.04	1	µA
Supply Current (Per Comparator)	I_{CC}	V_{CM} = V_{CC} = 3V	MAX9141		165	275	µA
			MAX9140/MAX9142/MAX9144		150	250	
		V_{CM} = V_{CC} = 5V	MAX9141		200	320	
			MAX9140/MAX9142/MAX9144		165	300	
		MAX9141 only, $\overline{SHDN}$ = GND; V_{CC} = V_{CM} = 3V			12	30	
Propagation Delay	t_{PD+}, t_{PD-}	V_{CC} = 3V, V_{OD} = 10mV			40		ns
Differential Propagation Delay	dt_{PD}	V_{OD} = 10mV (Note 9)			2		ns
Propagation Delay Skew		V_{OD} = 10mV (Note 10)			2		ns
Logic Input-Voltage High	V_{IH}	(Note 11)		(V_{CC} / 2) +0.4	V_{CC} / 2		V
Logic Input-Voltage Low	V_{IL}	(Note 11)			V_{CC} / 2	(V_{CC} / 2) -0.4	V
Logic Input Current	I_{IL}, I_{IH}	V_{LOGIC} = 0 to V_{CC} (Note 11)			2	10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{CM} = 0, $\overline{SHDN}$ = $\overline{LE}$ = V_{CC} (MAX9141 only), C_L = 15pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data-to-Latch Setup Time	t_S	(Note 12)		16		ns
Latch-to-Data Hold Time	t_H	(Note 12)		16		ns
Latch Pulse Width	t_{LPW}	(Note 12)		45		ns
Latch Propagation Delay	t_{LPD}	(Note 12)		60		ns
Shutdown Enable Time		(Note 13)		1		µs
Shutdown Disable Time		(Note 13)		5		µs

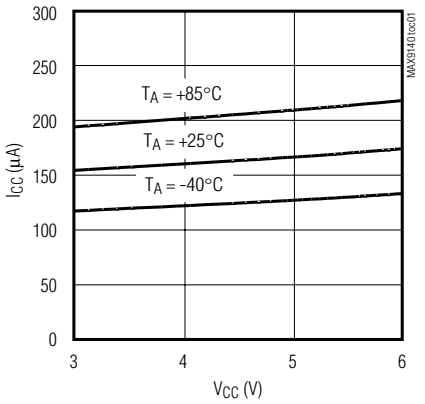
Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Inferred from PSRR test.
Note 3: Inferred from CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.
Note 4: V_{OS} is defined as the center of the input-referred hysteresis zone. See Figure 1.
Note 5: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone. See Figure 1.
Note 6: The polarity of I_B reverses direction as V_{CM} approaches either supply rail.
Note 7: Specified over the full common-mode voltage range (V_{CMR}).
Note 8: Specification is for current flowing into or out of the output pin for V_{OUT} driven to any voltage from V_{CC} to GND while the part is in shutdown.
Note 9: Specified between any two channels in the MAX9142/MAX9144.
Note 10: Specified as the difference between t_{PD+} and t_{PD-} for any one comparator.
Note 11: Applies to the MAX9141 only for both $\overline{SHDN}$ and $\overline{LE}$.
Note 12: Applies to the MAX9141 only. Comparator is active with $\overline{LE}$ driven high and is latched with $\overline{LE}$ driven low (V_{OD} = 10mV). See Figure 2.
Note 13: Applicable to the MAX9141 only. Comparator is active with the $\overline{SHDN}$ driven high and is shutdown with $\overline{SHDN}$ driven low. Shutdown enable time is the delay when the $\overline{SHDN}$ is driven high to the time the output is valid. Shutdown disable time is the delay when the $\overline{SHDN}$ is driven low to the time the comparator shuts down.

40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

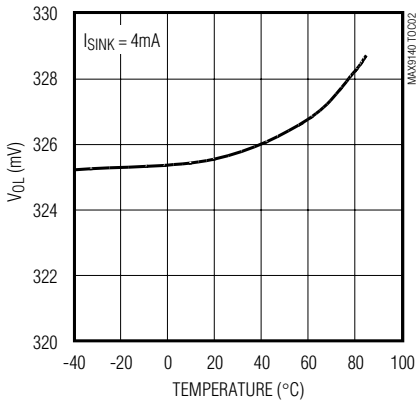
Typical Operating Characteristics

(V_{CC} = 3.0V, V_{CM} = 0, C_L = 15pF, V_{OD} = 10mV, T_A = +25°C, unless otherwise noted.)

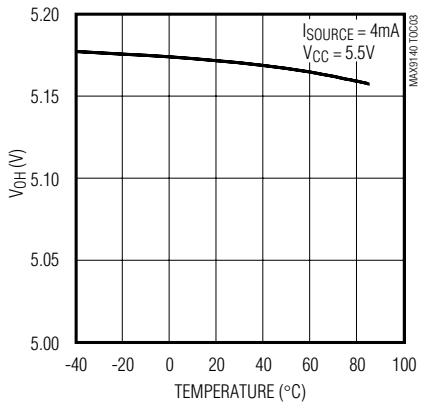
MAX9140 SUPPLY CURRENT vs. SUPPLY VOLTAGE



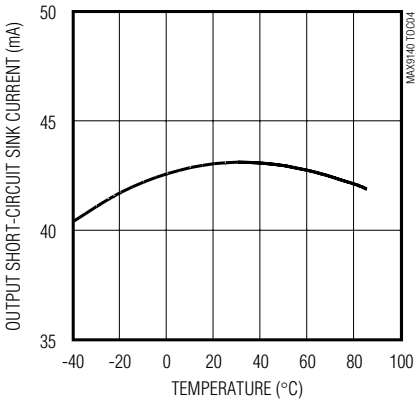
OUTPUT LOW VOLTAGE vs. TEMPERATURE



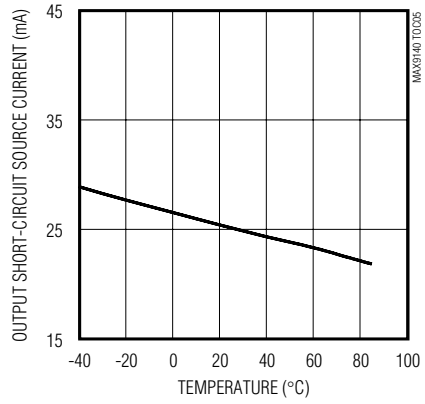
OUTPUT HIGH VOLTAGE vs. TEMPERATURE



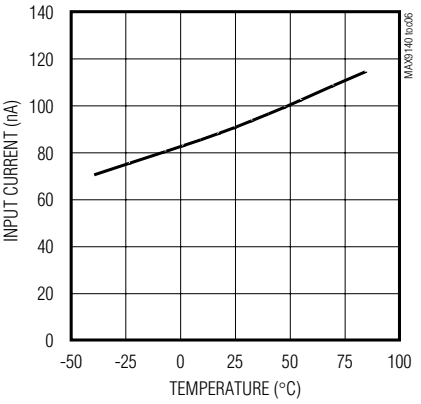
OUTPUT SHORT-CIRCUIT (SINK) CURRENT vs. TEMPERATURE



OUTPUT SHORT-CIRCUIT (SOURCE) CURRENT vs. TEMPERATURE



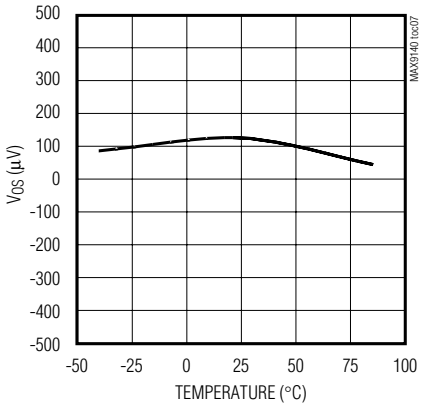
INPUT BIAS CURRENT vs. TEMPERATURE



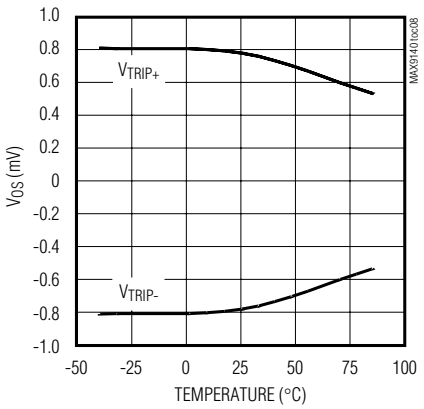
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, V_{CM} = 0, C_L = 15pF, V_{OD} = 10mV, T_A = +25°C, unless otherwise noted.)

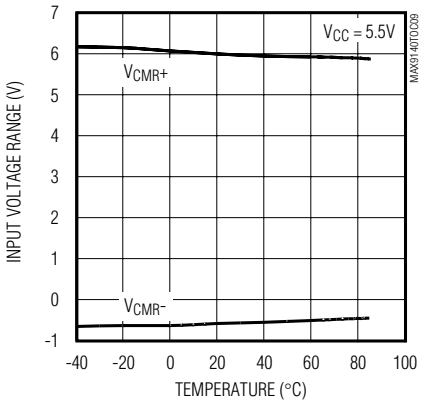
INPUT OFFSET VOLTAGE vs. TEMPERATURE



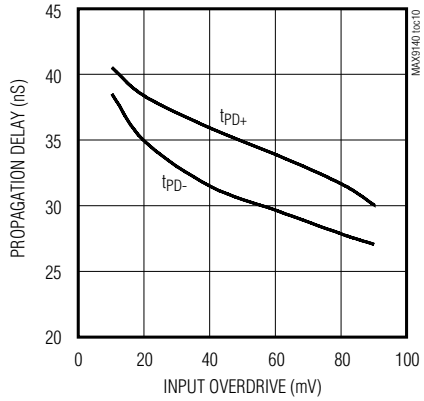
TRIP POINT vs. TEMPERATURE



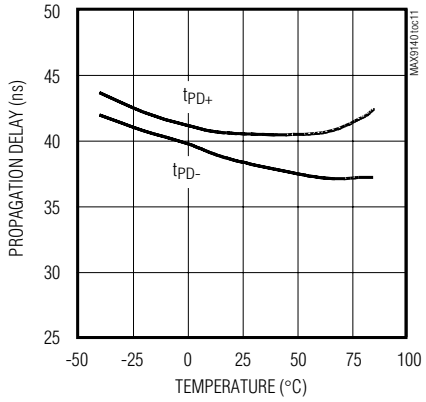
INPUT VOLTAGE RANGE vs. TEMPERATURE



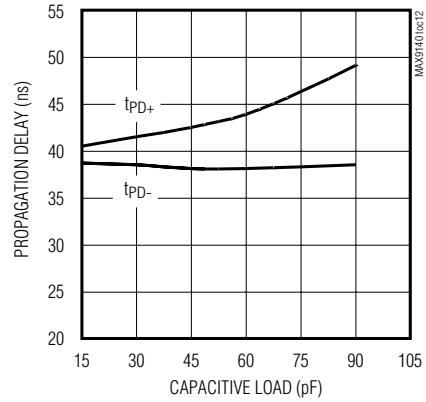
PROPAGATION DELAY vs. INPUT OVERDRIVE



PROPAGATION DELAY vs. TEMPERATURE



PROPAGATION DELAY vs. CAPACITIVE LOAD

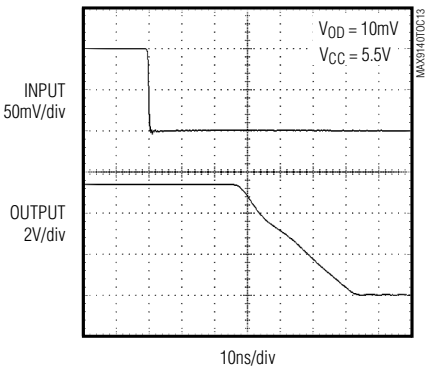


40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

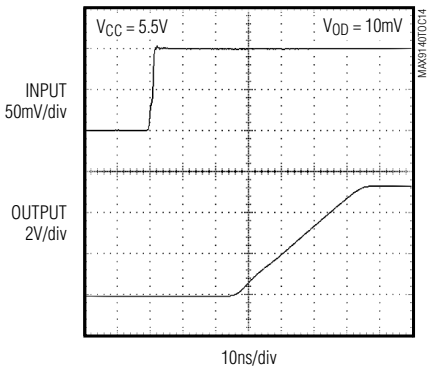
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, V_{CM} = 0, C_L = 15pF, V_{OD} = 10mV, T_A = +25°C, unless otherwise noted.)

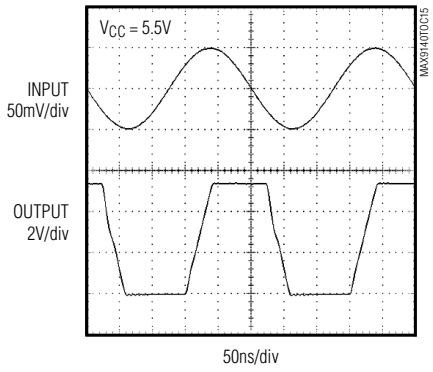
PROPAGATION DELAY (t_{PD}-)



PROPAGATION DELAY (t_{PD}+)



SINUSOID RESPONSE AT 4MHz



Pin Description

PIN				NAME	FUNCTION
MAX9140	MAX9141	MAX9142	MAX9144		
—	—	1	1	OUTA	Comparator A Output
—	—	2	2	INA-	Comparator A Inverting Input
—	—	3	3	INA+	Comparator A Noninverting Input
5	1	8	4	V_{CC}	Positive Supply
—	—	5	5	INB+	Comparator B Noninverting Input
—	—	6	6	INB-	Comparator B Inverting Input
—	—	7	7	OUTB	Comparator B Output
—	—	—	8	OUTC	Comparator C Output
—	—	—	9	INC-	Comparator C Inverting Input
—	—	—	10	INC+	Comparator C Noninverting Input
2	4	4	11	GND	Ground
—	—	—	12	IND+	Comparator D Noninverting Input
—	—	—	13	IND-	Comparator D Inverting Input
—	—	—	14	OUTD	Comparator D Output
3	2	—	—	IN+	Noninverting Input
4	3	—	—	IN-	Inverting Input
—	6	—	—	$\overline{SHDN}$	Shutdown: MAX9141 is active when $\overline{SHDN}$ is driven high; MAX9141 is in shutdown when $\overline{SHDN}$ is driven low.
—	5	—	—	$\overline{LE}$	The output is latched when $\overline{LE}$ is low. The latch is transparent when $\overline{LE}$ is high.
1	7	—	—	OUT	Comparator Output
—	8	—	—	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX9140/MAX9141/MAX9142/MAX9144 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are pulled to within 300mV of either supply rail without external pullup or pulldown circuitry. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment. The MAX9140/MAX9141/MAX9142/MAX9144 interface directly to CMOS and TTL logic.

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the MAX9140/MAX9141/MAX9142/MAX9144 have an internal hysteresis of 1.5mV.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. The average of the trip points is the offset voltage. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX9140/MAX9141/MAX9142/MAX9144's fixed internal hysteresis eliminates these resistors. To increase hysteresis and noise margin even more, add positive feedback with two resistors as a voltage divider from the output to the noninverting input.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX9141 includes an internal latch that allows storage of comparison results. The $\overline{LE}$ pin has a high input impedance. If $\overline{LE}$ is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is latched when $\overline{LE}$ is pulled low (Figure 2).

Shutdown Mode (MAX9141 Only)

The MAX9141 shuts down when the $\overline{SHDN}$ pin is low. When shut down, the supply current drops to less than 12µA, and the three-state output becomes high impedance. The $\overline{SHDN}$ pin has a high-input impedance. Connect $\overline{SHDN}$ to V_{CC} for normal operation. Exit shutdown with $\overline{LE}$ high (transparent state); otherwise, the output will be indeterminate.

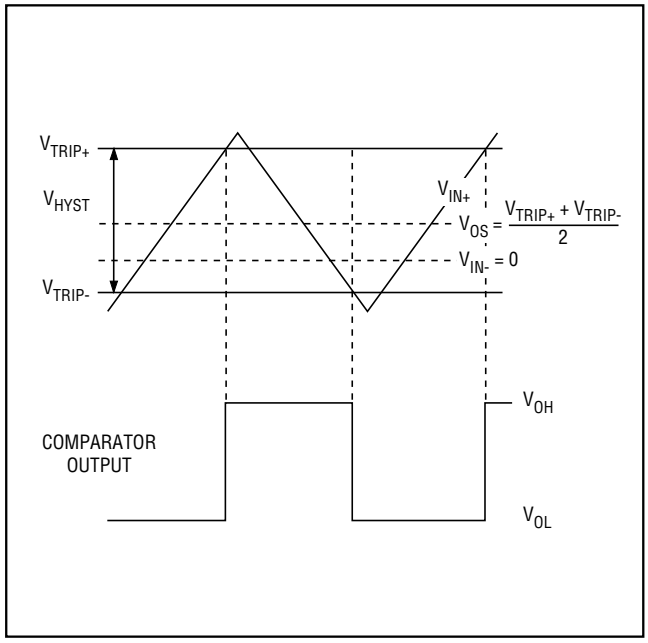


Figure 1. Input and Output Waveform, Noninverting Input Varied

Input Stage Circuitry

The MAX9140/MAX9141/MAX9142/MAX9144 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two back-to-back diodes between IN+ and IN- as well as two series 4.1kΩ resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to be no more than $2V_F$, where V_F is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding $2V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input Current} = \frac{(IN+ - IN-) - 2V_F}{2 \times 4.1k\Omega}$$

Input current with large differential input voltages should not be confused with input bias current (I_B). As long as the differential input voltage is less than $2V_F$, this input current is equal to I_B. The output is in the correct logic state if one or both inputs are within the common-mode range.

40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

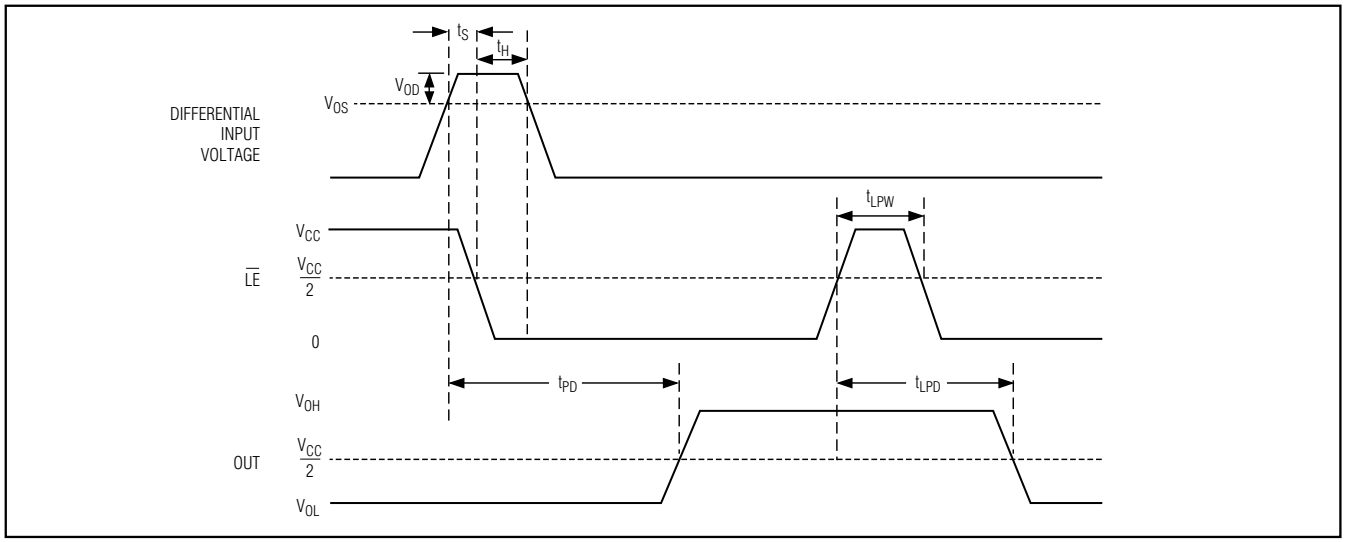


Figure 2. MAX9141 Timing Diagram with Latch Operator

Output Stage Circuitry

The MAX9140/MAX9141/MAX9142/MAX9144 contain a current-driven output stage as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noise-sensitive applications where fast edges may cause interference.

Applications Information

Circuit Layout and Bypassing

The high-gain bandwidth of the MAX9140/MAX9141/MAX9142/MAX9144 requires design precautions to realize the full high-speed capabilities of these comparators. The recommended precautions are:

1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V_{CC} as possible.

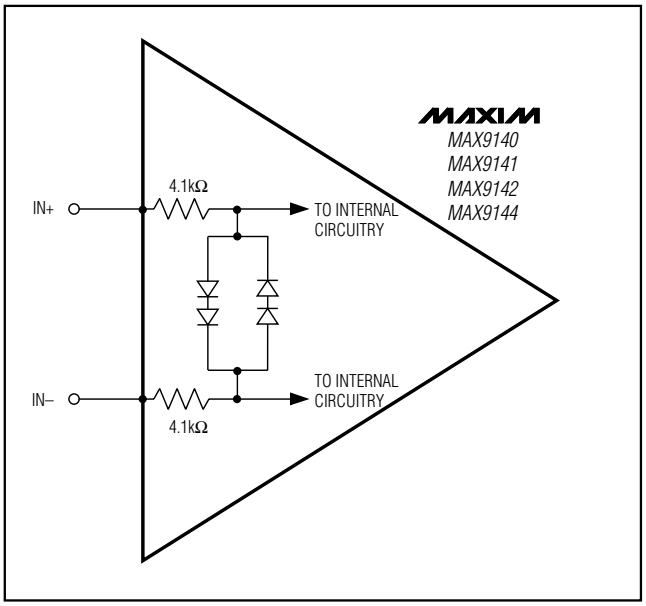


Figure 3. Input Stage Circuitry

3) Pay close attention to the decoupling capacitor's bandwidth, keeping leads short.
4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
5) Solder the device directly to the printed circuit board instead of using a socket.

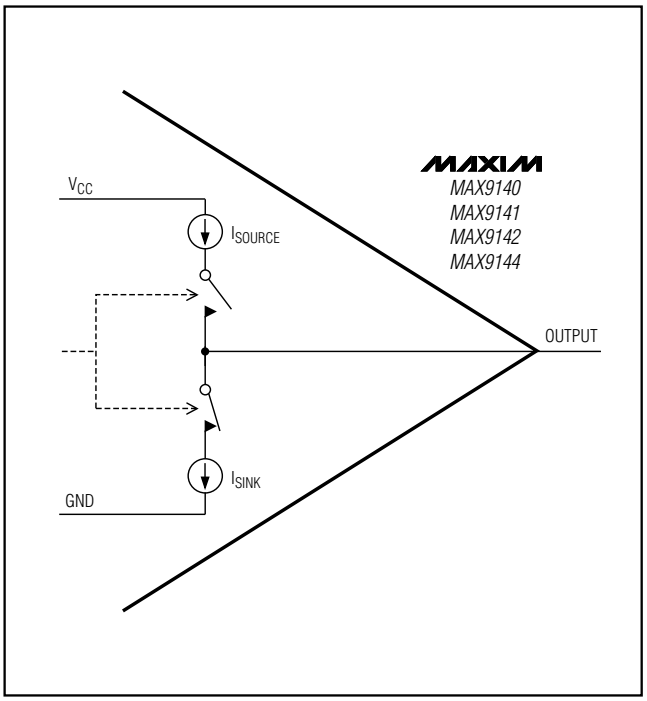


Figure 4. Output Stage Circuitry

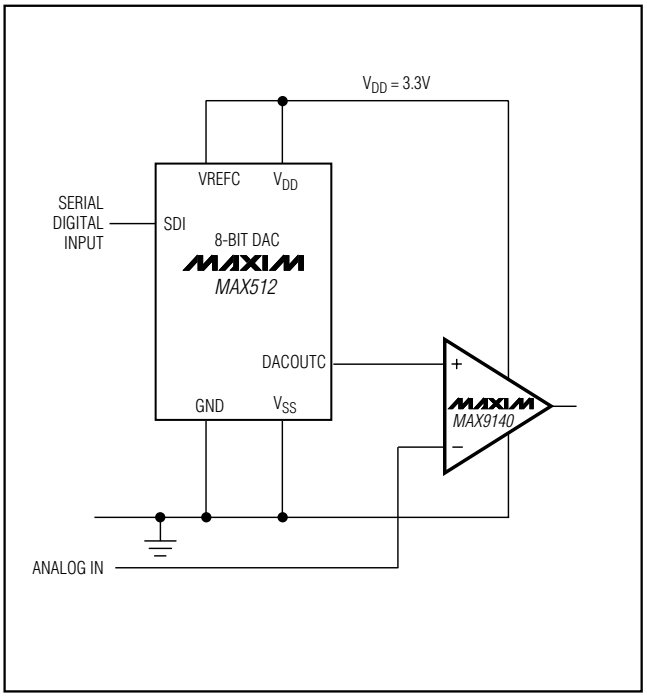


Figure 5. 3.3V Digitally Controlled Threshold Detector

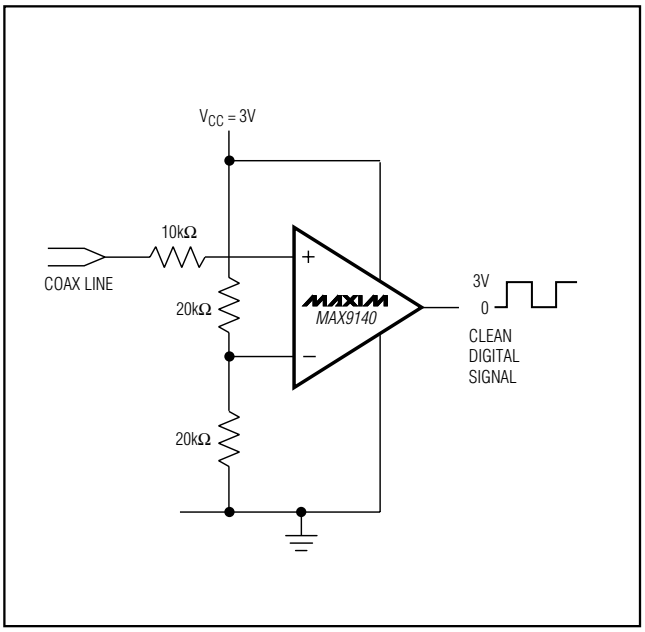


Figure 6. Line Receiver Application

Chip Information

MAX9140 TRANSISTOR COUNT: 158

MAX9141 TRANSISTOR COUNT: 192

MAX9142 TRANSISTOR COUNT: 314

MAX9144 TRANSISTOR COUNT: 620

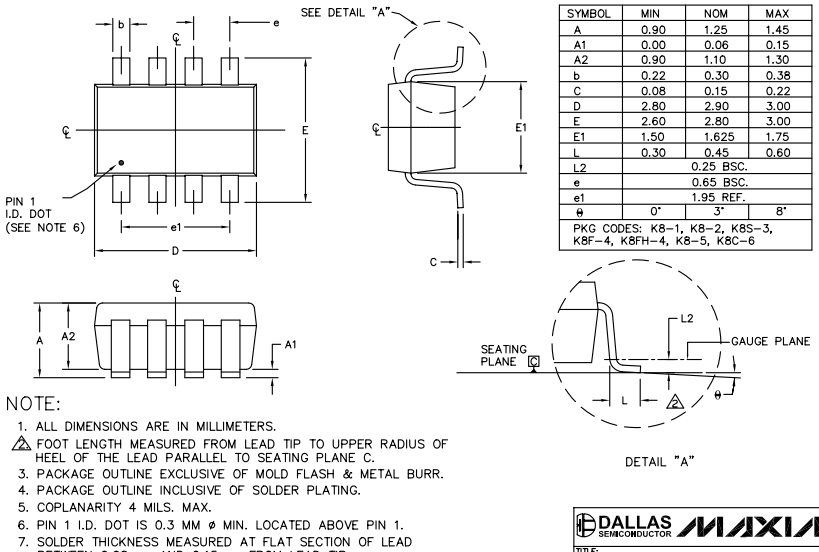
PROCESS: Bipolar

40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT23, 8L .EPS



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°

PKG CODES: K8-1, K8-2, K8S-3, K8F-4, K8FH-4, K8-5, K8C-6

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.

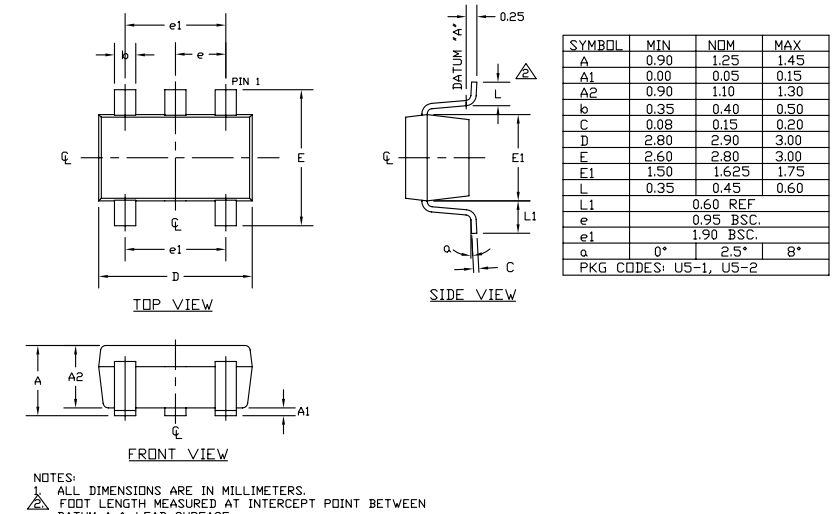
–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	F	1/1

SOT-23 5L .EPS



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
α	0°	2.5°	8°

PKG CODES: U5-1, U5-2

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. MEETS JEDEC MO178, VARIATION AA.
6. LEADS TO BE COPLANAR WITHIN 0.10 mm.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

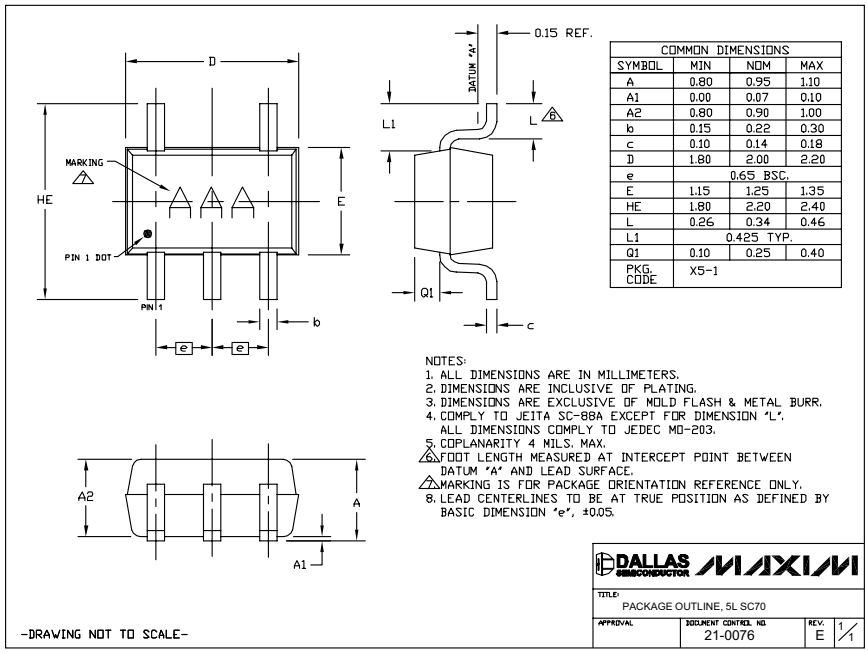
TITLE: PACKAGE OUTLINE, SOT-23, 5L

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0057	F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SC70, 5L.EPS



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODE	X5-1		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO JEITA SC-88A EXCEPT FOR DIMENSION "L". ALL DIMENSIONS COMPLY TO JEDEC MO-203.
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

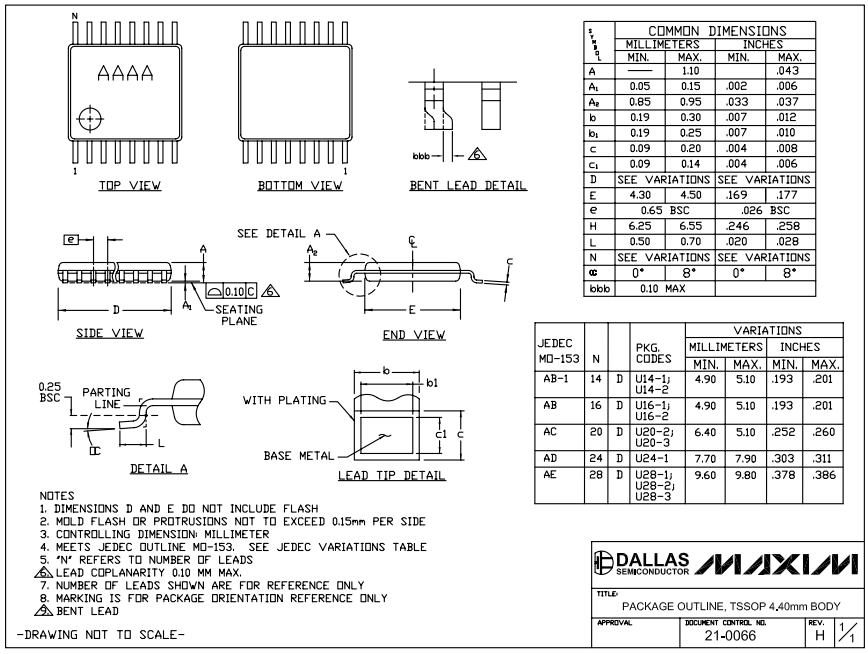
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 5L SC70

APPROVAL | DOCUMENT CONTROL NO. 21-0076 | REV. E | 1/1

-DRAWING NOT TO SCALE-

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	5.10	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4,40mm BODY

APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. H | 1/1

40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

Package Information (continued)

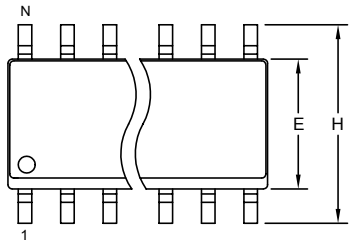
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

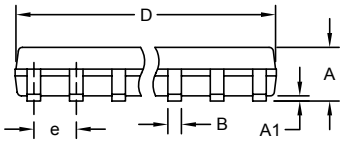
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

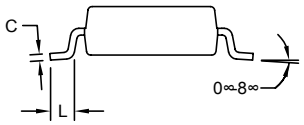
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Revision History

Pages changed at Rev 1: 1, 2, 4, 5, 6, 10, 11, 12

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