

# 93S47 *010543*

## HIGH SPEED 6-BIT IDENTITY COMPARATOR

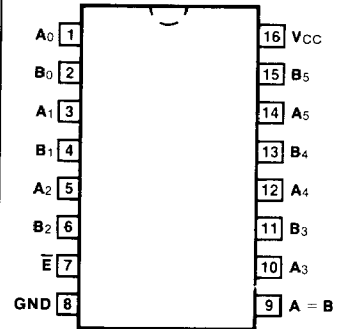
**DESCRIPTION** — The '47 is a very high speed 6-bit identity comparator. The device features an open-collector output for wired-OR expansion and active LOW Enable. The '47 is fabricated with the Schottky barrier diode process for high speed, and is completely compatible with all TTL families. This device is recommended for applications where wired-OR expansion is desired and the speed of an active pull-up is not required. The '47 is a pin-for-pin replacement for the DM7160/8160.

- SCHOTTKY PROCESS FOR HIGH SPEED
- COMPARE TWO 6-BIT WORDS IN 15 ns
- OPEN-COLLECTOR OUTPUT FOR WIRED-OR EXPANSION

**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	93S47PC		9B
Ceramic DIP (D)	A	93S47DC	93S47DM	6B
Flatpak (F)	A	93S47FC	93S47FM	4L

### CONNECTION DIAGRAM PINOUT A



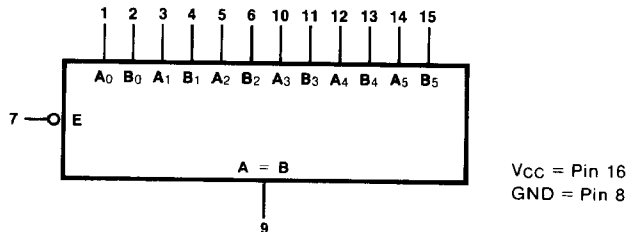
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**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93S (U.L.) HIGH/LOW
A <sub>0</sub> — A <sub>5</sub>	Word A Inputs	1.25/1.25
B <sub>0</sub> — B <sub>5</sub>	Word B Inputs	1.25/1.25
E	Enable Input (Active LOW)	1.25/1.25
A = B	A Equal to B Output	OC*/12.5

\*OC — Open Collector

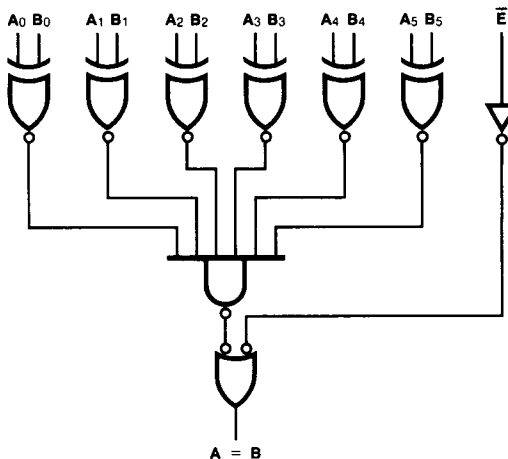
### LOGIC SYMBOL



**FUNCTIONAL DESCRIPTION** — The '47 is a very high speed 6-bit identity comparator. When enabled ( $\bar{E}$  input LOW), the  $A = B$  output is HIGH if the two 6-bit words are equal. When disabled ( $\bar{E}$  input HIGH), the  $A = B$  output is forced HIGH. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. Since the  $A = B$  output state is determined by the equality of each pair of inputs, the equivalent  $A_n$  and  $B_n$  pins can be interchanged to facilitate board layout or wiring. The active LOW Enable ( $\bar{E}$ ) can be used as a high speed strobe. When the Enable is HIGH, the  $A = B$  output is forced HIGH. This allows devices tied to a common wired-OR (actually wired-AND) node to be strobed individually or in groups. Only the enabled devices will determine the state of the output node.

$$(A = B) = \bar{E} + (\overline{A_0 \oplus B_0}) \cdot (\overline{A_1 \oplus B_1}) \cdot (\overline{A_2 \oplus B_2}) \cdot (\overline{A_3 \oplus B_3}) \cdot (\overline{A_4 \oplus B_4}) \cdot (\overline{A_5 \oplus B_5})$$

### LOGIC DIAGRAM



### TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}$	$A_n, B_n$	$A = B$
L	$A_n = B_n$	H
L	$A_n \neq B_n$	L
H	$A_n \neq B_n$	H
H	$A_n = B_n$	H

H = HIGH Voltage Level  
L = LOW Voltage Level

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93S		UNITS	CONDITIONS
		Min	Max		
$I_{CC}$	Power Supply Current		65	mA	$V_{CC} = \text{Max}$

### AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$ , $T_A = +25^\circ \text{C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93S		UNITS	CONDITIONS
		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$			
		Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $A = B$	5.0 5.0	17 17	ns	$\bar{E} = \text{Gnd}$ , Other Inputs = 4.5 V, Test each input individually, Figs. 3-2, 3-5
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $A = B$	4.0 4.0	14 15	ns	$\bar{E} = \text{Gnd}$ , Other Inputs = Gnd, Test each input individually, Figs. 3-2, 3-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}$ to $A = B$	3.0 3.0	10 10	ns	$A_n \neq B_n$ Figs. 3-2, 3-5