

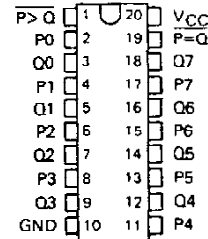
# SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688, SN74LS682, SN74LS684 THRU SN74LS688 8-BIT MAGNITUDE/IDENTITY COMPARATORS

D2617, JANUARY 1981—REVISED MARCH 1988

SDLS008

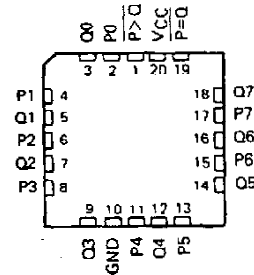
- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-kΩ Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 . . . JT and NT 24-Pin, 300-Mil Packages

SN54LS682, SN54LS684, SN54LS685 . . . J PACKAGE  
SN74LS682, SN74LS684, SN74LS685 . . . DW OR N PACKAGE  
(TOP VIEW)

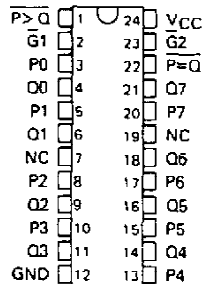


TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-kΩ PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
SN74LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no

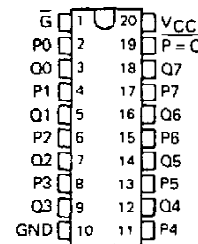
SN54LS682, SN54LS684, SN54LS685 . . . FK PACKAGE  
(TOP VIEW)



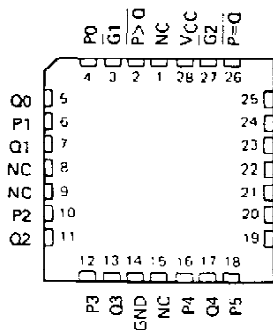
SN54LS687 . . . JT PACKAGE  
SN74LS686, SN74LS687 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54LS688 . . . J PACKAGE  
SN74LS688 . . . DW OR N PACKAGE  
(TOP VIEW)

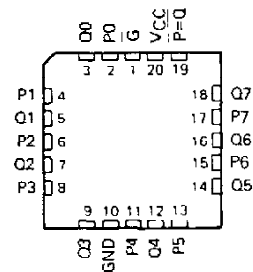


SN54LS687 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

SN54LS688 . . . FK PACKAGE  
(TOP VIEW)



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# SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688 SN74LS682, SN74LS684 THRU SN74LS688 8-BIT MAGNITUDE/IDENTITY COMPARATORS

## description

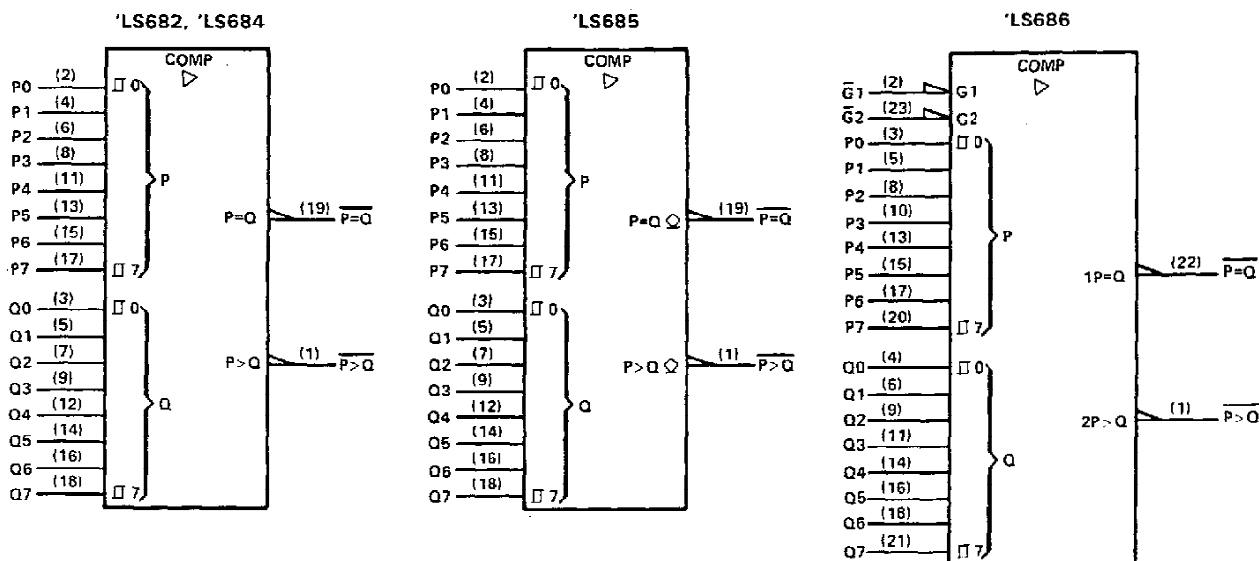
These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide  $\overline{P=Q}$  outputs and all except 'LS688 provide  $\overline{P>Q}$  outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-k $\Omega$  pullup termination resistors on the Q inputs for analog or switch data.

FUNCTION TABLE

DATA P, Q	ENABLES		OUTPUTS	
	$\overline{G1}$ , $\overline{G1}$	$\overline{G2}$	$\overline{P=Q}$	$\overline{P>Q}$
P=Q	L	X	L	H
P>Q	X	L	H	L
P<Q	X	X	H	H
P=Q	H	X	H	H
P>Q	X	H	H	H
X	H	H	H	H

- NOTES: 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS688.
2. The  $\overline{P<Q}$  function can be generated by applying the  $\overline{P=Q}$  and  $\overline{P>Q}$  outputs to a 2-input NAND gate.
3. For 'LS686 and 'LS687,  $\overline{G1}$  enables  $\overline{P=Q}$  and  $\overline{G2}$  enables  $\overline{P>Q}$ .

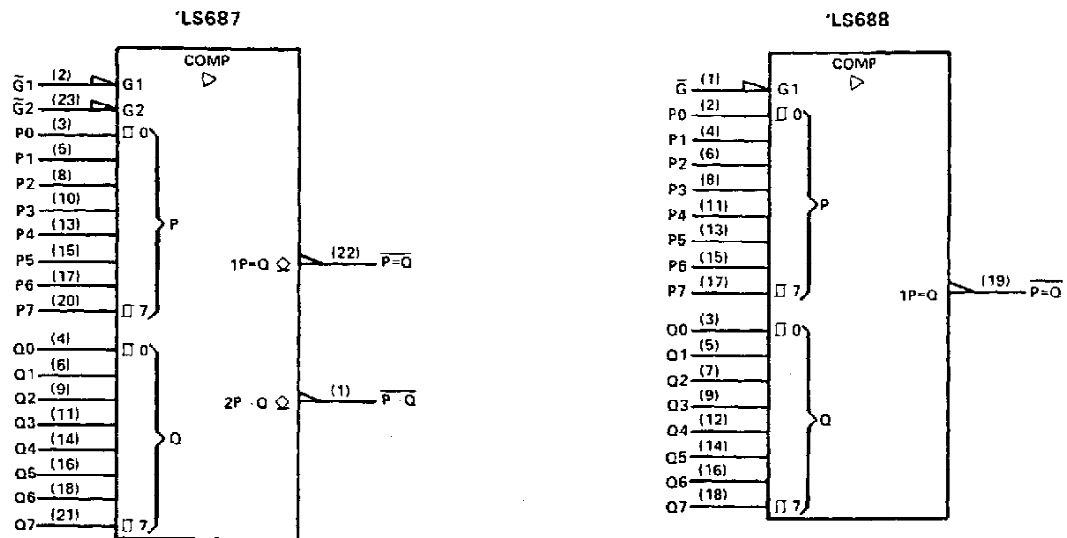
## logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

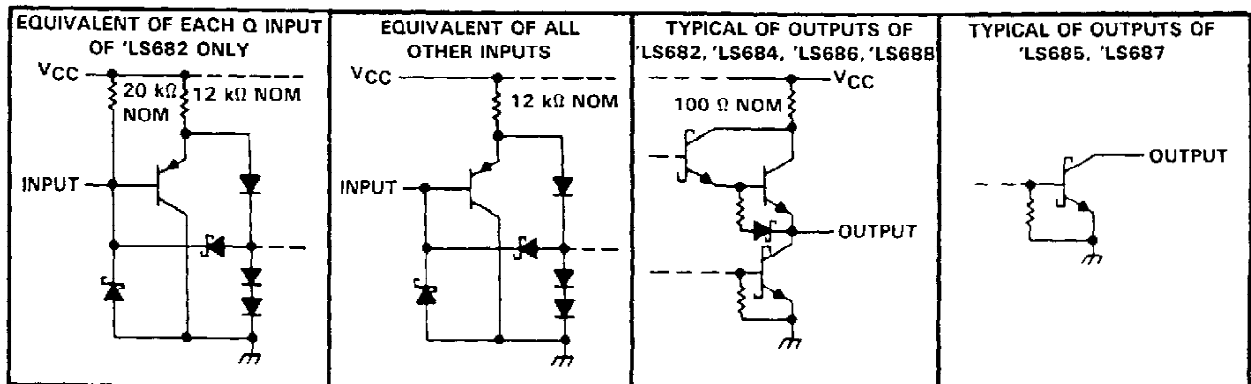
**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688,  
SN74LS682, SN74LS684 THRU SN74LS688  
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

logic symbols† (continued)



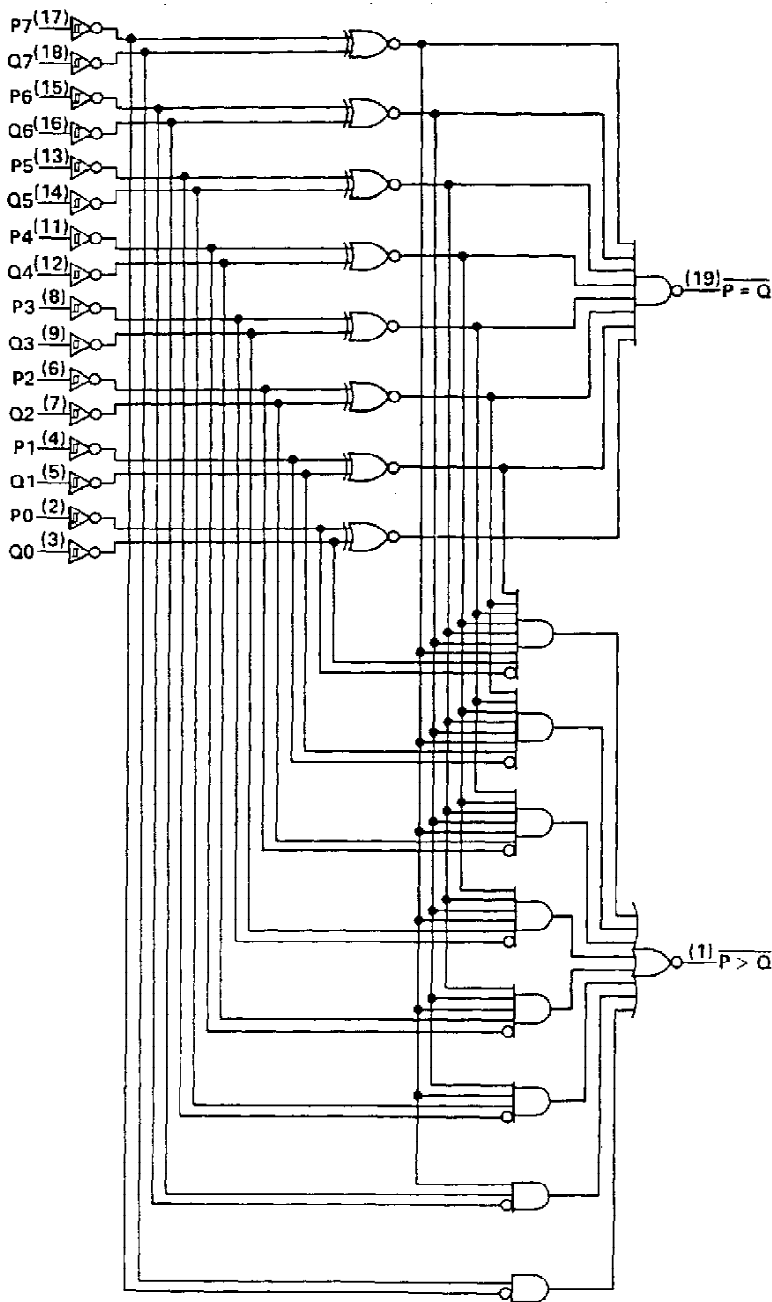
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

**schematics of inputs and outputs**



**SN54LS682, SN54LS684, SN54LS685  
 SN74LS682, SN74LS684, SN74LS685  
 8-BIT MAGNITUDE/IDENTITY COMPARATORS**

LS682, LS684, LS685 logic diagram (positive logic)



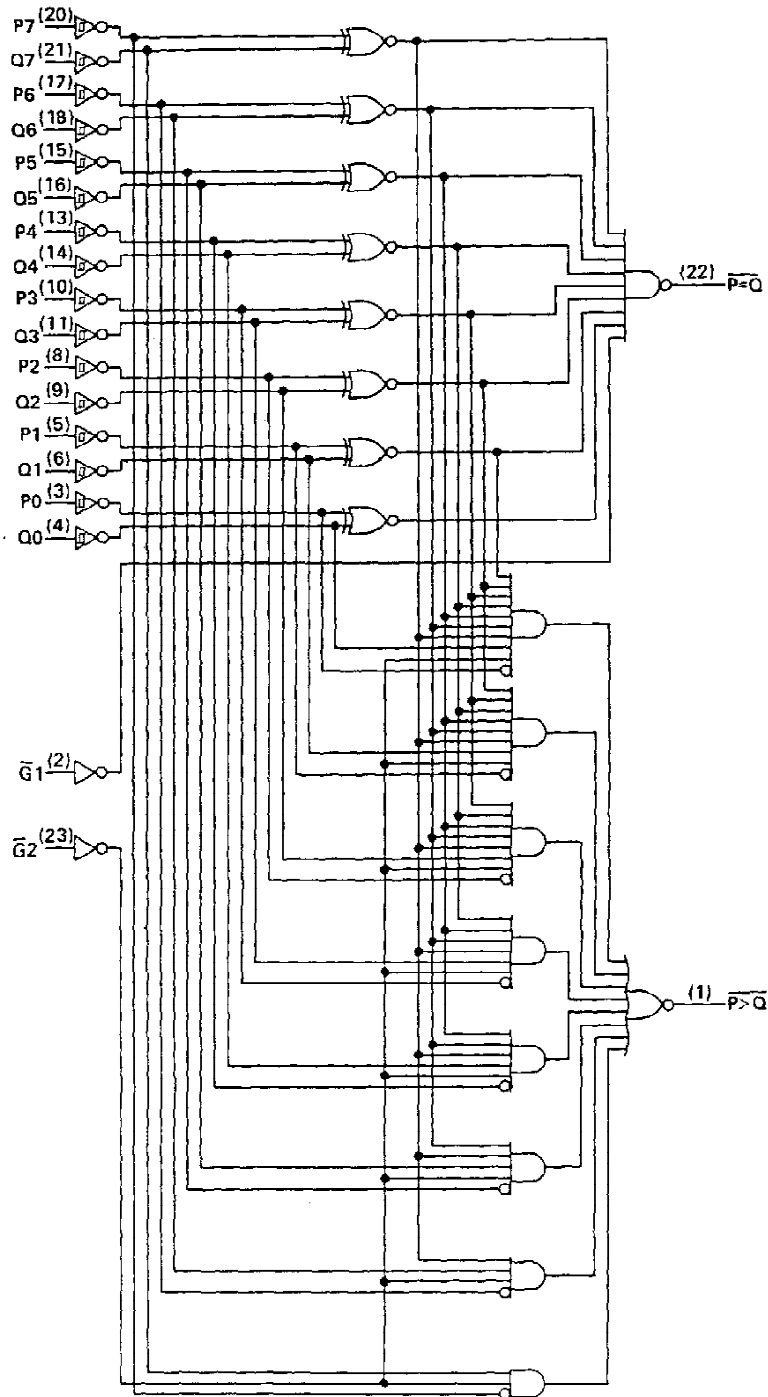
Pin numbers shown are for DW, J, and N packages.

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SN54LS687  
 SN74LS686, SN74LS687  
 8-BIT MAGNITUDE/IDENTITY COMPARATORS

'LS686, 'LS687 logic diagram (positive logic)



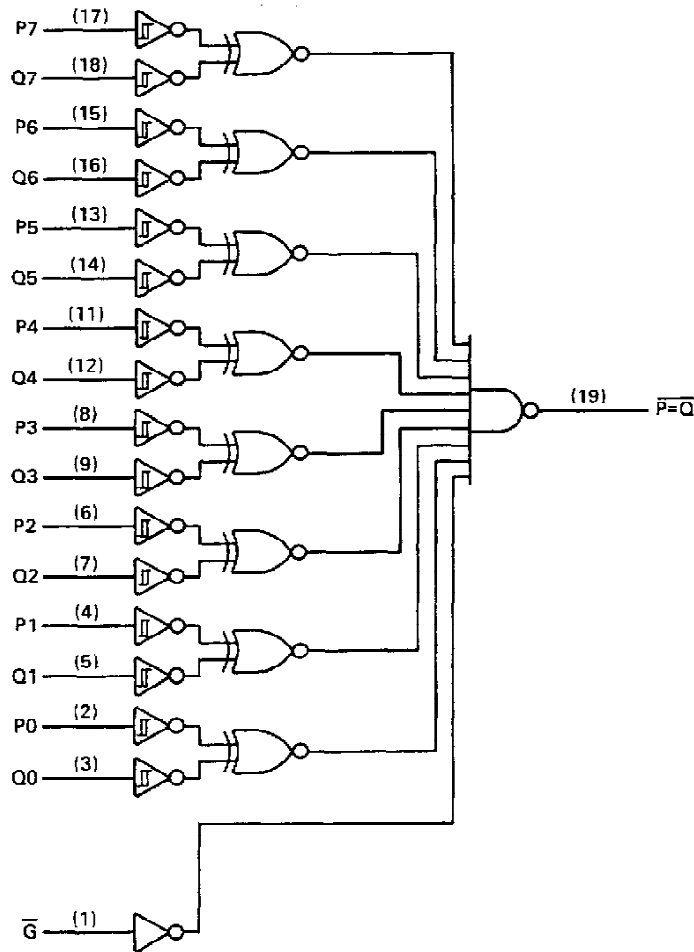
Pin numbers shown are for DW, JT, and NT packages.

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**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688  
SN74LS682, SN74LS684 THRU SN74LS688  
8-BIT IDENTITY COMPARATORS**

'LS688 logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage: Q inputs of 'LS682 .....	5.5 V
All other inputs .....	7 V
Off-state output voltage: 'LS685, 'LS687 .....	7 V
Operating free-air temperature range:	
SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688 .....	-55 °C to 125 °C
SN74LS682, SN74LS684 thru SN74LS688 .....	0 °C to 70 °C
Storage temperature range .....	-65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

**SN54LS682, SN54LS684, SN54LS688  
SN74LS682, SN74LS684, SN74LS686, SN74LS688  
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

**recommended operating conditions**

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.85	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT	
			MIN	TYP‡	MAX	MIN		TYP‡
$V_{IH}$	High-level input voltage		2		2		V	
$V_{IL}$	Low-level input voltage			0.7		0.8	V	
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs		0.4		0.4	V	
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}$				-1.5	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = V_{IL\text{max}}$ , $I_{OH} = -400 \mu\text{A}$	2.5		2.7		V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = V_{IL\text{max}}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4	V
			$I_{OL} = 24 \text{ mA}$			0.35	0.5	
$I_I$	Input current at maximum input voltage	Q inputs, 'LS682	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$					mA
		All other inputs	$V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$		0.1		0.1	
$I_{IH}$	High-level input current		$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$		20		20	$\mu$ A
$I_{IL}$	Low-level input current	Q inputs, 'LS682	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$		-0.4		-0.4	mA
		All other inputs			-0.2		-0.2	
$I_{OS}^{\S}$	Short-circuit output current		$V_{CC} = \text{MAX}$ , $V_O = 0$	-20	-100	-20	-100	mA
$I_{CC}$	Supply current	'LS682	$V_{CC} = \text{MAX}$ , See Note 1	42	70	42	70	mA
		'LS684		40	65	40	65	
		'LS686		44	75	44	75	
		'LS688		40	65	40	65	

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1:  $I_{CC}$  is measured with any  $\bar{Q}$  inputs grounded, all other inputs at 4.5 V, and all outputs open.

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**SN54LS682, SN54LS684, SN54LS688**  
**SN74LS682, SN74LS684, SN74LS686, SN74LS688**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682		'LS684		'LS686		'LS688		UNIT
				MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
$t_{PLH}$	P	$\overline{P=Q}$	$R_L = 667\ \Omega$ , $C_L = 45\ \text{pF}$ , All other inputs low, See Note 2	13	25	15	25	13	25	12	18	ns
$t_{PHL}$				15	25	17	25	20	30	17	23	
$t_{PLH}$	Q	$\overline{P=Q}$		14	25	16	25	13	25	12	18	ns
$t_{PHL}$				15	25	15	25	21	30	17	23	
$t_{PLH}$	$\overline{Q}, \overline{Q}1$	$\overline{P=Q}$						11	20	12	18	ns
$t_{PHL}$								19	30	13	20	
$t_{PLH}$	P	$\overline{P>Q}$			20	30	22	30	19	30		ns
$t_{PHL}$					15	30	17	30	15	30		
$t_{PLH}$	Q	$\overline{P>Q}$			21	30	24	30	18	30		ns
$t_{PHL}$					19	30	20	30	19	30		
$t_{PLH}$	$\overline{Q}2$	$\overline{P>Q}$						21	30		ns	
$t_{PHL}$								16	25			

† $t_{PLH}$  = propagation delay time, low-to-high-level outputs;  $t_{PHL}$  = propagation delay time, high-to-low-level output.  
 NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**SN54LS685, SN54LS687**  
**SN74LS685, SN74LS687, SN74LS688**

**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

**recommended operating conditions**

	SN54LS <sup>†</sup>			SN74LS <sup>†</sup>			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.85	5	5.25	V
High-level output current, $I_{OH}$			5.5			5.5	V
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN54LS <sup>†</sup>			SN74LS <sup>†</sup>			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
$V_{IH}$	High-level input voltage		2			2			V	
$V_{IL}$	Low-level input voltage				0.7			0.8	V	
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	0.4			0.4			V	
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V	
$I_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OH} = 5.5 \text{ V}$			250			100	$\mu\text{A}$	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$	$I_{OL} = 12 \text{ mA}$		0.25	0.4	$I_{OL} = 12 \text{ mA}$		0.25	0.4
			$I_{OL} = 24 \text{ mA}$				$I_{OL} = 24 \text{ mA}$		0.35	0.5
$I_I$		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.2			-0.2	mA	
$I_{CC}$	Supply current	'LS685	$V_{CC} = \text{MAX}, \text{ See Note 1}$		40	65	$V_{CC} = \text{MAX}, \text{ See Note 1}$		40	65
		'LS687			44	75			44	75

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

NOTE 1:  $I_{CC}$  is measure with any  $\bar{Q}$  inputs grounded, all other inputs at 4.5 V, and all outputs open.



**SN54LS685, SN54LS687**  
**SN74LS685, SN74LS687**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS685			'LS687			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$	P	$\overline{P=Q}$	$R_L = 667\ \Omega$ , $C_L = 45\ \text{pF}$ , All other inputs low, See Note 2	30	45		24	35	ns	
$t_{PHL}$				19	35		20	30		
$t_{PLH}$	Q	$\overline{P=Q}$		24	45		24	35	ns	
$t_{PHL}$				23	35		20	30		
$t_{PLH}$	$\overline{Q}, \overline{Q1}$	$\overline{P=Q}$					21	35	ns	
$t_{PHL}$							18	30		
$t_{PLH}$	P	$\overline{P>Q}$			32	45		24	35	ns
$t_{PHL}$					16	35		16	30	
$t_{PLH}$	Q	$\overline{P>Q}$			30	45		24	35	ns
$t_{PHL}$					20	35		16	30	
$t_{PLH}$	$\overline{Q2}$	$\overline{P>Q}$				24	35	ns		
$t_{PHL}$						15	30			

$t_{PLH}$  = propagation delay time, low-to-high-level outputs;  $t_{PHL}$  = propagation delay time, high-to-low-level output.  
 NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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## SN74LS684, Octal binary or BCD magnitude comparators

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS684	SN74LS684
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
No. of Bits	8	8
Logic	Inv	Inv
P = Q	YES	YES
P > Q	YES	YES

### FEATURES

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- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-k $\Omega$  Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 ... JT and NT 24-Pin, 300-Mil Packages

### DESCRIPTION

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These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide P = Q\ outputs and all except 'LS688 provide P > Q\ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-k $\Omega$  pullup termination resistors on the Q inputs for analog or switch data.

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- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)



								> 10k   25 Nov				
								> 10k   02 Dec				
								> 10k   09 Dec				

**Table Data Updated on: 9/26/2002**

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## SN74LS682, Octal binary or BCD magnitude comparators

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS682	SN74LS682
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
No. of Bits	8	8
Logic	Inv	Inv
P = Q		YES
P > Q		YES

### FEATURES

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- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-k $\Omega$  Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 ... JT and NT 24-Pin, 300-Mil Packages

### DESCRIPTION

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These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide P = Q\ outputs and all except 'LS688 provide P > Q\ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-k $\Omega$  pullup termination resistors on the Q inputs for analog or switch data.

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- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
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								> 10k   25 Nov				
								> 10k   02 Dec				
								> 10k   09 Dec				

**Table Data Updated on: 9/26/2002**

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## SN74LS688, 8-Bit Magnitude/Identity Comparators

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS688	SN74LS688
Voltage Nodes (V)	5	5

### FEATURES

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- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-kΩ Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 ... JT and NT 24-Pin, 300-Mil Packages

### DESCRIPTION

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These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide P = Q\ outputs and all except 'LS688 provide P > Q\ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

### TECHNICAL DOCUMENTS

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### DATASHEET

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Full datasheet in Acrobat PDF: [sn74ls688.pdf](#) (438 KB) (Updated: 03/01/1988)

### APPLICATION NOTES

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- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)

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View Related Documentation for [Digital Logic](#)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)



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